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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	256KB (128K x 16)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega256a3-mh

7. Memories

7.1 Features

- **Flash Program Memory**
 - One linear address space
 - In-System Programmable
 - Self-Programming and Bootloader support
 - Application Section for application code
 - Application Table Section for application code or data storage
 - Boot Section for application code or bootloader code
 - Separate lock bits and protection for all sections
 - Built in fast CRC check of a selectable flash program memory section
- **Data Memory**
 - One linear address space
 - Single cycle access from CPU
 - SRAM
 - EEPROM
 - Byte and page accessible
 - Optional memory mapping for direct load and store
 - I/O Memory
 - Configuration and Status registers for all peripherals and modules
 - 16 bit-accessible General Purpose Register for global variables or flags
 - Bus arbitration
 - Safe and deterministic handling of CPU and DMA Controller priority
 - Separate buses for SRAM, EEPROM, I/O Memory and External Memory access
 - Simultaneous bus access for CPU and DMA Controller
- **Production Signature Row Memory for factory programmed data**
 - Device ID for each microcontroller device type
 - Serial number for each device
 - Oscillator calibration bytes
 - ADC, DAC and temperature sensor calibration data
- **User Signature Row**
 - One flash page in size
 - Can be read and written from software
 - Content is kept after chip erase

7.2 Overview

The AVR architecture has two main memory spaces, the Program Memory and the Data Memory. In addition, the XMEGA A3 features an EEPROM Memory for non-volatile data storage. All three memory spaces are linear and require no paging. The available memory size configurations are shown in "Ordering Information" on page 2. In addition each device has a Flash memory signature row for calibration data, device identification, serial number etc.

Non-volatile memory spaces can be locked for further write or read/write operations. This prevents unrestricted access to the application software.

7.4.1 I/O Memory

All peripherals and modules are addressable through I/O memory locations in the data memory space. All I/O memory locations can be accessed by the Load (LD/LDS/LDD) and Store (ST/STS/STD) instructions, transferring data between the 32 general purpose registers in the CPU and the I/O Memory.

The IN and OUT instructions can address I/O memory locations in the range 0x00 - 0x3F directly.

I/O registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. The value of single bits can be checked by using the SBIS and SBIC instructions on these registers.

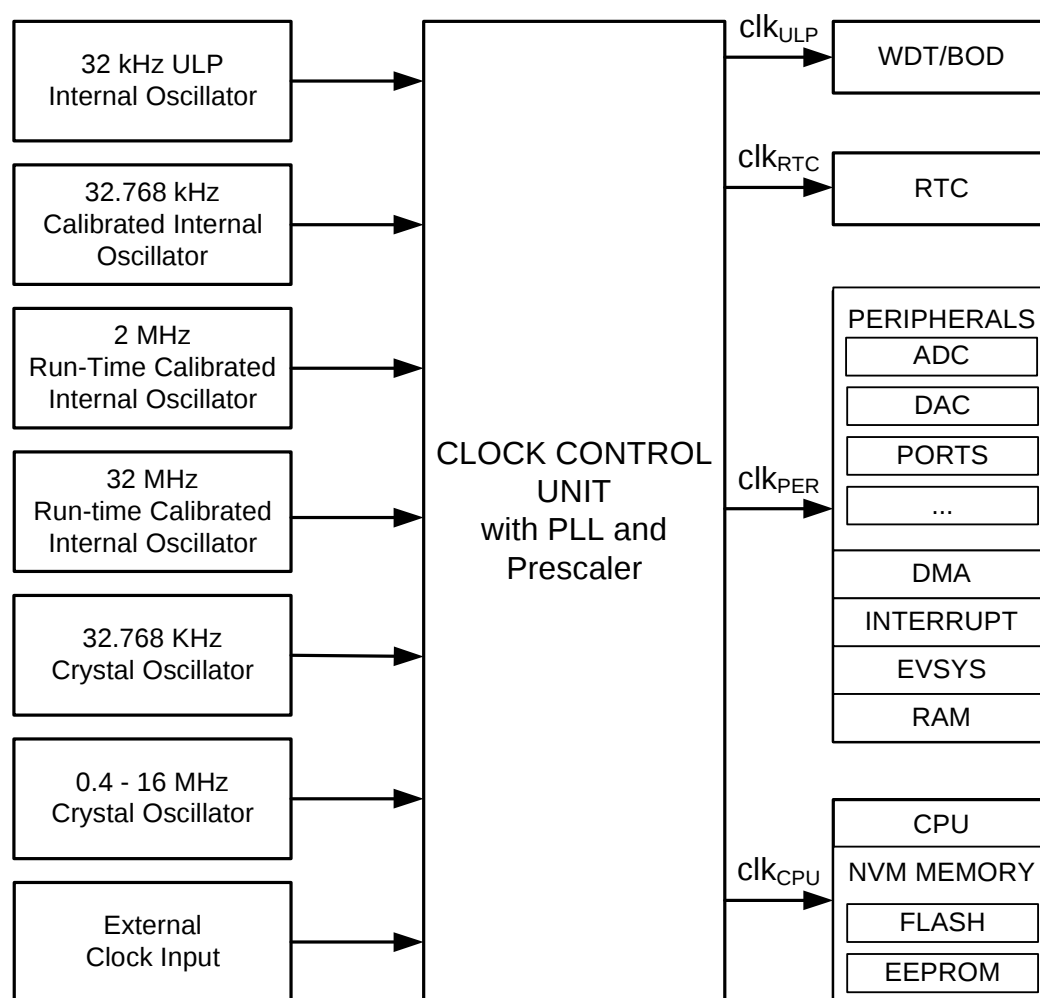
The I/O memory address for all peripherals and modules in XMEGA A3 is shown in the "Peripheral Module Address Map" on page 56.

7.4.2 SRAM Data Memory

The XMEGA A3 devices have internal SRAM memory for data storage.

7.4.3 EEPROM Data Memory

The XMEGA A3 devices have internal EEPROM memory for non-volatile data storage. It is addressable either in a separate data space or it can be memory mapped into the normal data memory space. The EEPROM memory supports both byte and page access.

Figure 10-1. Clock system overview


Each clock source is briefly described in the following sub-sections.

10.3 Clock Options

10.3.1 32 kHz Ultra Low Power Internal Oscillator

The 32 kHz Ultra Low Power (ULP) Internal Oscillator is a very low power consumption clock source. It is used for the Watchdog Timer, Brown-Out Detection and as an asynchronous clock source for the Real Time Counter. This oscillator cannot be used as the system clock source, and it cannot be directly controlled from software.

10.3.2 32.768 kHz Calibrated Internal Oscillator

The 32.768 kHz Calibrated Internal Oscillator is a high accuracy clock source that can be used as the system clock source or as an asynchronous clock source for the Real Time Counter. It is calibrated during production to provide a default frequency which is close to its nominal frequency.

10.3.3 32.768 kHz Crystal Oscillator

The 32.768 kHz Crystal Oscillator is a low power driver for an external watch crystal. It can be used as system clock source or as asynchronous clock source for the Real Time Counter.

10.3.4 0.4 - 16 MHz Crystal Oscillator

The 0.4 - 16 MHz Crystal Oscillator is a driver intended for driving both external resonators and crystals ranging from 400 kHz to 16 MHz.

10.3.5 2 MHz Run-time Calibrated Internal Oscillator

The 2 MHz Run-time Calibrated Internal Oscillator is a high frequency oscillator. It is calibrated during production to provide a default frequency which is close to its nominal frequency. The oscillator can use the 32.768 kHz Calibrated Internal Oscillator or the 32 kHz Crystal Oscillator as a source for calibrating the frequency run-time to compensate for temperature and voltage drift hereby optimizing the accuracy of the oscillator.

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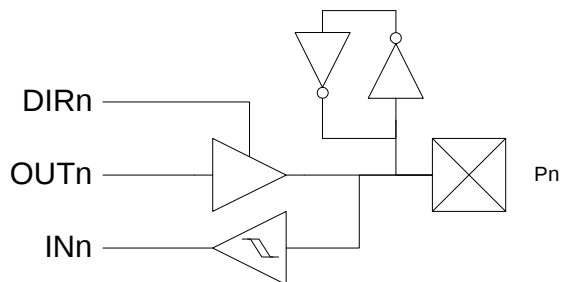
10.3.7 External Clock input

The external clock input gives the possibility to connect a clock from an external source.

10.3.8 PLL with Multiplication factor 1 - 31x

The PLL provides the possibility of multiplying a frequency by any number from 1 to 31. In combination with the prescalers, this gives a wide range of output frequencies from all clock sources.

Figure 15-4. I/O configuration - Totem-pole with bus-keeper



15.3.5 Others

Figure 15-5. Output configuration - Wired-OR with optional pull-down

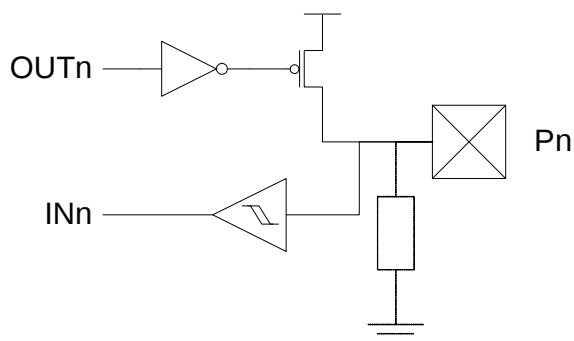
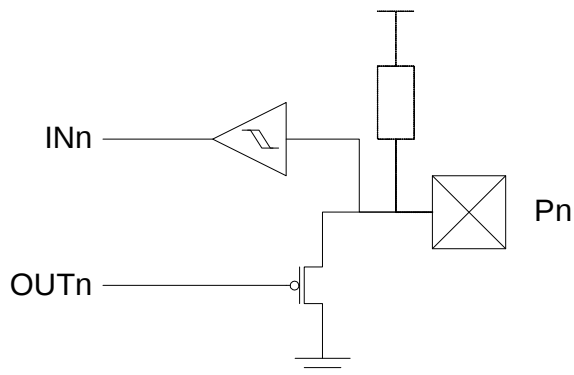


Figure 15-6. I/O configuration - Wired-AND with optional pull-up



22. USART

22.1 Features

- Seven Identical USART peripherals
- Full Duplex Operation (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation
- Master or Slave Clocked Synchronous Operation
- High-resolution Arithmetic Baud Rate Generator
- Supports Serial Frames with 5, 6, 7, 8, or 9 Data Bits and 1 or 2 Stop Bits
- Odd or Even Parity Generation and Parity Check Supported by Hardware
- Data OverRun Detection
- Framing Error Detection
- Noise Filtering Includes False Start Bit Detection and Digital Low Pass Filter
- Three Separate Interrupts on TX Complete, TX Data Register Empty and RX Complete
- Multi-processor Communication Mode
- Double Speed Asynchronous Communication Mode
- Master SPI mode for SPI communication
- IrDA support through the IRCOM module

22.2 Overview

The Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication module. The USART supports full duplex communication, and both asynchronous and clocked synchronous operation. The USART can also be set in Master SPI mode to be used for SPI communication.

Communication is frame based, and the frame format can be customized to support a wide range of standards. The USART is buffered in both direction, enabling continued data transmission without any delay between frames. There are separate interrupt vectors for receive and transmit complete, enabling fully interrupt driven communication. Frame error and buffer overflow are detected in hardware and indicated with separate status flags. Even or odd parity generation and parity check can also be enabled.

One USART can use the IRCOM module to support IrDA 1.4 physical compliant pulse modulation and demodulation for baud rates up to 115.2 kbps.

PORTC, PORTD, and PORTE each has two USARTs, while PORTF has one USART only. Notation of these peripherals are USARTC0, USARTC1, USARTE0, USARTE1 and USARTF0, respectively.

28. OCD - On-chip Debug

28.1 Features

- **Complete Program Flow Control**
 - Go, Stop, Reset, Step into, Step over, Step out, Run-to-Cursor
- **Debugging on C and high-level language source code level**
- **Debugging on Assembler and disassembler level**
- **1 dedicated program address or source level breakpoint for AVR Studio / debugger**
- **4 Hardware Breakpoints**
- **Unlimited Number of User Program Breakpoints**
- **Unlimited Number of User Data Breakpoints, with break on:**
 - Data location read, write or both read and write
 - Data location content equal or not equal to a value
 - Data location content is greater or less than a value
 - Data location content is within or outside a range
 - Bits of a data location are equal or not equal to a value
- **Non-Intrusive Operation**
 - No hardware or software resources in the device are used
- **High Speed Operation**
 - No limitation on debug/programming clock frequency versus system clock frequency

28.2 Overview

The XMEGA A3 has a powerful On-Chip Debug (OCD) system that - in combination with Atmel's development tools - provides all the necessary functions to debug an application. It has support for program and data breakpoints, and can debug an application from C and high level language source code level, as well as assembler and disassembler level. It has full Non-Intrusive Operation and no hardware or software resources in the device are used. The ODC system is accessed through an external debugging tool which connects to the JTAG or PDI physical interfaces. Refer to "Program and Debug Interfaces" on page 48.

29. Program and Debug Interfaces

29.1 Features

- PDI - Program and Debug Interface (Atmel proprietary 2-pin interface)
- JTAG Interface (IEEE std. 1149.1 compliant)
- Boundary-scan capabilities according to the IEEE Std. 1149.1 (JTAG)
- Access to the OCD system
- Programming of Flash, EEPROM, Fuses and Lock Bits

29.2 Overview

The programming and debug facilities are accessed through the JTAG and PDI physical interfaces. The PDI physical interface uses one dedicated pin together with the Reset pin, and no general purpose pins are used. JTAG uses four general purpose pins on PORTB.

The PDI is an Atmel proprietary protocol for communication between the microcontroller and Atmel's or third party development tools.

29.3 IEEE 1149.1 (JTAG) Boundary-scan

The JTAG physical layer handles the basic low-level serial communication over four I/O lines named TMS, TCK, TDI, and TDO. It complies to the IEEE Std. 1149.1 for test access port and boundary scan.

29.3.1 Boundary-scan Order

Table 30-8 on page 53 shows the Scan order between TDI and TDO when the Boundary-scan chain is selected as data path. Bit 0 is the LSB; the first bit scanned in, and the first bit scanned out. The scan order follows the pin-out order. Bit 4, 5, 6 and 7 of Port B is not in the scan chain, since these pins constitute the TAP pins when the JTAG is enabled.

29.3.2 Boundary-scan Description Language Files

Boundary-scan Description Language (BSDL) files describe Boundary-scan capable devices in a standard format used by automated test-generation software. The order and function of bits in the Boundary-scan Data Register are included in this description. BSDL files are available for ATxmega256/192/128/64A3 devices.

See Table 30-8 on page 53 for ATxmega256/192/128/64A3 Boundary Scan Order.

Table 30-3. Port C - Alternate functions

PORT C	PIN #	INTERRUPT	TCC0	AWEXC	TCC1	USARTC0	USARTC1	SPIC	TWIC	CLOCKOUT	EVENTOUT
PC0	16	SYNC	OC0A	OC0ALS					SDA		
PC1	17	SYNC	OC0B	OC0AHS		XCK0			SCL		
PC2	18	SYNC/ASYNC	OC0C	OC0BLS		RXD0					
PC3	19	SYNC	OC0D	OC0BHS		TXD0					
PC4	20	SYNC		OC0CLS	OC1A			$\overline{SS}$			
PC5	21	SYNC		OC0CHS	OC1B		XCK1	MOSI			
PC6	22	SYNC		OC0DLS			RXD1	MISO			
PC7	23	SYNC		OC0DHS			TXD1	SCK		CLKOUT	EVOUT
GND	24										
VCC	25										

Table 30-4. Port D - Alternate functions

PORT D	PIN #	INTERRUPT	TCD0	TCD1	USARTD0	USARTD1	SPID	CLOCKOUT	EVENTOUT
PD0	26	SYNC	OC0A						
PD1	27	SYNC	OC0B		XCK0				
PD2	28	SYNC/ASYNC	OC0C		RXD0				
PD3	29	SYNC	OC0D		TXD0				
PD4	30	SYNC		OC1A			$\overline{SS}$		
PD5	31	SYNC		OC1B		XCK1	MOSI		
PD6	32	SYNC				RXD1	MISO		
PD7	33	SYNC				TXD1	SCK	CLKOUT	EVOUT
GND	34								
VCC	35								

Table 30-5. Port E - Alternate functions

PORT E	PIN #	INTERRUPT	TCE0	TCE1	USARTE0	USARTE1	SPIE	TWIE	CLOCKOUT	EVENTOUT	TOSC
PE0	36	SYNC	OC0A					SDA			
PE1	37	SYNC	OC0B		XCK0			SCL			
PE2	38	SYNC/ASYNC	OC0C		RXD0						
PE3	39	SYNC	OC0D		TXD0						
PE4	40	SYNC		OC1A			$\overline{SS}$				
PE5	41	SYNC		OC1B		XCK1	MOSI				
PE6	42	SYNC				RXD1	MISO				TOSC2
PE7	43	SYNC				TXD1	SCK		CLKOUT	EVOUT	TOSC1
GND	44										
VCC	45										

Figure 35-11. Idle Supply Current vs. Vcc

$f_{SYS} = 32.768 \text{ kHz internal RC}$

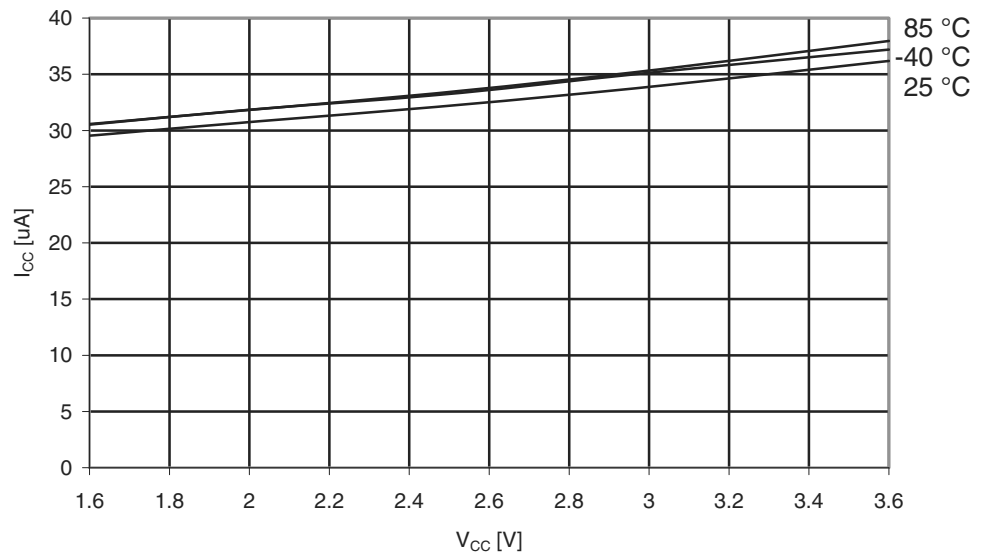


Figure 35-12. Idle Supply Current vs. Vcc

$f_{SYS} = 2.0 \text{ MHz internal RC}$

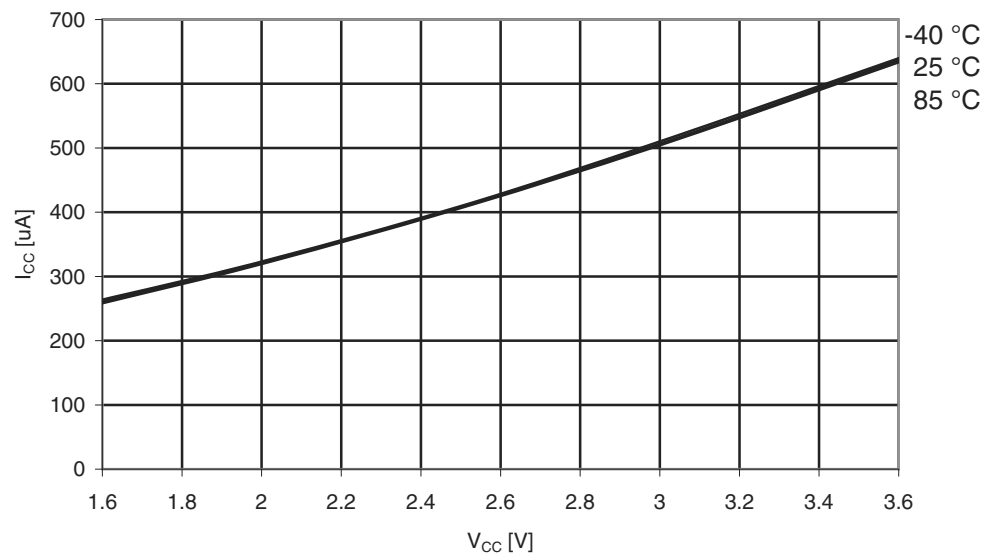


Figure 35-13. Idle Supply Current vs. V_{CC}

$f_{SYS} = 32 \text{ MHz}$ internal RC prescaled to 8 MHz

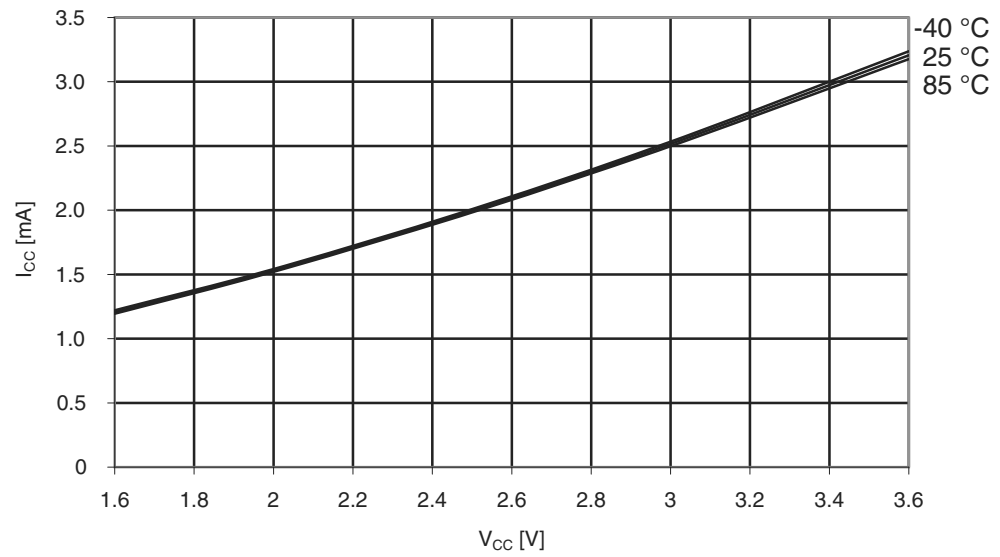
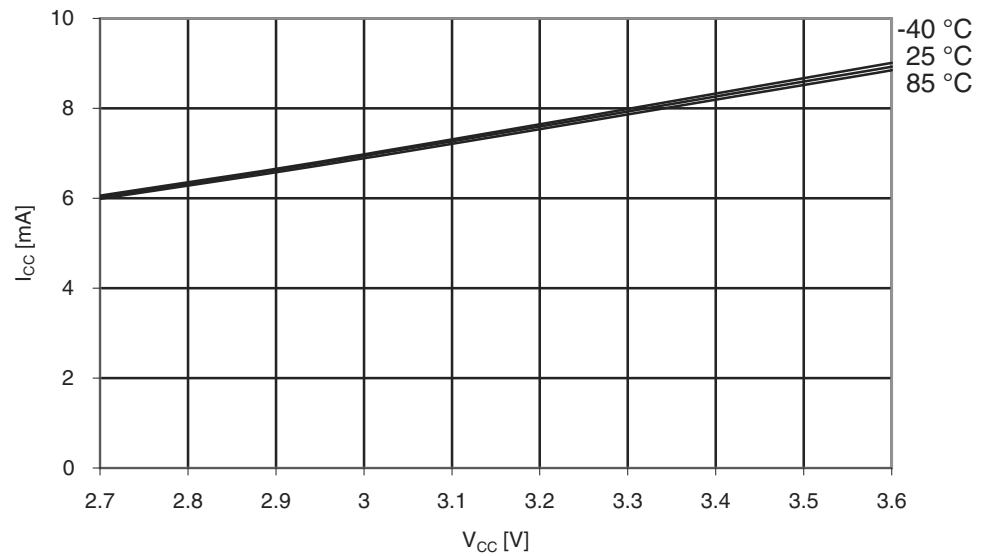


Figure 35-14. Idle Supply Current vs. V_{CC}

$f_{SYS} = 32 \text{ MHz}$ internal RC



35.6 Pin Output Voltage vs. Sink/Source Current

Figure 35-21. I/O Pin Output Voltage vs. Source Current

$V_{CC} = 1.8V$

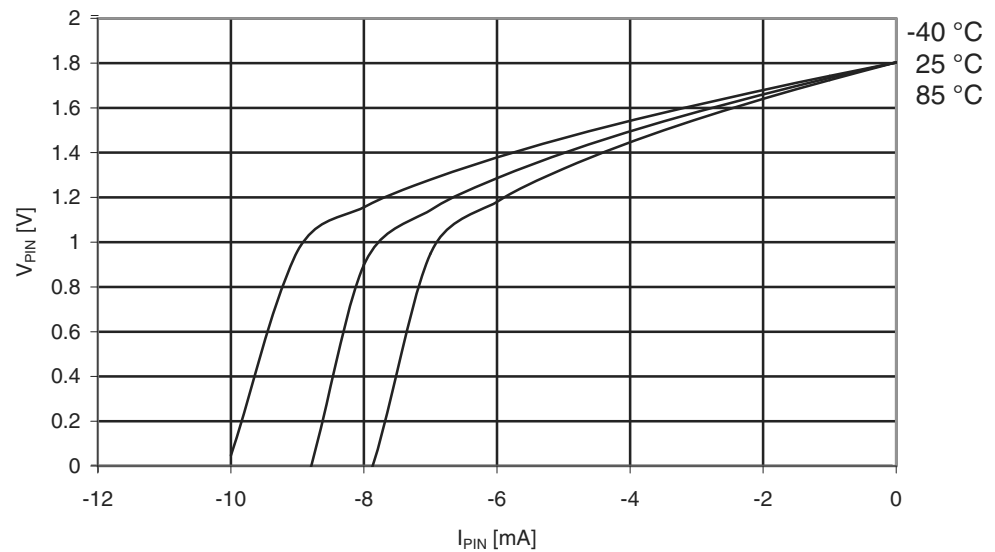


Figure 35-22. I/O Pin Output Voltage vs. Source Current

$V_{CC} = 3.0V$

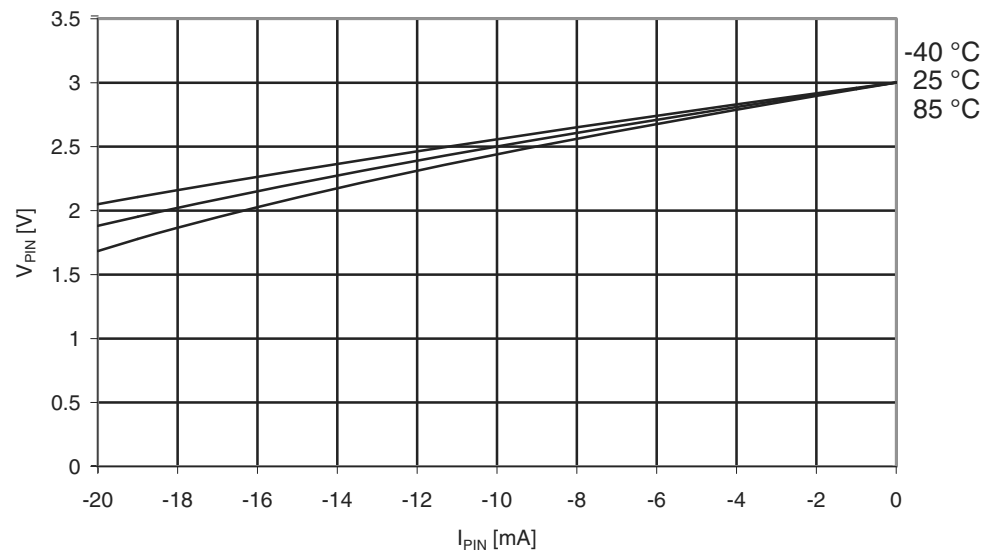


Figure 35-29. I/O Pin Input Hysteresis vs. V_{CC}

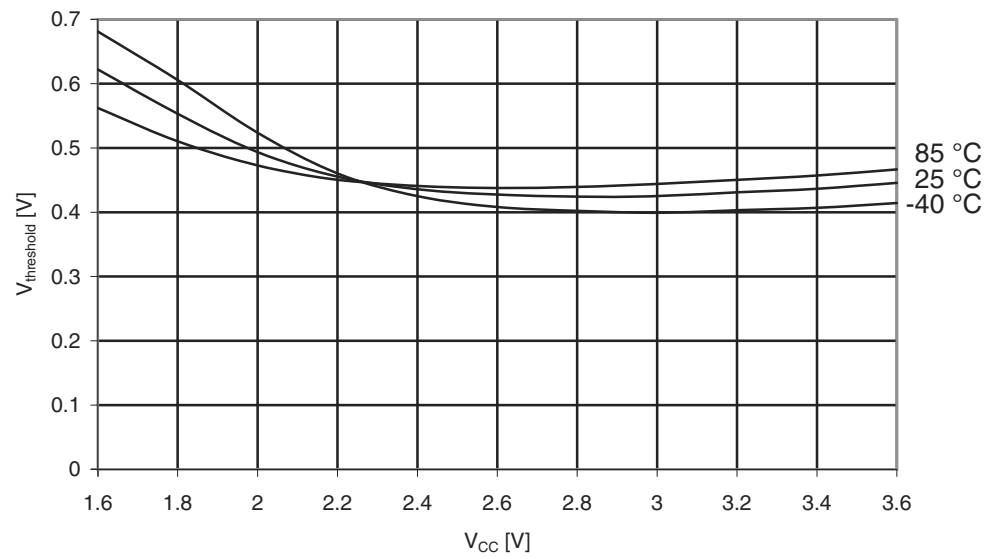
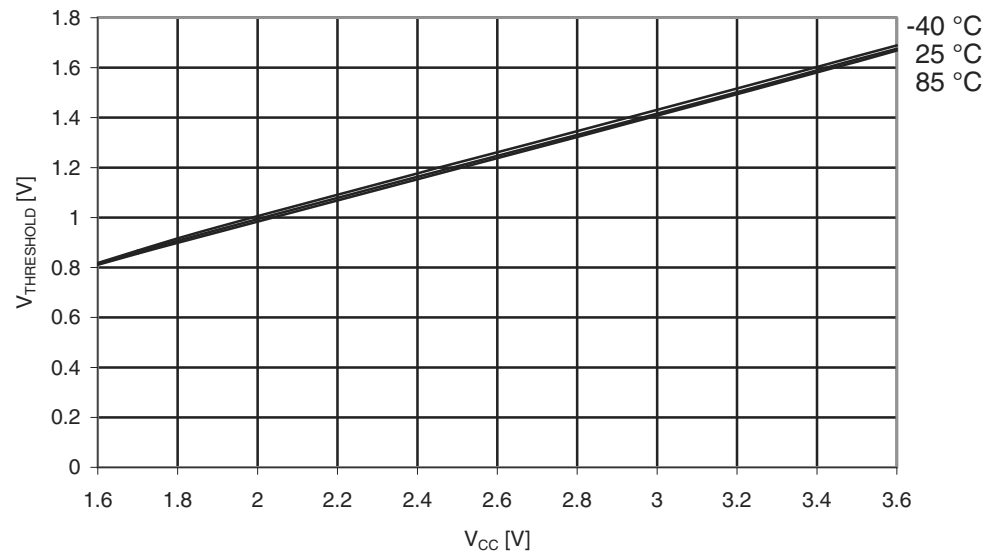


Figure 35-30. Reset Input Threshold Voltage vs. V_{CC}

V_{IH} - I/O Pin Read as "1"



35.10 Module current consumption

Figure 35-39. AC current consumption vs. V_{CC}
Low-power Mode

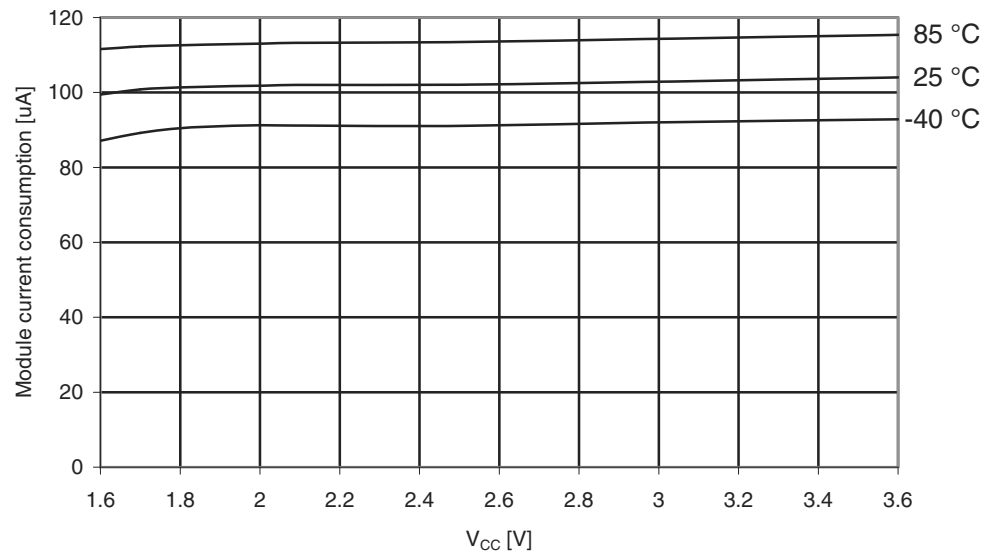
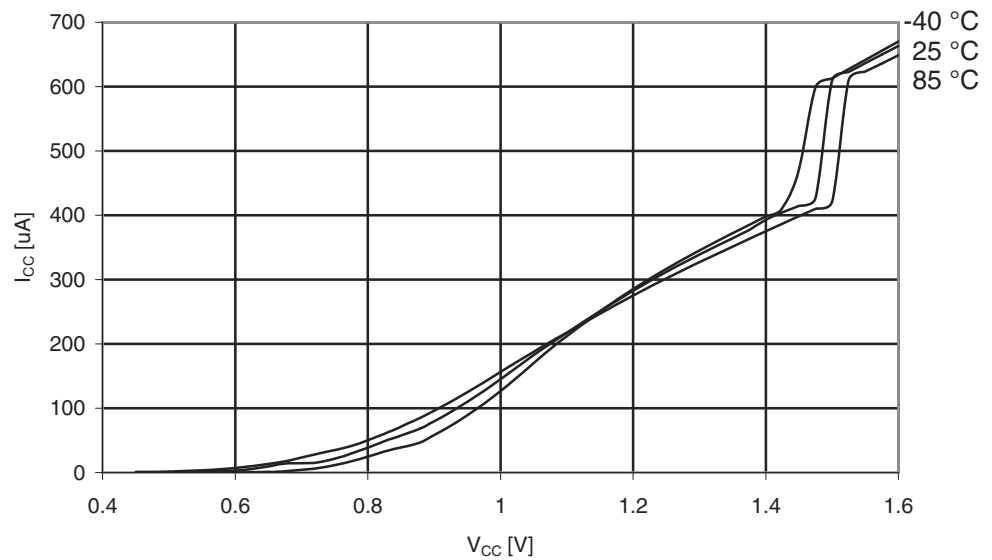


Figure 35-40. Power-up current consumption vs. V_{CC}



Problem fix/Workaround

Do not set the BOD level higher than VCC even if the BOD is not used.

11. DAC is nonlinear and inaccurate when reference is above 2.4V or VCC - 0.6V

Using the DAC with a reference voltage above 2.4V or VCC - 0.6V will give inaccurate output when converting codes that give below 0.75V output:

- ± 10 LSB for continuous mode
- ± 200 LSB for Sample and Hold mode

Problem fix/Workaround

None.

12. DAC has increased INL or noise for some operating conditions

Some DAC configurations or operating condition will result in increased output error.

- Continuous mode: ± 5 LSB
- Sample and hold mode: ± 15 LSB
- Sample and hold mode for reference above 2.0V: up to ± 100 LSB

Problem fix/Workaround

None.

13. DAC refresh may be blocked in S/H mode

If the DAC is running in Sample and Hold (S/H) mode and conversion for one channel is done at maximum rate (i.e. the DAC is always busy doing conversion for this channel), this will block refresh signals to the second channel.

Problem fix/Workaround

When using the DAC in S/H mode, ensure that none of the channels is running at maximum conversion rate, or ensure that the conversion rate of both channels is high enough to not require refresh.

14. Conversion lost on DAC channel B in event triggered mode

If during dual channel operation channel 1 is set in auto triggered conversion mode, channel 1 conversions are occasionally lost. This means that not all data-values written to the Channel 1 data register are converted.

Problem fix/Workaround

Keep the DAC conversion interval in the range 000-001 (1 and 3 CLK), and limit the Peripheral clock frequency so the conversion interval never is shorter than 1.5 μ s.

15. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/Workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELoad) is set. Do not write NVM DATA0 when EELoad is set.

36.1.3 rev. A

- Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously
- ADC gain stage output range is limited to 2.4V
- Sampled BOD in Active mode will cause noise when bandgap is used as reference
- Flash Power Reduction Mode can not be enabled when entering sleep mode
- JTAG enable does not override Analog Comparator B output
- Bandgap measurement with the ADC is non-functional when V_{CC} is below 2.7V
- DAC refresh may be blocked in S/H mode
- BOD will be enabled after any reset
- Both DFLLs and both oscillators has to be enabled for one to work
- Operating frequency and voltage limitations
- Inverted I/O enable does not affect Analog Comparator Output

1. Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously

If the bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for the another AC, the first comparator will be affected for up to 1 us and could potentially give a wrong comparison result.

Problem fix/Workaround

If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. ADC gain stage output range is limited to 2.4 V

The amplified output of the ADC gain stage will never go above 2.4 V, hence the differential input will only give correct output when below 2.4 V/gain. For the available gain settings, this gives a differential input range of:

–	1x	gain:	2.4	V
–	2x	gain:	1.2	V
–	4x	gain:	0.6	V
–	8x	gain:	300	mV
–	16x	gain:	150	mV
–	32x	gain:	75	mV
–	64x	gain:	38	mV

Problem fix/Workaround

Keep the amplified voltage output from the ADC gain stage below 2.4 V in order to get a correct result, or keep ADC voltage reference below 2.4 V.

3. Sampled BOD in Active mode will cause noise when bandgap is used as reference

Using the BOD in sampled mode when the device is running in Active or Idle mode will add noise on the bandgap reference for ADC, DAC and Analog Comparator.

Problem fix/Workaround

If the bandgap is used as reference for either the ADC, DAC and Analog Comparator, the BOD must not be set in sampled mode.

Problem fix/Workaround

Keep the amplified voltage output from the ADC gain stage below 2.4 V in order to get a correct result, or keep ADC voltage reference below 2.4 V.

5. ADC Event on compare match non-functional

ADC signalling event will be given at every conversion complete even if Interrupt mode (INT-MODE) is set to BELOW or ABOVE.

Problem fix/Workaround

Enable and use interrupt on compare match when using the compare function.

6. Bandgap measurement with the ADC is non-functional when VCC is below 2.7V

The ADC can not be used to do bandgap measurements when VCC is below 2.7V.

Problem fix/Workaround

None.

7. Accuracy lost on first three samples after switching input to ADC gain stage

Due to memory effect in the ADC gain stage, the first three samples after changing input channel must be disregarded to achieve 12-bit accuracy.

Problem fix/Workaround

Run three ADC conversions and discard these results after changing input channels to ADC gain stage.

8. Configuration of PGM and CWCM not as described in XMEGA A Manual

Enabling Common Waveform Channel Mode will enable Pattern generation mode (PGM), but not Common Waveform Channel Mode.

Enabling Pattern Generation Mode (PGM) and not Common Waveform Channel Mode (CWCM) will enable both Pattern Generation Mode and Common Waveform Channel Mode.

Problem fix/Workaround

Table 36-3. Configure PWM and CWCM according to this table:

PGM	CWCM	Description
0	0	PGM and CWCM disabled
0	1	PGM enabled
1	0	PGM and CWCM enabled
1	1	PGM enabled

9. PWM is not restarted properly after a fault in cycle-by-cycle mode

When the AWeX fault restore mode is set to cycle-by-cycle, the waveform output will not return to normal operation at first update after fault condition is no longer present.

Problem fix/Workaround

Do a write to any AWeX I/O register to re-enable the output.

10. BOD will be enabled after any reset

If any reset source goes active, the BOD will be enabled and keep the device in reset if the VCC voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until VCC is above the programmed BOD level even if the BOD is disabled.

36.2.2 rev. B

- Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously
- VCC voltage scaler for AC is non-linear
- ADC has increased INL error for some operating conditions
- ADC gain stage output range is limited to 2.4 V
- ADC Event on compare match non-functional
- Bandgap measurement with the ADC is non-functional when VCC is below 2.7V
- Accuracy lost on first three samples after switching input to ADC gain stage
- Configuration of PGM and CWCM not as described in XMEGA A Manual
- PWM is not restarted properly after a fault in cycle-by-cycle mode
- BOD will be enabled at any reset
- DAC is nonlinear and inaccurate when reference is above 2.4V or VCC - 0.6V
- DAC has increased INL or noise for some operating conditions
- DAC refresh may be blocked in S/H mode
- Conversion lost on DAC channel B in event triggered mode
- EEPROM page buffer always written when NVM DATA0 is written
- Pending full asynchronous pin change interrupts will not wake the device
- Pin configuration does not affect Analog Comparator Output
- NMI Flag for Crystal Oscillator Failure automatically cleared
- Writing EEPROM or Flash while reading any of them will not work
- Crystal start-up time required after power-save even if crystal is source for RTC
- RTC Counter value not correctly read after sleep
- Pending asynchronous RTC-interrupts will not wake up device
- TWI Transmit collision flag not cleared on repeated start
- Clearing TWI Stop Interrupt Flag may lock the bus
- TWI START condition at bus timeout will cause transaction to be dropped
- TWI Data Interrupt Flag (DIF) erroneously read as set
- WDR instruction inside closed window will not issue reset

1. Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously

If the Bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for another AC, the first comparator will be affected for up to 1 μ s and could potentially give a wrong comparison result.

Problem fix/Workaround

If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. VCC voltage scaler for AC is non-linear

The 6-bit VCC voltage scaler in the Analog Comparators is non-linear.

Problem fix/Workaround

Wait at least one prescaled RTC clock cycle before reading the RTC CNT value.

22. Pending asynchronous RTC-interrupts will not wake up device

Asynchronous Interrupts from the Real-Time-Counter that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again.

Problem fix/Workaround

None.

23. TWI Transmit collision flag not cleared on repeated start

The TWI transmit collision flag should be automatically cleared on start and repeated start, but is only cleared on start.

Problem fix/Workaround

Clear the flag in software after address interrupt.

24. Clearing TWI Stop Interrupt Flag may lock the bus

If software clears the STOP Interrupt Flag (APIF) on the same Peripheral Clock cycle as the hardware sets this flag due to a new address received, CLKHOLD is not cleared and the SCL line is not released. This will lock the bus.

Problem fix/Workaround

Check if the bus state is IDLE. If this is the case, it is safe to clear APIF. If the bus state is not IDLE, wait for the SCL pin to be low before clearing APIF.

Code:

```
/* Only clear the interrupt flag if within a "safe zone". */
while ( /* Bus not IDLE: */
        ((COMMS_TWI.MASTER.STATUS & TWI_MASTER_BUSSTATE_gm) !=
         TWI_MASTER_BUSSTATE_IDLE_gc) &&
        /* SCL not held by slave: */
        !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm)
      )
{
    /* Ensure that the SCL line is low */
    if ( !(COMMS_PORT.IN & PIN1_bm) )
        if ( !(COMMS_PORT.IN & PIN1_bm) )
            break;
}
/* Check for an pending address match interrupt */
if ( !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm) )
{
    /* Safely clear interrupt flag */
    COMMS_TWI.SLAVE.STATUS |= (uint8_t)TWI_SLAVE_APIF_bm;
}
```

25. TWI START condition at bus timeout will cause transaction to be dropped

If Bus Timeout is enabled and a timeout occurs on the same Peripheral Clock cycle as a START is detected, the transaction will be dropped.

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