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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	256KB (128K x 16)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega256a3-mhr

7.7 Flash and EEPROM Page Size

The Flash Program Memory and EEPROM data memory are organized in pages. The pages are word accessible for the Flash and byte accessible for the EEPROM.

Table 7-2 on page 14 shows the Flash Program Memory organization. Flash write and erase operations are performed on one page at a time, while reading the Flash is done one byte at a time. For Flash access the Z-pointer (Z[m:n]) is used for addressing. The most significant bits in the address (FPAGE) gives the page number and the least significant address bits (FWORD) gives the word in the page.

Table 7-2. Number of words and Pages in the Flash.

Devices	Flash Size	Page Size (words)	FWORD	FPAGE	Application		Boot	
					Size	No of Pages	Size	No of Pages
ATxmega64A3	64 KB + 4 KB	128	Z[7:1]	Z[16:8]	64K	256	4 KB	16
ATxmega128A3	128 KB + 8 KB	256	Z[8:1]	Z[17:9]	128K	256	8 KB	16
ATxmega192A3	192 KB + 8 KB	256	Z[8:1]	Z[18:9]	192K	384	8 KB	16
ATxmega256A3	256 KB + 8 KB	256	Z[8:1]	Z[18:9]	256K	512	8 KB	16

Table 7-3 on page 14 shows EEPROM memory organization for the XMEGA A3 devices. EEPROM write and erase operations can be performed one page or one byte at a time, while reading the EEPROM is done one byte at a time. For EEPROM access the NVM Address Register (ADDR[m:n]) is used for addressing. The most significant bits in the address (E2PAGE) gives the page number and the least significant address bits (E2BYTE) gives the byte in the page.

Table 7-3. Number of bytes and Pages in the EEPROM.

Devices	EEPROM Size	Page Size (Bytes)	E2BYTE	E2PAGE	No of Pages
ATxmega64A3	2 KB	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega128A3	2 KB	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega192A3	2 KB	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega256A3	4 KB	32	ADDR[4:0]	ADDR[11:5]	128

9. Event System

9.1 Features

- Inter-peripheral communication and signalling with minimum latency
- CPU and DMA independent operation
- 8 Event Channels allows for up to 8 signals to be routed at the same time
- Events can be generated by
 - Timer/Counters (TCxn)
 - Real Time Counter (RTC)
 - Analog to Digital Converters (ADCx)
 - Analog Comparators (ACx)
 - Ports (PORTx)
 - System Clock (Clk_{SYS})
 - Software (CPU)
- Events can be used by
 - Timer/Counters (TCxn)
 - Analog to Digital Converters (ADCx)
 - Digital to Analog Converters (DACx)
 - Ports (PORTx)
 - DMA Controller (DMAC)
 - IR Communication Module (IRCOM)
- The same event can be used by multiple peripherals for synchronized timing
- Advanced Features
 - Manual Event Generation from software (CPU)
 - Quadrature Decoding
 - Digital Filtering
- Functions in Active and Idle mode

9.2 Overview

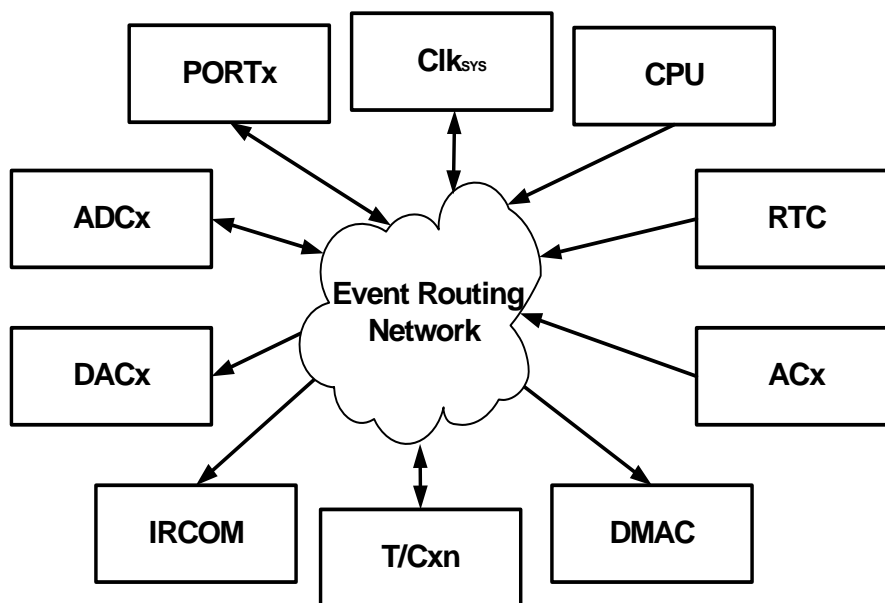
The Event System is a set of features for inter-peripheral communication. It enables the possibility for a change of state in one peripheral to automatically trigger actions in one or more peripherals. What changes in a peripheral that will trigger actions in other peripherals are configurable by software. It is a simple, but powerful system as it allows for autonomous control of peripherals without any use of interrupts, CPU or DMA resources.

The indication of a change in a peripheral is referred to as an event, and is usually the same as the interrupt conditions for that peripheral. Events are passed between peripherals using a dedicated routing network called the Event Routing Network. Figure 9-1 on page 17 shows a basic block diagram of the Event System with the Event Routing Network and the peripherals to which it is connected. This highly flexible system can be used for simple routing of signals, pin functions or for sequencing of events.

The maximum latency is two CPU clock cycles from when an event is generated in one peripheral, until the actions are triggered in one or more other peripherals.

The Event System is functional in both Active and Idle modes.

Figure 9-1. Event system block diagram.



The Event Routing Network can directly connect together ADCs, DACs, Analog Comparators (ACx), I/O ports (PORTx), the Real-time Counter (RTC), Timer/Counters (T/C) and the IR Communication Module (IRCOM). Events can also be generated from software (CPU).

All events from all peripherals are always routed into the Event Routing Network. This consists of eight multiplexers where each can be configured in software to select which event to be routed into that event channel. All eight event channels are connected to the peripherals that can use events, and each of these peripherals can be configured to use events from one or more event channels to automatically trigger a software selectable action.

10.3.3 32.768 kHz Crystal Oscillator

The 32.768 kHz Crystal Oscillator is a low power driver for an external watch crystal. It can be used as system clock source or as asynchronous clock source for the Real Time Counter.

10.3.4 0.4 - 16 MHz Crystal Oscillator

The 0.4 - 16 MHz Crystal Oscillator is a driver intended for driving both external resonators and crystals ranging from 400 kHz to 16 MHz.

10.3.5 2 MHz Run-time Calibrated Internal Oscillator

The 2 MHz Run-time Calibrated Internal Oscillator is a high frequency oscillator. It is calibrated during production to provide a default frequency which is close to its nominal frequency. The oscillator can use the 32.768 kHz Calibrated Internal Oscillator or the 32 kHz Crystal Oscillator as a source for calibrating the frequency run-time to compensate for temperature and voltage drift hereby optimizing the accuracy of the oscillator.

10.3.6 32 MHz Run-time Calibrated Internal Oscillator

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10.3.7 External Clock input

The external clock input gives the possibility to connect a clock from an external source.

10.3.8 PLL with Multiplication factor 1 - 31x

The PLL provides the possibility of multiplying a frequency by any number from 1 to 31. In combination with the prescalers, this gives a wide range of output frequencies from all clock sources.

12.3.6 Software reset

The MCU can be reset by the CPU writing to a special I/O register through a timed sequence.

13. WDT - Watchdog Timer

13.1 Features

- 11 selectable timeout periods, from 8 ms to 8s.
- Two operation modes
 - Standard mode
 - Window mode
- Runs from the 1 kHz output of the 32 kHz Ultra Low Power oscillator
- Configuration lock to prevent unwanted changes

13.2 Overview

The XMEGA A3 has a Watchdog Timer (WDT). The WDT will run continuously when turned on and if the Watchdog Timer is not reset within a software configurable time-out period, the microcontroller will be reset. The Watchdog Reset (WDR) instruction must be run by software to reset the WDT, and prevent microcontroller reset.

The WDT has a Window mode. In this mode the WDR instruction must be run within a specified period called a window. Application software can set the minimum and maximum limits for this window. If the WDR instruction is not executed inside the window limits, the microcontroller will be reset.

A protection mechanism using a timed write sequence is implemented in order to prevent unwanted enabling, disabling or change of WDT settings.

For maximum safety, the WDT also has an Always-on mode. This mode is enabled by programming a fuse. In Always-on mode, application software can not disable the WDT.

Table 14-1. Reset and Interrupt Vectors (Continued)

Program Address (Base Address)	Source	Interrupt Description
0x040	NVM_INT_base	Non-Volatile Memory Interrupt base
0x044	PORTB_INT_base	Port B Interrupt base
0x048	ACB_INT_base	Analog Comparator on Port B Interrupt base
0x04E	ADCB_INT_base	Analog to Digital Converter on Port B Interrupt base
0x056	PORTE_INT_base	Port E INT base
0x05A	TWIE_INT_base	Two-Wire Interface on Port E Interrupt base
0x05E	TCE0_INT_base	Timer/Counter 0 on port E Interrupt base
0x06A	TCE1_INT_base	Timer/Counter 1 on port E Interrupt base
0x072	SPIE_INT_vect	SPI on port E Interrupt vector
0x074	USARTE0_INT_base	USART 0 on port E Interrupt base
0x07A	USARTE1_INT_base	USART 1 on port E Interrupt base
0x080	PORTD_INT_base	Port D Interrupt base
0x084	PORTA_INT_base	Port A Interrupt base
0x088	ACA_INT_base	Analog Comparator on Port A Interrupt base
0x08E	ADCA_INT_base	Analog to Digital Converter on Port A Interrupt base
0x09A	TCD0_INT_base	Timer/Counter 0 on port D Interrupt base
0x0A6	TCD1_INT_base	Timer/Counter 1 on port D Interrupt base
0x0AE	SPID_INT_vector	SPI D Interrupt vector
0x0B0	USARTD0_INT_base	USART 0 on port D Interrupt base
0x0B6	USARTD1_INT_base	USART 1 on port D Interrupt base
0x0D0	PORTF_INT_base	Port F Interrupt base
0x0D8	TCF0_INT_base	Timer/Counter 0 on port F Interrupt base
0x0EE	USARTF0_INT_base	USART 0 on port F Interrupt base

17. AWEX - Advanced Waveform Extension

17.1 Features

- **Output with complementary output from each Capture channel**
- **Four Dead Time Insertion (DTI) Units, one for each Capture channel**
- **8-bit DTI Resolution**
- **Separate High and Low Side Dead-Time Setting**
- **Double Buffered Dead-Time**
- **Event Controlled Fault Protection**
- **Single Channel Multiple Output Operation (for BLDC motor control)**
- **Double Buffered Pattern Generation**

17.2 Overview

The Advanced Waveform Extension (AWEX) provides extra features to the Timer/Counter in Waveform Generation (WG) modes. The AWEX enables easy and safe implementation of for example, advanced motor control (AC, BLDC, SR, and Stepper) and power control applications.

Any WG output from a Timer/Counter 0 is split into a complimentary pair of outputs when any AWEX feature is enabled. These output pairs go through a Dead-Time Insertion (DTI) unit that enables generation of the non-inverted Low Side (LS) and inverted High Side (HS) of the WG output with dead time insertion between LS and HS switching. The DTI output will override the normal port value according to the port override setting. Optionally the final output can be inverted by using the invert I/O setting for the port pin.

The Pattern Generation unit can be used to generate a synchronized bit pattern on the port it is connected to. In addition, the waveform generator output from Compare Channel A can be distributed to, and override all port pins. When the Pattern Generator unit is enabled, the DTI unit is bypassed.

The Fault Protection unit is connected to the Event System. This enables any event to trigger a fault condition that will disable the AWEX output. Several event channels can be used to trigger fault on several different conditions.

The AWEX is available for TCC0. The notation of this is AWEXC.

22. USART

22.1 Features

- **Seven Identical USART peripherals**
- **Full Duplex Operation (Independent Serial Receive and Transmit Registers)**
- **Asynchronous or Synchronous Operation**
- **Master or Slave Clocked Synchronous Operation**
- **High-resolution Arithmetic Baud Rate Generator**
- **Supports Serial Frames with 5, 6, 7, 8, or 9 Data Bits and 1 or 2 Stop Bits**
- **Odd or Even Parity Generation and Parity Check Supported by Hardware**
- **Data OverRun Detection**
- **Framing Error Detection**
- **Noise Filtering Includes False Start Bit Detection and Digital Low Pass Filter**
- **Three Separate Interrupts on TX Complete, TX Data Register Empty and RX Complete**
- **Multi-processor Communication Mode**
- **Double Speed Asynchronous Communication Mode**
- **Master SPI mode for SPI communication**
- **IrDA support through the IRCOM module**

22.2 Overview

The Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication module. The USART supports full duplex communication, and both asynchronous and clocked synchronous operation. The USART can also be set in Master SPI mode to be used for SPI communication.

Communication is frame based, and the frame format can be customized to support a wide range of standards. The USART is buffered in both direction, enabling continued data transmission without any delay between frames. There are separate interrupt vectors for receive and transmit complete, enabling fully interrupt driven communication. Frame error and buffer overflow are detected in hardware and indicated with separate status flags. Even or odd parity generation and parity check can also be enabled.

One USART can use the IRCOM module to support IrDA 1.4 physical compliant pulse modulation and demodulation for baud rates up to 115.2 kbps.

PORTC, PORTD, and PORTE each has two USARTs, while PORTF has one USART only. Notation of these peripherals are USARTC0, USARTC1, USARTD0, USARTD1, USARTE0, USARTE1 and USARTF0, respectively.

26. DAC - 12-bit Digital to Analog Converter

26.1 Features

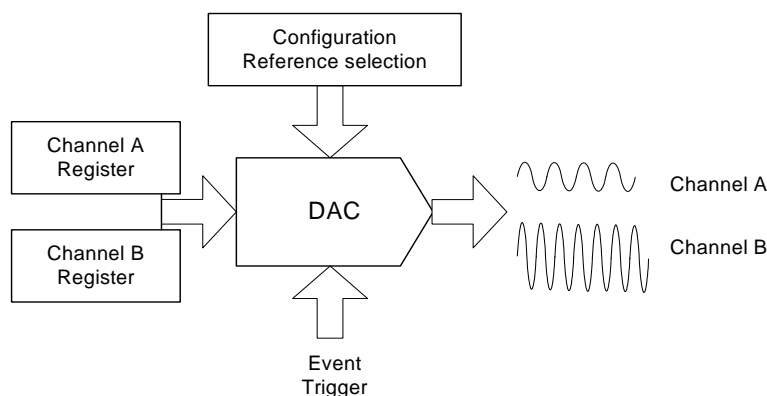
- One DAC with 12-bit resolution
- Up to 1 Msps conversion rate for each DAC
- Flexible conversion range
- Multiple trigger sources
- 1 continuous output or 2 Sample and Hold (S/H) outputs for each DAC
- Built-in offset and gain calibration
- High drive capabilities
- Low Power Mode

26.2 Overview

The XMEGA A3 features one two-channel, 12-bit, 1 Msps DACs with built-in offset and gain calibration, see Figure 26-1 on page 43.

A DAC converts a digital value into an analog signal. The DAC may use an internal 1.0 voltage as the upper limit for conversion, but it is also possible to use the supply voltage or any applied voltage in-between. The external reference input is shared with the ADC reference input.

Figure 26-1. DAC overview



The DAC has one continuous output with high drive capabilities for both resistive and capacitive loads. It is also possible to split the continuous time channel into two Sample and Hold (S/H) channels, each with separate data conversion registers.

A DAC conversion may be started from the application software by writing the data conversion registers. The DAC can also be configured to do conversions triggered by the Event System to have regular timing, independent of the application software. DMA may be used for transferring data from memory locations to DAC data registers.

The DAC has a built-in calibration system to reduce offset and gain error when loading with a calibration value from software.

PORTB each has one DAC. Notation of this peripheral is DACB.

27.3 Input Selection

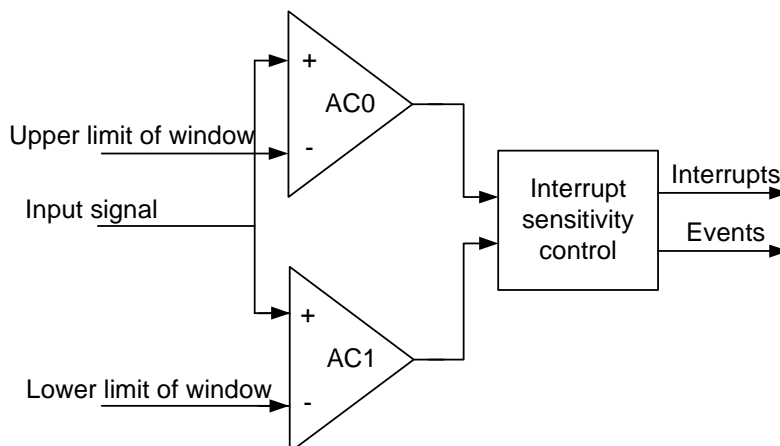
The Analog comparators have a very flexible input selection and the two comparators grouped in a pair may be used to realize a window function. One pair of analog comparators is shown in Figure 27-1 on page 45.

- Input selection from pin
 - Pin 0, 1, 2, 3, 4, 5, 6 selectable to positive input of analog comparator
 - Pin 0, 1, 3, 5, 7 selectable to negative input of analog comparator
- Internal signals available on positive analog comparator inputs
 - Output from 12-bit DAC
- Internal signals available on negative analog comparator inputs
 - 64-level scaler of the VCC, available on negative analog comparator input
 - Bandgap voltage reference
- Output from 12-bit DAC

27.4 Window Function

The window function is realized by connecting the external inputs of the two analog comparators in a pair as shown in Figure 27-2.

Figure 27-2. Analog comparator window function



Bit Number	Signal Name	Module
61	PD7.Bidir	PORT D
60	PD7.Control	
59	PD6.Bidir	
58	PD6.Control	
57	PD5.Bidir	
56	PD5.Control	
55	PD4.Bidir	
54	PD4.Control	
53	PD3.Bidir	
52	PD3.Control	
51	PD2.Bidir	
50	PD2.Control	
49	PD1.Bidir	
48	PD1.Control	
47	PD0.Bidir	
46	PD0.Control	
45	PC7.Bidir	PORT C
44	PC7.Control	
43	PC6.Bidir	
42	PC6.Control	
41	PC5.Bidir	
40	PC5.Control	
39	PC4.Bidir	
38	PC4.Control	
37	PC3.Bidir	
36	PC3.Control	
35	PC2.Bidir	
34	PC2.Control	
33	PC1.Bidir	
32	PC1.Control	
31	PC0.Bidir	
30	PC0.Control	
29	PB3.Bidir	PORT B
28	PB3.Control	
27	PB2.Bidir	
26	PB2.Control	
25	PB1.Bidir	
24	PB1.Control	
23	PB0.Bidir	
22	PB0.Control	
21	PA7.Bidir	PORT A
20	PA7.Control	
19	PA6.Bidir	
18	PA6.Control	
17	PA5.Bidir	
16	PA5.Control	
15	PA4.Bidir	
14	PA4.Control	
13	PA3.Bidir	
12	PA3.Control	
11	PA2.Bidir	
10	PA2.Control	
9	PA1.Bidir	
8	PA1.Control	
7	PA0.Bidir	
6	PA0.Control	
5	PR1.Bidir	PORT R
4	PR1.Control	
3	PR0.Bidir	
2	PR0.Control	
1	RESET.Observe_Only	RESET
0	PDI_DATA.Observe_Only	PDI Data

Figure 35-19. Reset Pull-up Resistor Current vs. Reset Pin Voltage

$V_{CC} = 3.0V$

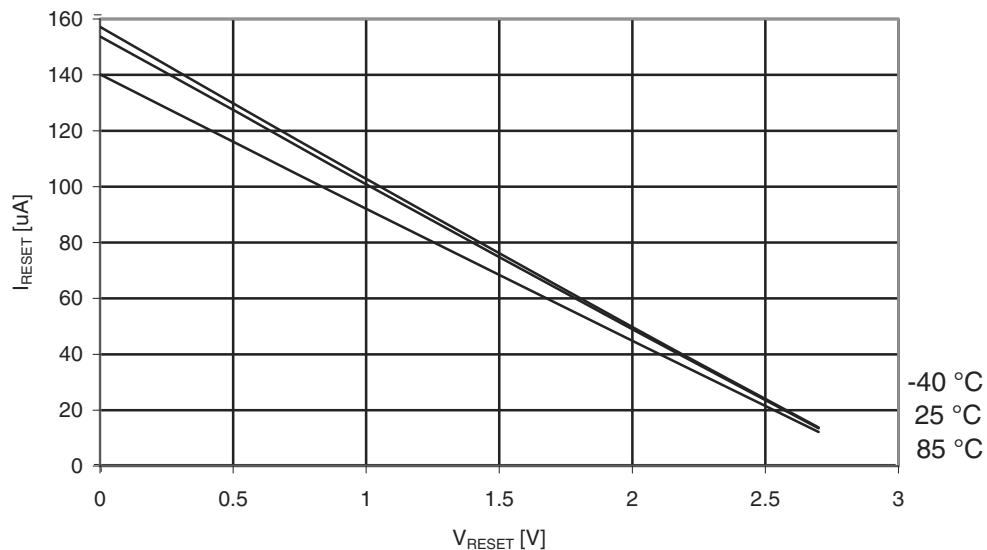


Figure 35-20. Reset Pull-up Resistor Current vs. Reset Pin Voltage

$V_{CC} = 3.3V$

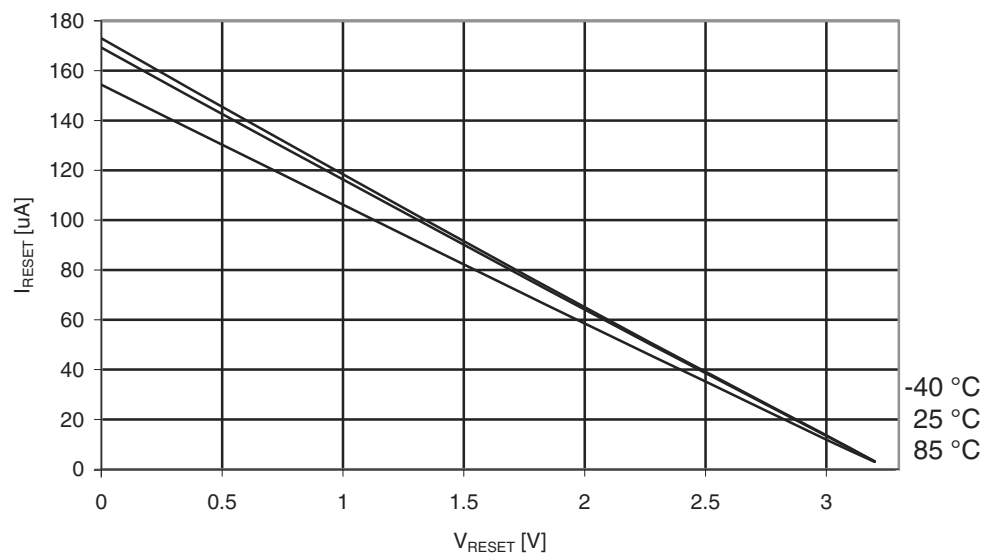


Figure 35-29. I/O Pin Input Hysteresis vs. V_{CC}

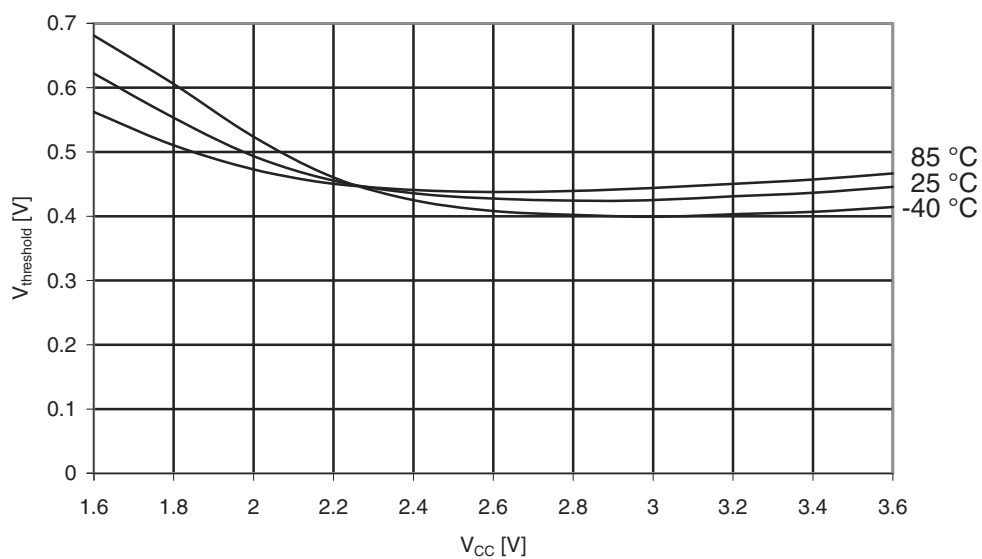
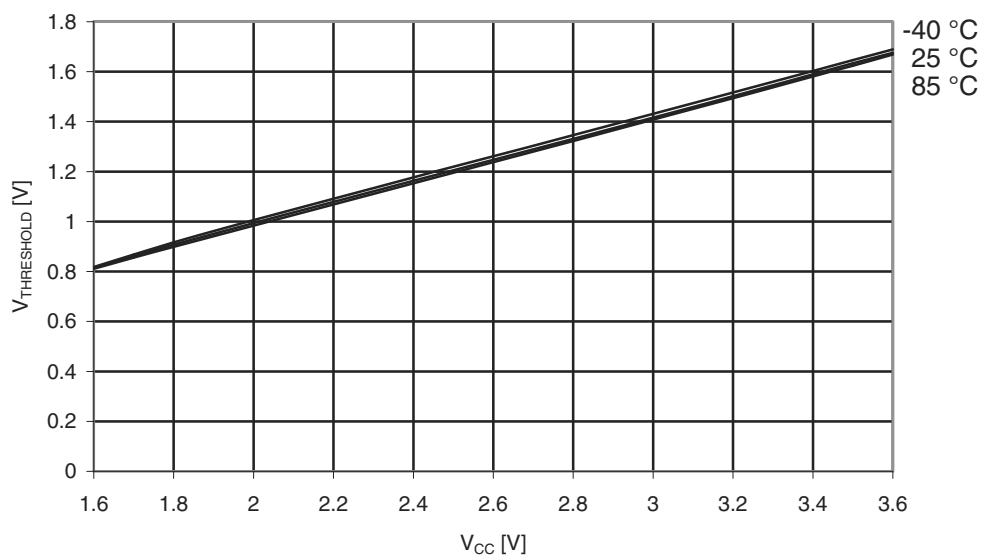


Figure 35-30. Reset Input Threshold Voltage vs. V_{CC}

V_{IH} - I/O Pin Read as "1"



Problem fix/Workaround

Do not set the BOD level higher than VCC even if the BOD is not used.

11. DAC is nonlinear and inaccurate when reference is above 2.4V or VCC - 0.6V

Using the DAC with a reference voltage above 2.4V or VCC - 0.6V will give inaccurate output when converting codes that give below 0.75V output:

- ± 10 LSB for continuous mode
- ± 200 LSB for Sample and Hold mode

Problem fix/Workaround

None.

12. DAC has increased INL or noise for some operating conditions

Some DAC configurations or operating condition will result in increased output error.

- Continuous mode: ± 5 LSB
- Sample and hold mode: ± 15 LSB
- Sample and hold mode for reference above 2.0V: up to ± 100 LSB

Problem fix/Workaround

None.

13. DAC refresh may be blocked in S/H mode

If the DAC is running in Sample and Hold (S/H) mode and conversion for one channel is done at maximum rate (i.e. the DAC is always busy doing conversion for this channel), this will block refresh signals to the second channel.

Problem fix/Workaround

When using the DAC in S/H mode, ensure that none of the channels is running at maximum conversion rate, or ensure that the conversion rate of both channels is high enough to not require refresh.

14. Conversion lost on DAC channel B in event triggered mode

If during dual channel operation channel 1 is set in auto triggered conversion mode, channel 1 conversions are occasionally lost. This means that not all data-values written to the Channel 1 data register are converted.

Problem fix/Workaround

Keep the DAC conversion interval in the range 000-001 (1 and 3 CLK), and limit the Peripheral clock frequency so the conversion interval never is shorter than 1.5 μ s.

15. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/Workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELoad) is set. Do not write NVM DATA0 when EELoad is set.

Problem fix/Workaround

Wait at least one prescaled RTC clock cycle before reading the RTC CNT value.

22. Pending asynchronous RTC-interrupts will not wake up device

Asynchronous Interrupts from the Real-Time-Counter that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again.

Problem fix/Workaround

None.

23. TWI Transmit collision flag not cleared on repeated start

The TWI transmit collision flag should be automatically cleared on start and repeated start, but is only cleared on start.

Problem fix/Workaround

Clear the flag in software after address interrupt.

24. Clearing TWI Stop Interrupt Flag may lock the bus

If software clears the STOP Interrupt Flag (APIF) on the same Peripheral Clock cycle as the hardware sets this flag due to a new address received, CLKHOLD is not cleared and the SCL line is not released. This will lock the bus.

Problem fix/Workaround

Check if the bus state is IDLE. If this is the case, it is safe to clear APIF. If the bus state is not IDLE, wait for the SCL pin to be low before clearing APIF.

Code:

```
/* Only clear the interrupt flag if within a "safe zone". */
while ( /* Bus not IDLE: */
        ((COMMS_TWI.MASTER.STATUS & TWI_MASTER_BUSSTATE_gm) !=
         TWI_MASTER_BUSSTATE_IDLE_gc) &&
        /* SCL not held by slave: */
        !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm)
      )
{
    /* Ensure that the SCL line is low */
    if ( !(COMMS_PORT.IN & PIN1_bm) )
        if ( !(COMMS_PORT.IN & PIN1_bm) )
            break;
}
/* Check for an pending address match interrupt */
if ( !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm) )
{
    /* Safely clear interrupt flag */
    COMMS_TWI.SLAVE.STATUS |= (uint8_t)TWI_SLAVE_APIF_bm;
}
```

25. TWI START condition at bus timeout will cause transaction to be dropped

If Bus Timeout is enabled and a timeout occurs on the same Peripheral Clock cycle as a START is detected, the transaction will be dropped.

26. WDR instruction inside closed window will not issue reset

When a WDR instruction is execute within one ULP clock cycle after updating the window control register, the counter can be cleared without giving a system reset.

Problem fix/Workaround

Wait at least one ULP clock cycle before executing a WDR instruction.

Problem fix/Workaround

Do not set the BOD level higher than VCC even if the BOD is not used.

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Problem fix/Workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELoad) is set. Do not write NVM DATA0 when EELoad is set.

8. Updated "DAC Characteristics" on page 68. Removed DC output impedance.
9. Updated Figure 35-6 on page 74. Replaced the figure by a correct one.
10. Fixed typo in "Errata" section.

37.5 8068Q – 02/10

1. Added "PDI Speed" on page 92.

37.6 8068P – 02/10

1. Updated the device pin-out Figure 2-1 on page 3. PDI_CLK and PDI_DATA renamed only PDI.
2. Removed JTAG Reset from the datasheet.
3. Updated "DAC - 12-bit Digital to Analog Converter" on page 43. DAC uses internal 1.0 voltage.
4. Added Table 34-19 on page 71.
5. Updated "Timer/Counter and AWEX functions" on page 49.
6. Updated "Alternate Pin Function Description" on page 49.
7. Updated all "Electrical Characteristics" on page 63.
8. Updated "PAD Characteristics" on page 69.
9. Changed Internal Oscillator Speed to "Oscillators and Wake-up Time" on page 88.
10. Updated "Errata" on page 93

37.7 8068O – 11/09

1. Updated Table 34-3 on page 66, Endurance and Data Retention.
2. Updated Table 34-11 on page 69, Input hysteresis is in V and not in mV.
3. Updated "Errata" on page 93.

37.8 8068N – 10/09

1. Updated "Errata" on page 93.

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