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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64a3-au

This concept enables instructions to be executed in every clock cycle. The program memory is In-System Re-programmable Flash memory.

6.3 Register File

The fast-access Register File contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This allows single-cycle Arithmetic Logic Unit (ALU) operation. In a typical ALU operation, two operands are output from the Register File, the operation is executed, and the result is stored back in the Register File - in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for Data Space addressing - enabling efficient address calculations. One of these address pointers can also be used as an address pointer for look up tables in Flash program memory.

6.4 ALU - Arithmetic Logic Unit

The high performance Arithmetic Logic Unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single register operations can also be executed. Within a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate are executed. After an arithmetic or logic operation, the Status Register is updated to reflect information about the result of the operation.

The ALU operations are divided into three main categories – arithmetic, logical, and bit-functions. Both 8- and 16-bit arithmetic is supported, and the instruction set allows for easy implementation of 32-bit arithmetic. The ALU also provides a powerful multiplier supporting both signed and unsigned multiplication and fractional format.

6.5 Program Flow

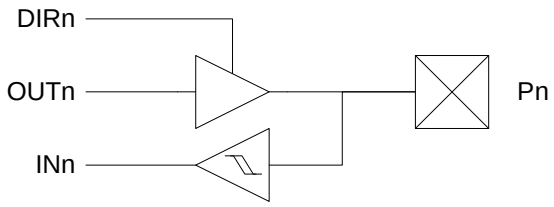
When the device is powered on, the CPU starts to execute instructions from the lowest address in the Flash Program Memory ‘0’. The Program Counter (PC) addresses the next instruction to be fetched. After a reset, the PC is set to location ‘0’.

Program flow is provided by conditional and unconditional jump and call instructions, capable of addressing the whole address space directly. Most AVR instructions use a 16-bit word format, while a limited number uses a 32-bit format.

During interrupts and subroutine calls, the return address PC is stored on the Stack. The Stack is effectively allocated in the general data SRAM, and consequently the Stack size is only limited by the total SRAM size and the usage of the SRAM. After reset the Stack Pointer (SP) points to the highest address in the internal SRAM. The SP is read/write accessible in the I/O memory space, enabling easy implementation of multiple stacks or stack areas. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR CPU.

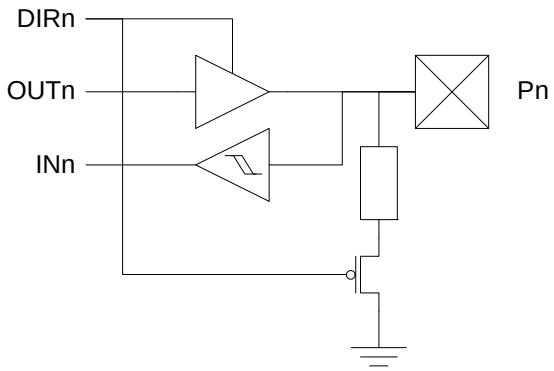
15.3.1 Push-pull

Figure 15-1. I/O configuration - Totem-pole



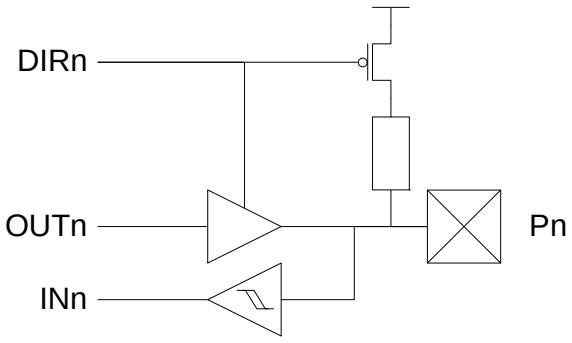
15.3.2 Pull-down

Figure 15-2. I/O configuration - Totem-pole with pull-down (on input)



15.3.3 Pull-up

Figure 15-3. I/O configuration - Totem-pole with pull-up (on input)



15.3.4 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

18. Hi-Res - High Resolution Extension

18.1 Features

- **Increases Waveform Generator resolution by 2-bits (4x)**
- **Supports Frequency, single- and dual-slope PWM operation**
- **Supports the AWEX when this is enabled and used for the same Timer/Counter**

18.2 Overview

The Hi-Resolution (Hi-Res) Extension is able to increase the resolution of the waveform generation output by a factor of 4. When enabled for a Timer/Counter, the Fast Peripheral clock running at four times the CPU clock speed will be as input to the Timer/Counter.

The High Resolution Extension can also be used when an AWEX is enabled and used with a Timer/Counter.

XMEGA A3 devices have four Hi-Res Extensions that each can be enabled for each Timer/Counters pair on PORTC, PORTD, PORTE and PORTF. The notation of these are HIRESC, HIRESD, HIRESE and HIRESF, respectively.

Table 30-6. Port F - Alternate functions

PORT F	PIN #	INTERRUPT	TCF0	USARTF0
PF0	46	SYNC	OC0A	
PF1	47	SYNC	OC0B	XCK0
PF2	48	SYNC/ASYNC	OC0C	RXD0
PF3	49	SYNC	OC0D	TXD0
PF4	50	SYNC		
PF5	51	SYNC		
PF6	54	SYNC		
PF7	55	SYNC		
GND	52			
VCC	53			

Table 30-7. Port R- Alternate functions

PORT R	PIN #	INTERRUPT	PROGR	XTAL
PDI	56		PDI_DATA	
$\overline{\text{RESET}}$	57		PDI_CLOCK	
PRO	58	SYNC		XTAL2
PR1	59	SYNC		XTAL1

Table 30-8. ATxmega256/192/128/64A3 Boundary Scan Order

Bit Number	Signal Name	Module
149	PQ3.Bidir	PORT Q
148	PQ3.Control	
147	PQ2.Bidir	
146	PQ2.Control	
145	PQ1.Bidir	
144	PQ1.Control	
143	PQ0.Bidir	
142	PQ0.Control	
141	PK7.Bidir	PORT K
140	PK7.Control	
139	PK6.Bidir	
138	PK6.Control	
137	PK5.Bidir	
136	PK5.Control	
135	PK4.Bidir	
134	PK4.Control	
133	PK3.Bidir	
132	PK3.Control	
131	PK2.Bidir	
130	PK2.Control	
129	PK1.Bidir	
128	PK1.Control	
127	PK0.Bidir	
126	PK0.Control	

34. Electrical Characteristics

All typical values are measured at T = 25°C unless other temperature condition is given. All minimum and maximum values are valid across operating temperature and voltage unless other conditions are given.

34.1 Absolute Maximum Ratings*

Operating Temperature..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Voltage on any Pin with respect to Ground..-0.5V to V_{CC}+0.5V
Maximum Operating Voltage 3.6V
DC Current per I/O Pin ..... 20.0 mA
DC Current V_{CC} and GND Pins..... 200.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

34.2 DC Characteristics

Table 34-1. Current Consumption

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{CC}	Power Supply Current(1)	Active	32 kHz, Ext. Clk	V_{CC} = 1.8V		25		µA
				V_{CC} = 3.0V		71		
			1 MHz, Ext. Clk	V_{CC} = 1.8V		317		
				V_{CC} = 3.0V		697		
			2 MHz, Ext. Clk	V_{CC} = 1.8V		613	800	
				V_{CC} = 3.0V		1340	1800	
			32 MHz, Ext. Clk	V_{CC} = 3.0V		15.7	18	mA
		Idle	32 kHz, Ext. Clk	V_{CC} = 1.8V		3.6		µA
				V_{CC} = 3.0V		6.9		
			1 MHz, Ext. Clk	V_{CC} = 1.8V		112		
				V_{CC} = 3.0V		215		
			2 MHz, Ext. Clk	V_{CC} = 1.8V		224	350	
				V_{CC} = 3.0V		430	650	
			32 MHz, Ext. Clk	V_{CC} = 3.0V		6.9	8	mA
	Power-down mode	All Functions Disabled, T = 25°C		V_{CC} = 3.0V		0.1	3	µA
		All Functions Disabled, T = 85°C		V_{CC} = 3.0V		1.75	5	
		ULP, WDT, Sampled BOD, T = 25°C		V_{CC} = 1.8V		1	6	
				V_{CC} = 3.0V		1	6	
		ULP, WDT, Sampled BOD, T=85°C		V_{CC} = 3.0V		2.7	10	

34.4 Flash and EEPROM Memory Characteristics

Table 34-3. Endurance and Data Retention

Symbol	Parameter	Condition		Min	Typ	Max	Units
	Flash	Write/Erase cycles	25°C	10K			Cycle
			85°C	10K			
		Data retention	25°C	100			Year
			55°C	25			
	EEPROM	Write/Erase cycles	25°C	80K			Cycle
			85°C	30K			
		Data retention	25°C	100			Year
			55°C	25			

Table 34-4. Programming time

Symbol	Parameter	Condition	Min	Typ(1)	Max	Units
	Chip Erase	Flash, EEPROM(2) and SRAM Erase		40		ms
	Flash	Page Erase		6		
		Page Write		6		
		Page WriteAutomatic Page Erase and Write		12		
	EEPROM	Page Erase		6		
		Page Write		6		
		Page WriteAutomatic Page Erase and Write		12		

Notes: 1. Programming is timed from the internal 2MHz oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

34.5 ADC Characteristics

Table 34-5. ADC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
RES	Resolution	Programmable: 8/12	8	12	12	Bits
INL	Integral Non-Linearity	Differential mode, 500ksps	-5	±2	5	LSB
DNL	Differential Non-Linearity	Differential mode, 500ksps		< ±1		
	Gain Error			< ±10		mV
	Offset Error			< ±2		
ADC_{clk}	ADC Clock frequency	Max is 1/4 of Peripheral Clock			2000	kHz
	Conversion rate				2000	ksps
	Conversion time (propagation delay)	(RES+2)/2+GAIN RES = 8 or 12, GAIN = 0, 1, 2 or 3	5	7	8	ADC_{clk} cycles
	Sampling Time	1/2 ADC_{clk} cycle	0.25			µS
	Conversion range		0		VREF	V
AVCC	Analog Supply Voltage		V_{cc}-0.3		V_{cc}+0.3	
VREF	Reference voltage		1.0		V_{cc}-0.6	
INT1V	Internal 1.00V reference(1)			1.00		V
INTVCC	Internal V_{CC}/1.6			V_{CC}/1.6		
SCALEDVCC	Scaled internal V_{CC}/10 input			V_{CC}/10		
R_{AREF}	Reference input resistance			> 10		MΩ
	Start-up time			12	24	ADC_{clk} cycles
	Internal input sampling speed	Temp. sensor, V_{CC}/10, Bandgap			100	ksps

Note: 1. Refer to ”Bandgap Characteristics” on page 68 for more parameter details.

Table 34-6. ADC Gain Stage Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Units
	Gain error	1 to 64 gain			< ±1		%
	Offset error				< ±1		mV
Vrms	Noise level at input	64x gain	VREF = Int. 1V		0.12		
			VREF = Ext. 2V		0.06		
	Clock rate	Same as ADC				1000	kHz

Figure 35-11. Idle Supply Current vs. Vcc

f_{SYS} = 32.768 kHz internal RC

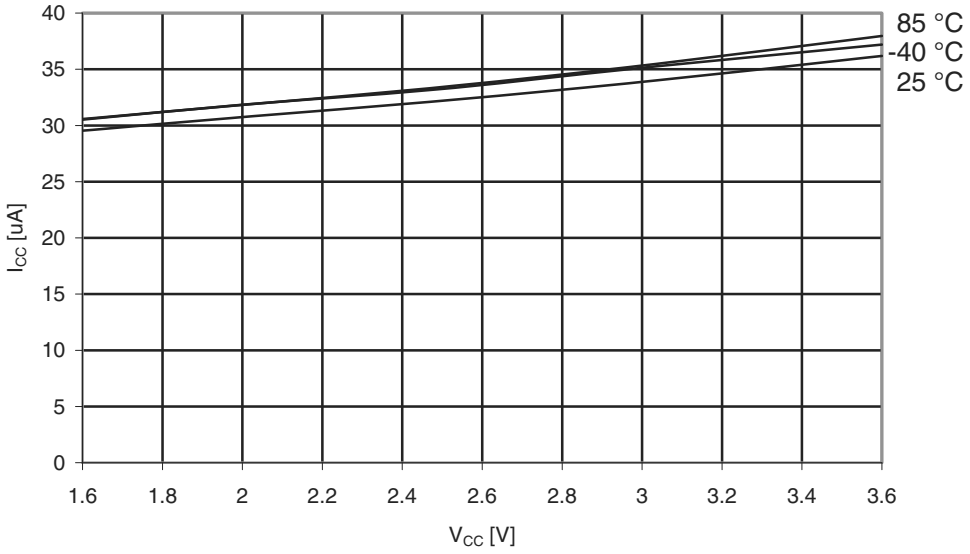
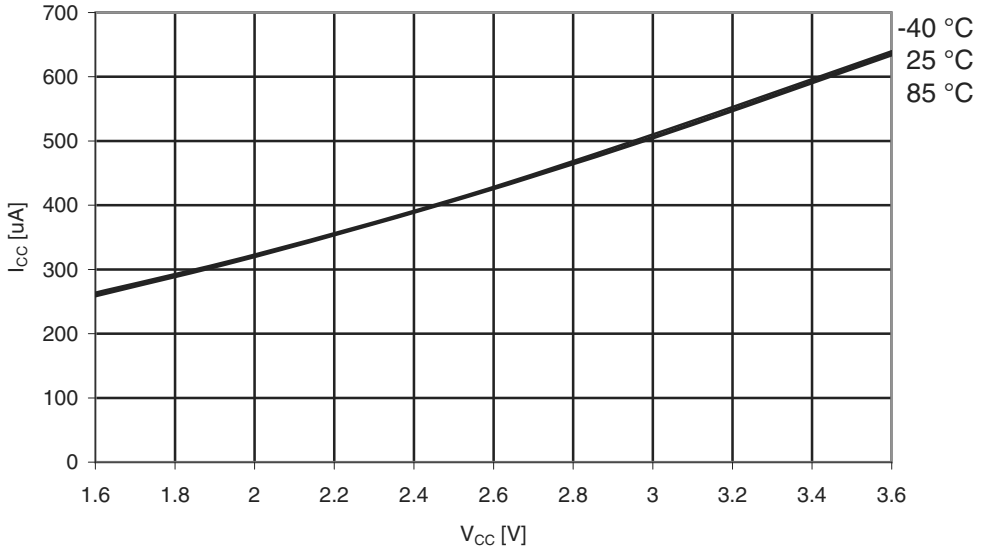


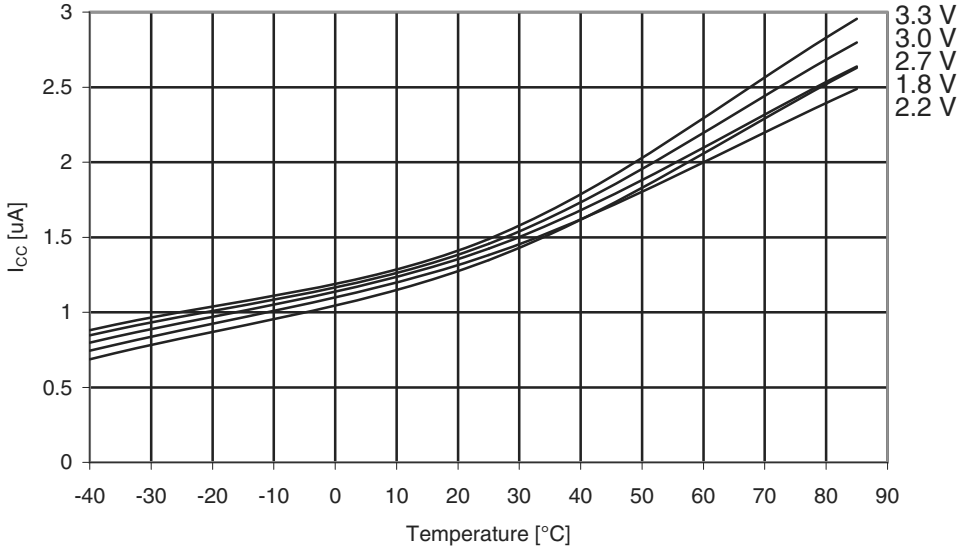
Figure 35-12. Idle Supply Current vs. Vcc

f_{SYS} = 2.0 MHz internal RC



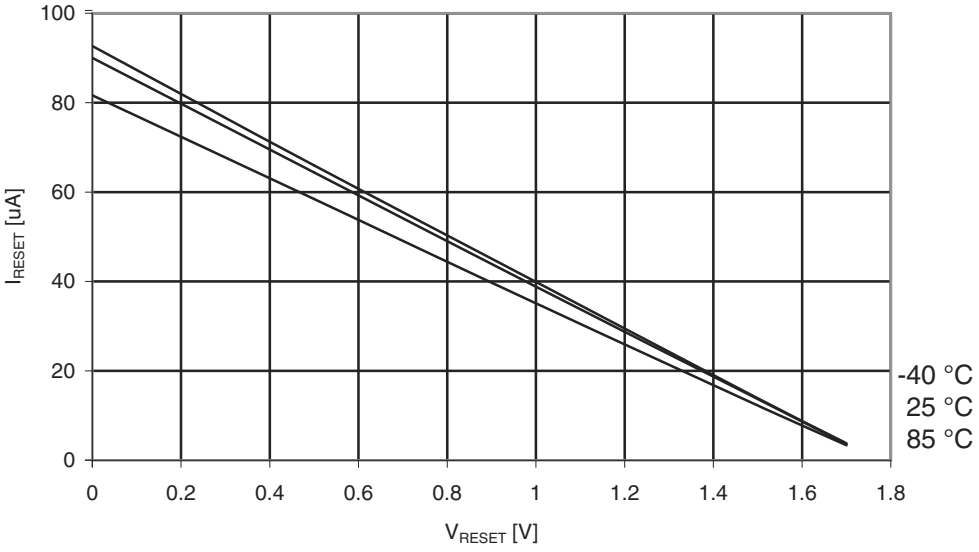
35.4 Power-save Supply Current

Figure 35-17. Power-save Supply Current vs. Temperature
With WDT, sampled BOD and RTC from ULP enabled



35.5 Pin Pull-up

Figure 35-18. Reset Pull-up Resistor Current vs. Reset Pin Voltage
V_{CC} = 1.8V



36. Errata

36.1 ATxmega256A3

36.1.1 rev. E

- **Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously**
- **VCC voltage scaler for AC is non-linear**
- **ADC has increased INL error for some operating conditions**
- **ADC gain stage output range is limited to 2.4 V**
- **ADC Event on compare match non-functional**
- **Bandgap measurement with the ADC is non-functional when VCC is below 2.7V**
- **Accuracy lost on first three samples after switching input to ADC gain stage**
- **Configuration of PGM and CWCM not as described in XMEGA A Manual**
- **PWM is not restarted properly after a fault in cycle-by-cycle mode**
- **BOD will be enabled at any reset**
- **DAC is nonlinear and inaccurate when reference is above 2.4V or VCC - 0.6V**
- **DAC has increased INL or noise for some operating conditions**
- **DAC refresh may be blocked in S/H mode**
- **Conversion lost on DAC channel B in event triggered mode**
- **EEPROM page buffer always written when NVM DATA0 is written**
- **Pending full asynchronous pin change interrupts will not wake the device**
- **Pin configuration does not affect Analog Comparator Output**
- **NMI Flag for Crystal Oscillator Failure automatically cleared**
- **Crystal start-up time required after power-save even if crystal is source for RTC**
- **RTC Counter value not correctly read after sleep**
- **Pending asynchronous RTC-interrupts will not wake up device**
- **TWI Transmit collision flag not cleared on repeated start**
- **Clearing TWI Stop Interrupt Flag may lock the bus**
- **TWI START condition at bus timeout will cause transaction to be dropped**
- **TWI Data Interrupt Flag (DIF) erroneously read as set**
- **WDR instruction inside closed window will not issue reset**

1. **Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously**

   If the Bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for another AC, the first comparator will be affected for up to 1 µs and could potentially give a wrong comparison result.

   Problem fix/Workaround

   If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. **VCC voltage scaler for AC is non-linear**

   The 6-bit VCC voltage scaler in the Analog Comparators is non-linear.

Problem fix/Workaround

Keep the amplified voltage output from the ADC gain stage below 2.4 V in order to get a correct result, or keep ADC voltage reference below 2.4 V.

5. ADC Event on compare match non-functional

ADC signalling event will be given at every conversion complete even if Interrupt mode (INTMODE) is set to BELOW or ABOVE.

Problem fix/Workaround

Enable and use interrupt on compare match when using the compare function.

6. Bandgap measurement with the ADC is non-functional when VCC is below 2.7V

The ADC can not be used to do bandgap measurements when VCC is below 2.7V.

Problem fix/Workaround

None.

7. Accuracy lost on first three samples after switching input to ADC gain stage

Due to memory effect in the ADC gain stage, the first three samples after changing input channel must be disregarded to achieve 12-bit accuracy.

Problem fix/Workaround

Run three ADC conversions and discard these results after changing input channels to ADC gain stage.

8. Configuration of PGM and CWCM not as described in XMEGA A Manual

Enabling Common Waveform Channel Mode will enable Pattern generation mode (PGM), but not Common Waveform Channel Mode.

Enabling Pattern Generation Mode (PGM) and not Common Waveform Channel Mode (CWCM) will enable both Pattern Generation Mode and Common Waveform Channel Mode.

Problem fix/Workaround

Table 36-1. Configure PWM and CWCM according to this table:

PGM	CWCM	Description
0	0	PGM and CWCM disabled
0	1	PGM enabled
1	0	PGM and CWCM enabled
1	1	PGM enabled

9. PWM is not restarted properly after a fault in cycle-by-cycle mode

When the AWeX fault restore mode is set to cycle-by-cycle, the waveform output will not return to normal operation at first update after fault condition is no longer present.

Problem fix/Workaround

Do a write to any AWeX I/O register to re-enable the output.

10. BOD will be enabled after any reset

If any reset source goes active, the BOD will be enabled and keep the device in reset if the VCC voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until VCC is above the programmed BOD level even if the BOD is disabled.

Problem fix/Workaround

Do not set the BOD level higher than VCC even if the BOD is not used.

11. DAC is nonlinear and inaccurate when reference is above 2.4V or VCC - 0.6V

Using the DAC with a reference voltage above 2.4V or VCC - 0.6V will give inaccurate output when converting codes that give below 0.75V output:

– ±10 LSB for continuous mode

– ±200 LSB for Sample and Hold mode

Problem fix/Workaround

None.

12. DAC has increased INL or noise for some operating conditions

Some DAC configurations or operating condition will result in increased output error.

– Continous mode: ±5 LSB

– Sample and hold mode: ±15 LSB

– Sample and hold mode for reference above 2.0v: up to ±100 LSB

Problem fix/Workaround

None.

13. DAC refresh may be blocked in S/H mode

If the DAC is running in Sample and Hold (S/H) mode and conversion for one channel is done at maximum rate (i.e. the DAC is always busy doing conversion for this channel), this will block refresh signals to the second channel.

Problem fix/Workaround

When using the DAC in S/H mode, ensure that none of the channels is running at maximum conversion rate, or ensure that the conversion rate of both channels is high enough to not require refresh.

14. Conversion lost on DAC channel B in event triggered mode

If during dual channel operation channel 1 is set in auto trigged conversion mode, channel 1 conversions are occasionally lost. This means that not all data-values written to the Channel 1 data register are converted.

Problem fix/Workaround

Keep the DAC conversion interval in the range 000-001 (1 and 3 CLK), and limit the Peripheral clock frequency so the conversion internal never is shorter than 1.5 µs.

15. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/Workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.

16. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

Problem fix/Workaround

None.

17. Pin configuration does not affect Analog Comparator output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output.

Problem fix/Workaround

None for Output/Pull configuration.

For inverted I/O, configure the Analog Comparator to give an inverted result (i.e. connect positive input to the negative AC input and vice versa), or use and external inverter to change polarity of Analog Comparator output.

18. NMI Flag for Crystal Oscillator Failure automatically cleared

NMI flag for Crystal Oscillator Failure (XOSCFDIF) will be automatically cleared when executing the NMI interrupt handler.

Problem fix/Workaround

This device revision has only one NMI interrupt source, so checking the interrupt source in software is not required.

19. Crystal start-up time required after power-save even if crystal is source for RTC

Even if 32.768 kHz crystal is used for RTC during sleep, the clock from the crystal will not be ready for the system before the specified start-up time. See "XOSCSEL[3:0]: Crystal Oscillator Selection" in XMEGA A Manual. If BOD is used in active mode, the BOD will be on during this period (0.5s).

Problem fix/Workaround

If faster start-up is required, go to sleep with internal oscillator as system clock.

20. RTC Counter value not correctly read after sleep

If the RTC is set to wake up the device on RTC Overflow and bit 0 of RTC CNT is identical to bit 0 of RTC PER as the device is entering sleep, the value in the RTC count register can not be read correctly within the first prescaled RTC clock cycle after wakeup. The value read will be the same as the value in the register when entering sleep.

The same applies if RTC Compare Match is used as wake-up source.

Problem fix/Workaround

Wait at least one prescaled RTC clock cycle before reading the RTC CNT value.

21. Pending asynchronous RTC-interrupts will not wake up device

Asynchronous Interrupts from the Real-Time-Counter that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again.

Problem fix/Workaround

None.

22. TWI Transmit collision flag not cleared on repeated start

The TWI transmit collision flag should be automatically cleared on start and repeated start, but is only cleared on start.

Problem fix/Workaround

Clear the flag in software after address interrupt.

23. Clearing TWI Stop Interrupt Flag may lock the bus

If software clears the STOP Interrupt Flag (APIF) on the same Peripheral Clock cycle as the hardware sets this flag due to a new address received, CLKHOLD is not cleared and the SCL line is not released. This will lock the bus.

Problem fix/Workaround

Check if the bus state is IDLE. If this is the case, it is safe to clear APIF. If the bus state is not IDLE, wait for the SCL pin to be low before clearing APIF.

Code:

```
/* Only clear the interrupt flag if within a "safe zone". */
while ( /* Bus not IDLE: */
       ((COMMS_TWI.MASTER.STATUS & TWI_MASTER_BUSSTATE_gm) !=
         TWI_MASTER_BUSSTATE_IDLE_gc)) &&
         /* SCL not held by slave: */
         !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm)
      )
{
    /* Ensure that the SCL line is low */
    if ( !(COMMS_PORT.IN & PIN1_bm) )
        if ( !(COMMS_PORT.IN & PIN1_bm) )
            break;
}
/* Check for an pending address match interrupt */
if ( !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm) )
{
    /* Safely clear interrupt flag */
    COMMS_TWI.SLAVE.STATUS |= (uint8_t)TWI_SLAVE_APIF_bm;
}
```

24. TWI START condition at bus timeout will cause transaction to be dropped

If Bus Timeout is enabled and a timeout occurs on the same Peripheral Clock cycle as a START is detected, the transaction will be dropped.

Problem fix/Workaround

None.

25. TWI Data Interrupt Flag erroneously read as set

When issuing the TWI slave response command CMD=0b11, it takes 1 Peripheral Clock cycle to clear the data interrupt flag (DIF). A read of DIF directly after issuing the command will show the DIF still set.

Problem fix/Workaround

Add one NOP instruction before checking DIF.

16. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

Problem fix/Workaround

None.

17. Pin configuration does not affect Analog Comparator output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output.

Problem fix/Workaround

None for Output/Pull configuration.

For inverted I/O, configure the Analog Comparator to give an inverted result (i.e. connect positive input to the negative AC input and vice versa), or use and external inverter to change polarity of Analog Comparator output.

18. NMI Flag for Crystal Oscillator Failure automatically cleared

NMI flag for Crystal Oscillator Failure (XOSCFDIF) will be automatically cleared when executing the NMI interrupt handler.

Problem fix/Workaround

This device revision has only one NMI interrupt source, so checking the interrupt source in software is not required.

19. Writing EEPROM or Flash while reading any of them will not work

The EEPROM and Flash cannot be written while reading EEPROM or Flash, or while executing code in Active mode.

Problem fix/Workaround

Enter IDLE sleep mode within 2.5 µs (Five 2 MHz clock cycles and 80 32 MHz clock cycles) after starting an EEPROM or flash write operation. Wake-up source must either be EEPROM ready or NVM ready interrupt. Alternatively set up a Timer/Counter to give an overflow interrupt 7 ms after the erase or write operation has started, or 13 ms after atomic erase-and-write operation has started, and then enter IDLE sleep mode.

20. Crystal start-up time required after power-save even if crystal is source for RTC

Even if 32.768 kHz crystal is used for RTC during sleep, the clock from the crystal will not be ready for the system before the specified start-up time. See "XOSCSEL[3:0]: Crystal Oscillator Selection" in XMEGA A Manual. If BOD is used in active mode, the BOD will be on during this period (0.5s).

Problem fix/Workaround

If faster start-up is required, go to sleep with internal oscillator as system clock.

21. RTC Counter value not correctly read after sleep

If the RTC is set to wake up the device on RTC Overflow and bit 0 of RTC CNT is identical to bit 0 of RTC PER as the device is entering sleep, the value in the RTC count register can not be read correctly within the first prescaled RTC clock cycle after wakeup. The value read will be the same as the value in the register when entering sleep.

The same applies if RTC Compare Match is used as wake-up source.

Problem fix/Workaround

None.

26. TWI Data Interrupt Flag erroneously read as set

When issuing the TWI slave response command CMD=0b11, it takes 1 Peripheral Clock cycle to clear the data interrupt flag (DIF). A read of DIF directly after issuing the command will show the DIF still set.

Problem fix/Workaround

Add one NOP instruction before checking DIF.

27. WDR instruction inside closed window will not issue reset

When a WDR instruction is execute within one ULP clock cycle after updating the window control register, the counter can be cleared without giving a system reset.

Problem fix/Workaround

Wait at least one ULP clock cycle before executing a WDR instruction.

22. TWI Transmit collision flag not cleared on repeated start

The TWI transmit collision flag should be automatically cleared on start and repeated start, but is only cleared on start.

Problem fix/Workaround

Clear the flag in software after address interrupt.

23. Clearing TWI Stop Interrupt Flag may lock the bus

If software clears the STOP Interrupt Flag (APIF) on the same Peripheral Clock cycle as the hardware sets this flag due to a new address received, CLKHOLD is not cleared and the SCL line is not released. This will lock the bus.

Problem fix/Workaround

Check if the bus state is IDLE. If this is the case, it is safe to clear APIF. If the bus state is not IDLE, wait for the SCL pin to be low before clearing APIF.

Code:

```
/* Only clear the interrupt flag if within a "safe zone". */
while ( /* Bus not IDLE: */
       ((COMMS_TWI.MASTER.STATUS & TWI_MASTER_BUSSTATE_gm) !=
         TWI_MASTER_BUSSTATE_IDLE_gc)) &&
         /* SCL not held by slave: */
         !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm)
      )
{
    /* Ensure that the SCL line is low */
    if ( !(COMMS_PORT.IN & PIN1_bm) )
        if ( !(COMMS_PORT.IN & PIN1_bm) )
            break;
}
/* Check for an pending address match interrupt */
if ( !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm) )
{
    /* Safely clear interrupt flag */
    COMMS_TWI.SLAVE.STATUS |= (uint8_t)TWI_SLAVE_APIF_bm;
}
```

24. TWI START condition at bus timeout will cause transaction to be dropped

If Bus Timeout is enabled and a timeout occurs on the same Peripheral Clock cycle as a START is detected, the transaction will be dropped.

Problem fix/Workaround

None.

25. TWI Data Interrupt Flag erroneously read as set

When issuing the TWI slave response command CMD=0b11, it takes 1 Peripheral Clock cycle to clear the data interrupt flag (DIF). A read of DIF directly after issuing the command will show the DIF still set.

Problem fix/Workaround

Add one NOP instruction before checking DIF.

26. WDR instruction inside closed window will not issue reset

When a WDR instruction is execute within one ULP clock cycle after updating the window control register, the counter can be cleared without giving a system reset.

Problem fix/Workaround

Wait at least one ULP clock cycle before executing a WDR instruction.

8. Updated ”DAC Characteristics” on page 68. Removed DC output impedence.
9. Updated Figure 35-6 on page 74. Replaced the figure by a correct one.
10. Fixed typo in “Errata” section.

37.5 8068Q – 02/10

1. Added ”PDI Speed” on page 92.

37.6 8068P – 02/10

1. Updated the device pin-out Figure 2-1 on page 3. PDI_CLK and PDI_DATA renamed only PDI.
2. Removed JTAG Reset from the datasheet.
3. Updated ”DAC - 12-bit Digital to Analog Converter” on page 43. DAC uses internal 1.0 voltage.
4. Added Table 34-19 on page 71.
5. Updated ”Timer/Counter and AWEX functions” on page 49.
6. Updated ”Alternate Pin Function Description” on page 49.
7. Updated all ”Electrical Characteristics” on page 63.
8. Updated ”PAD Characteristics” on page 69.
9. Changed Internal Oscillator Speed to ”Oscillators and Wake-up Time” on page 88.
10. Updated ”Errata” on page 93

37.7 8068O – 11/09

1. Updated Table 34-3 on page 66, Endurance and Data Retention.
2. Updated Table 34-11 on page 69, Input hysteresis is in V and not in mV.
3. Updated ”Errata” on page 93.

37.8 8068N – 10/09

1. Updated ”Errata” on page 93.

37.9 8068M – 09/09

1. Updated ”Electrical Characteristics” on page 63.
2. Added ”Flash and EEPROM Memory Characteristics” on page 66.
3. Added Errata for ”ATxmega192A3, ATxmega128A3, ATxmega64A3” on page 110.

37.10 8068L – 06/09

1. Updated ”Ordering Information” on page 2.
2. Updated ”Features” on page 39.
3. Updated ”Overview” on page 43.
4. Updated ”Overview” on page 48.
5. Added ”Electrical Characteristics” on page 63.
6. Added ”Typical Characteristics” on page 72.
7. Updated “”Errata” on page 93.

37.11 8068K – 02/09

1. Added ”Errata” on page 93 for ATxmega256A3 rev B.

37.12 8068J – 12/08

1. Added ”Errata” on page 93 for ATxmega256A3 rev A.

37.13 8068I – 11/08

1. Updated Featurelist in ”Memories” on page 9.

37.14 8068H – 10/08

1. Updated Table 14-1 on page 25.