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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64a3-aur

1. Ordering Information

Ordering Code	Flash	E2	SRAM	Speed (MHz)	Power Supply	Package(1)(2)(3)	Temp
ATxmega256A3-AU	256 KB + 8 KB	4 KB	16 KB	32	1.6 - 3.6V	64A	-40°C - 85°C
ATxmega192A3-AU	192 KB + 8 KB	2 KB	16 KB	32	1.6 - 3.6V		
ATxmega128A3-AU	128 KB + 8 KB	2 KB	8 KB	32	1.6 - 3.6V		
ATxmega64A3-AU	64 KB + 4 KB	2 KB	4 KB	32	1.6 - 3.6V		
ATxmega256A3-MH	256 KB + 8 KB	4 KB	16 KB	32	1.6 - 3.6V	64M2	
ATxmega192A3-MH	192 KB + 8 KB	2 KB	16 KB	32	1.6 - 3.6V		
ATxmega128A3-MH	128 KB + 8 KB	2 KB	8 KB	32	1.6 - 3.6V		
ATxmega64A3-MH	64 KB + 4 KB	2 KB	4 KB	32	1.6 - 3.6V		

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For packaging information, see ”Packaging information” on page 61.

Package Type	
64A	64-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)
64M2	64-Pad, 9 x 9 x 1.0 mm Body, Lead Pitch 0.50 mm, 7.65 mm Exposed Pad, Quad Flat No-Lead Package (QFN)

7.7 Flash and EEPROM Page Size

The Flash Program Memory and EEPROM data memory are organized in pages. The pages are word accessible for the Flash and byte accessible for the EEPROM.

Table 7-2 on page 14 shows the Flash Program Memory organization. Flash write and erase operations are performed on one page at a time, while reading the Flash is done one byte at a time. For Flash access the Z-pointer (Z[m:n]) is used for addressing. The most significant bits in the address (FPAGE) gives the page number and the least significant address bits (FWORD) gives the word in the page.

Table 7-2. Number of words and Pages in the Flash.

Devices	Flash Size	Page Size (words)	FWORD	FPAGE	Application		Boot	
					Size	No of Pages	Size	No of Pages
ATxmega64A3	64 KB + 4 KB	128	Z[7:1]	Z[16:8]	64K	256	4 KB	16
ATxmega128A3	128 KB + 8 KB	256	Z[8:1]	Z[17:9]	128K	256	8 KB	16
ATxmega192A3	192 KB + 8 KB	256	Z[8:1]	Z[18:9]	192K	384	8 KB	16
ATxmega256A3	256 KB + 8 KB	256	Z[8:1]	Z[18:9]	256K	512	8 KB	16

Table 7-3 on page 14 shows EEPROM memory organization for the XMEGA A3 devices. EEEPROM write and erase operations can be performed one page or one byte at a time, while reading the EEPROM is done one byte at a time. For EEPROM access the NVM Address Register (ADDR[m:n]) is used for addressing. The most significant bits in the address (E2PAGE) gives the page number and the least significant address bits (E2BYTE) gives the byte in the page.

Table 7-3. Number of bytes and Pages in the EEPROM.

Devices	EEPROM Size	Page Size (Bytes)	E2BYTE	E2PAGE	No of Pages
ATxmega64A3	2 KB	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega128A3	2 KB	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega192A3	2 KB	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega256A3	4 KB	32	ADDR[4:0]	ADDR[11:5]	128

8. DMAC - Direct Memory Access Controller

8.1 Features

- **Allows High-speed data transfer**
  - **From memory to peripheral**
  - **From memory to memory**
  - **From peripheral to memory**
  - **From peripheral to peripheral**
- **4 Channels**
- **From 1 byte and up to 16 M bytes transfers in a single transaction**
- **Multiple addressing modes for source and destination address**
  - **Increment**
  - **Decrement**
  - **Static**
- **1, 2, 4, or 8 bytes Burst Transfers**
- **Programmable priority between channels**

8.2 Overview

The XMEGA A3 has a Direct Memory Access (DMA) Controller to move data between memories and peripherals in the data space. The DMA controller uses the same data bus as the CPU to transfer data.

It has 4 channels that can be configured independently. Each DMA channel can perform data transfers in blocks of configurable size from 1 to 64K bytes. A repeat counter can be used to repeat each block transfer for single transactions up to 16M bytes. Each DMA channel can be configured to access the source and destination memory address with incrementing, decrementing or static addressing. The addressing is independent for source and destination address. When the transaction is complete the original source and destination address can automatically be reloaded to be ready for the next transaction.

The DMAC can access all the peripherals through their I/O memory registers, and the DMA may be used for automatic transfer of data to/from communication modules, as well as automatic data retrieval from ADC conversions, data transfer to DAC conversions, or data transfer to or from port pins. A wide range of transfer triggers is available from the peripherals, Event System and software. Each DMA channel has different transfer triggers.

To allow for continuous transfers, two channels can be interlinked so that the second takes over the transfer when the first is finished and vice versa.

The DMA controller can read from memory mapped EEPROM, but it cannot write to the EEPROM or access the Flash.

21. SPI - Serial Peripheral Interface

21.1 Features

- **Three Identical SPI peripherals**
- **Full-duplex, Three-wire Synchronous Data Transfer**
- **Master or Slave Operation**
- **LSB First or MSB First Data Transfer**
- **Seven Programmable Bit Rates**
- **End of Transmission Interrupt Flag**
- **Write Collision Flag Protection**
- **Wake-up from Idle Mode**
- **Double Speed (CK/2) Master SPI Mode**

21.2 Overview

The Serial Peripheral Interface (SPI) allows high-speed full-duplex, synchronous data transfer between different devices. Devices can communicate using a master-slave scheme, and data is transferred both to and from the devices simultaneously.

PORTC, PORTD, and PORTE each has one SPI. Notation of these peripherals are SPIC, SPID, and SPIE respectively.

27. AC - Analog Comparator

27.1 Features

- **Four Analog Comparators**
- **Selectable Power vs. Speed**
- **Selectable hysteresis**
  - **0, 20 mV, 50 mV**
- **Analog Comparator output available on pin**
- **Flexible Input Selection**
  - **All pins on the port**
  - **Output from the DAC**
  - **Bandgap reference voltage.**
  - **Voltage scaler that can perform a 64-level scaling of the internal VCC voltage.**
- **Interrupt and event generation on**
  - **Rising edge**
  - **Falling edge**
  - **Toggle**
- **Window function interrupt and event generation on**
  - **Signal above window**
  - **Signal inside window**
  - **Signal below window**

27.2 Overview

XMEGA A3 features four Analog Comparators (AC). An Analog Comparator compares two voltages, and the output indicates which input is largest. The Analog Comparator may be configured to give interrupt requests and/or events upon several different combinations of input change.

Both hysteresis and propagation delays may be adjusted in order to find the optimal operation for each application.

A wide range of input selection is available, both external pins and several internal signals can be used.

The Analog Comparators are always grouped in pairs (AC0 and AC1) on each analog port. They have identical behavior but separate control registers.

Optionally, the state of the comparator is directly available on a pin.

PORTA and PORTB each has one AC pair. Notations are ACA and ACB, respectively.

Table 30-3. Port C - Alternate functions

PORT C	PIN #	INTERRUPT	TCC0	AWEXC	TCC1	USARTC0	USARTC1	SPIC	TWIC	CLOCKOUT	EVENTOUT
PC0	16	SYNC	OC0A	OC0ALS					SDA		
PC1	17	SYNC	OC0B	OC0AHS		XCK0			SCL		
PC2	18	SYNC/ASYNC	OC0C	OC0BLS		RXD0					
PC3	19	SYNC	OC0D	OC0BHS		TXD0					
PC4	20	SYNC		OC0CLS	OC1A			$\overline{SS}$			
PC5	21	SYNC		OC0CHS	OC1B		XCK1	MOSI			
PC6	22	SYNC		OC0DLS			RXD1	MISO			
PC7	23	SYNC		OC0DHS			TXD1	SCK		CLKOUT	EVOUT
GND	24										
VCC	25										

Table 30-4. Port D - Alternate functions

PORT D	PIN #	INTERRUPT	TCD0	TCD1	USARTD0	USARTD1	SPID	CLOCKOUT	EVENTOUT
PD0	26	SYNC	OC0A						
PD1	27	SYNC	OC0B		XCK0				
PD2	28	SYNC/ASYNC	OC0C		RXD0				
PD3	29	SYNC	OC0D		TXD0				
PD4	30	SYNC		OC1A			$\overline{SS}$		
PD5	31	SYNC		OC1B		XCK1	MOSI		
PD6	32	SYNC				RXD1	MISO		
PD7	33	SYNC				TXD1	SCK	CLKOUT	EVOUT
GND	34								
VCC	35								

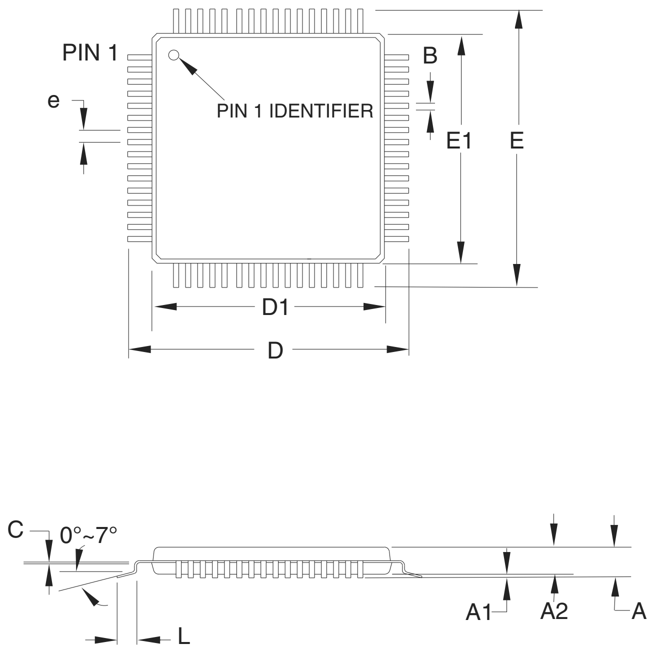
Table 30-5. Port E - Alternate functions

PORT E	PIN #	INTERRUPT	TCE0	TCE1	USARTE0	USARTE1	SPIE	TWIE	CLOCKOUT	EVENTOUT	TOSC
PE0	36	SYNC	OC0A					SDA			
PE1	37	SYNC	OC0B		XCK0			SCL			
PE2	38	SYNC/ASYNC	OC0C		RXD0						
PE3	39	SYNC	OC0D		TXD0						
PE4	40	SYNC		OC1A			$\overline{SS}$				
PE5	41	SYNC		OC1B		XCK1	MOSI				
PE6	42	SYNC				RXD1	MISO				TOSC2
PE7	43	SYNC				TXD1	SCK		CLKOUT	EVOUT	TOSC1
GND	44										
VCC	45										

Bit Number	Signal Name	Module
125	PJ7.Bidir	PORT J
124	PJ7.Control	
123	PJ6.Bidir	
122	PJ6.Control	
121	PJ5.Bidir	
120	PJ5.Control	
119	PJ4.Bidir	
118	PJ4.Control	
117	PJ3.Bidir	
116	PJ3.Control	
115	PJ2.Bidir	
114	PJ2.Control	
113	PJ1.Bidir	
112	PJ1.Control	
111	PJ0.Bidir	
110	PJ0.Control	
109	PH7.Bidir	PORT H
108	PH7.Control	
107	PH6.Bidir	
106	PH6.Control	
105	PH5.Bidir	
104	PH5.Control	
103	PH4.Bidir	
102	PH4.Control	
101	PH3.Bidir	
100	PH3.Control	
99	PH2.Bidir	
98	PH2.Control	
97	PH1.Bidir	
96	PH1.Control	
95	PH0.Bidir	
94	PH0.Control	
93	PF7.Bidir	PORT F
92	PF7.Control	
91	PF6.Bidir	
90	PF6.Control	
89	PF5.Bidir	
88	PF5.Control	
87	PF4.Bidir	
86	PF4.Control	
85	PF3.Bidir	
84	PF3.Control	
83	PF2.Bidir	
82	PF2.Control	
81	PF1.Bidir	
80	PF1.Control	
79	PF0.Bidir	
78	PF0.Control	
77	PE7.Bidir	PORT E
76	PE7.Control	
75	PE6.Bidir	
74	PE6.Control	
73	PE5.Bidir	
72	PE5.Control	
71	PE4.Bidir	
70	PE4.Control	
69	PE3.Bidir	
68	PE3.Control	
67	PE2.Bidir	
66	PE2.Control	
65	PE1.Bidir	
64	PE1.Control	
63	PE0.Bidir	
62	PE0.Control	

33. Packaging information

33.1 64A



COMMON DIMENSIONS
(Unit of measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

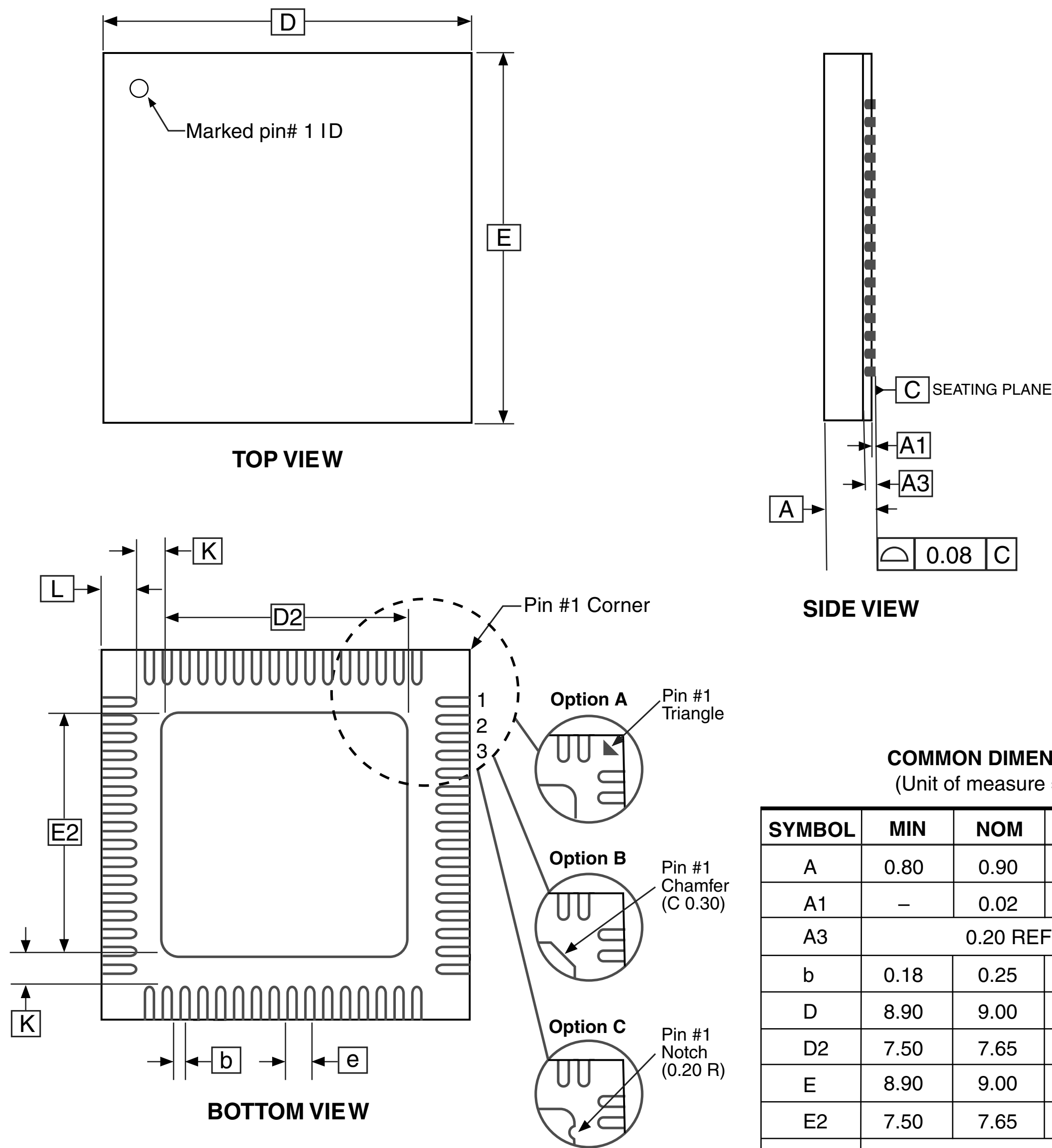
Notes:
1. This package conforms to JEDEC reference MS-026, Variation AEB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

2010-10-20

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**64A,** 64-lead, 14 x 14mm Body Size, 1.0mm Body Thickness, 0.8mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	64A	C

Not recommended for new designs - Use XMEGA A3U series

33.2 64M2



COMMON DIMENSIONS
(Unit of measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A3		0.20 REF		
b	0.18	0.25	0.30	
D	8.90	9.00	9.10	
D2	7.50	7.65	7.80	
E	8.90	9.00	9.10	
E2	7.50	7.65	7.80	
e		0.50 BSC		
L	0.35	0.40	0.45	
K	0.20	0.27	0.40	

Notes: 1. JEDEC Standard MO-220, (SAW Singulation) fig . 1, VMMD.
2. Dimension and tolerance conform to ASMEY14.5M-1994.

2010-10-20

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**64M2**, 64-pad, 9 x 9 x 1.0mm Bod y, Lead Pitch 0.50mm , 7.65mm Exposed Pad, Micro Lead Frame Package (MLF)	64M2	E

35.3 Power-down Supply Current

Figure 35-15. Power-down Supply Current vs. Temperature

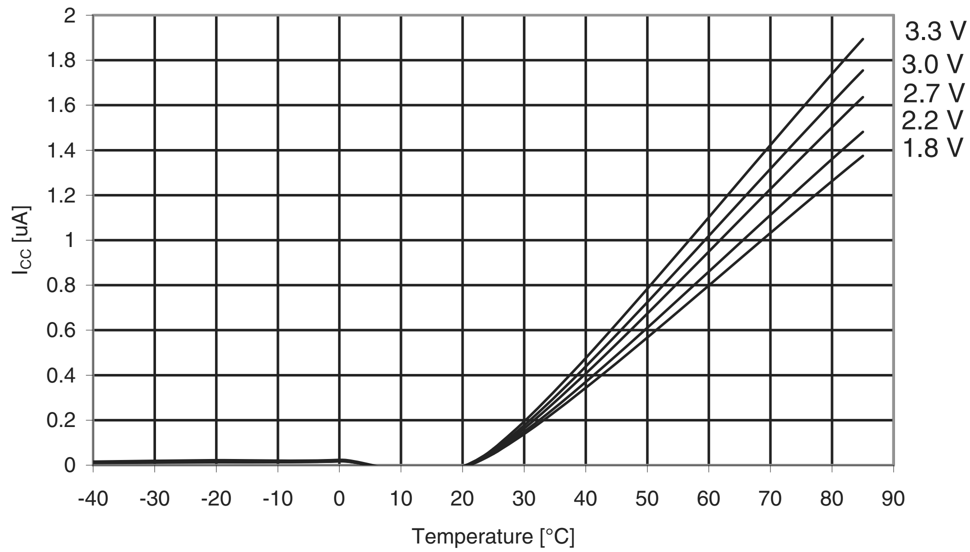
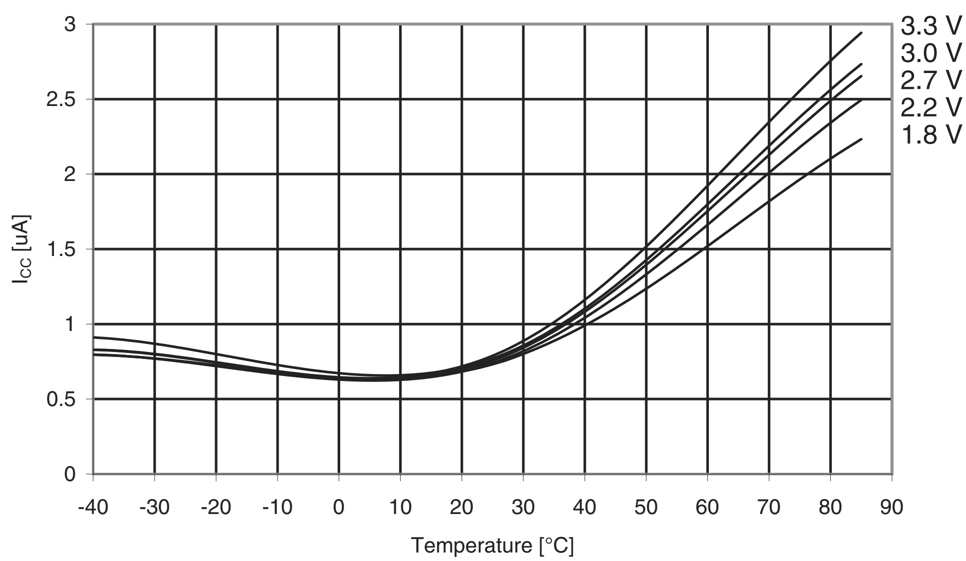


Figure 35-16. Power-down Supply Current vs. Temperature
With WDT and sampled BOD enabled.

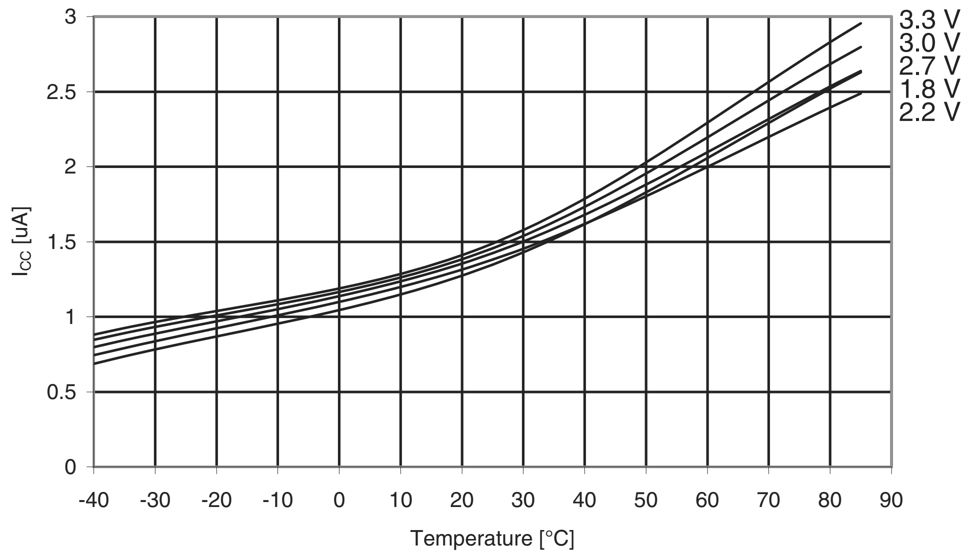


Not recommended for new designs - Use XMEGA A3U series

35.4 Power-save Supply Current

Figure 35-17. Power-save Supply Current vs. Temperature

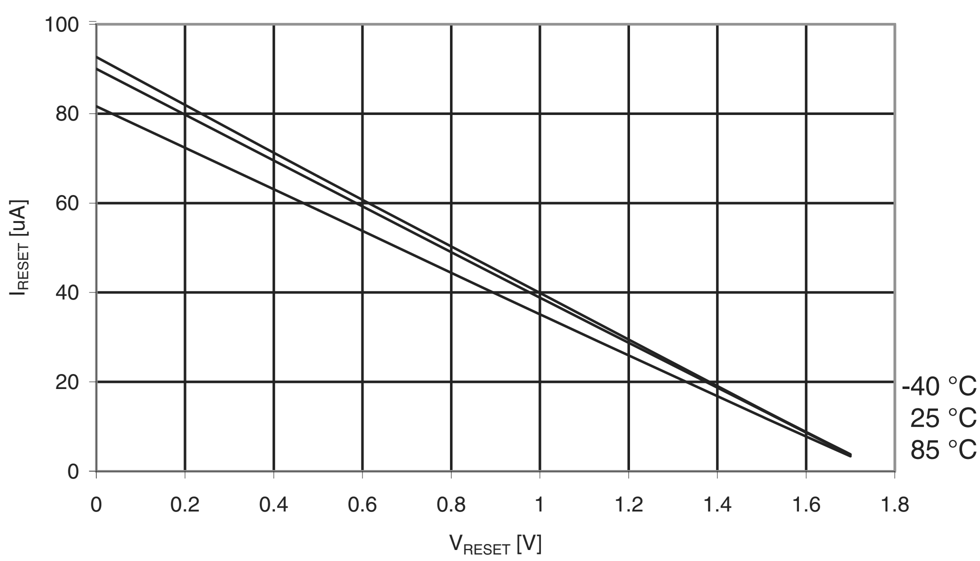
With WDT, sampled BOD and RTC from ULP enabled



35.5 Pin Pull-up

Figure 35-18. Reset Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 1.8V



Not recommended for new designs - Use XMEGA A3U series

35.6 Pin Output Voltage vs. Sink/Source Current

Figure 35-21. I/O Pin Output Voltage vs. Source Current

Vcc = 1.8V

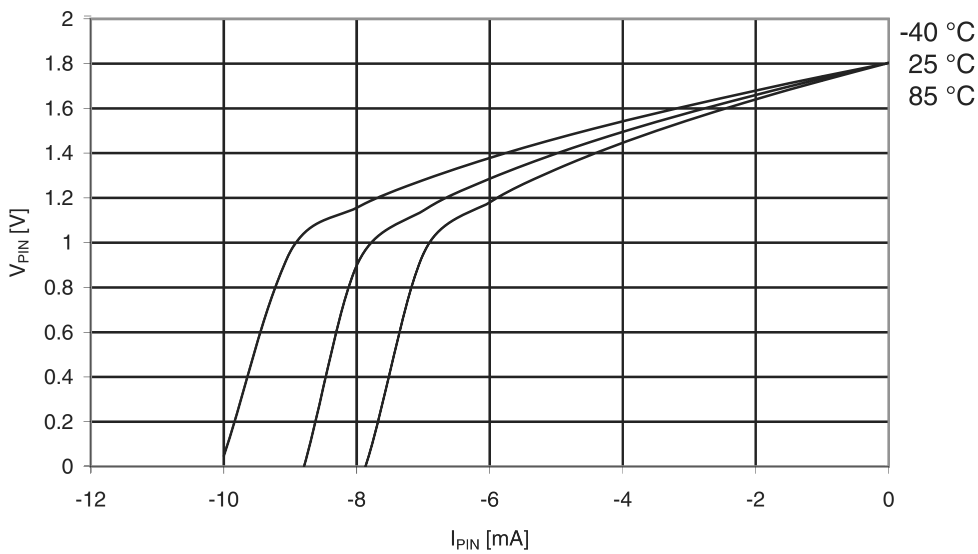


Figure 35-22. I/O Pin Output Voltage vs. Source Current

Vcc = 3.0V

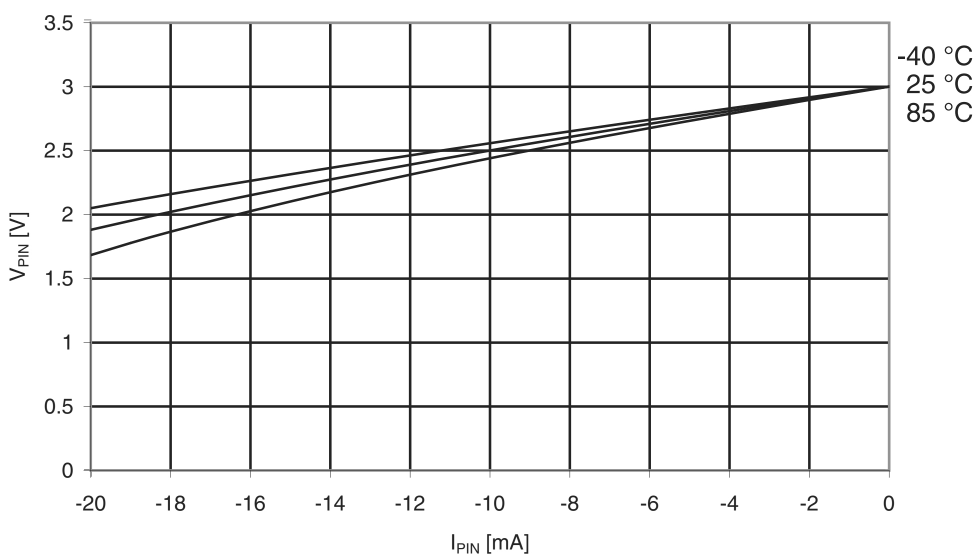
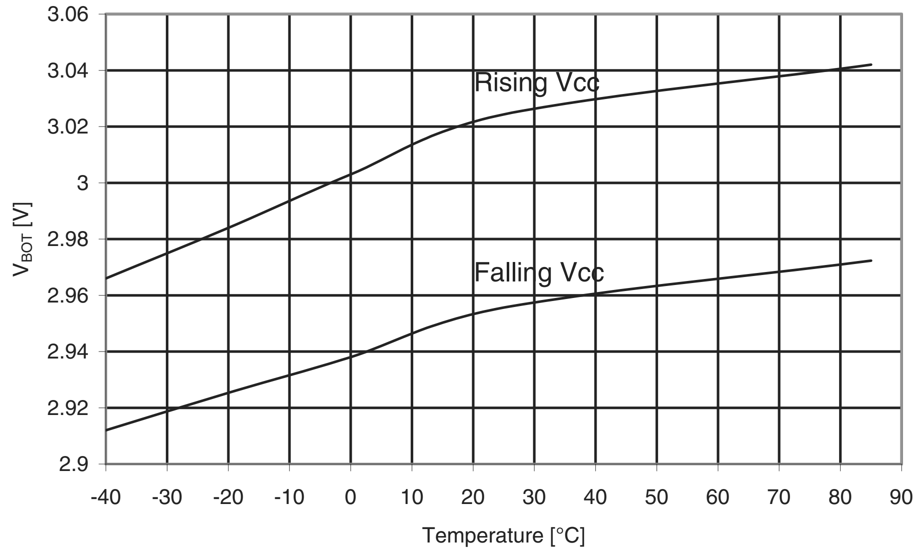


Figure 35-33. BOD Thresholds vs. Temperature

BOD Level = 2.9V

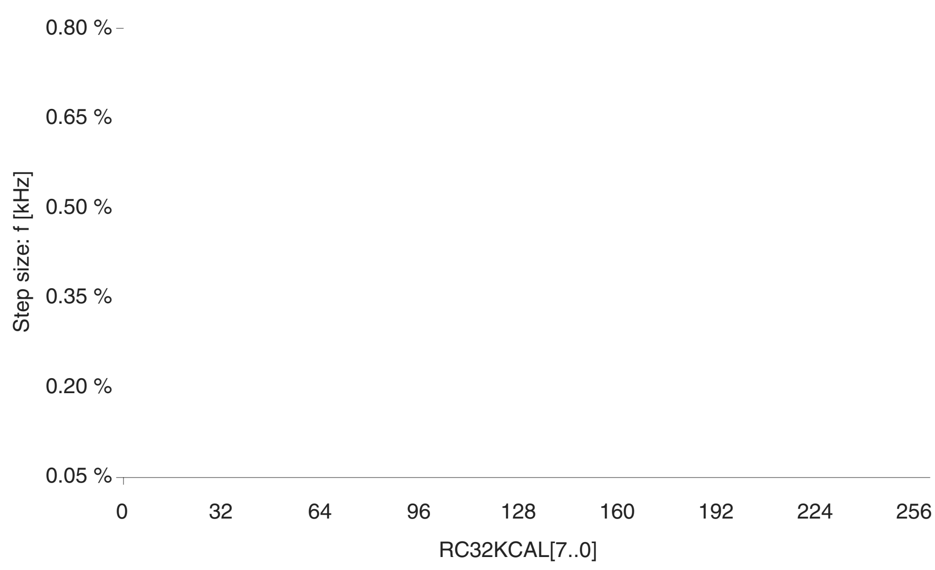


35.9 Oscillators and Wake-up Time

35.9.1 Internal 32.768 kHz Oscillator

Figure 35-34. Internal 32.768 kHz Oscillator Calibration Step Size

T = -40 to 85°C, V_{CC} = 3V



35.10 Module current consumption

Figure 35-39. AC current consumption vs. Vcc

Low-power Mode

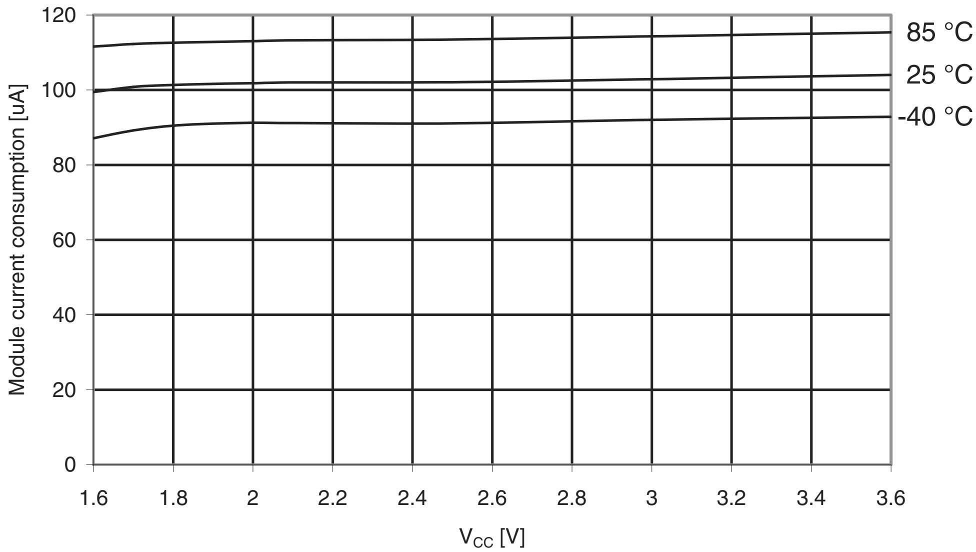
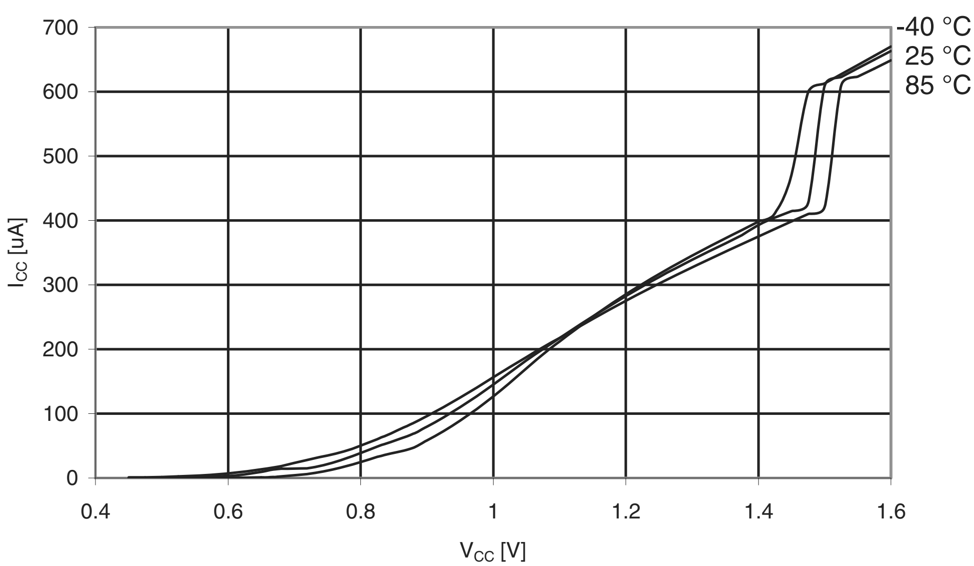


Figure 35-40. Power-up current consumption vs. Vcc



Problem fix/Workaround

Keep the amplified voltage output from the ADC gain stage below 2.4 V in order to get a correct result, or keep ADC voltage reference below 2.4 V.

5. **ADC Event on compare match non-functional**

ADC signalling event will be given at every conversion complete even if Interrupt mode (INTMODE) is set to BELOW or ABOVE.

Problem fix/Workaround

Enable and use interrupt on compare match when using the compare function.

6. **Bandgap measurement with the ADC is non-functional when VCC is below 2.7V**

The ADC can not be used to do bandgap measurements when VCC is below 2.7V.

Problem fix/Workaround

None.

7. **Accuracy lost on first three samples after switching input to ADC gain stage**

Due to memory effect in the ADC gain stage, the first three samples after changing input channel must be disregarded to achieve 12-bit accuracy.

Problem fix/Workaround

Run three ADC conversions and discard these results after changing input channels to ADC gain stage.

8. **Configuration of PGM and CWCM not as described in XMEGA A Manual**

Enabling Common Waveform Channel Mode will enable Pattern generation mode (PGM), but not Common Waveform Channel Mode.

Enabling Pattern Generation Mode (PGM) and not Common Waveform Channel Mode (CWCM) will enable both Pattern Generation Mode and Common Waveform Channel Mode.

Problem fix/Workaround

Table 36-1. Configure PWM and CWCM according to this table:

PGM	CWCM	Description
0	0	PGM and CWCM disabled
0	1	PGM enabled
1	0	PGM and CWCM enabled
1	1	PGM enabled

9. **PWM is not restarted properly after a fault in cycle-by-cycle mode**

When the AWeX fault restore mode is set to cycle-by-cycle, the waveform output will not return to normal operation at first update after fault condition is no longer present.

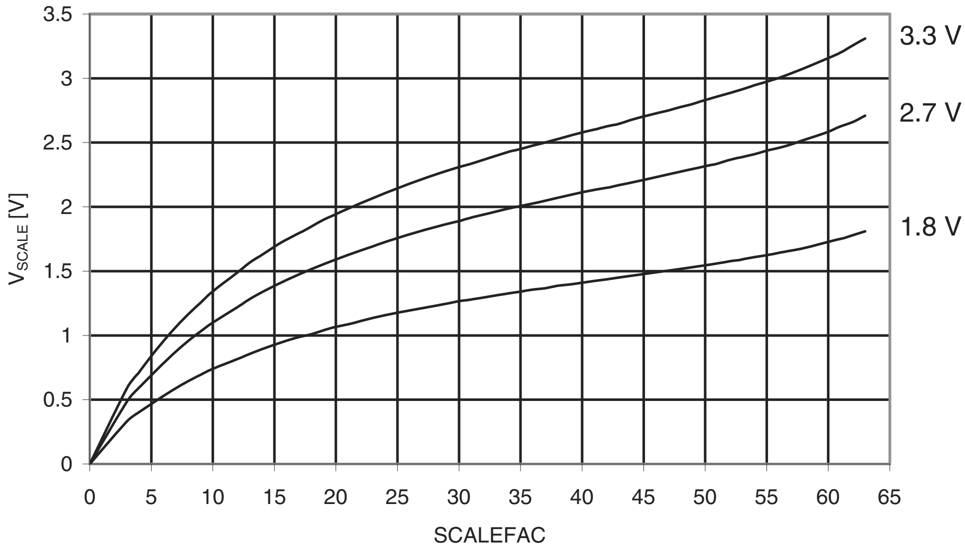
Problem fix/Workaround

Do a write to any AWeX I/O register to re-enable the output.

10. **BOD will be enabled after any reset**

If any reset source goes active, the BOD will be enabled and keep the device in reset if the VCC voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until VCC is above the programmed BOD level even if the BOD is disabled.

Figure 36-2. Analog Comparator Voltage Scaler vs. Scalefac
T = 25°C



Problem fix/Workaround

Use external voltage input for the analog comparator if accurate voltage levels are needed

3. **ADC has increased INL error for some operating conditions**

Some ADC configurations or operating condition will result in increased INL error.

In signed mode INL is increased to:

– 6LSB for sample rates above 1Msps, and up to 8LSB for 2Msps sample rate.
– 6LSB for reference voltage below 1.1V when VCC is above 3.0V.
– 20LSB for ambient temperature below 0 degree C and reference voltage below 1.3V.

In unsigned mode, the INL error cannot be guaranteed, and this mode should not be used.

Problem fix/Workaround

None, avoid using the ADC in the above configurations in order to prevent increased INL error. Use the ADC in signed mode also for single ended measurements.

4. **ADC gain stage output range is limited to 2.4 V**

The amplified output of the ADC gain stage will never go above 2.4 V, hence the differential input will only give correct output when below 2.4 V/gain. For the available gain settings, this gives a differential input range of:

–	1x	gain:	2.4	V
–	2x	gain:	1.2	V
–	4x	gain:	0.6	V
–	8x	gain:	300	mV
–	16x	gain:	150	mV
–	32x	gain:	75	mV
–	64x	gain:	38	mV

Problem fix/Workaround

Wait at least one prescaled RTC clock cycle before reading the RTC CNT value.

22. Pending asynchronous RTC-interrupts will not wake up device

Asynchronous Interrupts from the Real-Time-Counter that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again.

Problem fix/Workaround

None.

23. TWI Transmit collision flag not cleared on repeated start

The TWI transmit collision flag should be automatically cleared on start and repeated start, but is only cleared on start.

Problem fix/Workaround

Clear the flag in software after address interrupt.

24. Clearing TWI Stop Interrupt Flag may lock the bus

If software clears the STOP Interrupt Flag (APIF) on the same Peripheral Clock cycle as the hardware sets this flag due to a new address received, CLKHOLD is not cleared and the SCL line is not released. This will lock the bus.

Problem fix/Workaround

Check if the bus state is IDLE. If this is the case, it is safe to clear APIF. If the bus state is not IDLE, wait for the SCL pin to be low before clearing APIF.

Code:

```
/* Only clear the interrupt flag if within a "safe zone". */
while ( /* Bus not IDLE: */
       ((COMMS_TWI.MASTER.STATUS & TWI_MASTER_BUSSTATE_gm) !=
         TWI_MASTER_BUSSTATE_IDLE_gc)) &&
         /* SCL not held by slave: */
         !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm)
      )
{
    /* Ensure that the SCL line is low */
    if ( !(COMMS_PORT.IN & PIN1_bm) )
        if ( !(COMMS_PORT.IN & PIN1_bm) )
            break;
}
/* Check for an pending address match interrupt */
if ( !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm) )
{
    /* Safely clear interrupt flag */
    COMMS_TWI.SLAVE.STATUS |= (uint8_t)TWI_SLAVE_APIF_bm;
}
```

25. TWI START condition at bus timeout will cause transaction to be dropped

If Bus Timeout is enabled and a timeout occurs on the same Peripheral Clock cycle as a START is detected, the transaction will be dropped.

Problem fix/Workaround

Do not set the BOD level higher than VCC even if the BOD is not used.

11. DAC is nonlinear and inaccurate when reference is above 2.4V or VCC - 0.6V

Using the DAC with a reference voltage above 2.4V or VCC - 0.6V will give inaccurate output when converting codes that give below 0.75V output:

– ±10 LSB for continuous mode

– ±200 LSB for Sample and Hold mode

Problem fix/Workaround

None.

12. DAC has increased INL or noise for some operating conditions

Some DAC configurations or operating condition will result in increased output error.

– Continous mode: ±5 LSB

– Sample and hold mode: ±15 LSB

– Sample and hold mode for reference above 2.0v: up to ±100 LSB

Problem fix/Workaround

None.

13. DAC refresh may be blocked in S/H mode

If the DAC is running in Sample and Hold (S/H) mode and conversion for one channel is done at maximum rate (i.e. the DAC is always busy doing conversion for this channel), this will block refresh signals to the second channel.

Problem fix/Workaround

When using the DAC in S/H mode, ensure that none of the channels is running at maximum conversion rate, or ensure that the conversion rate of both channels is high enough to not require refresh.

14. Conversion lost on DAC channel B in event triggered mode

If during dual channel operation channel 1 is set in auto trigged conversion mode, channel 1 conversions are occasionally lost. This means that not all data-values written to the Channel 1 data register are converted.

Problem fix/Workaround

Keep the DAC conversion interval in the range 000-001 (1 and 3 CLK), and limit the Peripheral clock frequency so the conversion internal never is shorter than 1.5 µs.

15. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/Workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.

Problem fix/Workaround

Do not set the BOD level higher than VCC even if the BOD is not used.

11. DAC is nonlinear and inaccurate when reference is above 2.4V or VCC - 0.6V

Using the DAC with a reference voltage above 2.4V or VCC - 0.6V will give inaccurate output when converting codes that give below 0.75V output:

– ±10 LSB for continuous mode

– ±200 LSB for Sample and Hold mode

Problem fix/Workaround

None.

12. DAC has increased INL or noise for some operating conditions

Some DAC configurations or operating condition will result in increased output error.

– Continous mode: ±5 LSB

– Sample and hold mode: ±15 LSB

– Sample and hold mode for reference above 2.0v: up to ±100 LSB

Problem fix/Workaround

None.

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If the DAC is running in Sample and Hold (S/H) mode and conversion for one channel is done at maximum rate (i.e. the DAC is always busy doing conversion for this channel), this will block refresh signals to the second channel.

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Not recommended for new designs - Use XMEGA A3U series