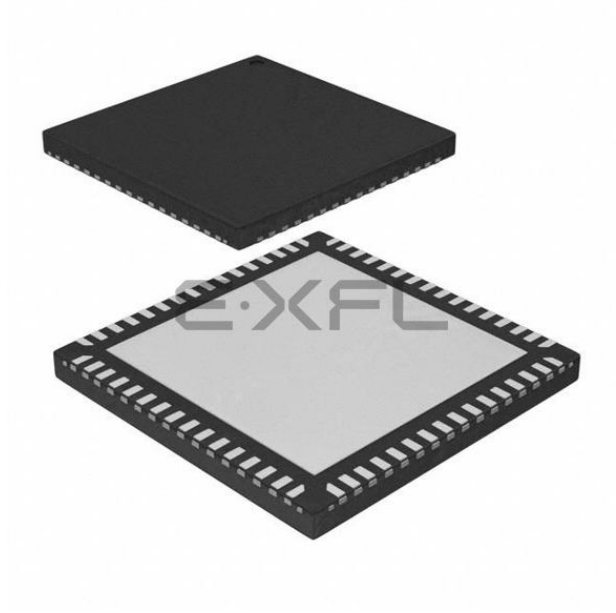


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

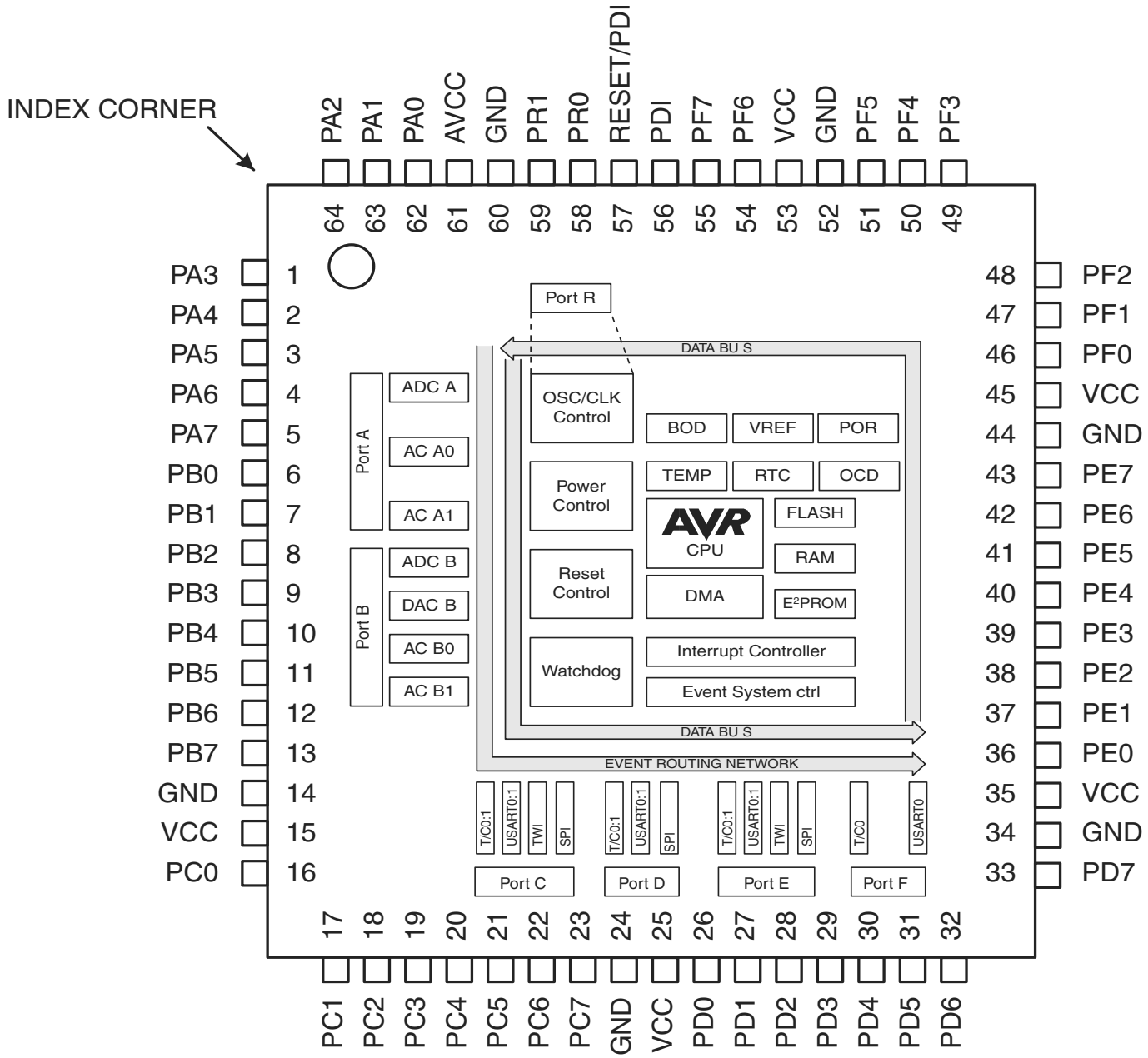
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64a3-mh

2. Pinout/Block Diagram

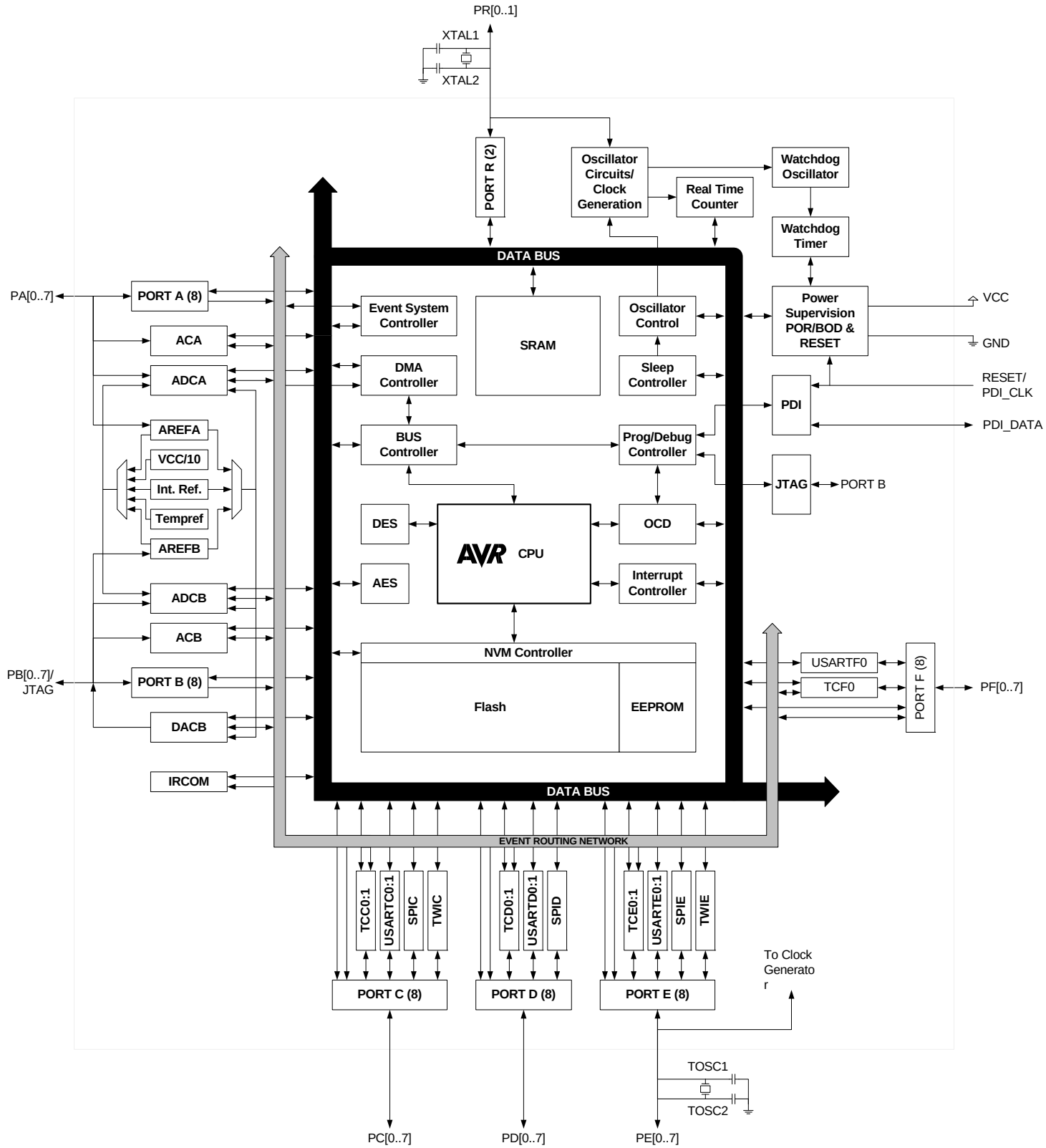
Figure 2-1. Block diagram and pinout.



Notes: 1. For full details on pinout and alternate pin functions refer to ”Pinout and Pin Functions” on page 49.
2. The large center pad underneath the QFN/MLF package should be soldered to ground on the board to ensure good mechanical stability.

3.1 Block Diagram

Figure 3-1. XMEGA A3 Block Diagram



15. I/O Ports

15.1 Features

- **Selectable input and output configuration for each pin individually**
- **Flexible pin configuration through dedicated Pin Configuration Register**
- **Synchronous and/or asynchronous input sensing with port interrupts and events**
  - **Sense both edges**
  - **Sense rising edges**
  - **Sense falling edges**
  - **Sense low level**
- **Asynchronous wake-up from all input sensing configurations**
- **Two port interrupts with flexible pin masking**
- **Highly configurable output driver and pull settings:**
  - **Totem-pole**
  - **Pull-up/-down**
  - **Wired-AND**
  - **Wired-OR**
  - **Bus-keeper**
  - **Inverted I/O**
- **Configuration of multiple pins in a single operation**
- **Read-Modify-Write (RMW) support**
- **Toggle/clear/set registers for Output and Direction registers**
- **Clock output on port pin**
- **Event Channel 0 output on port pin 7**
- **Mapping of port registers (virtual ports) into bit accessible I/O memory space**

15.2 Overview

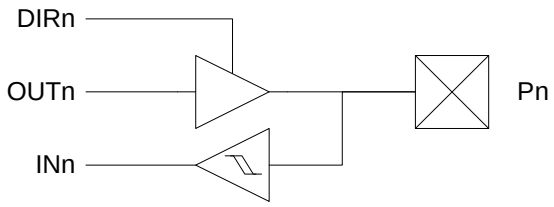
The XMEGA A3 devices have flexible General Purpose I/O Ports. A port consists of up to 8 pins, ranging from pin 0 to pin 7. The ports implement several functions, including synchronous/asynchronous input sensing, pin change interrupts and configurable output settings. All functions are individual per pin, but several pins may be configured in a single operation.

15.3 I/O configuration

All port pins (Pn) have programmable output configuration. In addition, all port pins have an inverted I/O function. For an input, this means inverting the signal between the port pin and the pin register. For an output, this means inverting the output signal between the port register and the port pin. The inverted I/O function can be used also when the pin is used for alternate functions.

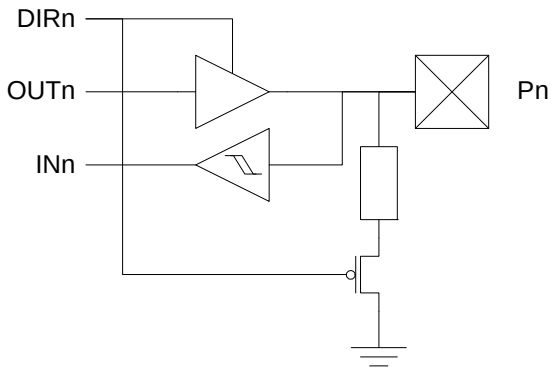
15.3.1 Push-pull

Figure 15-1. I/O configuration - Totem-pole



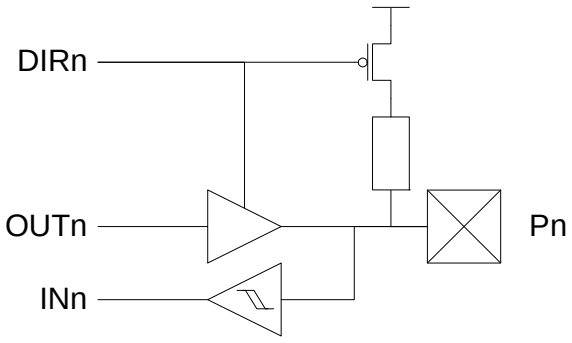
15.3.2 Pull-down

Figure 15-2. I/O configuration - Totem-pole with pull-down (on input)



15.3.3 Pull-up

Figure 15-3. I/O configuration - Totem-pole with pull-up (on input)



15.3.4 Bus-keeper

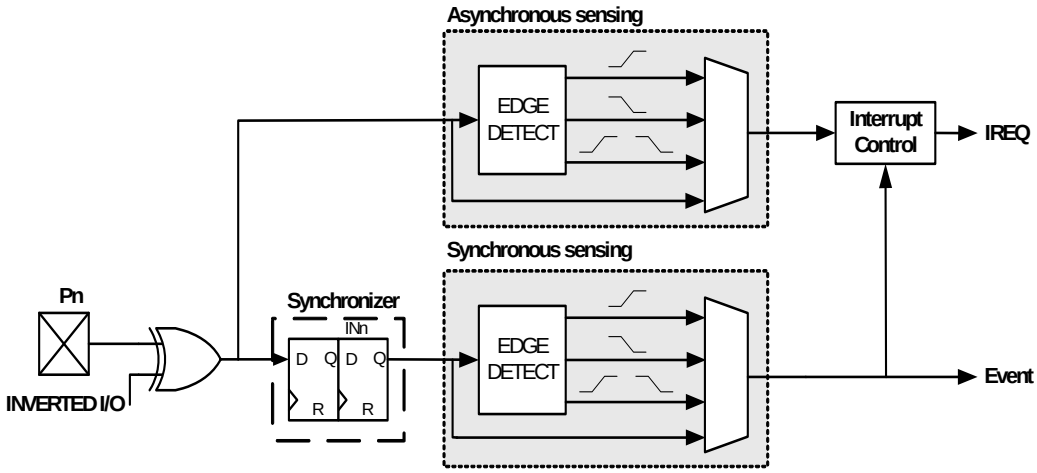
The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

15.4 Input sensing

- **Sense both edges**
- **Sense rising edges**
- **Sense falling edges**
- **Sense low level**

Input sensing is synchronous or asynchronous depending on the enabled clock for the ports, and the configuration is shown in Figure 15-7 on page 30.

Figure 15-7. Input sensing system overview



When a pin is configured with inverted I/O, the pin value is inverted before the input sensing.

15.5 Port Interrupt

Each port has two interrupts with separate priority and interrupt vector. All pins on the port can be individually selected as source for each of the interrupts. The interrupts are then triggered according to the input sense configuration for each pin configured as source for the interrupt.

15.6 Alternate Port Functions

In addition to the input/output functions on all port pins, most pins have alternate functions. This means that other modules or peripherals connected to the port can use the port pins for their functions, such as communication or pulse-width modulation. ”Pinout and Pin Functions” on page 49 shows which modules on peripherals that enable alternate functions on a pin, and which alternate functions that are available on a pin.

16. T/C - 16-bits Timer/Counter with PWM

16.1 Features

- **Seven 16-bit Timer/Counters**
  - **Four Timer/Counters of type 0**
  - **Three Timer/Counters of type 1**
- **Four Compare or Capture (CC) Channels in Timer/Counter 0**
- **Two Compare or Capture (CC) Channels in Timer/Counter 1**
- **Double Buffered Timer Period Setting**
- **Double Buffered Compare or Capture Channels**
- **Waveform Generation:**
  - **Single Slope Pulse Width Modulation**
  - **Dual Slope Pulse Width Modulation**
  - **Frequency Generation**
- **Input Capture:**
  - **Input Capture with Noise Cancelling**
  - **Frequency capture**
  - **Pulse width capture**
  - **32-bit input capture**
- **Event Counter with Direction Control**
- **Timer Overflow and Timer Error Interrupts and Events**
- **One Compare Match or Capture Interrupt and Event per CC Channel**
- **Supports DMA Operation**
- **Hi-Resolution Extension (Hi-Res)**
- **Advanced Waveform Extension (AWEX)**

16.2 Overview

XMEGA A3 has seven Timer/Counters, four Timer/Counter 0 and three Timer/Counter 1. The difference between them is that Timer/Counter 0 has four Compare/Capture channels, while Timer/Counter 1 has two Compare/Capture channels.

The Timer/Counters (T/C) are 16-bit and can count any clock, event or external input in the microcontroller. A programmable prescaler is available to get a useful T/C resolution. Updates of Timer and Compare registers are double buffered to ensure glitch free operation. Single slope PWM, dual slope PWM and frequency generation waveforms can be generated using the Compare Channels.

Through the Event System, any input pin or event in the microcontroller can be used to trigger input capture, hence no dedicated pins is required for this. The input capture has a noise canceller to avoid incorrect capture of the T/C, and can be used to do frequency and pulse width measurements.

A wide range of interrupt or event sources are available, including T/C Overflow, Compare match and Capture for each Compare/Capture channel in the T/C.

PORTC, PORTD and PORTE each has one Timer/Counter 0 and one Timer/Counter1. PORTF has one Timer/Counter 0. Notation of these are TCC0 (Time/Counter C0), TCC1, TCD0, TCD1, TCE0, TCE1 and TCF0, respectively.

22. USART

22.1 Features

- **Seven Identical USART peripherals**
- **Full Duplex Operation (Independent Serial Receive and Transmit Registers)**
- **Asynchronous or Synchronous Operation**
- **Master or Slave Clocked Synchronous Operation**
- **High-resolution Arithmetic Baud Rate Generator**
- **Supports Serial Frames with 5, 6, 7, 8, or 9 Data Bits and 1 or 2 Stop Bits**
- **Odd or Even Parity Generation and Parity Check Supported by Hardware**
- **Data OverRun Detection**
- **Framing Error Detection**
- **Noise Filtering Includes False Start Bit Detection and Digital Low Pass Filter**
- **Three Separate Interrupts on TX Complete, TX Data Register Empty and RX Complete**
- **Multi-processor Communication Mode**
- **Double Speed Asynchronous Communication Mode**
- **Master SPI mode for SPI communication**
- **IrDA support through the IRCOM module**

22.2 Overview

The Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication module. The USART supports full duplex communication, and both asynchronous and clocked synchronous operation. The USART can also be set in Master SPI mode to be used for SPI communication.

Communication is frame based, and the frame format can be customized to support a wide range of standards. The USART is buffered in both direction, enabling continued data transmission without any delay between frames. There are separate interrupt vectors for receive and transmit complete, enabling fully interrupt driven communication. Frame error and buffer overflow are detected in hardware and indicated with separate status flags. Even or odd parity generation and parity check can also be enabled.

One USART can use the IRCOM module to support IrDA 1.4 physical compliant pulse modulation and demodulation for baud rates up to 115.2 kbps.

PORTC, PORTD, and PORTE each has two USARTs, while PORTF has one USART only. Notation of these peripherals are USARTC0, USARTC1, USARTD0, USARTD1, USARTE0, USARTE1 and USARTF0, respectively.

27.3 Input Selection

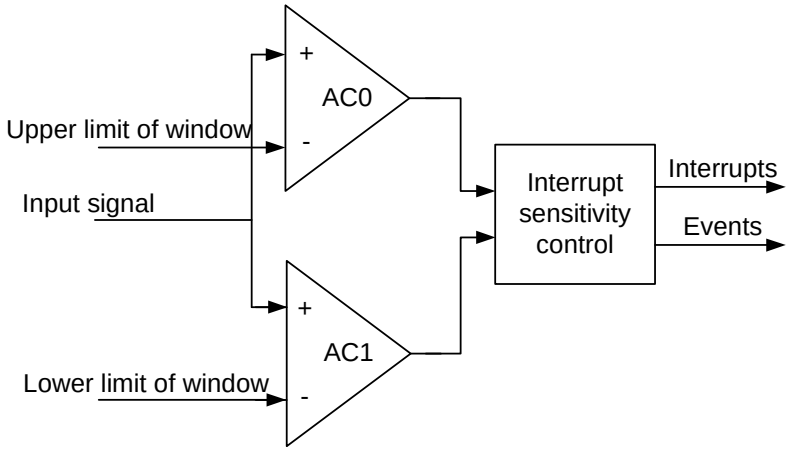
The Analog comparators have a very flexible input selection and the two comparators grouped in a pair may be used to realize a window function. One pair of analog comparators is shown in Figure 27-1 on page 45.

- **Input selection from pin**
  - **Pin 0, 1, 2, 3, 4, 5, 6 selectable to positive input of analog comparator**
  - **Pin 0, 1, 3, 5, 7 selectable to negative input of analog comparator**
- **Internal signals available on positive analog comparator inputs**
  - **Output from 12-bit DAC**
- **Internal signals available on negative analog comparator inputs**
  - **64-level scaler of the VCC, available on negative analog comparator input**
  - **Bandgap voltage reference**
- **Output from 12-bit DAC**

27.4 Window Function

The window function is realized by connecting the external inputs of the two analog comparators in a pair as shown in Figure 27-2.

Figure 27-2. Analog comparator window function



34.11 POR Characteristics

Table 34-12. Power-on Reset Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{POT-}	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	0.8		
		V_{CC} falls at 1V/ms or slower	0.8	1.3		V
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	

34.12 Reset Characteristics

Table 34-13. Reset Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Minimum reset pulse width			90	1000	ns
	Reset threshold voltage	V_{CC} = 2.7 - 3.6V		0.45*V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.42*V_{CC}		

34.13 Oscillator Characteristics

Table 34-14. Internal 32.768kHz Oscillator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Accuracy	T = 85°C, V_{CC} = 3V, After production calibration	-0.5		0.5	%

Table 34-15. Internal 2MHz Oscillator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Accuracy	T = 85°C, V_{CC} = 3V, After production calibration	-1.5		1.5	%
	DFLL Calibration step size	T = 25°C, V_{CC} = 3V		0.15		

Table 34-16. Internal 32MHz Oscillator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Accuracy	T = 85°C, V_{CC} = 3V, After production calibration	-1.5		1.5	%
	DFLL Calibration stepsize	T = 25°C, V_{CC} = 3V		0.2		

Table 34-17. Internal 32kHz, ULP Oscillator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Output frequency 32kHz ULP OSC	T = 85°C, V_{CC} = 3.0V		26		kHz

35. Typical Characteristics

35.1 Active Supply Current

Figure 35-1. Active Supply Current vs. Frequency
f_{SYS} = 0 - 1.0 MHz External clock, T = 25°C

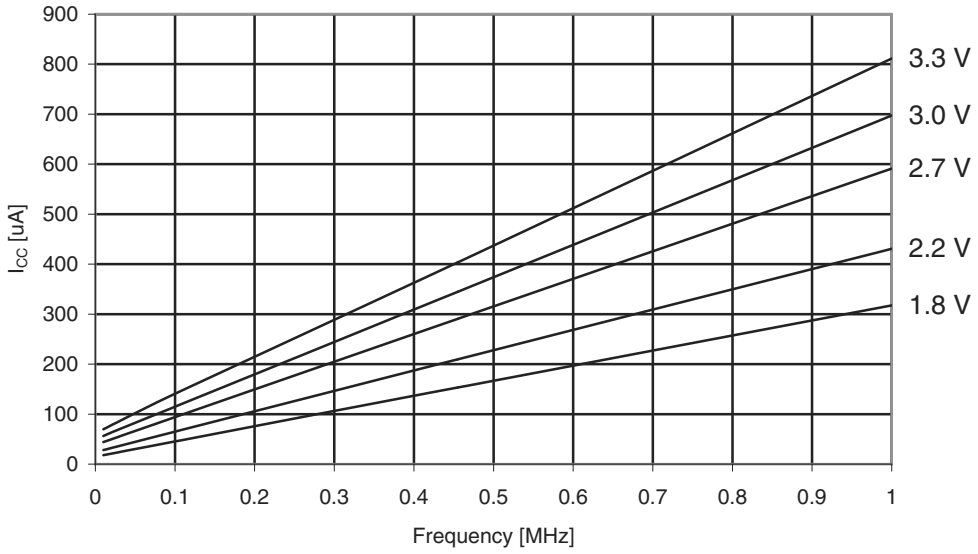


Figure 35-2. Active Supply Current vs. Frequency
f_{SYS} = 1 - 32 MHz External clock, T = 25°C

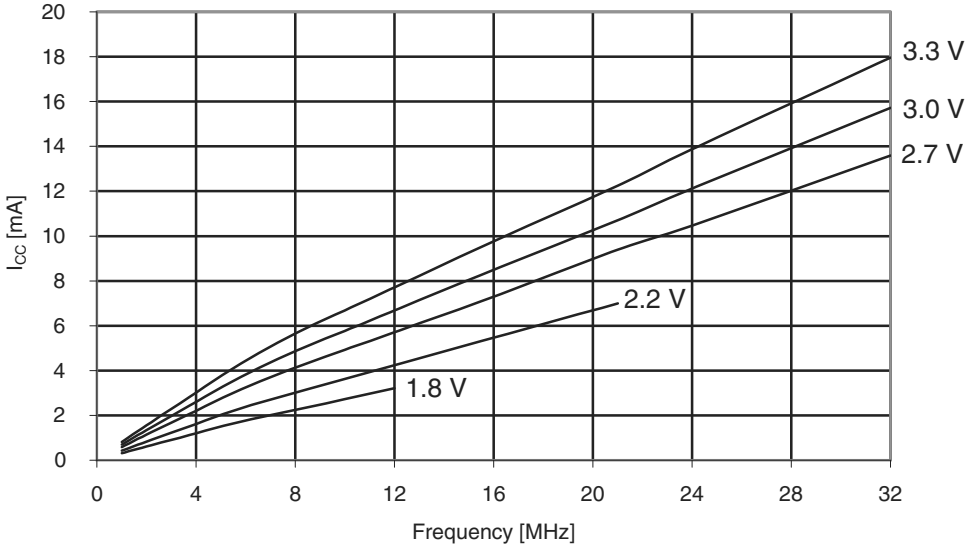


Figure 35-5. Active Supply Current vs. Vcc

f_{SYS} = 2.0 MHz internal RC

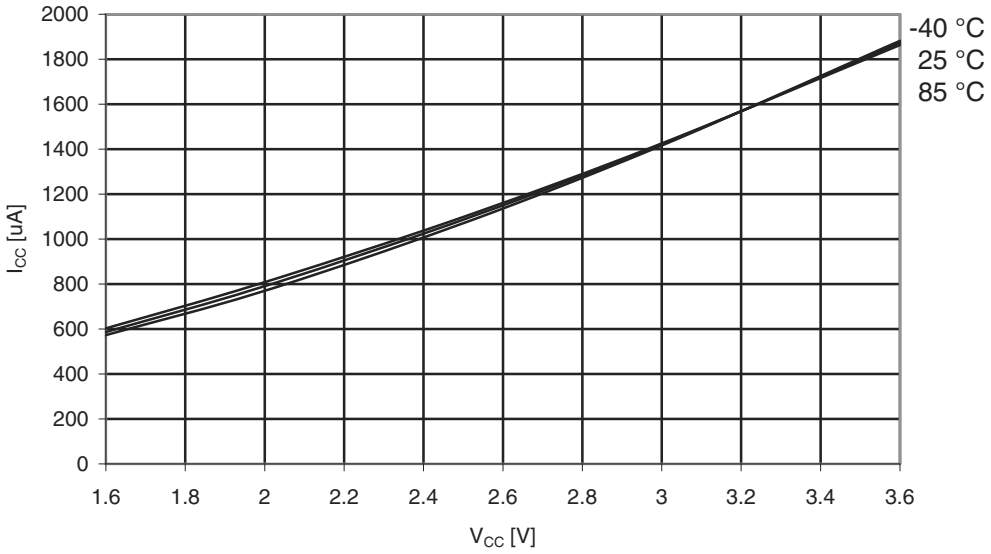


Figure 35-6. Active Supply Current vs. Vcc

f_{SYS} = 32 MHz internal RC prescaled to 8 MHz

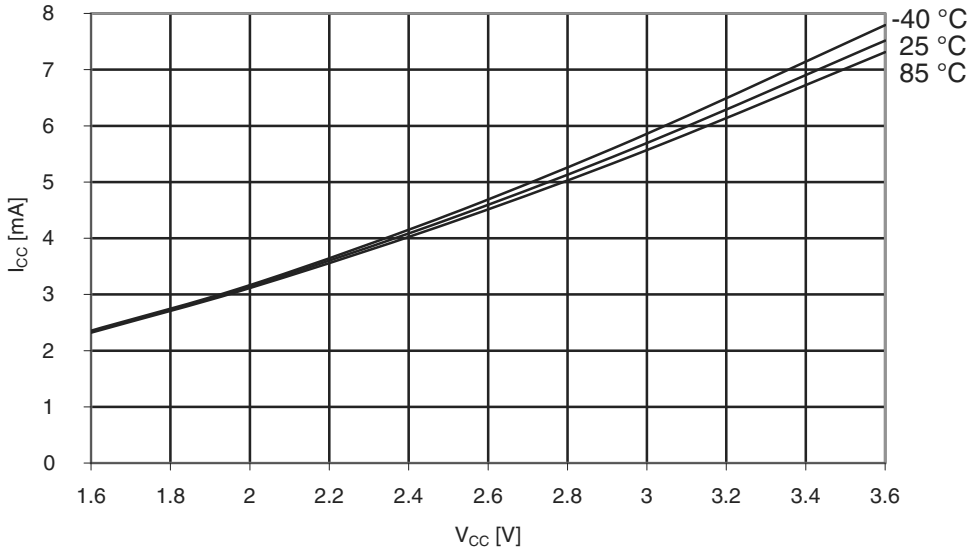
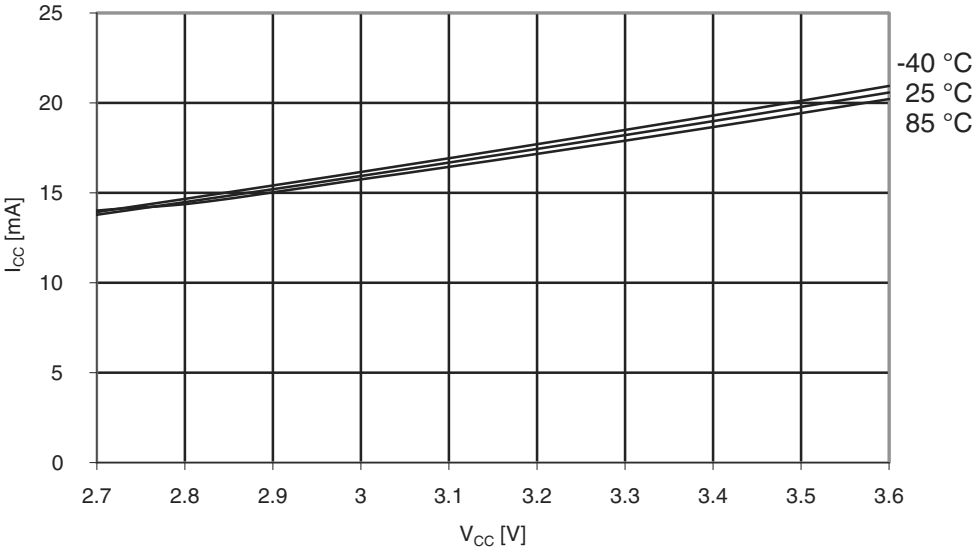


Figure 35-7. Active Supply Current vs. Vcc

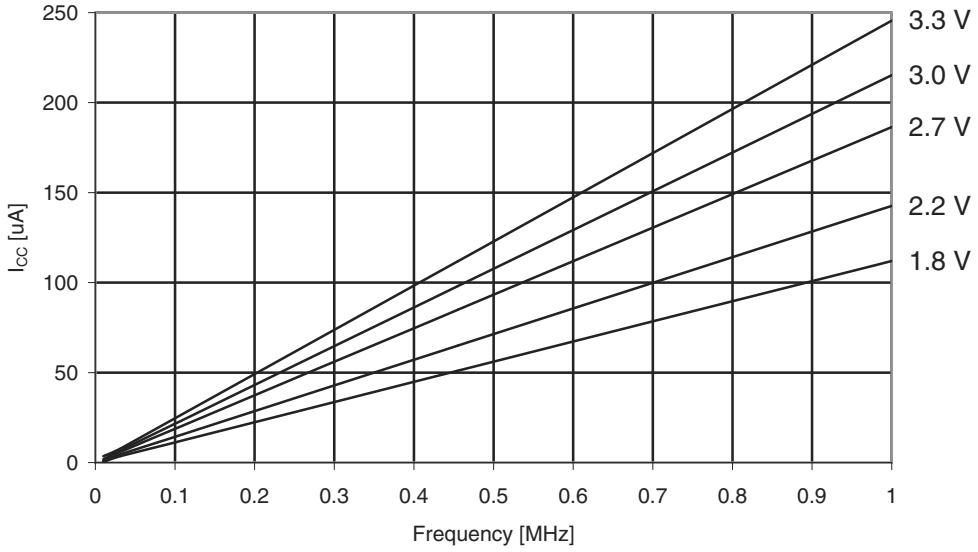
f_{SYS} = 32 MHz internal RC



35.2 Idle Supply Current

Figure 35-8. Idle Supply Current vs. Frequency

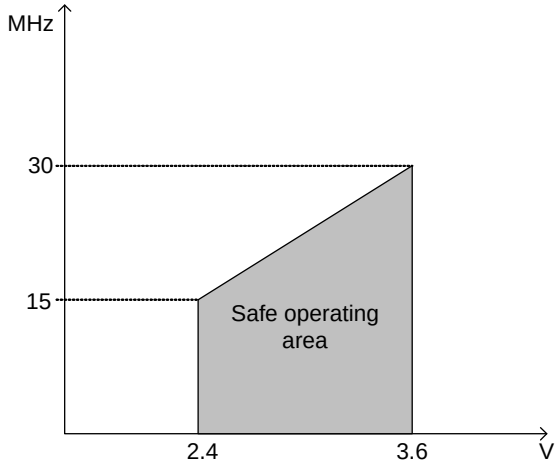
f_{SYS} = 0 - 1.0 MHz, T = 25°C



10. Operating Frequency and Voltage Limitation

To ensure correct operation, there is a limit on operating frequency and voltage. Figure 36-3 on page 109 shows the safe operating area.

Figure 36-3. Operating Frequnecy and Voltage Limitation



Problem fix/Workaround

None, avoid using the device outside these frequnecy and voltage limitations.

11. Inverted I/O enable does not affect Analog Comparator Output

The inverted I/O pin function does not affect the Analog Comparator output function.

Problem fix/Workarund

Configure the analog comparator setup to give a inverted result (i.e. connect positive input to the negative AC input and vice versa), or use and externel inverter to change polarity of Analog Comparator Output.

36.2 ATxmega192A3, ATxmega128A3, ATxmega64A3

36.2.1 rev. E

- **Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously**
- **VCC voltage scaler for AC is non-linear**
- **ADC has increased INL error for some operating conditions**
- **ADC gain stage output range is limited to 2.4 V**
- **ADC Event on compare match non-functional**
- **Bandgap measurement with the ADC is non-functional when VCC is below 2.7V**
- **Accuracy lost on first three samples after switching input to ADC gain stage**
- **Configuration of PGM and CWCM not as described in XMEGA A Manual**
- **PWM is not restarted properly after a fault in cycle-by-cycle mode**
- **BOD will be enabled at any reset**
- **DAC is nonlinear and inaccurate when reference is above 2.4V or VCC - 0.6V**
- **DAC has increased INL or noise for some operating conditions**
- **DAC refresh may be blocked in S/H mode**
- **Conversion lost on DAC channel B in event triggered mode**
- **EEPROM page buffer always written when NVM DATA0 is written**
- **Pending full asynchronous pin change interrupts will not wake the device**
- **Pin configuration does not affect Analog Comparator Output**
- **NMI Flag for Crystal Oscillator Failure automatically cleared**
- **Crystal start-up time required after power-save even if crystal is source for RTC**
- **RTC Counter value not correctly read after sleep**
- **Pending asynchronous RTC-interrupts will not wake up device**
- **TWI Transmit collision flag not cleared on repeated start**
- **Clearing TWI Stop Interrupt Flag may lock the bus**
- **TWI START condition at bus timeout will cause transaction to be dropped**
- **TWI Data Interrupt Flag (DIF) erroneously read as set**
- **WDR instruction inside closed window will not issue reset**

1. Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously

If the Bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for another AC, the first comparator will be affected for up to 1 µs and could potentially give a wrong comparison result.

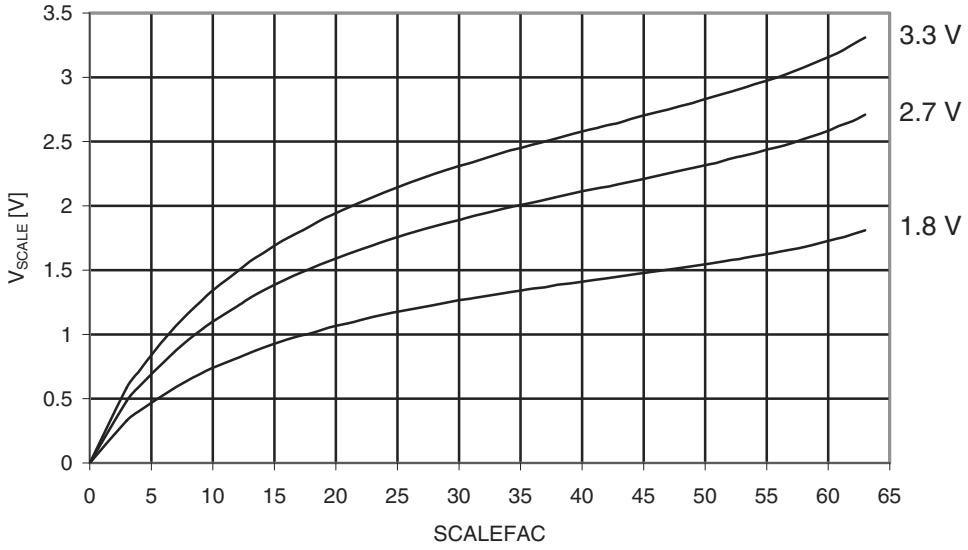
Problem fix/Workaround

If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. VCC voltage scaler for AC is non-linear

The 6-bit VCC voltage scaler in the Analog Comparators is non-linear.

Figure 36-4. Analog Comparator Voltage Scaler vs. Scalefac
T = 25°C



Problem fix/Workaround

Use external voltage input for the analog comparator if accurate voltage levels are needed

3. ADC has increased INL error for some operating conditions

Some ADC configurations or operating condition will result in increased INL error.

In signed mode INL is increased to:

– 6LSB for sample rates above 1Msps, and up to 8 LSB for 2Msps sample rate.

– 6LSB for reference voltage below 1.1V when VCC is above 3.0V.

– 20LSB for ambient temperature below 0 degree C and reference voltage below 1.3V.

In unsigned mode, the INL error cannot be guaranteed, and this mode should not be used.

Problem fix/Workaround

None, avoid using the ADC in the above configurations in order to prevent increased INL error. Use the ADC in signed mode also for single ended measurements.

4. ADC gain stage output range is limited to 2.4 V

The amplified output of the ADC gain stage will never go above 2.4 V, hence the differential input will only give correct output when below 2.4 V/gain. For the available gain settings, this gives a differential input range of:

– 1x gain: 2.4 V

– 2x gain: 1.2 V

– 4x gain: 0.6 V

– 8x gain: 300 mV

– 16x gain: 150 mV

– 32x gain: 75 mV

– 64x gain: 38 mV

22. TWI Transmit collision flag not cleared on repeated start

The TWI transmit collision flag should be automatically cleared on start and repeated start, but is only cleared on start.

Problem fix/Workaround

Clear the flag in software after address interrupt.

23. Clearing TWI Stop Interrupt Flag may lock the bus

If software clears the STOP Interrupt Flag (APIF) on the same Peripheral Clock cycle as the hardware sets this flag due to a new address received, CLKHOLD is not cleared and the SCL line is not released. This will lock the bus.

Problem fix/Workaround

Check if the bus state is IDLE. If this is the case, it is safe to clear APIF. If the bus state is not IDLE, wait for the SCL pin to be low before clearing APIF.

Code:

```
/* Only clear the interrupt flag if within a "safe zone". */
while ( /* Bus not IDLE: */
       ((COMMS_TWI.MASTER.STATUS & TWI_MASTER_BUSSTATE_gm) !=
         TWI_MASTER_BUSSTATE_IDLE_gc)) &&
         /* SCL not held by slave: */
         !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm)
      )
{
    /* Ensure that the SCL line is low */
    if ( !(COMMS_PORT.IN & PIN1_bm) )
        if ( !(COMMS_PORT.IN & PIN1_bm) )
            break;
}
/* Check for an pending address match interrupt */
if ( !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm) )
{
    /* Safely clear interrupt flag */
    COMMS_TWI.SLAVE.STATUS |= (uint8_t)TWI_SLAVE_APIF_bm;
}
```

24. TWI START condition at bus timeout will cause transaction to be dropped

If Bus Timeout is enabled and a timeout occurs on the same Peripheral Clock cycle as a START is detected, the transaction will be dropped.

Problem fix/Workaround

None.

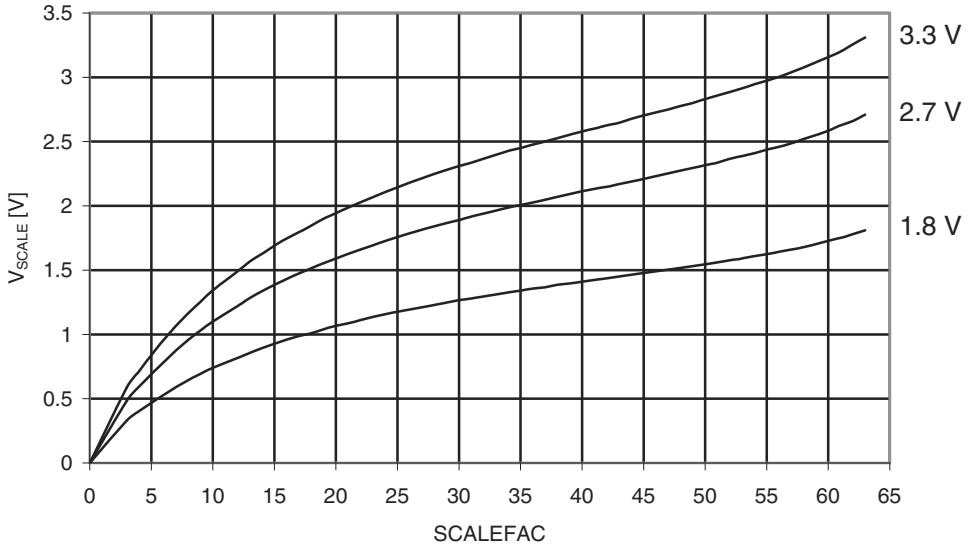
25. TWI Data Interrupt Flag erroneously read as set

When issuing the TWI slave response command CMD=0b11, it takes 1 Peripheral Clock cycle to clear the data interrupt flag (DIF). A read of DIF directly after issuing the command will show the DIF still set.

Problem fix/Workaround

Add one NOP instruction before checking DIF.

Figure 36-5. Analog Comparator Voltage Scaler vs. Scalefac
T = 25°C



Problem fix/Workaround

Use external voltage input for the analog comparator if accurate voltage levels are needed

3. ADC has increased INL error for some operating conditions

Some ADC configurations or operating condition will result in increased INL error.

In signed mode INL is increased to:

– 6LSB for sample rates above 1Msps, and up to 8 LSB for 2Msps sample rate.

– 6LSB for reference voltage below 1.1V when VCC is above 3.0V.

– 20LSB for ambient temperature below 0 degree C and reference voltage below 1.3V.

In unsigned mode, the INL error cannot be guaranteed, and this mode should not be used.

Problem fix/Workaround

None, avoid using the ADC in the above configurations in order to prevent increased INL error. Use the ADC in signed mode also for single ended measurements.

4. ADC gain stage output range is limited to 2.4 V

The amplified output of the ADC gain stage will never go above 2.4 V, hence the differential input will only give correct output when below 2.4 V/gain. For the available gain settings, this gives a differential input range of:

– 1x gain: 2.4 V

– 2x gain: 1.2 V

– 4x gain: 0.6 V

– 8x gain: 300 mV

– 16x gain: 150 mV

– 32x gain: 75 mV

– 64x gain: 38 mV

16. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

Problem fix/Workaround

None.

17. Pin configuration does not affect Analog Comparator output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output.

Problem fix/Workaround

None for Output/Pull configuration.

For inverted I/O, configure the Analog Comparator to give an inverted result (i.e. connect positive input to the negative AC input and vice versa), or use and external inverter to change polarity of Analog Comparator output.

18. NMI Flag for Crystal Oscillator Failure automatically cleared

NMI flag for Crystal Oscillator Failure (XOSCFDIF) will be automatically cleared when executing the NMI interrupt handler.

Problem fix/Workaround

This device revision has only one NMI interrupt source, so checking the interrupt source in software is not required.

19. Writing EEPROM or Flash while reading any of them will not work

The EEPROM and Flash cannot be written while reading EEPROM or Flash, or while executing code in Active mode.

Problem fix/Workaround

Enter IDLE sleep mode within 2.5 µs (Five 2 MHz clock cycles and 80 32 MHz clock cycles) after starting an EEPROM or flash write operation. Wake-up source must either be EEPROM ready or NVM ready interrupt. Alternatively set up a Timer/Counter to give an overflow interrupt 7 ms after the erase or write operation has started, or 13 ms after atomic erase-and-write operation has started, and then enter IDLE sleep mode.

20. Crystal start-up time required after power-save even if crystal is source for RTC

Even if 32.768 kHz crystal is used for RTC during sleep, the clock from the crystal will not be ready for the system before the specified start-up time. See "XOSCSEL[3:0]: Crystal Oscillator Selection" in XMEGA A Manual. If BOD is used in active mode, the BOD will be on during this period (0.5s).

Problem fix/Workaround

If faster start-up is required, go to sleep with internal oscillator as system clock.

21. RTC Counter value not correctly read after sleep

If the RTC is set to wake up the device on RTC Overflow and bit 0 of RTC CNT is identical to bit 0 of RTC PER as the device is entering sleep, the value in the RTC count register can not be read correctly within the first prescaled RTC clock cycle after wakeup. The value read will be the same as the value in the register when entering sleep.

The same applies if RTC Compare Match is used as wake-up source.

8. Updated ”DAC Characteristics” on page 68. Removed DC output impedence.
9. Updated Figure 35-6 on page 74. Replaced the figure by a correct one.
10. Fixed typo in “Errata” section.

37.5 8068Q – 02/10

1. Added ”PDI Speed” on page 92.

37.6 8068P – 02/10

1. Updated the device pin-out Figure 2-1 on page 3. PDI_CLK and PDI_DATA renamed only PDI.
2. Removed JTAG Reset from the datasheet.
3. Updated ”DAC - 12-bit Digital to Analog Converter” on page 43. DAC uses internal 1.0 voltage.
4. Added Table 34-19 on page 71.
5. Updated ”Timer/Counter and AWEX functions” on page 49.
6. Updated ”Alternate Pin Function Description” on page 49.
7. Updated all ”Electrical Characteristics” on page 63.
8. Updated ”PAD Characteristics” on page 69.
9. Changed Internal Oscillator Speed to ”Oscillators and Wake-up Time” on page 88.
10. Updated ”Errata” on page 93

37.7 8068O – 11/09

1. Updated Table 34-3 on page 66, Endurance and Data Retention.
2. Updated Table 34-11 on page 69, Input hysteresis is in V and not in mV.
3. Updated ”Errata” on page 93.

37.8 8068N – 10/09

1. Updated ”Errata” on page 93.