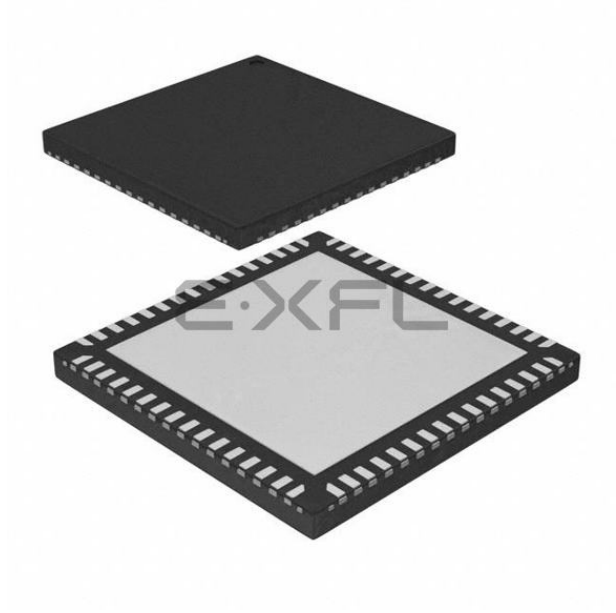

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64a3-mhr

1. Ordering Information

Ordering Code	Flash	E^2	SRAM	Speed (MHz)	Power Supply	Package[1][2][3]	Temp
ATxmega256A3-AU	256 KB + 8 KB	4 KB	16 KB	32	1.6 - 3.6V	64A	-40°C - 85°C
ATxmega192A3-AU	192 KB + 8 KB	2 KB	16 KB	32	1.6 - 3.6V		
ATxmega128A3-AU	128 KB + 8 KB	2 KB	8 KB	32	1.6 - 3.6V		
ATxmega64A3-AU	64 KB + 4 KB	2 KB	4 KB	32	1.6 - 3.6V		
ATxmega256A3-MH	256 KB + 8 KB	4 KB	16 KB	32	1.6 - 3.6V	64M2	
ATxmega192A3-MH	192 KB + 8 KB	2 KB	16 KB	32	1.6 - 3.6V		
ATxmega128A3-MH	128 KB + 8 KB	2 KB	8 KB	32	1.6 - 3.6V		
ATxmega64A3-MH	64 KB + 4 KB	2 KB	4 KB	32	1.6 - 3.6V		

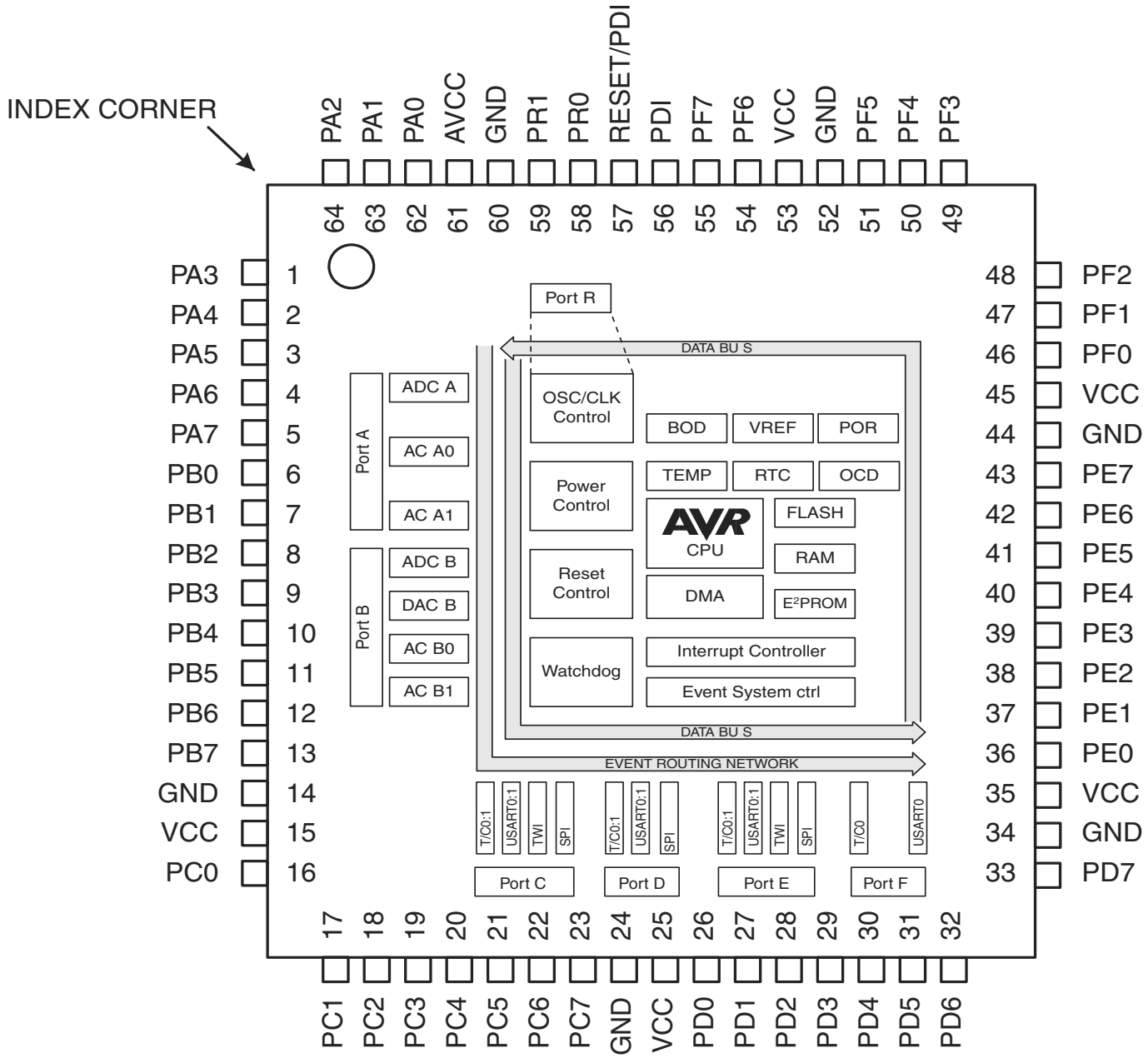
Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For packaging information, see ”Packaging information” on page 61.

Package Type	
64A	64-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)
64M2	64-Pad, 9 x 9 x 1.0 mm Body, Lead Pitch 0.50 mm, 7.65 mm Exposed Pad, Quad Flat No-Lead Package (QFN)

Not recommended for new designs - Use XMEGA A3U series

2. Pinout/Block Diagram

Figure 2-1. Block diagram and pinout.



Notes: 1. For full details on pinout and alternate pin functions refer to ”Pinout and Pin Functions” on page 49.
2. The large center pad underneath the QFN/MLF package should be soldered to ground on the board to ensure good mechanical stability.

3. Overview

The Atmel® AVR® XMEGA™ A3 is a family of low power, high performance and peripheral rich CMOS 8/16-bit microcontrollers based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the XMEGA A3 achieves throughputs approaching 1 Million Instructions Per Second (MIPS) per MHz allowing the system designer to optimize power consumption versus processing speed.

The AVR CPU combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction, executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs many times faster than conventional single-accumulator or CISC based microcontrollers.

The XMEGA A3 devices provide the following features: In-System Programmable Flash with Read-While-Write capabilities, Internal EEPROM and SRAM, four-channel DMA Controller, eight-channel Event System, Programmable Multi-level Interrupt Controller, 50 general purpose I/O lines, 16-bit Real Time Counter (RTC), seven flexible 16-bit Timer/Counters with compare modes and PWM, seven USARTs, two Two Wire Serial Interfaces (TWIs), three Serial Peripheral Interfaces (SPIs), AES and DES crypto engine, two 8-channel 12-bit ADCs with optional differential input with programmable gain, one 2-channel 12-bit DACs, four analog comparators with window mode, programmable Watchdog Timer with separate Internal Oscillator, accurate internal oscillators with PLL and prescaler and programmable Brown-Out Detection.

The Program and Debug Interface (PDI), a fast 2-pin interface for programming and debugging, is available. The devices also have an IEEE std. 1149.1 compliant JTAG test interface, and this can also be used for On-chip Debug and programming.

The XMEGA A3 devices have five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, DMA Controller, Event System, Interrupt Controller and all peripherals to continue functioning. The Power-down mode saves the SRAM and register contents but stops the oscillators, disabling all other functions until the next TWI or pin-change interrupt, or Reset. In Power-save mode, the asynchronous Real Time Counter continues to run, allowing the application to maintain a timer base while the rest of the device is sleeping. In Standby mode, the Crystal/Resonator Oscillator is kept running while the rest of the device is sleeping. This allows very fast start-up from external crystal combined with low power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run. To further reduce power consumption, the peripheral clock for each individual peripheral can optionally be stopped in Active mode and Idle sleep mode.

The device is manufactured using Atmel's high-density nonvolatile memory technology. The program Flash memory can be reprogrammed in-system through the PDI or JTAG. A Bootloader running in the device can use any interface to download the application program to the Flash memory. The Bootloader software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8/16-bit RISC CPU with In-System Self-Programmable Flash, the Atmel XMEGA A3 is a powerful microcontroller family that provides a highly flexible and cost effective solution for many embedded applications.

The XMEGA A3 devices are supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, programmers, and evaluation kits.

7.7 Flash and EEPROM Page Size

The Flash Program Memory and EEPROM data memory are organized in pages. The pages are word accessible for the Flash and byte accessible for the EEPROM.

Table 7-2 on page 14 shows the Flash Program Memory organization. Flash write and erase operations are performed on one page at a time, while reading the Flash is done one byte at a time. For Flash access the Z-pointer (Z[m:n]) is used for addressing. The most significant bits in the address (FPAGE) gives the page number and the least significant address bits (FWORD) gives the word in the page.

Table 7-2. Number of words and Pages in the Flash.

Devices	Flash Size	Page Size (words)	FWORD	FPAGE	Application		Boot	
					Size	No of Pages	Size	No of Pages
ATxmega64A3	64 KB + 4 KB	128	Z[7:1]	Z[16:8]	64K	256	4 KB	16
ATxmega128A3	128 KB + 8 KB	256	Z[8:1]	Z[17:9]	128K	256	8 KB	16
ATxmega192A3	192 KB + 8 KB	256	Z[8:1]	Z[18:9]	192K	384	8 KB	16
ATxmega256A3	256 KB + 8 KB	256	Z[8:1]	Z[18:9]	256K	512	8 KB	16

Table 7-3 on page 14 shows EEPROM memory organization for the XMEGA A3 devices. EEPROM write and erase operations can be performed one page or one byte at a time, while reading the EEPROM is done one byte at a time. For EEPROM access the NVM Address Register (ADDR[m:n]) is used for addressing. The most significant bits in the address (E2PAGE) gives the page number and the least significant address bits (E2BYTE) gives the byte in the page.

Table 7-3. Number of bytes and Pages in the EEPROM.

Devices	EEPROM Size	Page Size (Bytes)	E2BYTE	E2PAGE	No of Pages
ATxmega64A3	2 KB	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega128A3	2 KB	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega192A3	2 KB	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega256A3	4 KB	32	ADDR[4:0]	ADDR[11:5]	128

10. System Clock and Clock options

10.1 Features

- **Fast start-up time**
- **Safe run-time clock switching**
- **Internal Oscillators:**
  - **32 MHz run-time calibrated RC oscillator**
  - **2 MHz run-time calibrated RC oscillator**
  - **32.768 kHz calibrated RC oscillator**
  - **32 kHz Ultra Low Power (ULP) oscillator**
- **External clock options**
  - **0.4 - 16 MHz Crystal Oscillator**
  - **32.768 kHz Crystal Oscillator**
  - **External clock**
- **PLL with internal and external clock options with 2 to 31x multiplication**
- **Clock Prescalers with 2 to 2048x division**
- **Fast peripheral clock running at 2 and 4 times the CPU clock speed**
- **Automatic Run-Time Calibration of internal oscillators**
- **Crystal Oscillator failure detection**

10.2 Overview

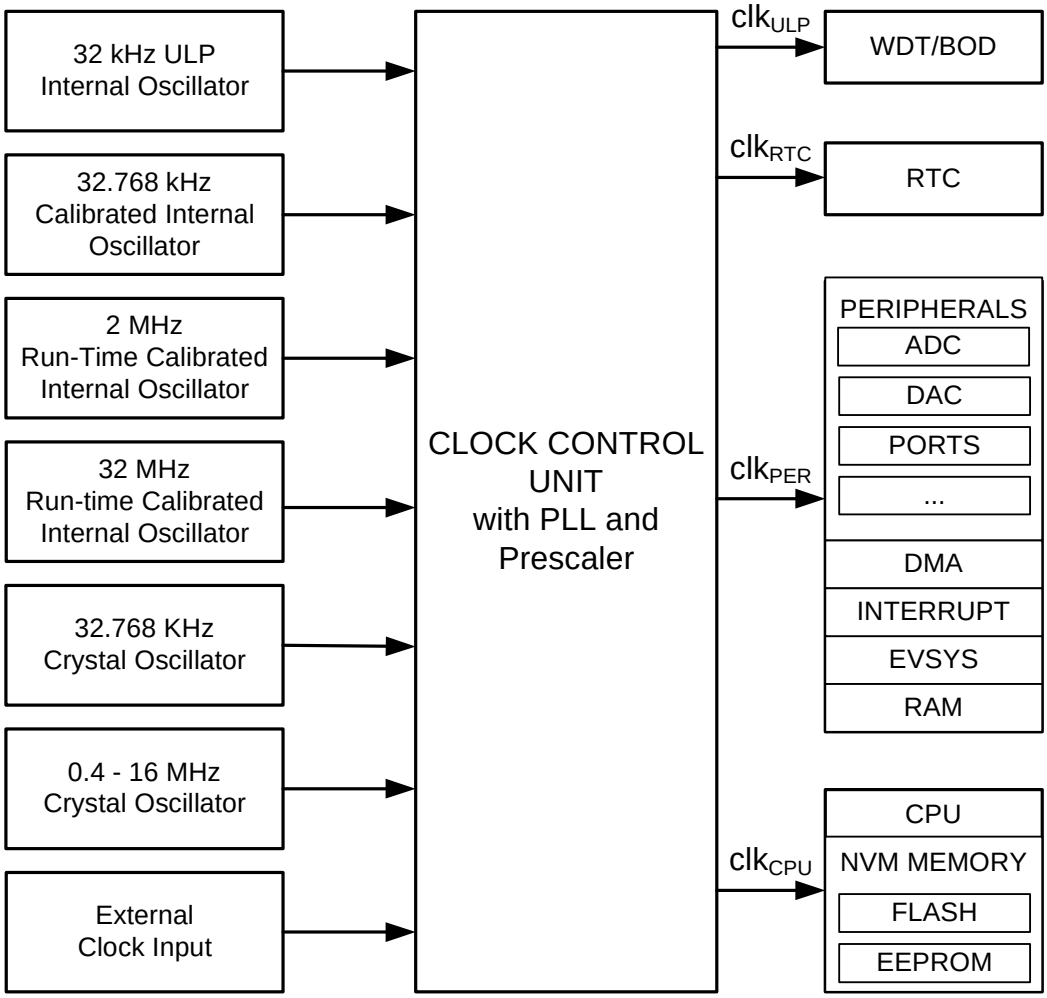
XMEGA A3 has an advanced clock system, supporting a large number of clock sources. It incorporates both integrated oscillators, external crystal oscillators and resonators. A high frequency Phase Locked Loop (PLL) and clock prescalers can be controlled from software to generate a wide range of clock frequencies from the clock source input.

It is possible to switch between clock sources from software during run-time. After reset the device will always start up running from the 2 Mhz internal oscillator.

A calibration feature is available, and can be used for automatic run-time calibration of the internal 2 MHz and 32 MHz oscillators. This reduce frequency drift over voltage and temperature.

A Crystal Oscillator Failure Monitor can be enabled to issue a Non-Maskable Interrupt and switch to internal oscillator if the external oscillator fails. Figure 10-1 on page 19 shows the principal clock system in XMEGA A3.

Figure 10-1. Clock system overview



Each clock source is briefly described in the following sub-sections.

10.3 Clock Options

10.3.1 32 kHz Ultra Low Power Internal Oscillator

The 32 kHz Ultra Low Power (ULP) Internal Oscillator is a very low power consumption clock source. It is used for the Watchdog Timer, Brown-Out Detection and as an asynchronous clock source for the Real Time Counter. This oscillator cannot be used as the system clock source, and it cannot be directly controlled from software.

10.3.2 32.768 kHz Calibrated Internal Oscillator

The 32.768 kHz Calibrated Internal Oscillator is a high accuracy clock source that can be used as the system clock source or as an asynchronous clock source for the Real Time Counter. It is calibrated during production to provide a default frequency which is close to its nominal frequency.

10.3.3 32.768 kHz Crystal Oscillator

The 32.768 kHz Crystal Oscillator is a low power driver for an external watch crystal. It can be used as system clock source or as asynchronous clock source for the Real Time Counter.

10.3.4 0.4 - 16 MHz Crystal Oscillator

The 0.4 - 16 MHz Crystal Oscillator is a driver intended for driving both external resonators and crystals ranging from 400 kHz to 16 MHz.

10.3.5 2 MHz Run-time Calibrated Internal Oscillator

The 2 MHz Run-time Calibrated Internal Oscillator is a high frequency oscillator. It is calibrated during production to provide a default frequency which is close to its nominal frequency. The oscillator can use the 32.768 kHz Calibrated Internal Oscillator or the 32 kHz Crystal Oscillator as a source for calibrating the frequency run-time to compensate for temperature and voltage drift hereby optimizing the accuracy of the oscillator.

10.3.6 32 MHz Run-time Calibrated Internal Oscillator

The 32 MHz Run-time Calibrated Internal Oscillator is a high frequency oscillator. It is calibrated during production to provide a default frequency which is close to its nominal frequency. The oscillator can use the 32.768 kHz Calibrated Internal Oscillator or the 32 kHz Crystal Oscillator as a source for calibrating the frequency run-time to compensate for temperature and voltage drift hereby optimizing the accuracy of the oscillator.

10.3.7 External Clock input

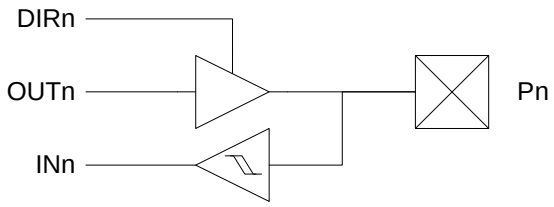
The external clock input gives the possibility to connect a clock from an external source.

10.3.8 PLL with Multiplication factor 1 - 31x

The PLL provides the possibility of multiplying a frequency by any number from 1 to 31. In combination with the prescalers, this gives a wide range of output frequencies from all clock sources.

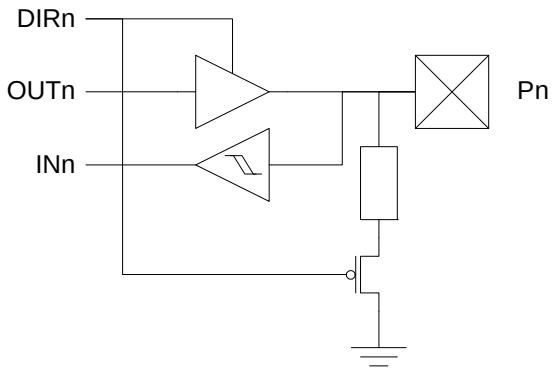
15.3.1 Push-pull

Figure 15-1. I/O configuration - Totem-pole



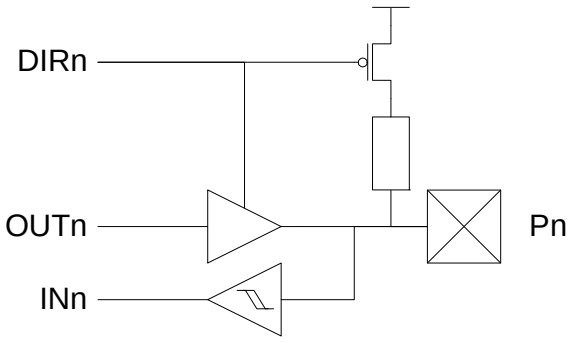
15.3.2 Pull-down

Figure 15-2. I/O configuration - Totem-pole with pull-down (on input)



15.3.3 Pull-up

Figure 15-3. I/O configuration - Totem-pole with pull-up (on input)



15.3.4 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

20. TWI - Two Wire Interface

20.1 Features

- **Two Identical TWI peripherals**
- **Simple yet Powerful and Flexible Communication Interface**
- **Both Master and Slave Operation Supported**
- **Device can Operate as Transmitter or Receiver**
- **7-bit Address Space Allows up to 128 Different Slave Addresses**
- **Multi-master Arbitration Support**
- **Up to 400 kHz Data Transfer Speed**
- **Slew-rate Limited Output Drivers**
- **Noise Suppression Circuitry Rejects Spikes on Bus Lines**
- **Fully Programmable Slave Address with General Call Support**
- **Address Recognition Causes Wake-up when in Sleep Mode**
- **I^2C and System Management Bus (SMBus) compatible**

20.2 Overview

The Two-Wire Interface (TWI) is a bi-directional wired-AND bus with only two lines, the clock (SCL) line and the data (SDA) line. The protocol makes it possible to interconnect up to 128 individually addressable devices. Since it is a multi-master bus, one or more devices capable of taking control of the bus can be connected.

The only external hardware needed to implement the bus is a single pull-up resistor for each of the TWI bus lines. Mechanisms for resolving bus contention are inherent in the TWI protocol.

PORTC and PORTE each has one TWI. Notation of these peripherals are TWIC and TWIE.

24. Crypto Engine

24.1 Features

- **Data Encryption Standard (DES) CPU instruction**
- **Advanced Encryption Standard (AES) Crypto module**
- **DES Instruction**
  - **Encryption and Decryption**
  - **Single-cycle DES instruction**
  - **Encryption/Decryption in 16 clock cycles per 8-byte block**
- **AES Crypto Module**
  - **Encryption and Decryption**
  - **Support 128-bit keys**
  - **Support XOR data load mode to the State memory for Cipher Block Chaining**
  - **Encryption/Decryption in 375 clock cycles per 16-byte block**

24.2 Overview

The Advanced Encryption Standard (AES) and Data Encryption Standard (DES) are two commonly used encryption standards. These are supported through an AES peripheral module and a DES CPU instruction. All communication interfaces and the CPU can optionally use AES and DES encrypted communication and data storage.

DES is supported by a DES instruction in the AVR XMEGA CPU. The 8-byte key and 8-byte data blocks must be loaded into the Register file, and then DES must be executed 16 times to encrypt/decrypt the data block.

The AES Crypto Module encrypts and decrypts 128-bit data blocks with the use of a 128-bit key. The key and data must be loaded into the key and state memory in the module before encryption/decryption is started. It takes 375 peripheral clock cycles before the encryption/decryption is done and decrypted/encrypted data can be read out, and an optional interrupt can be generated. The AES Crypto Module also has DMA support with transfer triggers when encryption/decryption is done and optional auto-start of encryption/decryption when the state memory is fully loaded.

Bit Number	Signal Name	Module
125	PJ7.Bidir	PORT J
124	PJ7.Control	
123	PJ6.Bidir	
122	PJ6.Control	
121	PJ5.Bidir	
120	PJ5.Control	
119	PJ4.Bidir	
118	PJ4.Control	
117	PJ3.Bidir	
116	PJ3.Control	
115	PJ2.Bidir	
114	PJ2.Control	
113	PJ1.Bidir	
112	PJ1.Control	
111	PJ0.Bidir	
110	PJ0.Control	
109	PH7.Bidir	PORT H
108	PH7.Control	
107	PH6.Bidir	
106	PH6.Control	
105	PH5.Bidir	
104	PH5.Control	
103	PH4.Bidir	
102	PH4.Control	
101	PH3.Bidir	
100	PH3.Control	
99	PH2.Bidir	
98	PH2.Control	
97	PH1.Bidir	
96	PH1.Control	
95	PH0.Bidir	
94	PH0.Control	
93	PF7.Bidir	PORT F
92	PF7.Control	
91	PF6.Bidir	
90	PF6.Control	
89	PF5.Bidir	
88	PF5.Control	
87	PF4.Bidir	
86	PF4.Control	
85	PF3.Bidir	
84	PF3.Control	
83	PF2.Bidir	
82	PF2.Control	
81	PF1.Bidir	
80	PF1.Control	
79	PF0.Bidir	
78	PF0.Control	
77	PE7.Bidir	PORT E
76	PE7.Control	
75	PE6.Bidir	
74	PE6.Control	
73	PE5.Bidir	
72	PE5.Control	
71	PE4.Bidir	
70	PE4.Control	
69	PE3.Bidir	
68	PE3.Control	
67	PE2.Bidir	
66	PE2.Control	
65	PE1.Bidir	
64	PE1.Control	
63	PE0.Bidir	
62	PE0.Control	

Mnemonics	Operands	Description	Operation	Flags	#Clocks
CALL	k	call Subroutine	PC ← k	None	3 / 4[1]
RET		Subroutine Return	PC ← STACK	None	4 / 5[1]
RETI		Interrupt Return	PC ← STACK	I	4 / 5[1]
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1 / 2 / 3
CP	Rd,Rr	Compare	Rd - Rr	Z,C,N,V,S,H	1
CPC	Rd,Rr	Compare with Carry	Rd - Rr - C	Z,C,N,V,S,H	1
CPI	Rd,K	Compare with Immediate	Rd - K	Z,C,N,V,S,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b) = 0) PC ← PC + 2 or 3	None	1 / 2 / 3
SBRS	Rr, b	Skip if Bit in Register Set	if (Rr(b) = 1) PC ← PC + 2 or 3	None	1 / 2 / 3
SBIC	A, b	Skip if Bit in I/O Register Cleared	if (I/O(A,b) = 0) PC ← PC + 2 or 3	None	2 / 3 / 4
SBIS	A, b	Skip if Bit in I/O Register Set	If (I/O(A,b) =1) PC ← PC + 2 or 3	None	2 / 3 / 4
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC ← PC + k + 1	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC ← PC + k + 1	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1 / 2
BRLT	k	Branch if Less Than, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1 / 2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2
Data Transfer Instructions					
MOV	Rd, Rr	Copy Register	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Pair	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LDS	Rd, k	Load Direct from data space	Rd ← (k)	None	2[1][2]
LD	Rd, X	Load Indirect	Rd ← (X)	None	1[1][2]
LD	Rd, X+	Load Indirect and Post-Increment	Rd ← (X) X ← X + 1	None	1[1][2]
LD	Rd, -X	Load Indirect and Pre-Decrement	X ← X - 1, ← X - 1 Rd ← (X) ← (X)	None	2[1][2]
LD	Rd, Y	Load Indirect	Rd ← (Y) ← (Y)	None	1[1][2]
LD	Rd, Y+	Load Indirect and Post-Increment	Rd ← (Y) Y ← Y + 1	None	1[1][2]

35.3 Power-down Supply Current

Figure 35-15. Power-down Supply Current vs. Temperature

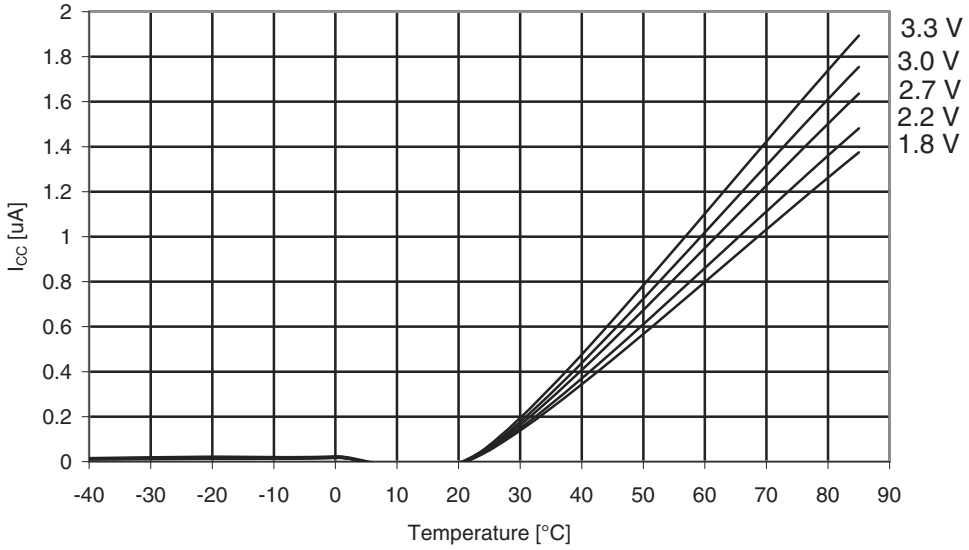


Figure 35-16. Power-down Supply Current vs. Temperature

With WDT and sampled BOD enabled.

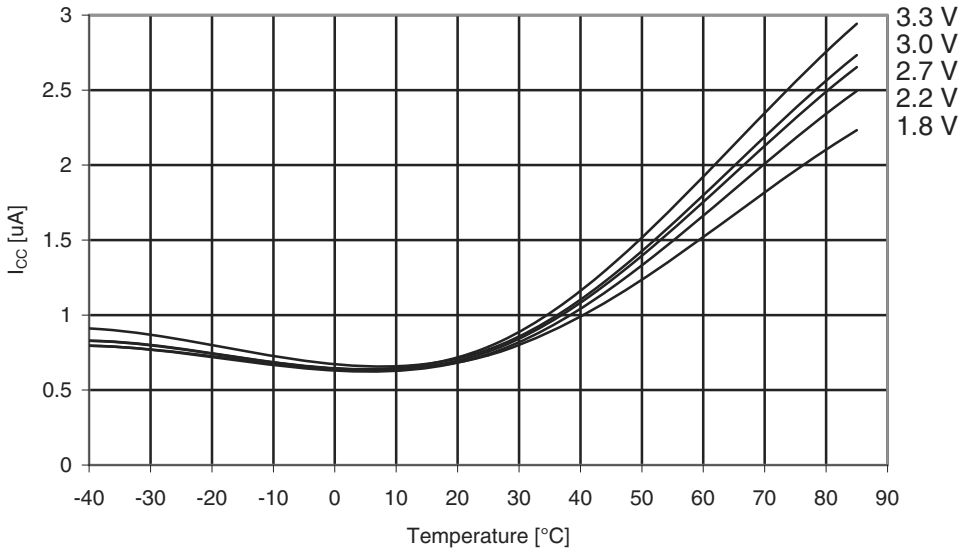


Figure 35-19. Reset Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 3.0V

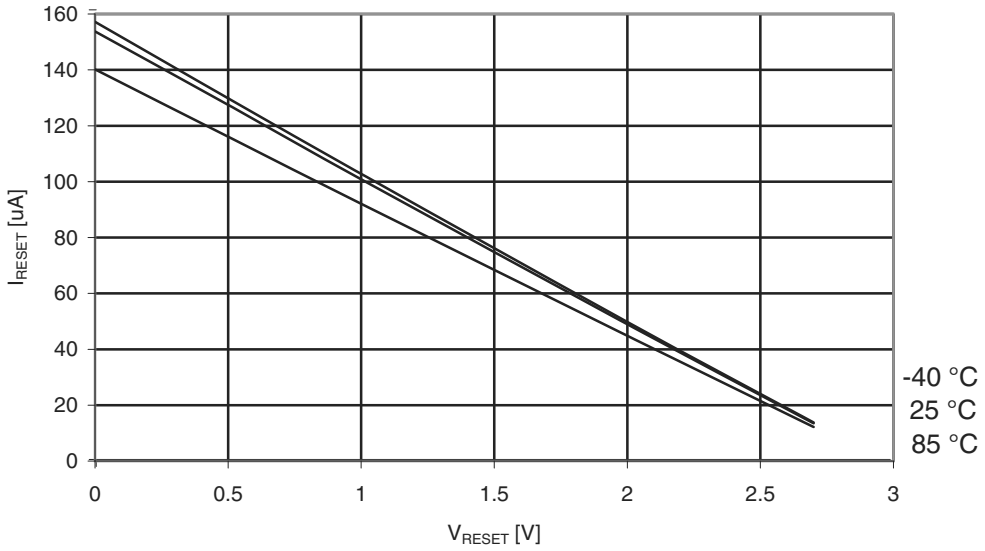
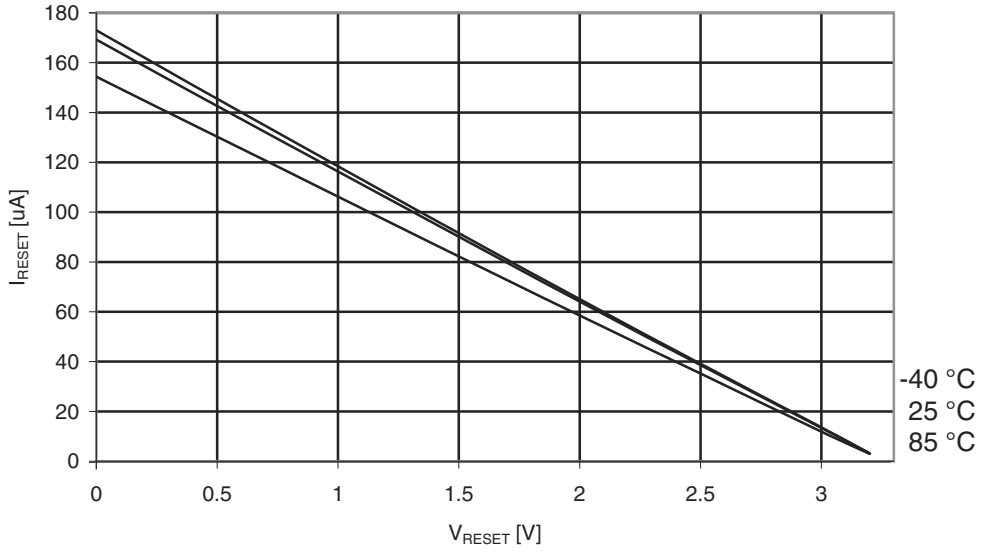


Figure 35-20. Reset Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 3.3V



35.6 Pin Output Voltage vs. Sink/Source Current

Figure 35-21. I/O Pin Output Voltage vs. Source Current

Vcc = 1.8V

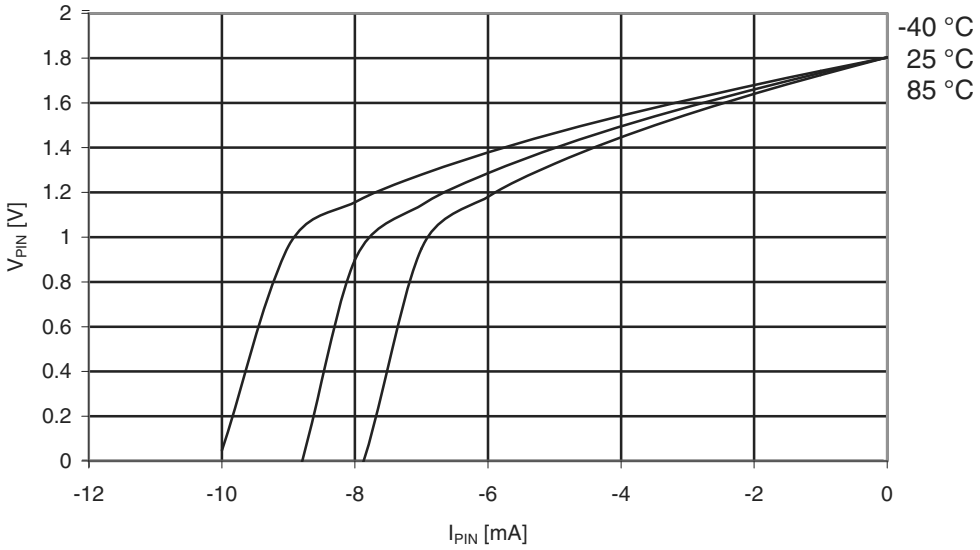
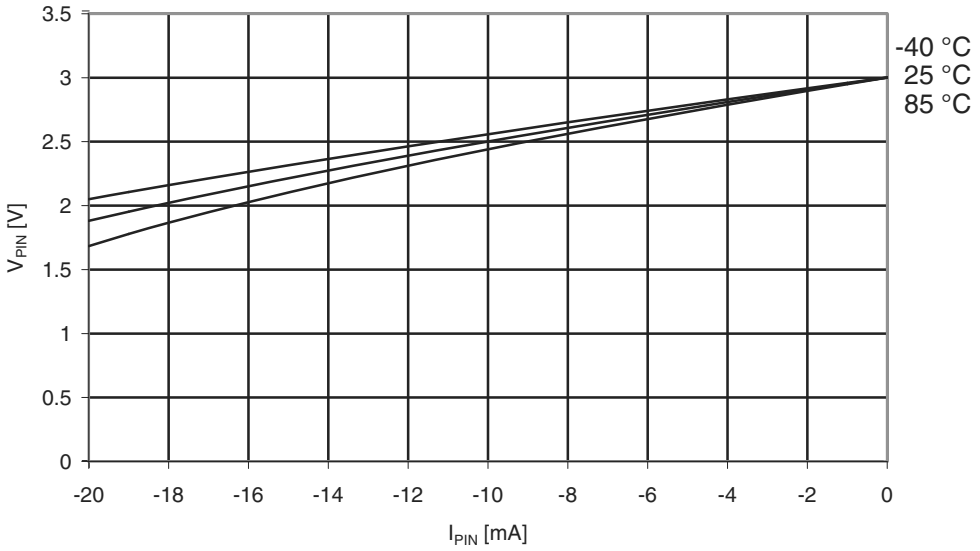


Figure 35-22. I/O Pin Output Voltage vs. Source Current

Vcc = 3.0V



35.9.2 Internal 2 MHz Oscillator

Figure 35-35. Internal 2 MHz Oscillator CALA Calibration Step Size

T = -40 to 85°C, V_{CC} = 3V

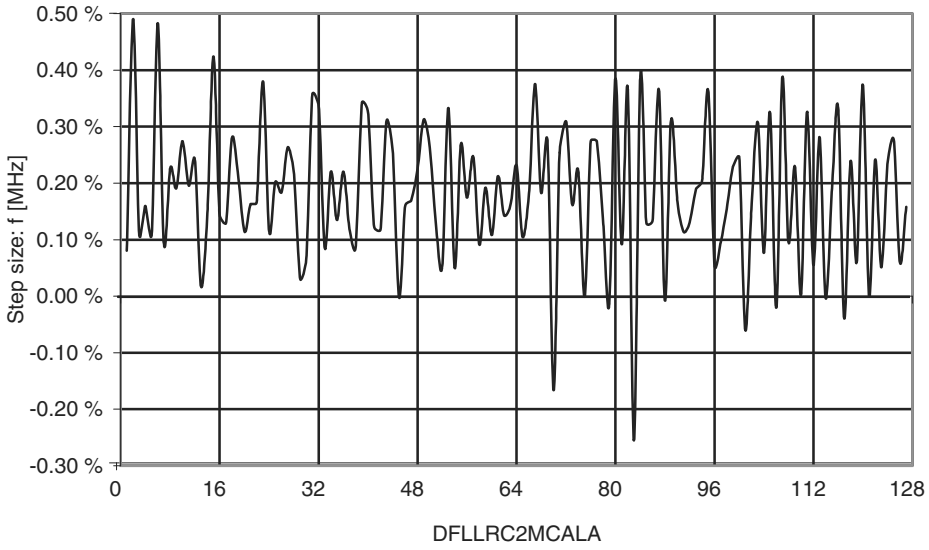
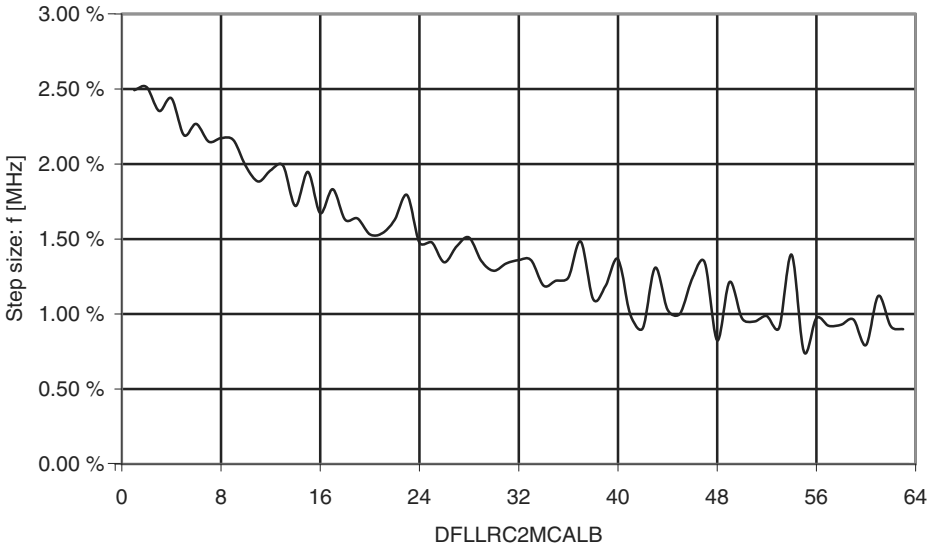


Figure 35-36. Internal 2 MHz Oscillator CALB Calibration Step Size

T = -40 to 85°C, V_{CC} = 3V



35.10 Module current consumption

Figure 35-39. AC current consumption vs. Vcc

Low-power Mode

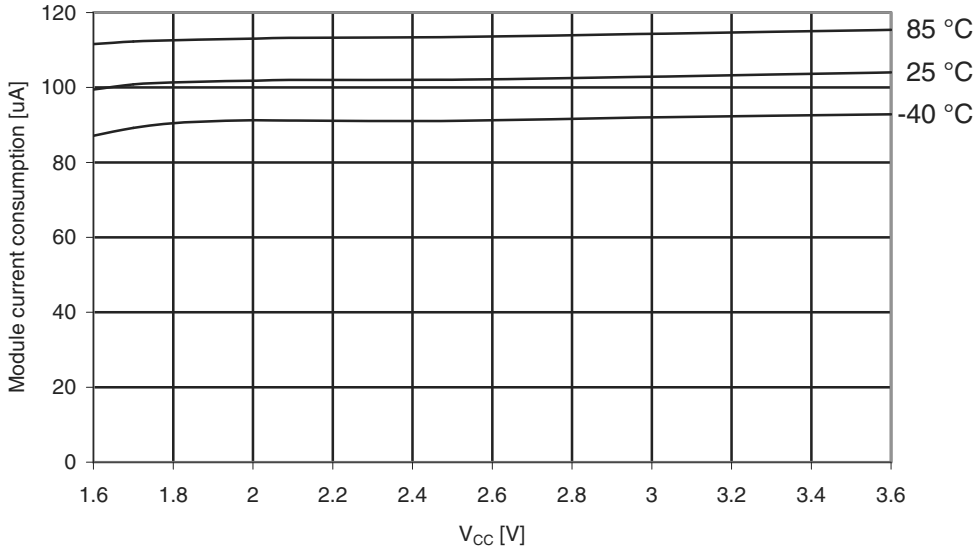
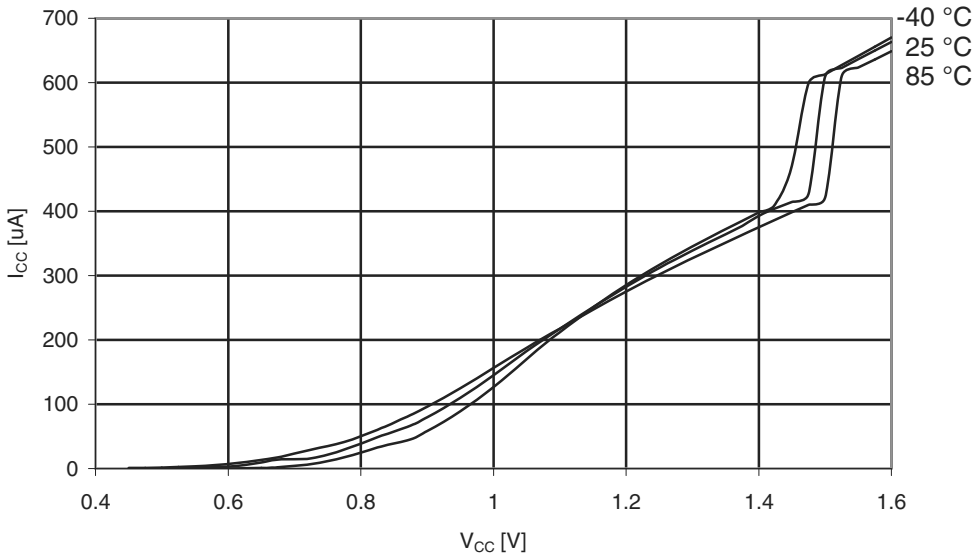


Figure 35-40. Power-up current consumption vs. Vcc



36. Errata

36.1 ATxmega256A3

36.1.1 rev. E

- **Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously**
- **VCC voltage scaler for AC is non-linear**
- **ADC has increased INL error for some operating conditions**
- **ADC gain stage output range is limited to 2.4 V**
- **ADC Event on compare match non-functional**
- **Bandgap measurement with the ADC is non-functional when VCC is below 2.7V**
- **Accuracy lost on first three samples after switching input to ADC gain stage**
- **Configuration of PGM and CWCM not as described in XMEGA A Manual**
- **PWM is not restarted properly after a fault in cycle-by-cycle mode**
- **BOD will be enabled at any reset**
- **DAC is nonlinear and inaccurate when reference is above 2.4V or VCC - 0.6V**
- **DAC has increased INL or noise for some operating conditions**
- **DAC refresh may be blocked in S/H mode**
- **Conversion lost on DAC channel B in event triggered mode**
- **EEPROM page buffer always written when NVM DATA0 is written**
- **Pending full asynchronous pin change interrupts will not wake the device**
- **Pin configuration does not affect Analog Comparator Output**
- **NMI Flag for Crystal Oscillator Failure automatically cleared**
- **Crystal start-up time required after power-save even if crystal is source for RTC**
- **RTC Counter value not correctly read after sleep**
- **Pending asynchronous RTC-interrupts will not wake up device**
- **TWI Transmit collision flag not cleared on repeated start**
- **Clearing TWI Stop Interrupt Flag may lock the bus**
- **TWI START condition at bus timeout will cause transaction to be dropped**
- **TWI Data Interrupt Flag (DIF) erroneously read as set**
- **WDR instruction inside closed window will not issue reset**

1. **Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously**

   If the Bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for another AC, the first comparator will be affected for up to 1 µs and could potentially give a wrong comparison result.

   Problem fix/Workaround

   If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. **VCC voltage scaler for AC is non-linear**

   The 6-bit VCC voltage scaler in the Analog Comparators is non-linear.

26. WDR instruction inside closed window will not issue reset

When a WDR instruction is execute within one ULP clock cycle after updating the window control register, the counter can be cleared without giving a system reset.

Problem fix/Workaround

Wait at least one ULP clock cycle before executing a WDR instruction.

Problem fix/Workaround

Do not set the BOD level higher than VCC even if the BOD is not used.

11. DAC is nonlinear and inaccurate when reference is above 2.4V or VCC - 0.6V

Using the DAC with a reference voltage above 2.4V or VCC - 0.6V will give inaccurate output when converting codes that give below 0.75V output:

– ±10 LSB for continuous mode

– ±200 LSB for Sample and Hold mode

Problem fix/Workaround

None.

12. DAC has increased INL or noise for some operating conditions

Some DAC configurations or operating condition will result in increased output error.

– Continous mode: ±5 LSB

– Sample and hold mode: ±15 LSB

– Sample and hold mode for reference above 2.0v: up to ±100 LSB

Problem fix/Workaround

None.

13. DAC refresh may be blocked in S/H mode

If the DAC is running in Sample and Hold (S/H) mode and conversion for one channel is done at maximum rate (i.e. the DAC is always busy doing conversion for this channel), this will block refresh signals to the second channel.

Problem fix/Workaround

When using the DAC in S/H mode, ensure that none of the channels is running at maximum conversion rate, or ensure that the conversion rate of both channels is high enough to not require refresh.

14. Conversion lost on DAC channel B in event triggered mode

If during dual channel operation channel 1 is set in auto trigged conversion mode, channel 1 conversions are occasionally lost. This means that not all data-values written to the Channel 1 data register are converted.

Problem fix/Workaround

Keep the DAC conversion interval in the range 000-001 (1 and 3 CLK), and limit the Peripheral clock frequency so the conversion internal never is shorter than 1.5 µs.

15. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/Workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.