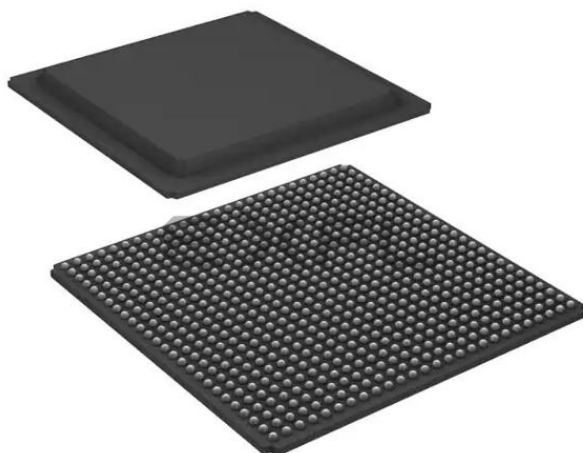




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	2816
Number of Logic Elements/Cells	25344
Total RAM Bits	589824
Number of I/O	502
Number of Gates	1400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1400a-4fg676i

I/O Timing

Pin-to-Pin Clock-to-Output Times

Table 18: Pin-to-Pin Clock-to-Output Times for the IOB Output Path

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Clock-to-Output Times						
T _{ICKOFDCM}	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use.	LVCMOS25 ⁽²⁾ , 12mA output drive, Fast slew rate, with DCM ⁽³⁾	XC3S50A	3.18	3.42	ns
			XC3S200A	3.21	3.27	ns
			XC3S400A	2.97	3.33	ns
			XC3S700A	3.39	3.50	ns
			XC3S1400A	3.51	3.99	ns
T _{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.	LVCMOS25 ⁽²⁾ , 12mA output drive, Fast slew rate, without DCM	XC3S50A	4.59	5.02	ns
			XC3S200A	4.88	5.24	ns
			XC3S400A	4.68	5.12	ns
			XC3S700A	4.97	5.34	ns
			XC3S1400A	5.06	5.69	ns

Notes:

1. The numbers in this table are tested using the methodology presented in [Table 27](#) and are based on the operating conditions set forth in [Table 8](#) and [Table 11](#).
2. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from [Table 23](#). If the latter is true, *add* the appropriate Output adjustment from [Table 26](#).
3. DCM output jitter is included in all measurements.

Table 22: Propagation Times for the IOB Input Path(Continued)

Symbol	Description	Conditions	DELAY_VALUE	Device	Speed Grade		Units
					-5	-4	
					Max	Max	
T _{IOPID}	The time it takes for data to travel from the Input pin to the I output with the input delay programmed	LVCMOS25 ⁽²⁾	5	XC3S1400A	3.17	3.52	ns
			6		3.52	3.92	ns
			7		3.82	4.18	ns
			8		4.10	4.57	ns
			9		3.84	4.31	ns
			10		4.20	4.79	ns
			11		4.46	5.06	ns
			12		4.87	5.51	ns
			13		5.07	5.73	ns
			14		5.43	6.08	ns
			15		5.73	6.33	ns
			16		6.01	6.77	ns
T _{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25 ⁽²⁾	IFD_DELAY_VALUE=0	XC3S50A	1.70	1.81	ns
				XC3S200A	1.85	2.04	ns
				XC3S400A	1.44	1.74	ns
				XC3S700A	1.48	1.74	ns
				XC3S1400A	1.50	1.97	ns
T _{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25 ⁽²⁾	1	XC3S50A	2.30	2.41	ns
			2		3.24	3.35	ns
			3		3.65	3.98	ns
			4		4.18	4.55	ns
			5		4.02	4.47	ns
			6		4.86	5.32	ns
			7		5.61	6.17	ns
			8		6.11	6.75	ns
			1	XC3S200A	2.19	2.43	ns
			2		2.86	3.16	ns
			3		3.52	4.01	ns
			4		4.02	4.60	ns
			5		3.83	4.43	ns
			6		4.70	5.46	ns
			7		5.48	6.33	ns
			8		5.99	6.94	ns
			1	XC3S400A	1.93	2.25	ns
			2		2.57	2.90	ns
			3		3.16	3.66	ns
			4		3.63	4.19	ns

Table 22: Propagation Times for the IOB Input Path(Continued)

Symbol	Description	Conditions	DELAY_VALUE	Device	Speed Grade		Units
					-5	-4	
					Max	Max	
T _{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25 ⁽²⁾	5	XC3S400A	3.55	4.18	ns
			6		4.34	5.03	ns
			7		5.09	5.88	ns
			8		5.58	6.42	ns
			1	XC3S700A	1.96	2.18	ns
			2		2.76	3.06	ns
			3		3.45	3.95	ns
			4		3.97	4.54	ns
			5		3.83	4.37	ns
			6		4.74	5.42	ns
			7		5.53	6.33	ns
			8		6.06	6.96	ns
			1	XC3S1400A	1.93	2.40	ns
			2		2.69	3.15	ns
			3		3.52	3.99	ns
			4		3.89	4.55	ns
			5		3.95	4.42	ns
			6		4.53	5.32	ns
			7		5.30	6.21	ns
			8		5.83	6.80	ns

Notes:

1. The numbers in this table are tested using the methodology presented in [Table 27](#) and are based on the operating conditions set forth in [Table 8](#) and [Table 11](#).
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from [Table 23](#).

Table 31: CLB Distributed RAM Switching Characteristics

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T _{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output	–	1.69	–	2.01	ns
Setup Times						
T _{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	–0.07	–	–0.02	–	ns
T _{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.18	–	0.36	–	ns
T _{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.30	–	0.59	–	ns
Hold Times						
T _{DH}	Hold time of the BX and BY data inputs after the active transition at the CLK input of the distributed RAM	0.13	–	0.13	–	ns
T _{AH} , T _{WH}	Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM	0.01	–	0.01	–	ns
Clock Pulse Width						
T _{WPH} , T _{WPL}	Minimum High or Low pulse width at CLK input	0.88	–	1.01	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in [Table 8](#).

Table 32: CLB Shift Register Switching Characteristics

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T _{REG}	Time from the active edge at the CLK input to data appearing on the shift register output	–	4.11	–	4.82	ns
Setup Times						
T _{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.13	–	0.18	–	ns
Hold Times						
T _{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0.16	–	0.16	–	ns
Clock Pulse Width						
T _{WPH} , T _{WPL}	Minimum High or Low pulse width at CLK input	0.90	–	1.01	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in [Table 8](#).

Table 37: Switching Characteristics for the DLL

Symbol	Description	Device	Speed Grade				Units	
			-5		-4			
			Min	Max	Min	Max		
Output Frequency Ranges								
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs	All	5	280	5	250	MHz	
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs		5	200	5	200	MHz	
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs		10	334	10	334	MHz	
CLKOUT_FREQ_DV	Frequency for the CLKDV output		0.3125	186	0.3125	166	MHz	
Output Clock Jitter ^(2,3,4)								
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output	All	—	±100	—	±100	ps	
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output		—	±150	—	±150	ps	
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output		—	±150	—	±150	ps	
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output		—	±150	—	±150	ps	
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs		—	±[0.5% of CLKIN period + 100]	—	±[0.5% of CLKIN period + 100]	ps	
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division		—	±150	—	±150	ps	
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division		—	±[0.5% of CLKIN period + 100]	—	±[0.5% of CLKIN period + 100]	ps	
Duty Cycle ⁽⁴⁾								
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion	All	—	±[1% of CLKIN period + 350]	—	±[1% of CLKIN period + 350]	ps	
Phase Alignment ⁽⁴⁾								
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs	All	—	±150	—	±150	ps	
CLKOUT_PHASE_DLL	Phase offset between DLL outputs		CLK0 to CLK2X (not CLK2X180)	—	±[1% of CLKIN period + 100]	—	±[1% of CLKIN period + 100]	ps
			All others	—	±[1% of CLKIN period + 150]	—	±[1% of CLKIN period + 150]	ps
Lock Time								
LOCK_DLL ⁽³⁾	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	5 MHz ≤ F _{CLKIN} ≤ 15 MHz	All	—	5	—	5	ms
		F _{CLKIN} > 15 MHz		—	600	—	600	μs
Delay Lines								
DCM_DELAY_STEP ⁽⁵⁾	Finest delay resolution, averaged over all steps	All	15	35	15	35	ps	

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8 and Table 36.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, the data sheet specifies a maximum jitter of "±[1% of CLKIN period + 150]". Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250ps.
5. The typical delay step size is 23 ps.

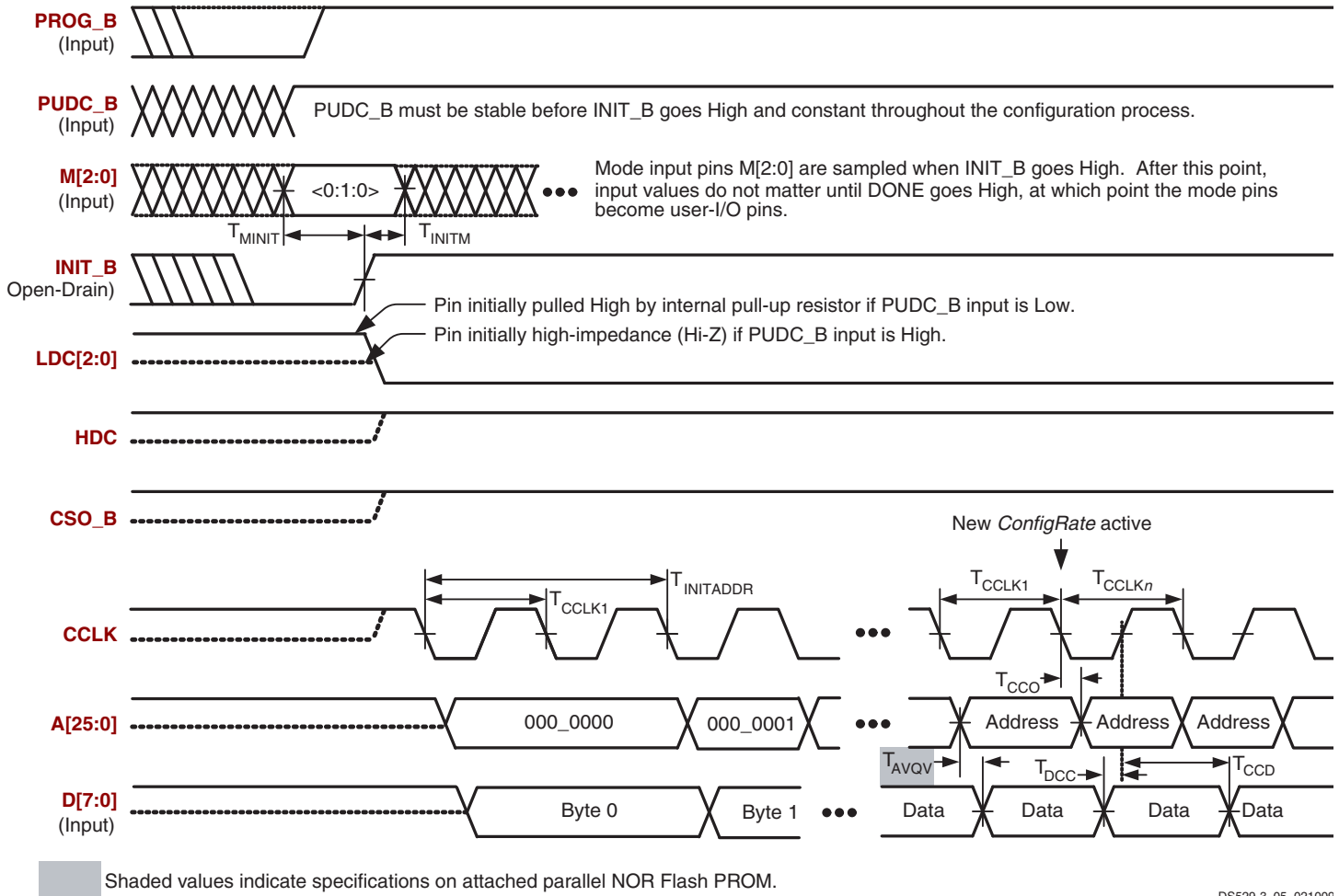
Table 53: Configuration Timing Requirements for Attached SPI Serial Flash

Symbol	Description	Requirement	Units
T_{CCS}	SPI serial Flash PROM chip-select time	$T_{CCS} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DSU}	SPI serial Flash PROM data input setup time	$T_{DSU} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DH}	SPI serial Flash PROM data input hold time	$T_{DH} \leq T_{MCCH1}$	ns
T_V	SPI serial Flash PROM data clock-to-output time	$T_V \leq T_{MCCLn} - T_{DCC}$	ns
f_C or f_R	Maximum SPI serial Flash PROM clock frequency (also depends on specific read command used)	$f_C \geq \frac{1}{T_{CCLKn(min)}}$	MHz

Notes:

1. These requirements are for successful FPGA configuration in SPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.

Byte Peripheral Interface (BPI) Configuration Timing



DS529-3_05_021009

Figure 15: Waveforms for Byte-wide Peripheral Interface (BPI) Configuration

Table 54: Timing for Byte-wide Peripheral Interface (BPI) Configuration Mode

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	See Table 46		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting	See Table 46		
T_{MINIT}	Setup time on M[2:0] mode pins before the rising edge of INIT_B	50	—	ns
T_{INITM}	Hold time on M[2:0] mode pins after the rising edge of INIT_B	0	—	ns
$T_{INITADDR}$	Minimum period of initial A[25:0] address cycle; LDC[2:0] and HDC are asserted and valid	5	5	T_{CCLK1} cycles
T_{CCO}	Address A[25:0] outputs valid after CCLK falling edge	See Table 50		
T_{DCC}	Setup time on D[7:0] data inputs before CCLK rising edge	See T_{SMDCC} in Table 51		
T_{CCD}	Hold time on D[7:0] data inputs after CCLK rising edge	0	—	ns

Introduction

This section describes how the various pins on a Spartan®-3A FPGA connect within the supported component packages, and provides device-specific thermal characteristics. For general information on the pin functions and the package characteristics, see the Packaging section of UG331: *Spartan-3 Generation FPGA User Guide*.

- **UG331: Spartan-3 Generation FPGA User Guide**
www.xilinx.com/support/documentation/user_guides/ug331.pdf

Spartan-3A FPGAs are available in both standard and Pb-free, RoHS versions of each package, with the Pb-free version adding a “G” to the middle of the package code.

Table 57: Types of Pins on Spartan-3A FPGAs

Type / Color Code	Description	Pin Name(s) in Type
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO_# IO_Lxxy_#
INPUT	Unrestricted, general-purpose input-only pin. This pin does not have an output structure, differential termination resistor, or PCI clamp diode.	IP_# IP_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. See UG332: Spartan-3 Generation Configuration User Guide for additional information on these signals.	M[2:0] PUDC_B CCLK MOSI/CSI_B D[7:1] D0/DIN DOUT CSO_B RDWR_B INIT_B A[25:0] VS[2:0] LDC[2:0] HDC
VREF	Dual-purpose pin that is either a user-I/O pin or Input-only pin, or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected.	IP/VREF_# IP_Lxxy_#/VREF_# IO/VREF_# IO_Lxxy_#/VREF_#
CLK	Either a user-I/O pin or an input to a specific clock buffer driver. Most packages have 16 global clock inputs that optionally clock the entire device. The exceptions are the TQ144 and the XC3S50A in the FT256 package). The RHCLK inputs optionally clock the right half of the device. The LHCLK inputs optionally clock the left half of the device. See the Using Global Clock Resources chapter in UG331: Spartan-3 Generation FPGA User Guide for additional information on these signals.	IO_Lxxy_#/GCLK[15:0], IO_Lxxy_#/LHCLK[7:0], IO_Lxxy_#/RHCLK[7:0]
CONFIG	Dedicated configuration pin, two per device. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See the UG332: Spartan-3 Generation Configuration User Guide for additional information on the DONE and PROG_B signals.	DONE, PROG_B

Except for the thermal characteristics, all information for the standard package applies equally to the Pb-free package.

Pin Types

Most pins on a Spartan-3A FPGA are general-purpose, user-defined I/O pins. There are, however, up to 12 different functional types of pins on Spartan-3A FPGA packages, as outlined in [Table 57](#). In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Package Overview

[Table 60](#) shows the six low-cost, space-saving production package styles for the Spartan-3A family.

Table 60: Spartan-3A Family Package Options

Package	Leads	Type	Maximum I/O	Lead Pitch (mm)	Body Area (mm)	Height (mm)	Mass ⁽¹⁾ (g)
VQ100 / VQG100	100	Very Thin Quad Flat Pack (VQFP)	68	0.5	14 x 14	1.20	0.6
TQ144 / TQG144	144	Thin Quad Flat Pack (TQFP)	108	0.5	20 x 20	1.60	1.4
FT256 / FTG256	256	Fine-pitch Thin Ball Grid Array (FBGA)	195	1.0	17 x 17	1.55	0.9
FG320 / FGG320	320	Fine-pitch Ball Grid Array (FBGA)	251	1.0	19 x 19	2.00	1.4
FG400 / FGG400	400	Fine-pitch Ball Grid Array (FBGA)	311	1.0	21 x 21	2.43	2.2
FG484 / FGG484	484	Fine-pitch Ball Grid Array (FBGA)	375	1.0	23 x 23	2.60	2.2
FG676 / FGG676	676	Fine-pitch Ball Grid Array (FBGA)	502	1.0	27 x 27	2.60	3.4

Notes:

1. Package mass is $\pm 10\%$.

Each package style is available in an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra 'G' in the package style name. For example, the standard "CS484" package becomes "CSG484" when ordered as the Pb-free option. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in [Table 61](#).

For additional package information, see [UG112: Device Package User Guide](#).

Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx web site at the specified location in [Table 61](#).

Material Declaration Data Sheets (MDDS) are also available on the [Xilinx web site](#) for each package.

Table 61: Xilinx Package Documentation

Package	Drawing	MDDS
VQ100	Package Drawing	PK173_VQ100
VQG100		PK130_VQG100
TQ144	Package Drawing	PK169_TQ144
TQG144		PK126_TQG144
FT256	Package Drawing	PK158_FT256
FTG256		PK115_FTG256
FG320	Package Drawing	PK152_FG320
FGG320		PK106_FGG320
FG400	Package Drawing	PK182_FG400
FGG400		PK108_FGG400
FG484	Package Drawing	PK183_FG484
FGG484		PK110_FGG484
FG676	Package Drawing	PK155_FG676
FGG676		PK111_FGG676

User I/Os by Bank

Table 64 indicates how the 68 available user-I/O pins are distributed between the four I/O banks on the VQ100 package.

Table 64: User I/Os Per Bank for the XC3S50A and XC3S200A in the VQ100 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	15	3	1	1	3	7
Right	1	13	6	0	0	1	6
Bottom	2	26	2	0	19	1	4
Left	3	14	6	1	0	1	6
TOTAL		68	17	2	20	6	23

Footprint Migration Differences

The XC3S50A and XC3S200 have common VQ100 pinouts except for some differences in alignment of differential I/O pairs.

Differential I/O Alignment Differences

Some differential I/O pairs in the VQ100 on the XC3S50A FPGA are aligned differently than the corresponding pairs on the XC3S200A FPGAs, as shown in Table 65. All the mismatched pairs are in I/O Bank 2. These differences are indicated with the black diamond character (◆) in the footprint diagrams Figure 17 and Figure 18.

Table 65: Differential I/O Differences in VQ100

VQ100 Pin	Bank	XC3S50A	XC3S200A
P29	2	IIO_L04P_2/VS2	IO_L03N_2/VS2
P30		IO_L03N_2/VS1	IO_L04P_2/VS1
P33		IO_L06P_2	IO_L05N_2
P34		IO_L05N_2/D7	IO_L06P_2/D7
P51		IO_L11N_2/D0/DIN/MISO	IO_L12P_2/D0/DIN/MISO
P52		IO_L12P_2/D1	IO_L11N_2/D1

FT256: 256-ball Fine-pitch, Thin Ball Grid Array

The 256-ball fine-pitch, thin ball grid array package, FT256, supports all five Spartan-3A FPGAs. The XC3S200A and XC3S400A have identical footprints, and the XC3S700A and XC3S1400A have identical footprints. The XC3S50A is compatible with the XC3S200A/XC3S400A but has 51 unconnected balls. The XC3S200A/XC3S400A is similar to the XC3S700A/XC3S1400A, but the XC3S700A/XC3S1400A adds more power and ground pins and therefore is not compatible.

Table 68 lists all the package pins for the XC3S50A, XC3S200A, and XC3S400A. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The highlighted rows indicate pinout differences between the XC3S50A, the XC3S200A, and the XC3S400A FPGAs. The XC3S50A has 51 unconnected balls, indicated as N.C. (No Connection) in **Table 68** and **Figure 20** and with the black diamond character (◆) in **Table 68**. **Figure 21** provides the common footprint for the XC3S200A and XC3S400A.

Table 68 also indicates that some differential I/O pairs have different assignments between the XC3S50A and the XC3S200A/XC3S400A, highlighted in light blue. See **"Footprint Migration Differences," page 99** for additional information.

All other balls have nearly identical functionality on all three devices. **Table 73** summarizes the XC3S50A FPGA footprint migration differences for the FT256 package.

The XC3S50A does not support the address output pins for the Byte-wide Peripheral Interface (BPI) configuration mode.

Table 69 lists all the package pins for the XC3S700A and XC3S1400A. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier. **Figure 22** provides the common footprint for the XC3S200A and XC3S400A.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 68: Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400)

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
0	IO_L01N_0	IO_L01N_0	C13	I/O
0	IO_L01P_0	IO_L01P_0	D13	I/O
0	IO_L02N_0	IO_L02N_0	B14	I/O
0	IO_L02P_0/ VREF_0	IO_L02P_0/ VREF_0	B15	VREF
0	IO_L03N_0	IO_L03N_0	D11	I/O
0	IO_L03P_0	IO_L03P_0	C12	I/O
0	IO_L04N_0	IO_L04N_0	A13	I/O
0	IO_L04P_0	IO_L04P_0	A14	I/O
0	N.C. (◆)	IO_L05N_0	A12	I/O
0	IP_0	IO_L05P_0	B12	I/O
0	N.C. (◆)	IO_L06N_0/ VREF_0	E10	VREF
0	N.C. (◆)	IO_L06P_0	D10	I/O
0	IO_L07N_0	IO_L07N_0	A11	I/O
0	IO_L07P_0	IO_L07P_0	C11	I/O
0	IO_L08N_0	IO_L08N_0	A10	I/O
0	IO_L08P_0	IO_L08P_0	B10	I/O
0	IO_L09N_0/ GCLK5	IO_L09N_0/ GCLK5	D9	GCLK
0	IO_L09P_0/ GCLK4	IO_L09P_0/ GCLK4	C10	GCLK
0	IO_L10N_0/ GCLK7	IO_L10N_0/ GCLK7	A9	GCLK
0	IO_L10P_0/ GCLK6	IO_L10P_0/ GCLK6	C9	GCLK
0	IO_L11N_0/ GCLK9	IO_L11N_0/ GCLK9	D8	GCLK
0	IO_L11P_0/ GCLK8	IO_L11P_0/ GCLK8	C8	GCLK
0	IO_L12N_0/ GCLK11	IO_L12N_0/ GCLK11	B8	GCLK
0	IO_L12P_0/ GCLK10	IO_L12P_0/ GCLK10	A8	GCLK
0	N.C. (◆)	IO_L13N_0	C7	I/O
0	N.C. (◆)	IO_L13P_0	A7	I/O
0	N.C. (◆)	IO_L14N_0/ VREF_0	E7	VREF
0	N.C. (◆)	IO_L14P_0	F8	I/O
0	IO_L15N_0	IO_L15N_0	B6	I/O
0	IO_L15P_0	IO_L15P_0	A6	I/O
0	IO_L16N_0	IO_L16N_0	C6	I/O
0	IO_L16P_0	IO_L16P_0	D7	I/O
0	IO_L17N_0	IO_L17N_0	C5	I/O

Table 68: Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400) (Continued)

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
VCCINT	VCCINT	VCCINT	K8	VCCINT
VCCINT	VCCINT	VCCINT	K10	VCCINT

Table 69: Spartan-3A FT256 Pinout (XC3S700A, XC3S1400A)

Bank	XC3S700A XC3S1400A	FT256 Ball	Type
0	IO_L01N_0	C13	I/O
0	IO_L01P_0	D13	I/O
0	IO_L02N_0	B14	I/O
0	IO_L02P_0/VREF_0	B15	VREF
0	IO_L03N_0	D12	I/O
0	IO_L03P_0	C12	I/O
0	IO_L04N_0	A13	I/O
0	IO_L04P_0	A14	I/O
0	IO_L05N_0	A12	I/O
0	IO_L05P_0	B12	I/O
0	IO_L06N_0/VREF_0	D10	VREF
0	IO_L06P_0	D11	I/O
0	IO_L07N_0	A11	I/O
0	IO_L07P_0	C11	I/O
0	IO_L08N_0	A10	I/O
0	IO_L08P_0	B10	I/O
0	IO_L09N_0/GCLK5	D9	GCLK
0	IO_L09P_0/GCLK4	C10	GCLK
0	IO_L10N_0/GCLK7	A9	GCLK
0	IO_L10P_0/GCLK6	C9	GCLK
0	IO_L11N_0/GCLK9	D8	GCLK
0	IO_L11P_0/GCLK8	C8	GCLK
0	IO_L12N_0/GCLK11	B8	GCLK
0	IO_L12P_0/GCLK10	A8	GCLK
0	IO_L13N_0	C7	I/O
0	IO_L13P_0	A7	I/O
0	IO_L14N_0/VREF_0	E7	VREF
0	IO_L14P_0	E9	I/O
0	IO_L15N_0	B6	I/O
0	IO_L15P_0	A6	I/O
0	IO_L16N_0	C6	I/O
0	IO_L16P_0	D7	I/O
0	IO_L17N_0	C5	I/O
0	IO_L17P_0	A5	I/O

Table 69: Spartan-3A FT256 Pinout (XC3S700A, XC3S1400A)

Bank	XC3S700A XC3S1400A	FT256 Ball	Type
0	IO_L18N_0	B4	I/O
0	IO_L18P_0	A4	I/O
0	IO_L19N_0	B3	I/O
0	IO_L19P_0	A3	I/O
0	IO_L20N_0/PUDC_B	D5	DUAL
0	IO_L20P_0/VREF_0	C4	VREF
0	IP_0	E6	INPUT
0	VCCO_0	B13	VCCO
0	VCCO_0	B5	VCCO
0	VCCO_0	B9	VCCO
0	VCCO_0	E8	VCCO
1	IO_L01N_1/LDC2	N14	DUAL
1	IO_L01P_1/HDC	N13	DUAL
1	IO_L02N_1/LDC0	P15	DUAL
1	IO_L02P_1/LDC1	R15	DUAL
1	IO_L03N_1/A1	N16	DUAL
1	IO_L03P_1/A0	P16	DUAL
1	IO_L06N_1/A3	K13	DUAL
1	IO_L06P_1/A2	L13	DUAL
1	IO_L07N_1/A5	M16	DUAL
1	IO_L07P_1/A4	M15	DUAL
1	IO_L08N_1/A7	L16	DUAL
1	IO_L08P_1/A6	L14	DUAL
1	IO_L10N_1/A9	J13	DUAL
1	IO_L10P_1/A8	J12	DUAL
1	IO_L11N_1/RHCLK1	K14	RHCLK
1	IO_L11P_1/RHCLK0	K15	RHCLK
1	IO_L12N_1/TRDY1/RHCLK3	J16	RHCLK
1	IO_L12P_1/RHCLK2	K16	RHCLK
1	IO_L15N_1/RHCLK7	H16	RHCLK
1	IO_L15P_1/IRDY1/RHCLK6	H15	RHCLK
1	IO_L16N_1/A11	F16	DUAL
1	IO_L16P_1/A10	G16	DUAL
1	IO_L17N_1/A13	G14	DUAL
1	IO_L17P_1/A12	H13	DUAL
1	IO_L18N_1/A15	F15	DUAL
1	IO_L18P_1/A14	E16	DUAL
1	IO_L19N_1/A17	F14	DUAL
1	IO_L19P_1/A16	G13	DUAL
1	IO_L20N_1/A19	F13	DUAL

Table 69: Spartan-3A FT256 Pinout (XC3S700A,

Bank	XC3S700A XC3S1400A	FT256 Ball	Type
VCCAUX	VCCAUX	F5	VCCAUX
VCCAUX	VCCAUX	H14	VCCAUX
VCCAUX	VCCAUX	H4	VCCAUX
VCCAUX	VCCAUX	L12	VCCAUX
VCCAUX	VCCAUX	L5	VCCAUX
VCCAUX	VCCAUX	M10	VCCAUX
VCCAUX	VCCAUX	M6	VCCAUX
VCCINT	VCCINT	F10	VCCINT
VCCINT	VCCINT	G11	VCCINT
VCCINT	VCCINT	G7	VCCINT
VCCINT	VCCINT	G9	VCCINT
VCCINT	VCCINT	H10	VCCINT
VCCINT	VCCINT	H6	VCCINT
VCCINT	VCCINT	H8	VCCINT
VCCINT	VCCINT	J11	VCCINT
VCCINT	VCCINT	J7	VCCINT
VCCINT	VCCINT	J9	VCCINT
VCCINT	VCCINT	K10	VCCINT
VCCINT	VCCINT	K6	VCCINT
VCCINT	VCCINT	K8	VCCINT
VCCINT	VCCINT	L7	VCCINT
VCCINT	VCCINT	L9	VCCINT

FT256 Footprint (XC3S50A)

		(Differential Outputs)					Bank 0				(Differential Outputs)						
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
(High Output Drive)	A	GND	PROG_B	I/O L19P_0	I/O L18P_0	I/O L17P_0	I/O L15P_0	N.C.	I/O L12P_0 GCLK10	I/O L10N_0 GCLK7	I/O L08N_0	I/O L07N_0	N.C.	I/O L04N_0	I/O L04P_0	TCK	GND
	B	TDI	TMS	I/O L19N_0	I/O L18N_0	VCCO_0	I/O L15N_0	GND	I/O L12N_0 GCLK11	VCCO_0	I/O L08P_0	GND	INPUT	VCCO_0	I/O L02N_0	I/O L02P_0 VREF_0	TDO
	C	I/O L01N_3	I/O L01P_3	GND	I/O L20P_0 VREF_0	I/O L17N_0	I/O L16N_0	N.C.	I/O L11P_0 GCLK8	I/O L10P_0 GCLK6	I/O L09P_0 GCLK4	I/O L07P_0	I/O L03P_0	I/O L01N_0	GND	I/O L24N_1	I/O L24P_1
	D	I/O L03P_3	VCCO_3	I/O L02N_3	I/O L02P_3	I/O L20N_0 PUDC_B	INPUT	I/O L16P_0	I/O L11N_0 GCLK9	I/O L09N_0 GCLK5	N.C.	I/O L03N_0	INPUT	I/O L01P_0	I/O L23N_1	I/O L22N_1	I/O L22P_1
	E	I/O L03N_3	N.C.	N.C.	INPUT L04P_3	GND	INPUT	N.C.	VCCO_0	INPUT VREF_0	N.C.	VCCAUX	GND	I/O L23P_1	I/O L20P_1	VCCO_1	N.C.
	F	I/O L08P_3	GND	N.C.	INPUT L04N_3 VREF_3	VCCAUX	GND	INPUT	N.C.	INPUT	INPUT	INPUT L25N_1	INPUT L25P_1 VREF_1	I/O L20N_1	N.C.	N.C.	N.C.
	G	I/O L08N_3 VREF_3	I/O L11P_3 LHCLK0	N.C.	N.C.	N.C.	N.C.	VCCINT	GND	VCCINT	GND	INPUT L21N_1	INPUT L21P_1 VREF_1	N.C.	N.C.	GND	N.C.
	H	I/O L11N_3 LHCLK1	VCCO_3	I/O L12P_3 LHCLK2	N.C.	N.C.	N.C.	INPUT L13P_3	VCCINT	GND	INPUT L13P_1	INPUT L13N_1	VCCO_1	N.C.	I/O L14N_1 RHCLK5	I/O L15P_1 IRDY1 RHCLK6	I/O L15N_1 RHCLK7
	J	I/O L14N_3 LHCLK5	I/O L14P_3 LHCLK4	I/O L12N_3 IRDY2 LHCLK3	N.C.	VCCO_3	N.C.	INPUT L13N_3	GND	VCCINT	N.C.	N.C.	I/O L10P_1	I/O L10N_1	I/O L14P_1 RHCLK4	VCCO_1	I/O L12N_1 TRDY1 RHCLK3
	K	I/O L15N_3 LHCLK7	GND	I/O L15P_3 TRDY2 LHCLK6	N.C.	INPUT L21P_3	INPUT L21N_3	GND	VCCINT	GND	VCCINT	INPUT L04P_1	INPUT L04N_1 VREF_1	N.C.	I/O L11N_1 RHCLK1	I/O L11P_1 RHCLK0	I/O L12P_1 RHCLK2
	L	N.C.	N.C.	N.C.	N.C.	INPUT L25P_3	INPUT L25N_3 VREF_3	INPUT	INPUT	INPUT VREF_2	INPUT VREF_2	GND	VCCAUX	N.C.	N.C.	GND	N.C.
	M	I/O L20P_3	VCCO_3	N.C.	I/O L24N_3	GND	VCCAUX	INPUT VREF_2	INPUT VREF_2	VCCO_2	N.C.	INPUT VREF_2	GND	N.C.	N.C.	N.C.	N.C.
	N	I/O L20N_3	I/O L22P_3	I/O L24P_3	I/O L01P_2 M1	INPUT VREF_2	I/O L03N_2 VS1	N.C.	I/O L08N_2 D4	I/O L11P_2 GCLK0	N.C.	I/O L16N_2	N.C.	I/O L01P_1 HDC	I/O L01N_1 LDC2	VCCO_1	I/O L03N_1
	P	I/O L22N_3	I/O L23N_3	GND	I/O L01N_2 M0	I/O L04N_2 VS0	N.C.	I/O L08P_2 D5	I/O L10P_2 GCLK14	I/O L11N_2 GCLK1	I/O L14P_2 MOSI CSI_B	I/O L16P_2	I/O L17N_2 D3	N.C.	GND	I/O L02N_1 LDC0	I/O L03P_1
	R	I/O L23P_3	I/O L02P_2 M2	I/O L03P_2 RDWR_B	VCCO_2	I/O L06P_2	GND	N.C.	VCCO_2	I/O L12P_2 GCLK2	GND	I/O L15N_2 DOUT	VCCO_2	I/O L20P_2 D1	I/O L20N_2 CCLK	I/O L02P_1 LDC1	SUSPEND
	T	GND	I/O L02N_2 CSO_B	I/O L04P_2 VS2	I/O L05P_2	I/O L05N_2 D7	I/O L06N_2 D6	N.C.	I/O L10N_2 GCLK15	I/O L12N_2 GCLK3	I/O L14N_2	I/O L15P_2 AWAKE	I/O L17P_2 INIT_B	I/O L18P_2 D2	I/O L18N_2 D0 DIN/MISO	DONE	GND
		(Differential Outputs)					Bank 2				(Differential Outputs)						

Figure 20: XC3S50A FT256 Package Footprint (Top View)

53	I/O: Unrestricted, general-purpose user I/O	25	DUAL: Configuration pins, then possible user I/O	15	VREF: User I/O or input voltage reference for bank	2	SUSPEND: Dedicated SUSPEND and dual-purpose AWAKE Power Management pins
20	INPUT: Unrestricted, general-purpose input pin	30	CLK: User I/O, input, or global buffer input	16	VCCO: Output voltage supply for bank		
2	CONFIG: Dedicated configuration pins	4	JTAG: Dedicated JTAG port pins	6	VCCINT: Internal core supply voltage (+1.2V)		
51	N.C.: Not connected (XC3S50A only)	28	GND: Ground	4	VCCAUX: Auxiliary supply voltage		

FT256 Footprint (XC3S700A, XC3S1400A)

Bank 0																
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	GND	PROG_B	I/O L19P_0	I/O L18P_0	I/O L17P_0	I/O L15P_0	I/O L13P_0	I/O L12P_0 GCLK10	I/O L10N_0 GCLK7	I/O L08N_0	I/O L07N_0	I/O L05N_0	I/O L04N_0	I/O L04P_0	TCK	GND
B	TDI	TMS	I/O L19N_0	I/O L18N_0	VCCO_0	I/O L15N_0	GND	I/O L12N_0 GCLK11	VCCO_0	I/O L08P_0	GND	I/O L05P_0	VCCO_0	I/O L02N_0	I/O L02P_0 VREF_0	TDO
C	I/O L01N_3	I/O L01P_3	GND	I/O L20P_0 VREF_0	I/O L17N_0	I/O L16N_0	I/O L13N_0	I/O L11P_0 GCLK8	I/O L10P_0 GCLK6	I/O L09P_0 GCLK4	I/O L07P_0	I/O L03P_0	I/O L01N_0	GND	I/O L24N_1 A25	I/O L24P_1 A24
D	I/O L03P_3	VCCO_3	I/O L02N_3	I/O L02P_3	I/O L20N_0 PUDC_B	VCCAUX	I/O L16P_0	I/O L11N_0 GCLK9	I/O L09N_0 GCLK5	I/O L06N_0 VREF_0	I/O L06P_0	I/O L03N_0	I/O L01P_0	I/O L23N_1 A23	I/O L22N_1 A21	I/O L22P_1 A20
E	I/O L03N_3	I/O L05N_3	I/O L05P_3	I/O L04P_3	GND	INPUT	I/O L14N_0 VREF_0	VCCO_0	I/O L14P_0	GND	VCCAUX	GND	I/O L23P_1 A22	I/O L20P_1 A18	VCCO_1	I/O L18P_1 A14
F	I/O L08P_3	GND	I/O L07P_3	I/O L04N_3	VCCAUX	GND	GND	GND	GND	VCCINT	GND	VCCAUX	I/O L20N_1 A19	I/O L19N_1 A17	I/O L18N_1 A15	I/O L16N_1 A11
G	I/O L08N_3 VREF_3	I/O L11P_3 LHCLK0	I/O L07N_3	INPUT VREF_3	GND	GND	VCCINT	GND	VCCINT	GND	VCCINT	GND	I/O L19P_1 A16	I/O L17N_1 A13	GND	I/O L16P_1 A10
H	I/O L11N_3 LHCLK1	VCCO_3	I/O L12P_3 LHCLK2	VCCAUX	GND	VCCINT	GND	VCCINT	GND	VCCINT	GND	INPUT VREF_1	I/O L17P_1 A12	VCCAUX	I/O L15P_1 IRDY1 RHCLK6	I/O L15N_1 RHCLK7
J	I/O L14N_3 LHCLK5	I/O L14P_3 LHCLK4	I/O L12N_3 IRDY2 LHCLK3	INPUT	INPUT VREF_3	GND	VCCINT	GND	VCCINT	GND	VCCINT	I/O L10P_1 A8	I/O L10N_1 A9	INPUT VREF_1	VCCO_1	I/O L12N_1 TRDY1 RHCLK3
K	I/O L15N_3 LHCLK7	GND	I/O L15P_3 TRDY2 LHCLK6	I/O L18P_3	GND	VCCINT	GND	VCCINT	GND	VCCINT	GND	GND	I/O L06N_1 A3	I/O L11N_1 RHCLK1	I/O L11P_1 RHCLK0	I/O L12P_1 RHCLK2
L	I/O L16P_3 VREF_3	I/O L16N_3	I/O L18N_3	I/O L19N_3	VCCAUX	GND	VCCINT	GND	VCCINT	GND	GND	VCCAUX	I/O L06P_1 A2	I/O L08P_1 A6	GND	I/O L08N_1 A7
M	I/O L20P_3	VCCO_3	I/O L19P_3	I/O L24N_3	GND	VCCAUX	INPUT VREF_2	GND	INPUT VREF_2	VCCAUX	INPUT VREF_2	GND	INPUT VREF_1	INPUT VREF_1	I/O L07P_1 A4	I/O L07N_1 A5
N	I/O L20N_3	I/O L22P_3 VREF_3	I/O L24P_3	I/O L01P_2 M1	INPUT VREF_2	I/O L04P_2 VS1	GND	I/O L08N_2 D4	I/O L11P_2 GCLK0	GND	I/O L16N_2	I/O L19P_2	I/O L01P_1 HDC	I/O L01N_1 LDC2	VCCO_1	I/O L03N_1 A1
P	I/O L22N_3	I/O L23N_3	GND	I/O L01N_2 M0	I/O L04N_2 VS0	INPUT VREF_2	I/O L08P_2 D5	I/O L10P_2 GCLK14	I/O L11N_2 GCLK1	I/O L14N_2 MOSI CSI_B	I/O L16P_2	I/O L17N_2 D3	I/O L19N_2	GND	I/O L02N_1 LDC0	I/O L03P_1 A0
R	I/O L23P_3	I/O L02P_2 M2	I/O L03P_2 RDWR_B	VCCO_2	I/O L05N_2	GND	I/O L09P_2 GCLK12	VCCO_2	I/O L12P_2 GCLK2	GND	I/O L15N_2 DOUT	VCCO_2	I/O L18N_2 D1	I/O L20N_2 CCLK	I/O L02P_1 LDC1	SUSPEND
T	GND	I/O L02N_2 CSO_B	I/O L03N_2 VS2	I/O L05P_2	I/O L06P_2 D7	I/O L06N_2 D6	I/O L09N_2 GCLK13	I/O L10N_2 GCLK15	I/O L12N_2 GCLK3	I/O L14P_2	I/O L15P_2 AWAKE	I/O L17P_2 INIT_B	I/O L18P_2 D2	I/O L20P_2 DO/DIN MISO	DONE	GND
Bank 2																

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Figure 22: XC3S700A and XC3S1400A FT256 Package Footprint (Top View)

59	I/O: Unrestricted, general-purpose user I/O	51	DUAL: Configuration, then possible user I/O	18	VREF: User I/O or input voltage reference for bank	2	SUSPEND: Dedicated SUSPEND and dual-purpose AWAKE Power Management pins
2	INPUT: Unrestricted, general-purpose input pin	30	CLK: User I/O, input, or global buffer input	13	VCCO: Output voltage supply for bank		
2	CONFIG: Dedicated configuration pins	4	JTAG: Dedicated JTAG port pins	15	VCCINT: Internal core supply voltage (+1.2V)		
0	N.C.: Not connected	50	GND: Ground	10	VCCAUX: Auxiliary supply voltage		

Table 77: Spartan-3A FG320 Pinout(Continued)

Bank	Pin Name	FG320 Ball	Type
GND	GND	R15	GND
GND	GND	T9	GND
GND	GND	V1	GND
GND	GND	V7	GND
GND	GND	V12	GND
GND	GND	V18	GND
VCCAUX	SUSPEND	T16	PWR MGMT
VCCAUX	DONE	V17	CONFIG
VCCAUX	PROG_B	C4	CONFIG
VCCAUX	TCK	A17	JTAG
VCCAUX	TDI	E4	JTAG
VCCAUX	TDO	E14	JTAG
VCCAUX	TMS	C3	JTAG
VCCAUX	VCCAUX	A9	VCCAUX
VCCAUX	VCCAUX	G10	VCCAUX
VCCAUX	VCCAUX	J12	VCCAUX
VCCAUX	VCCAUX	J18	VCCAUX
VCCAUX	VCCAUX	K1	VCCAUX
VCCAUX	VCCAUX	K7	VCCAUX
VCCAUX	VCCAUX	M10	VCCAUX
VCCAUX	VCCAUX	V10	VCCAUX
VCCINT	VCCINT	H9	VCCINT
VCCINT	VCCINT	H11	VCCINT
VCCINT	VCCINT	J8	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	L8	VCCINT
VCCINT	VCCINT	L10	VCCINT

Table 81: Spartan-3A FG400 Pinout(Continued)

Bank	Pin Name	FG400 Ball	Type
1	IP_1/VREF_1	N14	VREF
1	IP_L04N_1/VREF_1	P15	VREF
1	IP_L04P_1	P14	INPUT
1	IP_L11N_1/VREF_1	M15	VREF
1	IP_L11P_1	M16	INPUT
1	IP_L15N_1	M13	INPUT
1	IP_L15P_1/VREF_1	M14	VREF
1	IP_L19N_1	L13	INPUT
1	IP_L19P_1	L14	INPUT
1	IP_L23N_1	K14	INPUT
1	IP_L23P_1/VREF_1	K15	VREF
1	IP_L27N_1	J15	INPUT
1	IP_L27P_1	J16	INPUT
1	IP_L31N_1	J13	INPUT
1	IP_L31P_1/VREF_1	J14	VREF
1	IP_L35N_1	H14	INPUT
1	IP_L35P_1	H15	INPUT
1	IP_L39N_1	G14	INPUT
1	IP_L39P_1/VREF_1	G15	VREF
1	VCCO_1	D19	VCCO
1	VCCO_1	H16	VCCO
1	VCCO_1	K19	VCCO
1	VCCO_1	N16	VCCO
1	VCCO_1	T19	VCCO
2	IO_L01N_2/M0	V4	DUAL
2	IO_L01P_2/M1	U4	DUAL
2	IO_L02N_2/CSO_B	Y2	DUAL
2	IO_L02P_2/M2	W3	DUAL
2	IO_L03N_2	W4	I/O
2	IO_L03P_2	Y3	I/O
2	IO_L04N_2	R7	I/O
2	IO_L04P_2	T6	I/O
2	IO_L05N_2	U5	I/O
2	IO_L05P_2	V5	I/O
2	IO_L06N_2	U6	I/O
2	IO_L06P_2	T7	I/O
2	IO_L07N_2/VS2	U7	DUAL
2	IO_L07P_2/RDWR_B	T8	DUAL
2	IO_L08N_2	Y5	I/O
2	IO_L08P_2	Y4	I/O

Table 81: Spartan-3A FG400 Pinout(Continued)

Bank	Pin Name	FG400 Ball	Type
2	IO_L09N_2/VS0	W6	DUAL
2	IO_L09P_2/VS1	V6	DUAL
2	IO_L10N_2	Y7	I/O
2	IO_L10P_2	Y6	I/O
2	IO_L11N_2	U9	I/O
2	IO_L11P_2	T9	I/O
2	IO_L12N_2/D6	W8	DUAL
2	IO_L12P_2/D7	V7	DUAL
2	IO_L13N_2	V9	I/O
2	IO_L13P_2	V8	I/O
2	IO_L14N_2/D4	T10	DUAL
2	IO_L14P_2/D5	U10	DUAL
2	IO_L15N_2/GCLK13	Y9	GCLK
2	IO_L15P_2/GCLK12	W9	GCLK
2	IO_L16N_2/GCLK15	W10	GCLK
2	IO_L16P_2/GCLK14	V10	GCLK
2	IO_L17N_2/GCLK1	V11	GCLK
2	IO_L17P_2/GCLK0	Y11	GCLK
2	IO_L18N_2/GCLK3	V12	GCLK
2	IO_L18P_2/GCLK2	U11	GCLK
2	IO_L19N_2	R12	I/O
2	IO_L19P_2	T12	I/O
2	IO_L20N_2/MOSI/CSI_B	W12	DUAL
2	IO_L20P_2	Y12	I/O
2	IO_L21N_2	W13	I/O
2	IO_L21P_2	Y13	I/O
2	IO_L22N_2/DOUT	V13	DUAL
2	IO_L22P_2/AWAKE	U13	PWR MGMT
2	IO_L23N_2	R13	I/O
2	IO_L23P_2	T13	I/O
2	IO_L24N_2/D3	W14	DUAL
2	IO_L24P_2/INIT_B	Y14	DUAL
2	IO_L25N_2	T14	I/O
2	IO_L25P_2	V14	I/O
2	IO_L26N_2/D1	V15	DUAL
2	IO_L26P_2/D2	Y15	DUAL
2	IO_L27N_2	T15	I/O
2	IO_L27P_2	U15	I/O
2	IO_L28N_2	W16	I/O

Table 87: Spartan-3A FG676 Pinout(Continued)

Bank	Pin Name	FG676 Ball	Type
2	IO_L16N_2	W12	I/O
2	IO_L16P_2	V12	I/O
2	IO_L17N_2/VS2	AA12	DUAL
2	IO_L17P_2/RDWR_B	Y12	DUAL
2	IO_L18N_2	AF8	I/O
2	IO_L18P_2	AE8	I/O
2	IO_L19N_2/VS0	AF9	DUAL
2	IO_L19P_2/VS1	AE9	DUAL
2	IO_L20N_2	W13	I/O
2	IO_L20P_2	V13	I/O
2	IO_L21N_2	AC12	I/O
2	IO_L21P_2	AB12	I/O
2	IO_L22N_2/D6	AF10	DUAL
2	IO_L22P_2/D7	AE10	DUAL
2	IO_L23N_2	AC11	I/O
2	IO_L23P_2	AD11	I/O
2	IO_L24N_2/D4	AE12	DUAL
2	IO_L24P_2/D5	AF12	DUAL
2	IO_L25N_2/GCLK13	Y13	GCLK
2	IO_L25P_2/GCLK12	AA13	GCLK
2	IO_L26N_2/GCLK15	AE13	GCLK
2	IO_L26P_2/GCLK14	AF13	GCLK
2	IO_L27N_2/GCLK1	AA14	GCLK
2	IO_L27P_2/GCLK0	Y14	GCLK
2	IO_L28N_2/GCLK3	AE14	GCLK
2	IO_L28P_2/GCLK2	AF14	GCLK
2	IO_L29N_2	AC14	I/O
2	IO_L29P_2	AD14	I/O
2	IO_L30N_2/MOSI/CSI_B	AB15	DUAL
2	IO_L30P_2	AC15	I/O
2	IO_L31N_2	W15	I/O
2	IO_L31P_2	V14	I/O
2	IO_L32N_2/DOUT	AE15	DUAL
2	IO_L32P_2/AWAKE	AD15	PWR MGMT
2	IO_L33N_2	AD17	I/O
2	IO_L33P_2	AE17	I/O
2	IO_L34N_2/D3	Y15	DUAL
2	IO_L34P_2/INIT_B	AA15	DUAL
2	IO_L35N_2	U15	I/O

Table 87: Spartan-3A FG676 Pinout(Continued)

Bank	Pin Name	FG676 Ball	Type
2	IO_L35P_2	V15	I/O
2	IO_L36N_2/D1	AE18	DUAL
2	IO_L36P_2/D2	AF18	DUAL
2	IO_L37N_2	AE19	I/O
2	IO_L37P_2	AF19	I/O
2	IO_L38N_2	AB16	I/O
2	IO_L38P_2	AC16	I/O
2	IO_L39N_2	AE20	I/O
2	IO_L39P_2	AF20	I/O
2	IO_L40N_2	AC19	I/O
2	IO_L40P_2	AD19	I/O
2	IO_L41N_2	AC20	I/O
2	IO_L41P_2	AD20	I/O
2	IO_L42N_2	U16	I/O
2	IO_L42P_2	V16	I/O
2	IO_L43N_2	Y17	I/O
2	IO_L43P_2	AA17	I/O
2	IO_L44N_2	AD21	I/O
2	IO_L44P_2	AE21	I/O
2	IO_L45N_2	AC21	I/O
2	IO_L45P_2	AD22	I/O
2	IO_L46N_2	V17	I/O
2	IO_L46P_2	W17	I/O
2	IO_L47N_2	AA18	I/O
2	IO_L47P_2	AB18	I/O
2	IO_L48N_2	AE23	I/O
2	IO_L48P_2	AF23	I/O
2	IO_L51N_2	AE25	I/O
2	IO_L51P_2	AF25	I/O
2	IO_L52N_2/CCLK	AE24	DUAL
2	IO_L52P_2/D0/DIN/MISO	AF24	DUAL
2	IP_2	AA19	INPUT
2	IP_2	AB13	INPUT
2	IP_2	AB17	INPUT
2	IP_2	AB20	INPUT
2	IP_2	AC7	INPUT
2	IP_2	AC13	INPUT
2	IP_2	AC17	INPUT
2	IP_2	AC18	INPUT
2	IP_2	AD9	INPUT

Bank 0																									
14	15	16	17	18	19	20	21	22	23	24	25	26													
I/O L26N_0 GCLK7	I/O L23N_0	GND	INPUT	I/O L18N_0	I/O L15N_0	I/O L14N_0	GND	I/O L07N_0	INPUT	N.C. ◆	TCK	GND	A												
I/O L26P_0 GCLK6	I/O L23P_0	VCCO_0	I/O L19N_0	I/O L18P_0	I/O L15P_0	I/O L14P_0 VREF_0	I/O L09N_0	VCCO_0	I/O L07P_0	N.C. ◆	INPUT L65N_1	INPUT L65P_1 VREF_1	B												
GND	I/O L22N_0	I/O L21N_0	I/O L19P_0	I/O L17N_0	GND	I/O L11N_0	I/O L09P_0	I/O L05N_0	I/O L06N_0	GND	I/O L63N_1 A23	I/O L63P_1 A22	C												
INPUT VREF_0	INPUT	I/O L22P_0	I/O L21P_0	I/O L17P_0	INPUT	I/O L11P_0	I/O L10N_0	I/O L05P_0	I/O L06P_0	I/O L61N_1	I/O L61P_1	I/O L60N_1	D												
I/O L24P_0	I/O L20N_0 VREF_0	VCCAUX	I/O L13N_0	INPUT	VCCO_0	INPUT	I/O L10P_0	VCCAUX	TDO	I/O L56P_1	VCCO_1	I/O L60P_1	E												
I/O L24N_0	I/O L20P_0	GND	I/O L13P_0	N.C. ◆	I/O L02N_0	I/O L01N_0	GND	I/O L58P_1 VREF_1	I/O L56N_1	I/O L54N_1	I/O L54P_1	GND	F												
INPUT	I/O L16P_0	INPUT	I/O L08N_0	N.C. ◆	I/O L02P_0 VREF_0	I/O L01P_0	I/O L64N_1 A25	I/O L58N_1	I/O L51P_1	I/O L51N_1	INPUT L52N_1 VREF_1	INPUT L52P_1	G												
GND	I/O L16N_0	VCCO_0	I/O L08P_0	INPUT	GND	I/O L64P_1 A24	I/O L62N_1 A21	VCCO_1	INPUT L48P_1	INPUT L48N_1	INPUT L44N_1	INPUT L44P_1 VREF_1	H												
I/O L25N_0 GCLK5	INPUT	I/O L12P_0	INPUT VREF_0	VCCAUX	I/O L59P_1	I/O L59N_1	I/O L62P_1 A20	I/O L49N_1	I/O L49P_1	GND	I/O L43N_1 A19	I/O L43P_1 A18	J												
I/O L25P_0 GCLK4	VCCINT	I/O L12N_0	GND	I/O L57N_1	I/O L57P_1	I/O L53N_1	I/O L50N_1	I/O L46N_1	I/O L46P_1	INPUT L40P_1	I/O L41P_1	I/O L41N_1	K												
VCCINT	GND	VCCINT	I/O L55N_1	I/O L55P_1	VCCO_1	I/O L53P_1	GND	I/O L50P_1	INPUT L40N_1	I/O L38P_1 A12	VCCO_1	GND	L												
GND	VCCINT	GND	VCCINT	I/O L47N_1	I/O L47P_1	I/O L42N_1 A17	I/O L45P_1	I/O L45N_1	I/O L38N_1 A13	INPUT L36P_1 VREF_1	I/O L35N_1 A11	I/O L35P_1 A10	M												
VCCINT	GND	VCCINT	I/O L39N_1 A15	I/O L39P_1 A14	I/O L34N_1 RHCLK7	I/O L42P_1 A16	I/O L37N_1	VCCO_1	INPUT L36N_1	I/O L33N_1 RHCLK5	INPUT L32N_1	INPUT L32P_1	N												
VCCINT	VCCINT	GND	VCCAUX	I/O L34P_1 TRDY1 RHCLK6	GND	I/O L30N_1 RHCLK1	I/O L30P_1 RHCLK0	I/O L37P_1	I/O L33P_1 RHCLK4	GND	I/O L31N_1 TRDY1 RHCLK3	I/O L31P_1 RHCLK2	P											Bank 1	
VCCINT	GND	VCCINT	I/O L27N_1 A7	I/O L27P_1 A6	I/O L22P_1	I/O L22N_1	I/O L25P_1 A2	I/O L25N_1 A3	INPUT L28P_1 VREF_1	INPUT L28N_1	I/O L29P_1 A8	I/O L29N_1 A9	R												
GND	VCCINT	GND	I/O L17N_1	I/O L17P_1	VCCO_1	I/O L14N_1	GND	VCCAUX	I/O L26P_1 A4	I/O L26N_1 A5	VCCO_1	GND	T												
VCCAUX	I/O L35N_2	I/O L42N_2	GND	I/O L12N_1	I/O L12P_1	I/O L10N_1	I/O L14P_1	I/O L21N_1	I/O L23P_1	I/O L23N_1 VREF_1	INPUT L24P_1	INPUT L24N_1 VREF_1	U												
I/O L31P_2	I/O L35P_2	I/O L42P_2	I/O L46N_2	I/O L08P_1	I/O L08N_1	SUSPEND	I/O L10P_1	I/O L18N_1	I/O L21P_1	I/O L19P_1	I/O L19N_1	INPUT L20N_1 VREF_1	V												
GND	I/O L31N_2	VCCO_2	I/O L46P_2	N.C. ◆	GND	I/O L04P_1	I/O L04N_1	VCCO_1	I/O L18P_1	GND	INPUT L16P_1	INPUT L20P_1	W												
I/O L27P_2 GCLK0	I/O L34N_2 D3	INPUT 2 VREF_2	I/O L43N_2	N.C. ◆	N.C. ◆	I/O L01P_1 HDC	I/O L01N_1 LDC2	I/O L13P_1	I/O L13N_1	I/O L15P_1	I/O L15N_1	INPUT L16N_1	Y												
I/O L27N_2 GCLK1	I/O L34P_2 INIT_B	GND	I/O L43P_2	I/O L47N_2	INPUT	INPUT VREF_2	GND	I/O L09P_1	I/O L09N_1	I/O L11P_1	I/O L11N_1	GND	A											A A	
VCCO_2	I/O L30N_2 MOSI CSI_B	I/O L38N_2	INPUT	I/O L47P_2	VCCO_2	INPUT	DONE	VCCAUX	I/O L07P_1	I/O L07N_1 VREF_1	VCCO_1	I/O L06N_1	A											A B	
I/O L29N_2	I/O L30P_2	I/O L38P_2	INPUT	INPUT	I/O L40N_2	I/O L41N_2	I/O L45N_2	N.C. ◆	I/O L03P_1 A0	I/O L03N_1 A1	I/O L05N_1	I/O L06P_1	A											A C	
I/O L29P_2	I/O L32P_2 AWAKE	INPUT	I/O L33N_2	GND	I/O L40P_2	I/O L41P_2	I/O L44N_2	I/O L45P_2	N.C. ◆	GND	I/O L02N_1 LDC0	I/O L05P_1	A											A D	
I/O L28N_2 GCLK3	I/O L32N_2 DDOUT	VCCO_2	I/O L33P_2	I/O L36N_2 D1	I/O L37N_2	I/O L39N_2	I/O L44P_2	VCCO_2	I/O L48N_2	I/O L52N_2 CCLK	I/O L51N_2	I/O L02P_1 LDC1	A											A E	
I/O L28P_2 GCLK2	INPUT VREF_2	GND	INPUT VREF_2	I/O L36P_2 D2	I/O L37P_2	I/O L39P_2	GND	INPUT VREF_2	I/O L48P_2	I/O L52P_2 D0 DIN/MISO	I/O L51P_2	GND	A											A F	
Bank 2																									

Right Half of FG676
Package (Top View)

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