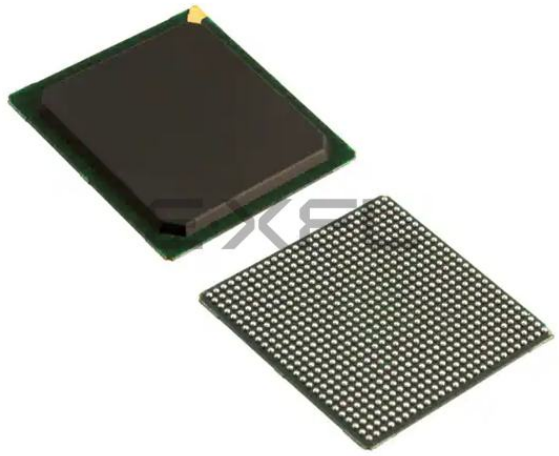

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	2816
Number of Logic Elements/Cells	25344
Total RAM Bits	589824
Number of I/O	502
Number of Gates	1400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1400a-4fgg676c

Spartan-3A FPGA Family: Introduction and Ordering Information

DS529-1 (v2.0) August 19, 2010 **Product Specification**

Introduction

The Spartan®-3A family of Field-Programmable Gate Arrays (FPGAs) solves the design challenges in most high-volume, cost-sensitive, I/O-intensive electronic applications. The five-member family offers densities ranging from 50,000 to 1.4 million system gates, as shown in Table 1.

The Spartan-3A FPGAs are part of the Extended Spartan-3A family, which also include the non-volatile Spartan-3AN and the higher density Spartan-3A DSP FPGAs. The Spartan-3A family builds on the success of the earlier Spartan-3E and Spartan-3 FPGA families. New features improve system performance and reduce the cost of configuration. These Spartan-3A family enhancements, combined with proven 90 nm process technology, deliver more functionality and bandwidth per dollar than ever before, setting the new standard in the programmable logic industry.

Because of their exceptionally low cost, Spartan-3A FPGAs are ideally suited to a wide range of consumer electronics applications, including broadband access, home networking, display/projection, and digital television equipment.

The Spartan-3A family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, lengthy development cycles, and the inherent inflexibility of conventional ASICs, and permit field design upgrades.

Features

- Very low cost, high-performance logic solution for high-volume, cost-conscious applications
- Dual-range V_{CCAUX} supply simplifies 3.3V-only design
- Suspend, Hibernate modes reduce system power
- Multi-voltage, multi-standard SelectIO™ interface pins
  - Up to 502 I/O pins or 227 differential signal pairs
  - LVCMOS, LVTTL, HSTL, and SSTL single-ended I/O
  - 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V signaling
  - Selectable output drive, up to 24 mA per pin
  - QUIETIO standard reduces I/O switching noise
  - Full 3.3V ± 10% compatibility and hot swap compliance
  - 640+ Mb/s data transfer rate per differential I/O
  - LVDS, RSDS, mini-LVDS, HSTL/SSTL differential I/O with integrated differential termination resistors
  - Enhanced Double Data Rate (DDR) support
  - DDR/DDR2 SDRAM support up to 400 Mb/s
  - Fully compliant 32-/64-bit, 33/66 MHz PCI® technology support
- Abundant, flexible logic resources
  - Densities up to 25,344 logic cells, including optional shift register or distributed RAM support
  - Efficient wide multiplexers, wide logic
  - Fast look-ahead carry logic
  - Enhanced 18 x 18 multipliers with optional pipeline
  - IEEE 1149.1/1532 JTAG programming/debug port
- Hierarchical SelectRAM™ memory architecture
  - Up to 576 Kbits of fast block RAM with byte write enables for processor applications
  - Up to 176 Kbits of efficient distributed RAM
- Up to eight Digital Clock Managers (DCMs)
  - Clock skew elimination (delay locked loop)
  - Frequency synthesis, multiplication, division
  - High-resolution phase shifting
  - Wide frequency range (5 MHz to over 320 MHz)
- Eight low-skew global clock networks, eight additional clocks per half device, plus abundant low-skew routing
- Configuration interface to industry-standard PROMs
  - Low-cost, space-saving SPI serial Flash PROM
  - x8 or x8/x16 BPI parallel NOR Flash PROM
  - Low-cost Xilinx® Platform Flash with JTAG
  - Unique Device DNA identifier for design authentication
  - Load multiple bitstreams under FPGA control
  - Post-configuration CRC checking
- Complete Xilinx ISE® and WebPACK™ development system software support plus Spartan-3A Starter Kit
- MicroBlaze™ and PicoBlaze™ embedded processors
- Low-cost QFP and BGA packaging, Pb-free options
  - Common footprints support easy density migration
  - Compatible with select Spartan-3AN nonvolatile FPGAs
  - Compatible with higher density Spartan-3A DSP FPGAs
- XA Automotive version available

Table 1: **Summary of Spartan-3A FPGA Attributes**

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM bits(1)	Block RAM bits(1)	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	CLBs	Slices						
XC3S50A	50K	1,584	16	12	176	704	11K	54K	3	2	144	64
XC3S200A	200K	4,032	32	16	448	1,792	28K	288K	16	4	248	112
XC3S400A	400K	8,064	40	24	896	3,584	56K	360K	20	4	311	142
XC3S700A	700K	13,248	48	32	1,472	5,888	92K	360K	20	8	372	165
XC3S1400A	1400K	25,344	72	40	2,816	11,264	176K	576K	32	8	502	227

Notes:
1. By convention, one Kb is equivalent to 1,024 bits.

Configuration

Spartan-3A FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored externally in a PROM or some other non-volatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of seven different modes:

- Master Serial from a Xilinx Platform Flash PROM
- Serial Peripheral Interface (SPI) from an industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary Scan (JTAG), typically downloaded from a processor or system tester

Furthermore, Spartan-3A FPGAs support MultiBoot configuration, allowing two or more FPGA configuration bitstreams to be stored in a single SPI serial Flash or a BPI parallel NOR Flash. The FPGA application controls which configuration to load next and when to load it.

Additionally, each Spartan-3A FPGA contains a unique, factory-programmed Device DNA identifier useful for tracking purposes, anti-cloning designs, or IP protection.

I/O Capabilities

The Spartan-3A FPGA SelectIO interface supports many popular single-ended and differential standards. Table 2 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination. Some of the user I/Os are unidirectional input-only pins as indicated in Table 2.

Spartan-3A FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3.3V PCI at 33 MHz or 66 MHz
- HSTL I, II, and III at 1.5V and 1.8V, commonly used in memory applications
- SSTL I and II at 1.8V, 2.5V, and 3.3V, commonly used for memory applications

Spartan-3A FPGAs support the following differential standards:

- LVDS, mini-LVDS, RSDS, and PPDS I/O at 2.5V or 3.3V
- Bus LVDS I/O at 2.5V
- TMDS I/O at 3.3V
- Differential HSTL and SSTL I/O
- LVPECL inputs at 2.5V or 3.3V

Table 2: **Available User I/Os and Differential (Diff) I/O Pairs**

Package	VQ100 VQG100		TQ144 TQG144		FT256 FTG256		FG320 FGG320		FG400 FGG400		FG484 FGG484		FG676 FGG676	
Body Size (mm)	14 x 14(2)		20 x 20(2)		17 x 17		19 x 19		21 x 21		23 x 23		27 x 27	
Device	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff
XC3S50A	**68** *(13)*	**60** *(24)*	**108** *(7)*	**50** *(24)*	**144** *(32)*	**64** *(32)*	-	-	-	-	-	-	-	-
XC3S200A	**68** *(13)*	**60** *(24)*	-	-	**195** *(35)*	**90** *(50)*	**248** *(56)*	**112** *(64)*	-	-	-	-	-	-
XC3S400A	-	-	-	-	**195** *(35)*	**90** *(50)*	**251** *(59)*	**112** *(64)*	**311** *(63)*	**142** *(78)*	-	-	-	-
XC3S700A	-	-	-	-	**161** *(13)*	**74** *(36)*	-	-	**311** *(63)*	**142** *(78)*	**372** *(84)*	**165** *(93)*	-	-
XC3S1400A	-	-	-	-	**161** *(13)*	**74** *(36)*	-	-	-	-	**375** *(87)*	**165** *(93)*	**502** *(94)*	**227** *(131)*

Notes:

1. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in (*italics*) indicates the number of input-only pins. The differential (Diff) input-only pin count includes both differential pairs on input-only pins and differential pairs on I/O pins within I/O banks that are restricted to differential inputs.
2. The footprints for the VQ/TQ packages are larger than the package body. See the Package Drawings for details.

DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

Advance: Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

Production: These specifications are approved once the silicon has been characterized over numerous production lots. Parameter values are considered stable with no future changes expected.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan®-3A devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Absolute Maximum Ratings

Stresses beyond those listed under Table 4: Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 4: **Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Max	Units
V_{CCINT}	Internal supply voltage		–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage		–0.5	3.75	V
V_{CCO}	Output driver supply voltage		–0.5	3.75	V
V_{REF}	Input reference voltage		–0.5	V_{CCO} + 0.5	V
V_{IN}	Voltage applied to all User I/O pins and dual-purpose pins	Driver in a high-impedance state	–0.95	4.6	V
	Voltage applied to all Dedicated pins		–0.5	4.6	V
I_{IK}	Input clamp current per I/O pin	$-0.5V < V_{IN} < (V_{CCO} + 0.5V)$ (1)	–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model	–	±2000	V
		Charged device model	–	±500	V
		Machine model	–	±200	V
T_J	Junction temperature		–	125	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Upper clamp applies only when using PCI IOSTANDARDs.
2. For soldering guidelines, see UG112: *Device Packaging and Thermal Characteristics* and XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

Table 12: **DC Characteristics of User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
LVTTL(3)	2	2	–2	0.4	2.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
LVCMOS33(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24(4)	24	–24		
LVCMOS25(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16(4)	16	–16		
	24(4)	24	–24		
LVCMOS18(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12(4)	12	–12		
	16(4)	16	–16		
LVCMOS15(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8(4)	8	–8		
	12(4)	12	–12		
LVCMOS12(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4(4)	4	–4		
	6(4)	6	–6		

Table 12: **DC Characteristics of User I/Os Using Single-Ended Standards *(Continued)***

IOSTANDARD Attribute	Test Conditions		Logic Level Characteristics	
	I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
PCI33_3(5)	1.5	–0.5	10% V_{CCO}	90% V_{CCO}
PCI66_3(5)	1.5	–0.5	10% V_{CCO}	90% V_{CCO}
HSTL_I(4)	8	–8	0.4	V_{CCO} - 0.4
HSTL_III(4)	24	–8	0.4	V_{CCO} - 0.4
HSTL_I_18	8	–8	0.4	V_{CCO} - 0.4
HSTL_II_18(4)	16	–16	0.4	V_{CCO} - 0.4
HSTL_III_18	24	–8	0.4	V_{CCO} - 0.4
SSTL18_I	6.7	–6.7	V_{TT} – 0.475	V_{TT} + 0.475
SSTL18_II(4)	13.4	–13.4	V_{TT} – 0.603	V_{TT} + 0.603
SSTL2_I	8.1	–8.1	V_{TT} – 0.61	V_{TT} + 0.61
SSTL2_II(4)	16.2	–16.2	V_{TT} – 0.81	V_{TT} + 0.81
SSTL3_I	8	–8	V_{TT} – 0.6	V_{TT} + 0.6
SSTL3_II	16	–16	V_{TT} – 0.8	V_{TT} + 0.8

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8 and Table 11.
2. Descriptions of the symbols used in this table are as follows:
   I_{OL} — the output current condition under which V_{OL} is tested
   I_{OH} — the output current condition under which V_{OH} is tested
   V_{OL} — the output voltage that indicates a Low logic level
   V_{OH} — the output voltage that indicates a High logic level
   V_{CCO} — the supply voltage for output drivers
   V_{TT} — the voltage applied to a resistor termination
3. For the LVCMOS and LVTTL standards: the same V_{OL} and V_{OH} limits apply for the Fast, Slow, and QUIETIO slew attributes.
4. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
5. Tested according to the relevant PCI specifications. For information on PCI IP solutions, see www.xilinx.com/pci. The PCIX IOSTANDARD is available and has equivalent characteristics but no PCI-X IP is supported.

Table 22: **Propagation Times for the IOB Input Path *(Continued)***

Symbol	Description	Conditions	DELAY_VALUE	Device	Speed Grade		Units
					-5	-4	
					Max	Max	
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25(2)	5	XC3S400A	3.55	4.18	ns
			6		4.34	5.03	ns
			7		5.09	5.88	ns
			8		5.58	6.42	ns
			1	XC3S700A	1.96	2.18	ns
			2		2.76	3.06	ns
			3		3.45	3.95	ns
			4		3.97	4.54	ns
			5		3.83	4.37	ns
			6		4.74	5.42	ns
			7		5.53	6.33	ns
			8		6.06	6.96	ns
			1	XC3S1400A	1.93	2.40	ns
			2		2.69	3.15	ns
			3		3.52	3.99	ns
			4		3.89	4.55	ns
			5		3.95	4.42	ns
			6		4.53	5.32	ns
			7		5.30	6.21	ns
			8		5.83	6.80	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 23.

Output Timing Adjustments

Table 26: **Output Timing Adjustments for IOB**

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
Single-Ended Standards					
LVTTL	Slow	2 mA	5.58	5.58	ns
		4 mA	3.16	3.16	ns
		6 mA	3.17	3.17	ns
		8 mA	2.09	2.09	ns
		12 mA	1.62	1.62	ns
		16 mA	1.24	1.24	ns
		24 mA	2.74(3)	2.74(3)	ns
	Fast	2 mA	3.03	3.03	ns
		4 mA	1.71	1.71	ns
		6 mA	1.71	1.71	ns
		8 mA	0.53	0.53	ns
		12 mA	0.53	0.53	ns
		16 mA	0.59	0.59	ns
		24 mA	0.60	0.60	ns
	QuietIO	2 mA	27.67	27.67	ns
		4 mA	27.67	27.67	ns
		6 mA	27.67	27.67	ns
		8 mA	16.71	16.71	ns
		12 mA	16.67	16.67	ns
		16 mA	16.22	16.22	ns
		24 mA	12.11	12.11	ns

Table 26: **Output Timing Adjustments for IOB*(Continued)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS33	Slow	2 mA	5.58	5.58	ns
		4 mA	3.17	3.17	ns
		6 mA	3.17	3.17	ns
		8 mA	2.09	2.09	ns
		12 mA	1.24	1.24	ns
		16 mA	1.15	1.15	ns
		24 mA	2.55(3)	2.55(3)	ns
	Fast	2 mA	3.02	3.02	ns
		4 mA	1.71	1.71	ns
		6 mA	1.72	1.72	ns
		8 mA	0.53	0.53	ns
		12 mA	0.59	0.59	ns
		16 mA	0.59	0.59	ns
		24 mA	0.51	0.51	ns
	QuietIO	2 mA	27.67	27.67	ns
		4 mA	27.67	27.67	ns
		6 mA	27.67	27.67	ns
		8 mA	16.71	16.71	ns
		12 mA	16.29	16.29	ns
		16 mA	16.18	16.18	ns
		24 mA	12.11	12.11	ns

Table 26: **Output Timing Adjustments for IOB*(Continued)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS25	Slow	2 mA	5.33	5.33	ns
		4 mA	2.81	2.81	ns
		6 mA	2.82	2.82	ns
		8 mA	1.14	1.14	ns
		12 mA	1.10	1.10	ns
		16 mA	0.83	0.83	ns
		24 mA	2.26(3)	2.26(3)	ns
	Fast	2 mA	4.36	4.36	ns
		4 mA	1.76	1.76	ns
		6 mA	1.25	1.25	ns
		8 mA	0.38	0.38	ns
		12 mA	0	0	ns
		16 mA	0.01	0.01	ns
		24 mA	0.01	0.01	ns
	QuietIO	2 mA	25.92	25.92	ns
		4 mA	25.92	25.92	ns
		6 mA	25.92	25.92	ns
		8 mA	15.57	15.57	ns
		12 mA	15.59	15.59	ns
		16 mA	14.27	14.27	ns
		24 mA	11.37	11.37	ns
LVCMOS18	Slow	2 mA	4.48	4.48	ns
		4 mA	3.69	3.69	ns
		6 mA	2.91	2.91	ns
		8 mA	1.99	1.99	ns
		12 mA	1.57	1.57	ns
		16 mA	1.19	1.19	ns
	Fast	2 mA	3.96	3.96	ns
		4 mA	2.57	2.57	ns
		6 mA	1.90	1.90	ns
		8 mA	1.06	1.06	ns
		12 mA	0.83	0.83	ns
		16 mA	0.63	0.63	ns
	QuietIO	2 mA	24.97	24.97	ns
		4 mA	24.97	24.97	ns
		6 mA	24.08	24.08	ns
		8 mA	16.43	16.43	ns
		12 mA	14.52	14.52	ns
		16 mA	13.41	13.41	ns

Table 26: **Output Timing Adjustments for IOB*(Continued)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS15	Slow	2 mA	5.82	5.82	ns
		4 mA	3.97	3.97	ns
		6 mA	3.21	3.21	ns
		8 mA	2.53	2.53	ns
		12 mA	2.06	2.06	ns
	Fast	2 mA	5.23	5.23	ns
		4 mA	3.05	3.05	ns
		6 mA	1.95	1.95	ns
		8 mA	1.60	1.60	ns
		12 mA	1.30	1.30	ns
	QuietIO	2 mA	34.11	34.11	ns
		4 mA	25.66	25.66	ns
		6 mA	24.64	24.64	ns
		8 mA	22.06	22.06	ns
		12 mA	20.64	20.64	ns
LVCMOS12	Slow	2 mA	7.14	7.14	ns
		4 mA	4.87	4.87	ns
		6 mA	5.67	5.67	ns
	Fast	2 mA	6.77	6.77	ns
		4 mA	5.02	5.02	ns
		6 mA	4.09	4.09	ns
	QuietIO	2 mA	50.76	50.76	ns
		4 mA	43.17	43.17	ns
		6 mA	37.31	37.31	ns
PCI33_3			0.34	0.34	ns
PCI66_3			0.34	0.34	ns
HSTL_I			0.78	0.78	ns
HSTL_III			1.16	1.16	ns
HSTL_I_18			0.35	0.35	ns
HSTL_II_18			0.30	0.30	ns
HSTL_III_18			0.47	0.47	ns
SSTL18_I			0.40	0.40	ns
SSTL18_II			0.30	0.30	ns
SSTL2_I			0	0	ns
SSTL2_II			–0.05	–0.05	ns
SSTL3_I			0	0	ns
SSTL3_II			0.17	0.17	ns

Digital Frequency Synthesizer (DFS)

Table 38: **Recommended Operating Conditions for the DFS**

Symbol		Description		Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges(2)								
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input		0.200	333(4)	0.200	333(4)	MHz
Input Clock Jitter Tolerance(3)								
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency	$F_{CLKFX} \leq 150$ MHz	–	±300	–	±300	ps
CLKIN_CYC_JITT_FX_HF			$F_{CLKFX} > 150$ MHz	–	±150	–	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input		–	±1	–	±1	ns

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 36.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.
4. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM.

Table 39: **Switching Characteristics for the DFS**

Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_FX(2)	Frequency for the CLKFX and CLKFX180 outputs		All	5	350	5	320	MHz
Output Clock Jitter(3,4)								
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.		All	**Typ**	**Max**	**Typ**	**Max**	
		CLKIN ≤ 20 MHz		Use the Spartan-3A Jitter Calculator: www.xilinx.com/support/documentation/data_sheets/s3a_jitter_calc.zip				ps
		CLKIN > 20 MHz		±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	ps
Duty Cycle(5,6)								
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	–	±[1% of CLKFX period + 350]	–	±[1% of CLKFX period + 350]	ps
Phase Alignment(6)								
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used		All	–	±200	–	±200	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used		All	–	±[1% of CLKFX period + 200]	–	±[1% of CLKFX period + 200]	ps

Configuration Clock (CCLK) Characteristics

Table 46: **Master Mode CCLK Output Period by *ConfigRate* Opti0on Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
T_{CCLK1}	CCLK clock period by ***ConfigRate*** setting	1 *(power-on value)*	Commercial	1,254	2,500	ns
			Industrial	1,180		ns
T_{CCLK3}		3	Commercial	413	833	ns
			Industrial	390		ns
T_{CCLK6}		6 (default)	Commercial	207	417	ns
			Industrial	195		ns
T_{CCLK7}		7	Commercial	178	357	ns
			Industrial	168		ns
T_{CCLK8}		8	Commercial	156	313	ns
			Industrial	147		ns
T_{CCLK10}		10	Commercial	123	250	ns
			Industrial	116		ns
T_{CCLK12}		12	Commercial	103	208	ns
			Industrial	97		ns
T_{CCLK13}		13	Commercial	93	192	ns
			Industrial	88		ns
T_{CCLK17}		17	Commercial	72	147	ns
			Industrial	68		ns
T_{CCLK22}		22	Commercial	54	114	ns
			Industrial	51		ns
T_{CCLK25}		25	Commercial	47	100	ns
			Industrial	45		ns
T_{CCLK27}		27	Commercial	44	93	ns
			Industrial	42		ns
T_{CCLK33}		33	Commercial	36	76	ns
			Industrial	34		ns
T_{CCLK44}		44	Commercial	26	57	ns
			Industrial	25		ns
T_{CCLK50}		50	Commercial	22	50	ns
			Industrial	21		ns
$T_{CCLK100}$		100	Commercial	11.2	25	ns
			Industrial	10.6		ns

Notes:

1. Set the ***ConfigRate*** option value when generating a configuration bitstream.

Byte Peripheral Interface (BPI) Configuration Timing

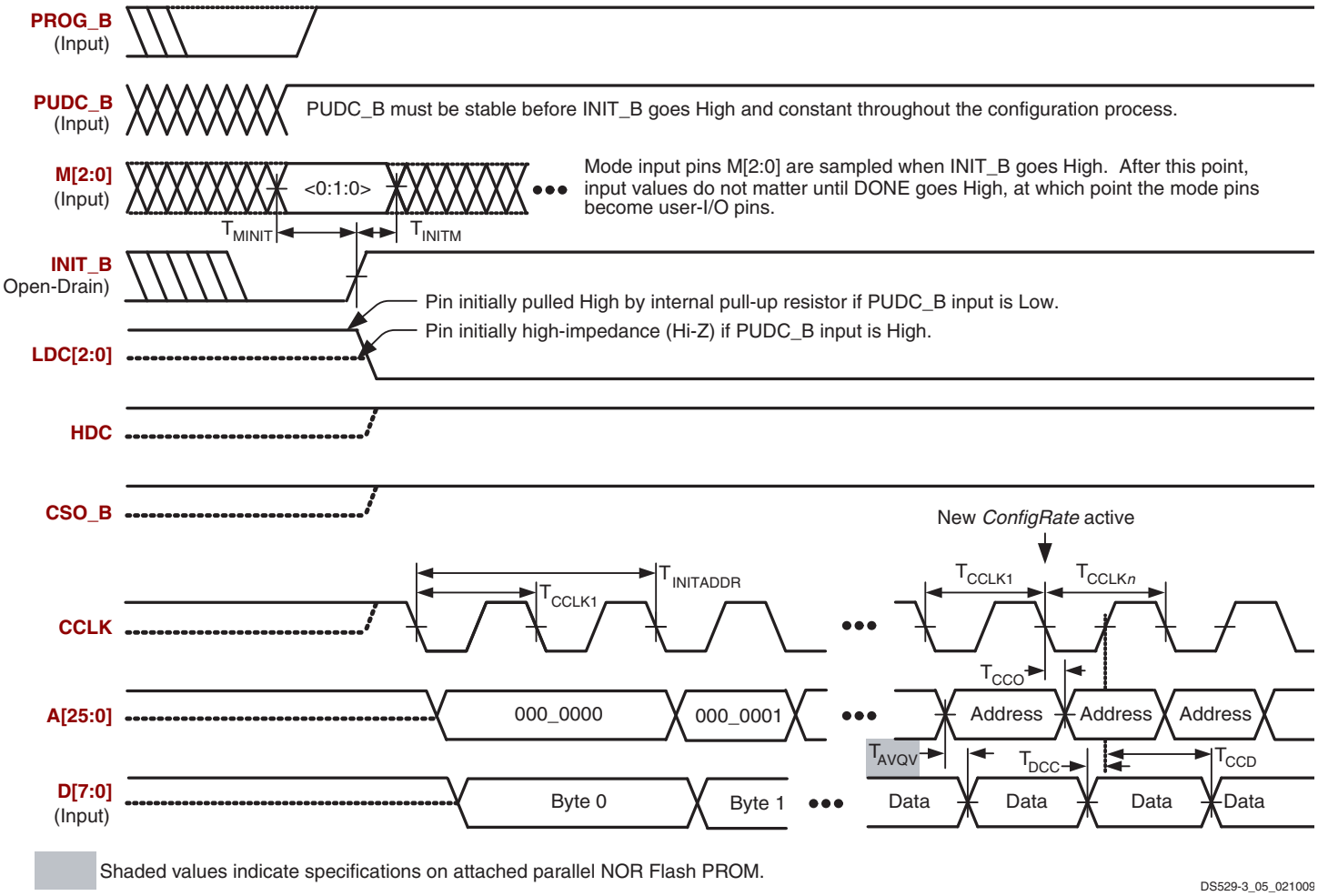

Figure 15: **Waveforms for Byte-wide Peripheral Interface (BPI) Configuration**

Table 54: **Timing for Byte-wide Peripheral Interface (BPI) Configuration Mode**

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	See Table 46		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting	See Table 46		
T_{MINIT}	Setup time on M[2:0] mode pins before the rising edge of INIT_B	50	–	ns
T_{INITM}	Hold time on M[2:0] mode pins after the rising edge of INIT_B	0	–	ns
$T_{INITADDR}$	Minimum period of initial A[25:0] address cycle; LDC[2:0] and HDC are asserted and valid	5	5	T_{CCLK1} cycles
T_{CCO}	Address A[25:0] outputs valid after CCLK falling edge	See Table 50		
T_{DCC}	Setup time on D[7:0] data inputs before CCLK rising edge	See T_{SMDCC} in Table 51		
T_{CCD}	Hold time on D[7:0] data inputs after CCLK rising edge	0	–	ns

Table 55: **Configuration Timing Requirements for Attached Parallel NOR BPI Flash**

Symbol	Description	Requirement	Units
T_{CE} (t_{ELQV})	Parallel NOR Flash PROM chip-select time	$T_{CE} \leq T_{INITADDR}$	ns
T_{OE} (t_{GLQV})	Parallel NOR Flash PROM output-enable time	$T_{OE} \leq T_{INITADDR}$	ns
T_{ACC} (t_{AVQV})	Parallel NOR Flash PROM read access time	$T_{ACC} \leq 50\% T_{CCLKn(min)} - T_{CCO} - T_{DCC} - PCB$	ns
T_{BYTE} (t_{FLQV}, t_{FHQV})	For x8/x16 PROMs only: BYTE# to output valid time(3)	$T_{BYTE} \leq T_{INITADDR}$	ns

Notes:

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's PUDC_B pin is High or Low.

Package Thermal Characteristics

The power dissipated by an FPGA application has implications on package selection and system design. The power consumed by a Spartan-3A FPGA is reported using either the XPower Power Estimator or the XPower Analyzer calculator integrated in the Xilinx® ISE® development software. Table 62 provides the thermal characteristics for the various Spartan-3A FPGA package offerings. This information is also available using the Thermal Query tool on xilinx.com (www.xilinx.com/cgi-bin/thermal/thermal.pl).

The junction-to-case thermal resistance (θ_{JC}) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board (θ_{JB}) value similarly reports the difference between the board and junction temperature. The junction-to-ambient (θ_{JA}) value reports the temperature difference between the ambient environment and the junction temperature. The θ_{JA} value is reported at different air velocities, measured in linear feet per minute (LFM). The “Still Air (0 LFM)” column shows the θ_{JA} value in a system without a fan. The thermal resistance drops with increasing air flow.

Table 62: **Spartan-3A Package Thermal Characteristics**

Package	Device	Junction-to-Case (θ_{JC})	Junction-to-Board (θ_{JB})	Junction-to-Ambient (θ_{JA}) at Different Air Flows				Units
				Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	
VQ100 VQG100	XC3S50A	12.9	30.1	48.5	40.4	37.6	36.6	°C/Watt
	XC3S200A	10.9	25.7	42.9	35.7	33.2	32.4	°C/Watt
TQ144 TQG144	XC3S50A	16.5	32.0	42.4	36.3	35.8	34.9	°C/Watt
FT256 FTG256	XC3S50A	16.0	33.5	42.3	35.6	35.5	34.5	°C/Watt
	XC3S200A	10.3	23.8	32.7	26.6	26.1	25.2	°C/Watt
	XC3S400A	8.4	19.3	29.9	24.9	23.0	22.3	°C/Watt
	XC3S700A	7.8	18.6	28.1	22.3	21.2	20.7	°C/Watt
	XC3S1400A	5.4	14.1	24.2	18.7	17.5	17.0	°C/Watt
FG320 FGG320	XC3S200A	11.7	18.5	27.8	22.3	21.1	20.3	°C/Watt
	XC3S400A	9.9	15.4	25.2	19.8	18.6	17.8	°C/Watt
FG400 FGG400	XC3S400A	9.8	15.5	25.6	19.2	18.0	17.3	°C/Watt
	XC3S700A	8.2	13.0	23.1	17.9	16.7	16.0	°C/Watt
FG484 FGG484	XC3S700A	7.9	12.8	22.3	17.4	16.2	15.5	°C/Watt
	XC3S1400A	6.0	9.9	19.5	14.7	13.5	12.8	°C/Watt
FG676 FGG676	XC3S1400A	5.8	9.4	17.8	13.5	12.4	11.8	°C/Watt

User I/Os by Bank

Table 64 indicates how the 68 available user-I/O pins are distributed between the four I/O banks on the VQ100 package.

Table 64: **User I/Os Per Bank for the XC3S50A and XC3S200A in the VQ100 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	15	3	1	1	3	7
Right	1	13	6	0	0	1	6
Bottom	2	26	2	0	19	1	4
Left	3	14	6	1	0	1	6
TOTAL		**68**	**17**	**2**	**20**	**6**	**23**

Footprint Migration Differences

The XC3S50A and XC3S200 have common VQ100 pinouts except for some differences in alignment of differential I/O pairs.

Differential I/O Alignment Differences

Some differential I/O pairs in the VQ100 on the XC3S50A FPGA are aligned differently than the corresponding pairs on the XC3S200A FPGAs, as shown in Table 65. All the mismatched pairs are in I/O Bank 2. These differences are indicated with the black diamond character (◆) in the footprint diagrams Figure 17 and Figure 18.

Table 65: **Differential I/O Differences in VQ100**

VQ100 Pin	Bank	XC3S50A	XC3S200A
P29	2	IIO_L04P_2/VS2	IO_L03N_2/VS2
P30		IO_L03N_2/VS1	IO_L04P_2/VS1
P33		IO_L06P_2	IO_L05N_2
P34		IO_L05N_2/D7	IO_L06P_2/D7
P51		IO_L11N_2/D0/DIN/MISO	IO_L12P_2/D0/DIN/MISO
P52		IO_L12P_2/D1	IO_L11N_2/D1

Table 68: **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400) *(Continued)***

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
VCCINT	VCCINT	VCCINT	K8	VCCINT
VCCINT	VCCINT	VCCINT	K10	VCCINT

Table 69: **Spartan-3A FT256 Pinout (XC3S700A, XC3S1400A)**

Bank	XC3S700A XC3S1400A	FT256 Ball	Type
0	IO_L01N_0	C13	I/O
0	IO_L01P_0	D13	I/O
0	IO_L02N_0	B14	I/O
0	IO_L02P_0/VREF_0	B15	VREF
0	IO_L03N_0	D12	I/O
0	IO_L03P_0	C12	I/O
0	IO_L04N_0	A13	I/O
0	IO_L04P_0	A14	I/O
0	IO_L05N_0	A12	I/O
0	IO_L05P_0	B12	I/O
0	IO_L06N_0/VREF_0	D10	VREF
0	IO_L06P_0	D11	I/O
0	IO_L07N_0	A11	I/O
0	IO_L07P_0	C11	I/O
0	IO_L08N_0	A10	I/O
0	IO_L08P_0	B10	I/O
0	IO_L09N_0/GCLK5	D9	GCLK
0	IO_L09P_0/GCLK4	C10	GCLK
0	IO_L10N_0/GCLK7	A9	GCLK
0	IO_L10P_0/GCLK6	C9	GCLK
0	IO_L11N_0/GCLK9	D8	GCLK
0	IO_L11P_0/GCLK8	C8	GCLK
0	IO_L12N_0/GCLK11	B8	GCLK
0	IO_L12P_0/GCLK10	A8	GCLK
0	IO_L13N_0	C7	I/O
0	IO_L13P_0	A7	I/O
0	IO_L14N_0/VREF_0	E7	VREF
0	IO_L14P_0	E9	I/O
0	IO_L15N_0	B6	I/O
0	IO_L15P_0	A6	I/O
0	IO_L16N_0	C6	I/O
0	IO_L16P_0	D7	I/O
0	IO_L17N_0	C5	I/O
0	IO_L17P_0	A5	I/O
0	IO_L18N_0	B4	I/O
0	IO_L18P_0	A4	I/O
0	IO_L19N_0	B3	I/O
0	IO_L19P_0	A3	I/O
0	IO_L20N_0/PUDC_B	D5	DUAL
0	IO_L20P_0/VREF_0	C4	VREF
0	IP_0	E6	INPUT
0	VCCO_0	B13	VCCO
0	VCCO_0	B5	VCCO
0	VCCO_0	B9	VCCO
0	VCCO_0	E8	VCCO
1	IO_L01N_1/LDC2	N14	DUAL
1	IO_L01P_1/HDC	N13	DUAL
1	IO_L02N_1/LDC0	P15	DUAL
1	IO_L02P_1/LDC1	R15	DUAL
1	IO_L03N_1/A1	N16	DUAL
1	IO_L03P_1/A0	P16	DUAL
1	IO_L06N_1/A3	K13	DUAL
1	IO_L06P_1/A2	L13	DUAL
1	IO_L07N_1/A5	M16	DUAL
1	IO_L07P_1/A4	M15	DUAL
1	IO_L08N_1/A7	L16	DUAL
1	IO_L08P_1/A6	L14	DUAL
1	IO_L10N_1/A9	J13	DUAL
1	IO_L10P_1/A8	J12	DUAL
1	IO_L11N_1/RHCLK1	K14	RHCLK
1	IO_L11P_1/RHCLK0	K15	RHCLK
1	IO_L12N_1/TRDY1/RHCLK3	J16	RHCLK
1	IO_L12P_1/RHCLK2	K16	RHCLK
1	IO_L15N_1/RHCLK7	H16	RHCLK
1	IO_L15P_1/IRDY1/RHCLK6	H15	RHCLK
1	IO_L16N_1/A11	F16	DUAL
1	IO_L16P_1/A10	G16	DUAL
1	IO_L17N_1/A13	G14	DUAL
1	IO_L17P_1/A12	H13	DUAL
1	IO_L18N_1/A15	F15	DUAL
1	IO_L18P_1/A14	E16	DUAL
1	IO_L19N_1/A17	F14	DUAL
1	IO_L19P_1/A16	G13	DUAL
1	IO_L20N_1/A19	F13	DUAL

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
3	IO_L10N_3/VREF_3	F1	VREF
3	IO_L10P_3	F2	I/O
3	IO_L11N_3	J6	I/O
3	IO_L11P_3	J7	I/O
3	IO_L13N_3	H1	I/O
3	IO_L13P_3	H2	I/O
3	IO_L14N_3/LHCLK1	J3	LHCLK
3	IO_L14P_3/LHCLK0	H3	LHCLK
3	IO_L15N_3/IRDY2/LHCLK3	J1	LHCLK
3	IO_L15P_3/LHCLK2	J2	LHCLK
3	IO_L17N_3/LHCLK5	K5	LHCLK
3	IO_L17P_3/LHCLK4	J4	LHCLK
3	IO_L18N_3/LHCLK7	K3	LHCLK
3	IO_L18P_3/TRDY2/LHCLK6	K2	LHCLK
3	IO_L19N_3	L2	I/O
3	IO_L19P_3/VREF_3	L1	VREF
3	IO_L21N_3	M2	I/O
3	IO_L21P_3	N1	I/O
3	IO_L22N_3	N2	I/O
3	IO_L22P_3	P1	I/O
3	IO_L23N_3	L4	I/O
3	IO_L23P_3	L3	I/O
3	IO_L25N_3	R2	I/O
3	IO_L25P_3	R1	I/O
3	IO_L26N_3	N4	I/O
3	IO_L26P_3	N3	I/O
3	IO_L27N_3	T2	I/O
3	IO_L27P_3	T1	I/O
3	IO_L29N_3	N6	I/O
3	IO_L29P_3	N5	I/O
3	IO_L30N_3	R3	I/O
3	IO_L30P_3	P3	I/O
3	IO_L31N_3	U2	I/O
3	IO_L31P_3	U1	I/O
3	IP_L04N_3/VREF_3	H7	VREF
3	IP_L04P_3	G6	INPUT
3	IP_L08N_3/VREF_3	H5	VREF
3	IP_L08P_3	H6	INPUT
3	IP_L12N_3	G2	INPUT
3	IP_L12P_3	G3	INPUT

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
3	IP_L16N_3	K6	INPUT
3	IP_L16P_3	J5	INPUT
3	IP_L20N_3	L6	INPUT
3	IP_L20P_3	L7	INPUT
3	IP_L24N_3	M4	INPUT
3	IP_L24P_3	M3	INPUT
3	IP_L28N_3	M5	INPUT
3	IP_L28P_3	M6	INPUT
3	IP_L32N_3/VREF_3	P4	VREF
3	IP_L32P_3	P5	INPUT
3	VCCO_3	E2	VCCO
3	VCCO_3	H4	VCCO
3	VCCO_3	L5	VCCO
3	VCCO_3	P2	VCCO
GND	GND	A1	GND
GND	GND	A7	GND
GND	GND	A12	GND
GND	GND	A18	GND
GND	GND	C10	GND
GND	GND	D4	GND
GND	GND	D7	GND
GND	GND	D15	GND
GND	GND	F6	GND
GND	GND	G1	GND
GND	GND	G12	GND
GND	GND	G18	GND
GND	GND	H8	GND
GND	GND	H10	GND
GND	GND	J11	GND
GND	GND	J15	GND
GND	GND	K4	GND
GND	GND	K8	GND
GND	GND	L9	GND
GND	GND	L11	GND
GND	GND	M1	GND
GND	GND	M7	GND
GND	GND	M18	GND
GND	GND	N13	GND
GND	GND	R4	GND
GND	GND	R12	GND

Table 81: **Spartan-3A FG400 Pinout*(Continued)***

Bank	Pin Name	FG400 Ball	Type
3	IO_L34P_3	U1	I/O
3	IO_L36N_3	T4	I/O
3	IO_L36P_3	R5	I/O
3	IO_L37N_3	V2	I/O
3	IO_L37P_3	V1	I/O
3	IO_L38N_3	W2	I/O
3	IO_L38P_3	W1	I/O
3	IP_3	H7	INPUT
3	IP_L04N_3/VREF_3	G6	VREF
3	IP_L04P_3	G7	INPUT
3	IP_L11N_3/VREF_3	J7	VREF
3	IP_L11P_3	J8	INPUT
3	IP_L15N_3	K7	INPUT
3	IP_L15P_3	K8	INPUT
3	IP_L19N_3	K5	INPUT
3	IP_L19P_3	K6	INPUT
3	IP_L23N_3	L6	INPUT
3	IP_L23P_3	L7	INPUT
3	IP_L27N_3	M7	INPUT
3	IP_L27P_3	M8	INPUT
3	IP_L31N_3	N7	INPUT
3	IP_L31P_3	M6	INPUT
3	IP_L35N_3	N6	INPUT
3	IP_L35P_3	P5	INPUT
3	IP_L39N_3/VREF_3	P7	VREF
3	IP_L39P_3	P6	INPUT
3	VCCO_3	E2	VCCO
3	VCCO_3	H5	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	N5	VCCO
3	VCCO_3	U2	VCCO
GND	GND	A1	GND
GND	GND	A11	GND
GND	GND	A20	GND
GND	GND	B6	GND
GND	GND	B14	GND
GND	GND	C3	GND
GND	GND	C18	GND
GND	GND	D9	GND
GND	GND	E5	GND

Table 81: **Spartan-3A FG400 Pinout*(Continued)***

Bank	Pin Name	FG400 Ball	Type
GND	GND	E12	GND
GND	GND	F15	GND
GND	GND	G2	GND
GND	GND	G19	GND
GND	GND	H8	GND
GND	GND	H13	GND
GND	GND	J9	GND
GND	GND	J11	GND
GND	GND	K1	GND
GND	GND	K10	GND
GND	GND	K12	GND
GND	GND	K17	GND
GND	GND	L4	GND
GND	GND	L9	GND
GND	GND	L11	GND
GND	GND	L20	GND
GND	GND	M10	GND
GND	GND	M12	GND
GND	GND	N8	GND
GND	GND	N11	GND
GND	GND	N13	GND
GND	GND	P2	GND
GND	GND	P19	GND
GND	GND	R6	GND
GND	GND	R9	GND
GND	GND	T16	GND
GND	GND	U12	GND
GND	GND	V3	GND
GND	GND	V18	GND
GND	GND	W7	GND
GND	GND	W15	GND
GND	GND	Y1	GND
GND	GND	Y10	GND
GND	GND	Y20	GND
VCCAUX	SUSPEND	R15	PWR MGMT
VCCAUX	DONE	W19	CONFIG
VCCAUX	PROG_B	D5	CONFIG
VCCAUX	TCK	A19	JTAG
VCCAUX	TDI	F5	JTAG

FG484 Footprint

Left Half of FG484 Package (Top View)

195 **I/O:** Unrestricted, general-purpose user I/O

60-62 **INPUT:** Unrestricted, general-purpose input pin

51 **DUAL:** Configuration pins, then possible user I/O

33-34 **VREF:** User I/O or input voltage reference for bank

32 **CLK:** User I/O, input, or clock buffer input

2 **SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins

2 **CONFIG:** Dedicated configuration pins

4 **JTAG:** Dedicated JTAG port pins

53 **GND:** Ground

24 **VCCO:** Output voltage supply for bank

15 **VCCINT:** Internal core supply voltage (+1.2V)

10 **VCCAUX:** Auxiliary supply voltage

3 ◆ **N.C.:** Not connected (XC3S700A only)

Bank 0

	1	2	3	4	5	6	7	8	9	10	11
A	GND	I/O L36N_0 PUDC_B	I/O L33P_0	I/O L31P_0	I/O L28N_0	I/O L26N_0	I/O L26P_0	I/O L22N_0	I/O L22P_0	I/O L21P_0	I/O L18N_0 GCLK7
B	I/O L02P_3	I/O L36P_0 VREF_0	I/O L33N_0	I/O L31N_0	VCCO_0	I/O L28P_0	GND	I/O L25P_0	I/O L24P_0	VCCO_0	I/O L19P_0 GCLK8
C	I/O L01P_3	I/O L02N_3	GND	PROG_B	I/O L32P_0	I/O L29P_0	I/O L27N_0	I/O L25N_0	I/O L24N_0 VREF_0	I/O L21N_0	I/O L19N_0 GCLK9
D	I/O L06P_3	I/O L01N_3	I/O L03P_3	TMS	I/O L32N_0	I/O L29N_0	I/O L27P_0	I/O L30N_0	GND	I/O L23P_0	I/O L20P_0 GCLK10
E	I/O L06N_3	VCCO_3	I/O L07N_3	I/O L03N_3	VCCAUX	I/O L35N_0	I/O L34P_0	INPUT	I/O L30P_0	I/O L23N_0	I/O L20N_0 GCLK11
F	I/O L12N_3	I/O L12P_3	I/O L08P_3	I/O L07P_3	TDI	GND	I/O L35P_0	I/O L34N_0	VCCO_0	INPUT	GND
G	I/O L13N_3	GND	I/O L13P_3	I/O L08N_3	I/O L05N_3	I/O L05P_3	INPUT	INPUT VREF_0	INPUT	INPUT	INPUT
H	I/O L16N_3	I/O L16P_3	I/O L14N_3	I/O L14P_3	I/O L09P_3	I/O L09N_3	INPUT L04N_3 VREF_3	INPUT L04P_3	INPUT VREF_0	INPUT	VCCAUX
J	I/O L17N_3 VREF_3	VCCO_3	I/O L17P_3	GND	I/O L10N_3	VCCO_3	INPUT L11P_3	INPUT VREF_3	GND	VCCINT	GND
K	I/O L22P_3 LHCLK2	I/O L20N_3	I/O L20P_3	I/O L18N_3	I/O L18P_3	I/O L10P_3	INPUT L15P_3	INPUT L11N_3	VCCINT	GND	VCCINT
L	I/O L22N_3 IRDY2 LHCLK3	GND	I/O L21N_3 LHCLK1	VCCAUX	I/O L21P_3 LHCLK0	GND	INPUT L19P_3	INPUT L15N_3 VREF_3	GND	VCCINT	GND
M	I/O L24P_3 LHCLK4	I/O L24N_3 LHCLK5	I/O L25P_3 TRDY2 LHCLK6	I/O L25N_3 LHCLK7	I/O L30P_3	INPUT L23N_3	INPUT L23P_3	INPUT L19N_3	VCCINT	GND	VCCINT
N	I/O L26P_3 VREF_3	VCCO_3	I/O L26N_3	I/O L30N_3	INPUT L31N_3	INPUT L31P_3	INPUT L35P_3	INPUT L27P_3	INPUT L27N_3	VCCINT	GND
P	I/O L28P_3	I/O L28N_3	I/O L29P_3	GND	I/O L29N_3	VCCO_3	INPUT L39P_3	INPUT L35N_3	GND	GND	VCCAUX
R	I/O L32P_3	I/O L32N_3	I/O L33P_3	I/O L33N_3	I/O L34P_3	INPUT VREF_3	INPUT L46P_3	INPUT L39N_3	INPUT	INPUT	INPUT
T	I/O L36P_3 VREF_3	GND	I/O L36N_3	I/O L34N_3	I/O L40P_3	INPUT L46N_3 VREF_3	INPUT VREF_2	INPUT VREF_2 ◆	INPUT	INPUT VREF_2	INPUT VREF_2
U	I/O L37P_3	I/O L37N_3	I/O L41P_3	I/O L41N_3	I/O L40N_3	GND	INPUT ◆	INPUT	VCCO_2	INPUT	I/O L17P_2 GCLK12
V	I/O L38P_3	VCCO_3	I/O L38N_3	I/O L43P_3	VCCAUX	I/O L01P_2 M1	INPUT	INPUT VREF_2	I/O L09P_2 RDWR_B	I/O L13P_2	I/O L17N_2 GCLK13
W	I/O L42P_3	I/O L42N_3	I/O L43N_3	I/O L02P_2 M2	I/O L01N_2 M0	I/O L05P_2	I/O L07P_2	I/O L11P_2 VS1	I/O L09N_2 VS2	GND	VCCAUX
Y	I/O L44P_3	I/O L44N_3	GND	I/O L02N_2 CSO_B	I/O L05N_2	I/O L07N_2	I/O L10P_2	I/O L11N_2 VS0	I/O L14P_2 D7	I/O L13N_2	I/O L16P_2 D5
AA	I/O L45P_3	I/O L45N_3	I/O L03N_2	I/O L04N_2	VCCO_2	I/O L08P_2	GND	I/O L12P_2	VCCO_2	I/O L15P_2	GND
AB	GND	I/O L03P_2	I/O L04P_2	I/O L06P_2	I/O L06N_2	I/O L08N_2	I/O L10N_2	I/O L12N_2	I/O L14N_2 D6	I/O L15N_2	I/O L16N_2 D4

Bank 3 (rows A–AB)

Bank 2

DS529-4_01_101106

Figure 25: **FG484 Package Footprint (Top View)**

FG676: 676-ball Fine-pitch Ball Grid Array

The 676-ball fine-pitch ball grid array, FG676, supports the XC3S1400A FPGA.

Table 87 lists all the FG676 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The XC3S1400A has 17 unconnected balls, indicated as N.C. (No Connection) in Table 87 and with the black diamond character (◆) in Table 87 and Figure 27.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at:

www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 87: **Spartan-3A FG676 Pinout**

Bank	Pin Name	FG676 Ball	Type
0	IO_L01N_0	F20	I/O
0	IO_L01P_0	G20	I/O
0	IO_L02N_0	F19	I/O
0	IO_L02P_0/VREF_0	G19	VREF
0	IO_L05N_0	C22	I/O
0	IO_L05P_0	D22	I/O
0	IO_L06N_0	C23	I/O
0	IO_L06P_0	D23	I/O
0	IO_L07N_0	A22	I/O
0	IO_L07P_0	B23	I/O
0	IO_L08N_0	G17	I/O
0	IO_L08P_0	H17	I/O
0	IO_L09N_0	B21	I/O
0	IO_L09P_0	C21	I/O
0	IO_L10N_0	D21	I/O
0	IO_L10P_0	E21	I/O
0	IO_L11N_0	C20	I/O
0	IO_L11P_0	D20	I/O
0	IO_L12N_0	K16	I/O
0	IO_L12P_0	J16	I/O
0	IO_L13N_0	E17	I/O
0	IO_L13P_0	F17	I/O
0	IO_L14N_0	A20	I/O
0	IO_L14P_0/VREF_0	B20	VREF

Table 87: **Spartan-3A FG676 Pinout *(Continued)***

Bank	Pin Name	FG676 Ball	Type
0	IO_L15N_0	A19	I/O
0	IO_L15P_0	B19	I/O
0	IO_L16N_0	H15	I/O
0	IO_L16P_0	G15	I/O
0	IO_L17N_0	C18	I/O
0	IO_L17P_0	D18	I/O
0	IO_L18N_0	A18	I/O
0	IO_L18P_0	B18	I/O
0	IO_L19N_0	B17	I/O
0	IO_L19P_0	C17	I/O
0	IO_L20N_0/VREF_0	E15	VREF
0	IO_L20P_0	F15	I/O
0	IO_L21N_0	C16	I/O
0	IO_L21P_0	D17	I/O
0	IO_L22N_0	C15	I/O
0	IO_L22P_0	D16	I/O
0	IO_L23N_0	A15	I/O
0	IO_L23P_0	B15	I/O
0	IO_L24N_0	F14	I/O
0	IO_L24P_0	E14	I/O
0	IO_L25N_0/GCLK5	J14	GCLK
0	IO_L25P_0/GCLK4	K14	GCLK
0	IO_L26N_0/GCLK7	A14	GCLK
0	IO_L26P_0/GCLK6	B14	GCLK
0	IO_L27N_0/GCLK9	G13	GCLK
0	IO_L27P_0/GCLK8	F13	GCLK
0	IO_L28N_0/GCLK11	C13	GCLK
0	IO_L28P_0/GCLK10	B13	GCLK
0	IO_L29N_0	B12	I/O
0	IO_L29P_0	A12	I/O
0	IO_L30N_0	C12	I/O
0	IO_L30P_0	D13	I/O
0	IO_L31N_0	F12	I/O
0	IO_L31P_0	E12	I/O
0	IO_L32N_0/VREF_0	D11	VREF
0	IO_L32P_0	C11	I/O
0	IO_L33N_0	B10	I/O
0	IO_L33P_0	A10	I/O

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
2	IO_L16N_2	W12	I/O
2	IO_L16P_2	V12	I/O
2	IO_L17N_2/VS2	AA12	DUAL
2	IO_L17P_2/RDWR_B	Y12	DUAL
2	IO_L18N_2	AF8	I/O
2	IO_L18P_2	AE8	I/O
2	IO_L19N_2/VS0	AF9	DUAL
2	IO_L19P_2/VS1	AE9	DUAL
2	IO_L20N_2	W13	I/O
2	IO_L20P_2	V13	I/O
2	IO_L21N_2	AC12	I/O
2	IO_L21P_2	AB12	I/O
2	IO_L22N_2/D6	AF10	DUAL
2	IO_L22P_2/D7	AE10	DUAL
2	IO_L23N_2	AC11	I/O
2	IO_L23P_2	AD11	I/O
2	IO_L24N_2/D4	AE12	DUAL
2	IO_L24P_2/D5	AF12	DUAL
2	IO_L25N_2/GCLK13	Y13	GCLK
2	IO_L25P_2/GCLK12	AA13	GCLK
2	IO_L26N_2/GCLK15	AE13	GCLK
2	IO_L26P_2/GCLK14	AF13	GCLK
2	IO_L27N_2/GCLK1	AA14	GCLK
2	IO_L27P_2/GCLK0	Y14	GCLK
2	IO_L28N_2/GCLK3	AE14	GCLK
2	IO_L28P_2/GCLK2	AF14	GCLK
2	IO_L29N_2	AC14	I/O
2	IO_L29P_2	AD14	I/O
2	IO_L30N_2/MOSI/CSI_B	AB15	DUAL
2	IO_L30P_2	AC15	I/O
2	IO_L31N_2	W15	I/O
2	IO_L31P_2	V14	I/O
2	IO_L32N_2/DOUT	AE15	DUAL
2	IO_L32P_2/AWAKE	AD15	PWR MGMT
2	IO_L33N_2	AD17	I/O
2	IO_L33P_2	AE17	I/O
2	IO_L34N_2/D3	Y15	DUAL
2	IO_L34P_2/INIT_B	AA15	DUAL
2	IO_L35N_2	U15	I/O

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
2	IO_L35P_2	V15	I/O
2	IO_L36N_2/D1	AE18	DUAL
2	IO_L36P_2/D2	AF18	DUAL
2	IO_L37N_2	AE19	I/O
2	IO_L37P_2	AF19	I/O
2	IO_L38N_2	AB16	I/O
2	IO_L38P_2	AC16	I/O
2	IO_L39N_2	AE20	I/O
2	IO_L39P_2	AF20	I/O
2	IO_L40N_2	AC19	I/O
2	IO_L40P_2	AD19	I/O
2	IO_L41N_2	AC20	I/O
2	IO_L41P_2	AD20	I/O
2	IO_L42N_2	U16	I/O
2	IO_L42P_2	V16	I/O
2	IO_L43N_2	Y17	I/O
2	IO_L43P_2	AA17	I/O
2	IO_L44N_2	AD21	I/O
2	IO_L44P_2	AE21	I/O
2	IO_L45N_2	AC21	I/O
2	IO_L45P_2	AD22	I/O
2	IO_L46N_2	V17	I/O
2	IO_L46P_2	W17	I/O
2	IO_L47N_2	AA18	I/O
2	IO_L47P_2	AB18	I/O
2	IO_L48N_2	AE23	I/O
2	IO_L48P_2	AF23	I/O
2	IO_L51N_2	AE25	I/O
2	IO_L51P_2	AF25	I/O
2	IO_L52N_2/CCLK	AE24	DUAL
2	IO_L52P_2/D0/DIN/MISO	AF24	DUAL
2	IP_2	AA19	INPUT
2	IP_2	AB13	INPUT
2	IP_2	AB17	INPUT
2	IP_2	AB20	INPUT
2	IP_2	AC7	INPUT
2	IP_2	AC13	INPUT
2	IP_2	AC17	INPUT
2	IP_2	AC18	INPUT
2	IP_2	AD9	INPUT