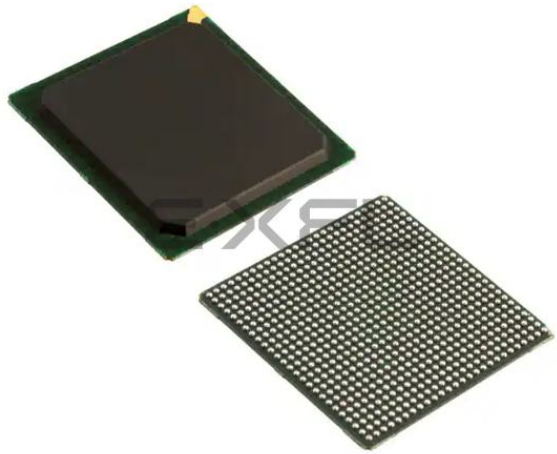

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Details	
Product Status	Active
Number of LABs/CLBs	2816
Number of Logic Elements/Cells	25344
Total RAM Bits	589824
Number of I/O	502
Number of Gates	1400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1400a-4fgg676i

Production Status

Table 3 indicates the production status of each Spartan-3A FPGA by temperature range and speed grade. The table also lists the earliest speed file version required for creating a production configuration bitstream. Later versions are also supported.

Table 3: **Spartan-3A FPGA Production Status (Production Speed File)**

Temperature Range		Commercial (C)		Industrial
Speed Grade		Standard (–4)	High-Performance (–5)	Standard (–4)
Part Number	XC3S50A	**Production** (v1.35)	**Production** (v1.35)	**Production** (v1.35)
	XC3S200A	**Production** (v1.35)	**Production** (v1.35)	**Production** (v1.35)
	XC3S400A	**Production** (v1.36)	**Production** (v1.36)	**Production** (v1.36)
	XC3S700A	**Production** (v1.34)	**Production** (v1.35)	**Production** (v1.34)
	XC3S1400A	**Production** (v1.34)	**Production** (v1.35)	**Production** (v1.34)

Package Marking

Figure 2 provides a top marking example for Spartan-3A FPGAs in the quad-flat packages. Figure 3 shows the top marking for Spartan-3A FPGAs in BGA packages. The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator.

The "5C" and "4I" Speed Grade/Temperature Range part combinations may be dual marked as "5C/4I". Devices with a single mark are only guaranteed for the marked speed grade and temperature range.

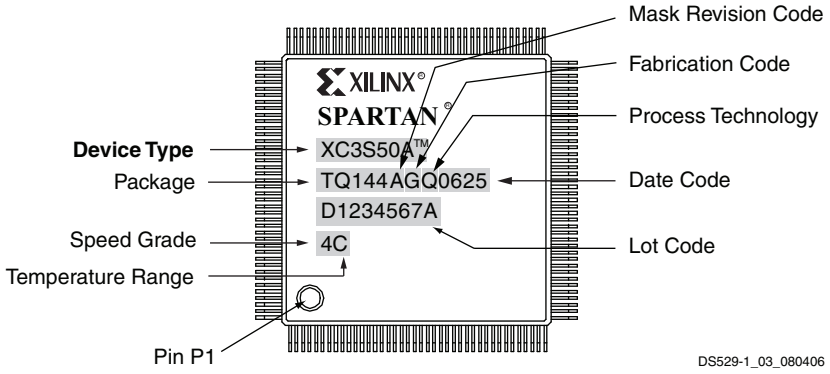

Figure 2: **Spartan-3A QFP Package Marking Example**

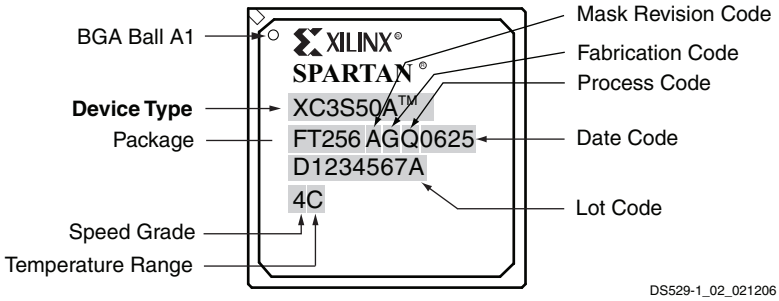

Figure 3: **Spartan-3A BGA Package Marking Example**

General DC Characteristics for I/O Pins

Table 9: **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins**(1)

Symbol	Description	Test Conditions		Min	Typ	Max	Units
I_L(2)	Leakage current at User I/O, input-only, dual-purpose, and dedicated pins, FPGA powered	Driver is in a high-impedance state, V_{IN} = 0V or V_{CCO} max, sample-tested		–10	–	+10	µA
I_{HS}	Leakage current on pins during hot socketing, FPGA unpowered	All pins except INIT_B, PROG_B, DONE, and JTAG pins when PUDC_B = 1.		–10	–	+10	µA
		INIT_B, PROG_B, DONE, and JTAG pins or other pins when PUDC_B = 0.		Add I_{HS} + I_{RPU}			µA
I_{RPU}(3)	Current through pull-up resistor at User I/O, dual-purpose, input-only, and dedicated pins. Dedicated pins are powered by V_{CCAUX}.	V_{IN} = GND	V_{CCO} or V_{CCAUX} = 3.0V to 3.6V	–151	–315	–710	µA
			V_{CCO} or V_{CCAUX} = 2.3V to 2.7V	–82	–182	–437	µA
			V_{CCO} = 1.7V to 1.9V	–36	–88	–226	µA
			V_{CCO} = 1.4V to 1.6V	–22	–56	–148	µA
			V_{CCO} = 1.14V to 1.26V	–11	–31	–83	µA
R_{PU}(3)	Equivalent pull-up resistor value at User I/O, dual-purpose, input-only, and dedicated pins (based on I_{RPU} per Note 3)	V_{IN} = GND	V_{CCO} = 3.0V to 3.6V	5.1	11.4	23.9	kΩ
			V_{CCO} = 2.3V to 2.7V	6.2	14.8	33.1	kΩ
			V_{CCO} = 1.7V to 1.9V	8.4	21.6	52.6	kΩ
			V_{CCO} = 1.4V to 1.6V	10.8	28.4	74.0	kΩ
			V_{CCO} = 1.14V to 1.26V	15.3	41.1	119.4	kΩ
I_{RPD}(3)	Current through pull-down resistor at User I/O, dual-purpose, input-only, and dedicated pins. Dedicated pins are powered by V_{CCAUX}.	V_{IN} = V_{CCO}	V_{CCAUX} = 3.0V to 3.6V	167	346	659	µA
			V_{CCAUX} = 2.25V to 2.75V	100	225	457	µA
R_{PD}(3)	Equivalent pull-down resistor value at User I/O, dual-purpose, input-only, and dedicated pins (based on I_{RPD} per Note 3)	V_{CCAUX} = 3.0V to 3.6V	V_{IN} = 3.0V to 3.6V	5.5	10.4	20.8	kΩ
			V_{IN} = 2.3V to 2.7V	4.1	7.8	15.7	kΩ
			V_{IN} = 1.7V to 1.9V	3.0	5.7	11.1	kΩ
			V_{IN} = 1.4V to 1.6V	2.7	5.1	9.6	kΩ
			V_{IN} = 1.14V to 1.26V	2.4	4.5	8.1	kΩ
		V_{CCAUX} = 2.25V to 2.75V	V_{IN} = 3.0V to 3.6V	7.9	16.0	35.0	kΩ
			V_{IN} = 2.3V to 2.7V	5.9	12.0	26.3	kΩ
			V_{IN} = 1.7V to 1.9V	4.2	8.5	18.6	kΩ
			V_{IN} = 1.4V to 1.6V	3.6	7.2	15.7	kΩ
			V_{IN} = 1.14V to 1.26V	3.0	6.0	12.5	kΩ
I_{REF}	V_{REF} current per pin	All V_{CCO} levels		–10	–	+10	µA
C_{IN}	Input capacitance	–		–	–	10	pF
R_{DT}	Resistance of optional differential termination circuit within a differential I/O pair. Not available on Input-only pairs.	V_{CCO} = 3.3V ± 10%	LVDS_33, MINI_LVDS_33, RSDS_33	90	100	115	Ω
		V_{CCO} = 2.5V ± 10%	LVDS_25, MINI_LVDS_25, RSDS_25	90	110	–	Ω

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8.
2. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See "Parasitic Leakage" in UG331, *Spartan-3 Generation FPGA User Guide*.
3. This parameter is based on characterization. The pull-up resistance R_{PU} = V_{CCO} / I_{RPU}. The pull-down resistance R_{PD} = V_{IN} / I_{RPD}.

Quiescent Current Requirements

Table 10: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Typical(2)	Commercial Maximum(2)	Industrial Maximum(2)	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC3S50A	2	20	30	mA
		XC3S200A	7	50	70	mA
		XC3S400A	10	85	125	mA
		XC3S700A	13	120	185	mA
		XC3S1400A	24	220	310	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC3S50A	0.2	2	3	mA
		XC3S200A	0.2	2	3	mA
		XC3S400A	0.3	3	4	mA
		XC3S700A	0.3	3	4	mA
		XC3S1400A	0.3	3	4	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC3S50A	3	8	10	mA
		XC3S200A	5	12	15	mA
		XC3S400A	5	18	24	mA
		XC3S700A	6	28	34	mA
		XC3S1400A	10	50	58	mA

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8.
2. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using typical devices at room temperature (T_J of 25°C at V_{CCINT} = 1.2V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.6V, and V_{CCAUX} = 3.6V. The FPGA is programmed with a "blank" configuration data file (that is, a design with no functional elements instantiated). For conditions other than those described above (for example, a design including functional elements), measured quiescent current levels will be different than the values in the table.
3. For more accurate estimates for a specific design, use the Xilinx XPower tools. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3A FPGA XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer uses a netlist as input to provide maximum estimates as well as more accurate typical estimates.
4. The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.
5. For information on the power-saving Suspend mode, see XAPP480: *Using Suspend Mode in Spartan-3 Generation FPGAs*. Suspend mode typically saves 40% total power consumption compared to quiescent current.

Input Timing Adjustments

Table 23: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Single-Ended Standards			
LVTTL	0.62	0.62	ns
LVCMOS33	0.54	0.54	ns
LVCMOS25	0	0	ns
LVCMOS18	0.83	0.83	ns
LVCMOS15	0.60	0.60	ns
LVCMOS12	0.31	0.31	ns
PCI33_3	0.41	0.41	ns
PCI66_3	0.41	0.41	ns
HSTL_I	0.72	0.72	ns
HSTL_III	0.77	0.77	ns
HSTL_I_18	0.69	0.69	ns
HSTL_II_18	0.69	0.69	ns
HSTL_III_18	0.79	0.79	ns
SSTL18_I	0.71	0.71	ns
SSTL18_II	0.71	0.71	ns
SSTL2_I	0.68	0.68	ns
SSTL2_II	0.68	0.68	ns
SSTL3_I	0.78	0.78	ns
SSTL3_II	0.78	0.78	ns

Table 23: **Input Timing Adjustments by IOSTANDARD*(Continued)***

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Differential Standards			
LVDS_25	0.76	0.76	ns
LVDS_33	0.79	0.79	ns
BLVDS_25	0.79	0.79	ns
MINI_LVDS_25	0.78	0.78	ns
MINI_LVDS_33	0.79	0.79	ns
LVPECL_25	0.78	0.78	ns
LVPECL_33	0.79	0.79	ns
RSDS_25	0.79	0.79	ns
RSDS_33	0.77	0.77	ns
TMDS_33	0.79	0.79	ns
PPDS_25	0.79	0.79	ns
PPDS_33	0.79	0.79	ns
DIFF_HSTL_I_18	0.74	0.74	ns
DIFF_HSTL_II_18	0.72	0.72	ns
DIFF_HSTL_III_18	1.05	1.05	ns
DIFF_HSTL_I	0.72	0.72	ns
DIFF_HSTL_III	1.05	1.05	ns
DIFF_SSTL18_I	0.71	0.71	ns
DIFF_SSTL18_II	0.71	0.71	ns
DIFF_SSTL2_I	0.74	0.74	ns
DIFF_SSTL2_II	0.75	0.75	ns
DIFF_SSTL3_I	1.06	1.06	ns
DIFF_SSTL3_II	1.06	1.06	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8, Table 11, and Table 13.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Table 28: **Equivalent V_{CCO}/GND Pairs per Bank**

Device	Package Style *(including Pb-free)*						
	VQ100	TQ144	FT256	FG320	FG400	FG484	FG676
XC3S50A	1	2	3	–	–	–	–
XC3S200A	1	–	4	4	–	–	–
XC3S400A	–	–	4	4	5	–	–
XC3S700A	–	–	4	–	5	5	–
XC3S1400A	–	–	4	–	–	6	9

Table 29: **Recommended Number of Simultaneously Switching Outputs per VCCO-GND Pair (V_{CCAUX}=3.3V)**

Signal Standard (IOSTANDARD)			Package Type			
			VQ100, TQ144		FT256, FG320, FG400, FG484, FG676	
			Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)
Single-Ended Standards						
LVTTL	Slow	2	20	20	60	60
		4	10	10	41	41
		6	10	10	29	29
		8	6	6	22	22
		12	6	6	13	13
		16	5	5	11	11
		24	4	4	9	9
	Fast	2	10	10	10	10
		4	6	6	6	6
		6	5	5	5	5
		8	3	3	3	3
		12	3	3	3	3
		16	3	3	3	3
		24	2	2	2	2
	QuietIO	2	40	40	80	80
		4	24	24	48	48
		6	20	20	36	36
		8	16	16	27	27
		12	12	12	16	16
		16	9	9	13	13
		24	9	9	12	12

Table 29: **Recommended Number of Simultaneously Switching Outputs per VCCO-GND Pair (V_{CCAUX}=3.3V)*(Continued)***

Signal Standard (IOSTANDARD)			Package Type			
			VQ100, TQ144		FT256, FG320, FG400, FG484, FG676	
			Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)
LVCMOS33	Slow	2	24	24	76	76
		4	14	14	46	46
		6	11	11	27	27
		8	10	10	20	20
		12	9	9	13	13
		16	8	8	10	10
		24	–	8	–	9
	Fast	2	10	10	10	10
		4	8	8	8	8
		6	5	5	5	5
		8	4	4	4	4
		12	4	4	4	4
		16	2	2	2	2
		24	–	2	–	2
	QuietIO	2	36	36	76	76
		4	32	32	46	46
		6	24	24	32	32
		8	16	16	26	26
		12	16	16	18	18
		16	12	12	14	14
		24	–	10	–	10

18 x 18 Embedded Multiplier Timing

Table 34: **18 x 18 Embedded Multiplier Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Combinatorial Delay						
T_{MULT}	Combinational multiplier propagation delay from the A and B inputs to the P outputs, assuming 18-bit inputs and a 36-bit product (AREG, BREG, and PREG registers unused)	–	4.36	–	4.88	ns
Clock-to-Output Times						
T_{MSCKP_P}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using the PREG register(2,3)	–	0.84	–	1.30	ns
T_{MSCKP_A} T_{MSCKP_B}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using either the AREG or BREG register(2,4)	–	4.44	–	4.97	ns
Setup Times						
T_{MSDCK_P}	Data setup time at the A or B input before the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused)(3)	3.56	–	3.98	–	ns
T_{MSDCK_A}	Data setup time at the A input before the active transition at the CLK when using the AREG input register(4)	0.00	–	0.00	–	ns
T_{MSDCK_B}	Data setup time at the B input before the active transition at the CLK when using the BREG input register(4)	0.00	–	0.00	–	ns
Hold Times						
T_{MSCKD_P}	Data hold time at the A or B input after the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused)(3)	0.00	–	0.00	–	ns
T_{MSCKD_A}	Data hold time at the A input after the active transition at the CLK when using the AREG input register(4)	0.35	–	0.45	–	ns
T_{MSCKD_B}	Data hold time at the B input after the active transition at the CLK when using the BREG input register(4)	0.35	–	0.45	–	ns
Clock Frequency						
F_{MULT}	Internal operating frequency for a two-stage 18x18 multiplier using the AREG and BREG input registers and the PREG output register(1)	0	280	0	250	MHz

Notes:

1. Combinational delay is less and pipelined performance is higher when multiplying input data with less than 18 bits.
2. The PREG register is typically used in both single-stage and two-stage pipelined multiplier implementations.
3. The PREG register is typically used when inferring a single-stage multiplier.
4. Input registers AREG or BREG are typically used when inferring a two-stage multiplier.
5. The numbers in this table are based on the operating conditions set forth in Table 8.

Digital Frequency Synthesizer (DFS)

Table 38: **Recommended Operating Conditions for the DFS**

Symbol		Description		Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges(2)								
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input		0.200	333(4)	0.200	333(4)	MHz
Input Clock Jitter Tolerance(3)								
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency	$F_{CLKFX} \leq 150$ MHz	–	±300	–	±300	ps
CLKIN_CYC_JITT_FX_HF			$F_{CLKFX} > 150$ MHz	–	±150	–	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input		–	±1	–	±1	ns

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 36.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.
4. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM.

Table 39: **Switching Characteristics for the DFS**

Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_FX(2)	Frequency for the CLKFX and CLKFX180 outputs		All	5	350	5	320	MHz
Output Clock Jitter(3,4)								
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.		All	**Typ**	**Max**	**Typ**	**Max**	
		CLKIN ≤ 20 MHz		Use the Spartan-3A Jitter Calculator: www.xilinx.com/support/documentation/data_sheets/s3a_jitter_calc.zip				ps
		CLKIN > 20 MHz		±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	ps
Duty Cycle(5,6)								
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	–	±[1% of CLKFX period + 350]	–	±[1% of CLKFX period + 350]	ps
Phase Alignment(6)								
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used		All	–	±200	–	±200	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used		All	–	±[1% of CLKFX period + 200]	–	±[1% of CLKFX period + 200]	ps

Table 39: **Switching Characteristics for the DFS*(Continued)***

Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Lock Time								
LOCK_FX[2, 3]	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. If using both the DLL and the DFS, use the longer locking time.	5 MHz ≤ F_{CLKIN} ≤ 15 MHz	All	–	5	–	5	ms
		F_{CLKIN} > 15 MHz		–	450	–	450	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8 and Table 38.
2. DFS performance requires the additional logic automatically added by ISE 9.1i and later software revisions.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Maximum output jitter is characterized within a reasonable noise environment (150 ps input period jitter, 40 SSOs and 25% CLB switching) on an XC3S1400A FPGA. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply and PCB design. The actual maximum output jitter depends on the system application.
5. The CLKFX and CLKFX180 outputs always have an approximate 50% duty cycle.
6. Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, the data sheet specifies a maximum CLKFX jitter of "±[1% of CLKFX period + 200]". Assume the CLKFX output frequency is 100 MHz. The equivalent CLKFX period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 200 ps] = ±300 ps.

Miscellaneous DCM Timing

Table 42: **Miscellaneous DCM Timing**

Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN	Minimum duration of a RST pulse width	3	–	CLKIN cycles
DCM_RST_PW_MAX(2)	Maximum duration of a RST pulse width	N/A	N/A	seconds
		N/A	N/A	seconds
DCM_CONFIG_LAG_TIME(3)	Maximum duration from V_{CCINT} applied to FPGA configuration successfully completed (DONE pin goes High) and clocks applied to DCM DLL	N/A	N/A	minutes
		N/A	N/A	minutes

Notes:

1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFX180) are unaffected.
2. This specification is equivalent to the Virtex®-4 DCM_RESET specification. This specification does not apply for Spartan-3A FPGAs.
3. This specification is equivalent to the Virtex-4 TCONFIG specification. This specification does not apply for Spartan-3A FPGAs.

DNA Port Timing

Table 43: **DNA_PORT Interface Timing**

Symbol	Description	Min	Max	Units
T_{DNASSU}	Setup time on SHIFT before the rising edge of CLK	1.0	–	ns
T_{DNASH}	Hold time on SHIFT after the rising edge of CLK	0.5	–	ns
T_{DNADSU}	Setup time on DIN before the rising edge of CLK	1.0	–	ns
T_{DNADH}	Hold time on DIN after the rising edge of CLK	0.5	–	ns
T_{DNARSU}	Setup time on READ before the rising edge of CLK	5.0	10,000	ns
T_{DNARH}	Hold time on READ after the rising edge of CLK	0	–	ns
$T_{DNADCKO}$	Clock-to-output delay on DOUT after rising edge of CLK	0.5	1.5	ns
$T_{DNACLKF}$	CLK frequency	0	100	MHz
$T_{DNACLKH}$	CLK High time	1.0	∞	ns
$T_{DNACLKL}$	CLK Low time	1.0	∞	ns

Notes:

1. The minimum READ pulse width is 5 ns, the maximum READ pulse width is 10 µs.
2. The numbers in this table are based on the operating conditions set forth in Table 8.

Master Serial and Slave Serial Mode Timing

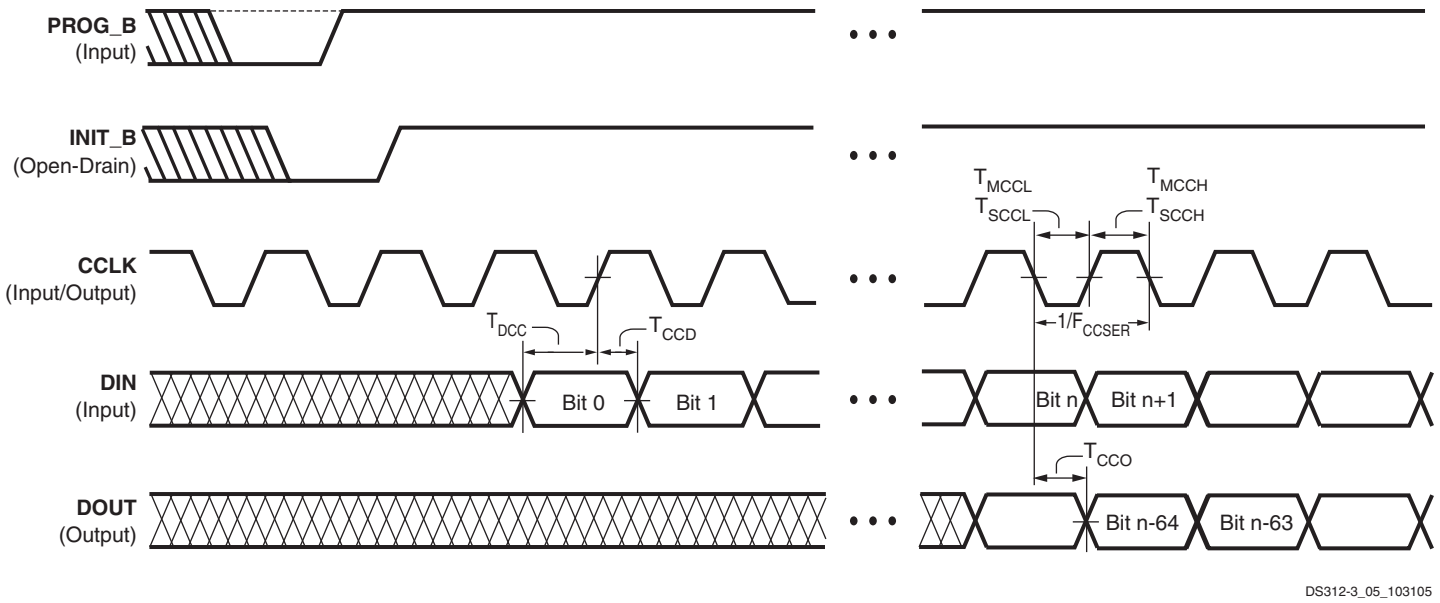

Figure 12: **Waveforms for Master Serial and Slave Serial Configuration**

Table 50: **Timing for the Master Serial and Slave Serial Configuration Modes**

Symbol	Description		Slave/ Master	All Speed Grades		Units
				Min	Max	
Clock-to-Output Times						
T_{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin		Both	1.5	10	ns
Setup Times						
T_{DCC}	The time from the setup of data at the DIN pin to the rising transition at the CCLK pin		Both	7	–	ns
Hold Times						
T_{CCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin		Master	0	–	ns
			Slave	1.0		
Clock Timing						
T_{CCH}	High pulse width at the CCLK input pin		Master	See Table 48		
			Slave	See Table 49		
T_{CCL}	Low pulse width at the CCLK input pin		Master	See Table 48		
			Slave	See Table 49		
F_{CCSER}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	Slave	0	100	MHz
		With bitstream compression		0	100	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Table 57: **Types of Pins on Spartan-3A FPGAs *(Continued)***

Type / Color Code	Description	Pin Name(s) in Type
PWR MGMT	Control and status pins for the power-saving Suspend mode. SUSPEND is a dedicated pin and is powered by V_{CCAUX}. AWAKE is a dual-purpose pin. Unless Suspend mode is enabled in the application, AWAKE is available as a user-I/O pin.	SUSPEND, AWAKE
JTAG	Dedicated JTAG pin - 4 per device. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX.	TDI, TMS, TCK, TDO
GND	Dedicated ground pin. The number of GND pins depends on the package used. All must be connected.	GND
VCCAUX	Dedicated auxiliary power supply pin. The number of VCCAUX pins depends on the package used. All must be connected. V_{CCAUX} can be either 2.5V or 3.3V. Set on board and using CONFIG VCCAUX constraint.	VCCAUX
VCCINT	Dedicated internal core logic power supply pin. The number of VCCINT pins depends on the package used. All must be connected to +1.2V.	VCCINT
VCCO	Along with all the other VCCO pins in the same bank, this pin supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards. All must be connected.	VCCO_#
N.C.	This package pin is not connected in this specific device/package combination but may be connected in larger devices in the same package.	N.C.

Notes:

1. # = I/O bank number, an integer between 0 and 3.

Package Pins by Type

Each package has three separate voltage supply inputs—VCCINT, VCCAUX, and VCCO—and a common ground return, GND. The numbers of pins dedicated to these functions vary by package, as shown in Table 58.

Table 58: **Power and Ground Supply Pins by Package**

Package	VCCINT	VCCAUX	VCCO	GND
VQ100	4	3	6	13
TQ144	4	4	8	13
FT256 (50A/200A/400A)	6	4	16	28
FT256 (700A/1400A)	15	10	13	50
FG320	6	8	16	32
FG400	9	8	22	43
FG484	15	10	24	53
FG676	23	14	36	77

A majority of package pins are user-defined I/O or input pins. However, the numbers and characteristics of these I/O depend on the device type and the package in which it is available, as shown in Table 59. The table shows the maximum number of single-ended I/O pins available, assuming that all I/O-, INPUT-, DUAL-, VREF-, and CLK-type pins are used as general-purpose I/O. AWAKE is counted here as a dual-purpose I/O pin. Likewise, the table shows the maximum number of differential pin-pairs available on the package. Finally, the table shows how the total maximum user-I/Os are distributed by pin type, including the number of unconnected—N.C.—pins on the device.

Not all I/O standards are supported on all I/O banks. The left and right banks (I/O banks 1 and 3) support higher output drive current than the top and bottom banks (I/O banks 0 and 2). Similarly, true differential output standards, such as LVDS, RSDS, PPDS, miniLVDS, and TMDS, are only supported in the top or bottom banks (I/O banks 0 and 2). Inputs are unrestricted. For more details, see the chapter "*Using I/O Resources*" in UG331.

Package Overview

Table 60 shows the six low-cost, space-saving production package styles for the Spartan-3A family.

Table 60: **Spartan-3A Family Package Options**

Package	Leads	Type	Maximum I/O	Lead Pitch (mm)	Body Area (mm)	Height (mm)	Mass[1] (g)
VQ100 / VQG100	100	Very Thin Quad Flat Pack (VQFP)	68	0.5	14 x 14	1.20	0.6
TQ144 / TQG144	144	Thin Quad Flat Pack (TQFP)	108	0.5	20 x 20	1.60	1.4
FT256 / FTG256	256	Fine-pitch Thin Ball Grid Array (FBGA)	195	1.0	17 x 17	1.55	0.9
FG320 / FGG320	320	Fine-pitch Ball Grid Array (FBGA)	251	1.0	19 x 19	2.00	1.4
FG400 / FGG400	400	Fine-pitch Ball Grid Array (FBGA)	311	1.0	21 x 21	2.43	2.2
FG484 / FGG484	484	Fine-pitch Ball Grid Array (FBGA)	375	1.0	23 x 23	2.60	2.2
FG676 / FGG676	676	Fine-pitch Ball Grid Array (FBGA)	502	1.0	27 x 27	2.60	3.4

Notes:

1. Package mass is ±10%.

Each package style is available in an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra 'G' in the package style name. For example, the standard "CS484" package becomes "CSG484" when ordered as the Pb-free option. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 61.

For additional package information, see UG112: *Device Package User Guide*.

Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx web site at the specified location in Table 61.

Material Declaration Data Sheets (MDDS) are also available on the **Xilinx web site** for each package.

Table 61: **Xilinx Package Documentation**

Package	Drawing	MDDS
VQ100	Package Drawing	PK173_VQ100
VQG100		PK130_VQG100
TQ144	Package Drawing	PK169_TQ144
TQG144		PK126_TQG144
FT256	Package Drawing	PK158_FT256
FTG256		PK115_FTG256
FG320	Package Drawing	PK152_FG320
FGG320		PK106_FGG320
FG400	Package Drawing	PK182_FG400
FGG400		PK108_FGG400
FG484	Package Drawing	PK183_FG484
FGG484		PK110_FGG484
FG676	Package Drawing	PK155_FG676
FGG676		PK111_FGG676

VQ100: 100-lead Very Thin Quad Flat Package

The XC3S50A and XC3S200 are available in the 100-lead very thin quad flat package, VQ100.

Table 63 lists all the package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The VQ100 does not support Suspend mode (SUSPEND and AWAKE are not connected), the address output pins for the Byte-wide Peripheral Interface (BPI) configuration mode, or daisy chain configuration (DOUT is not connected).

Table 63 also indicates that some differential I/O pairs have different assignments between the XC3S50A and the XC3S200A, highlighted in light blue. See "Footprint Migration Differences," page 72 for additional information.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 63: **Spartan-3A VQ100 Pinout**

Bank	Pin Name	Pin	Type
0	IO_0/GCLK11	P90	CLK
0	IO_L01N_0	P78	IO
0	IO_L01P_0/VREF_0	P77	VREF
0	IO_L02N_0/GCLK5	P84	CLK
0	IO_L02P_0/GCLK4	P83	CLK
0	IO_L03N_0/GCLK7	P86	CLK
0	IO_L03P_0/GCLK6	P85	CLK
0	IO_L04N_0/GCLK9	P89	CLK
0	IO_L04P_0/GCLK8	P88	CLK
0	IO_L05N_0	P94	IO
0	IO_L05P_0	P93	IO
0	IO_L06N_0/PUDC_B	P99	DUAL
0	IO_L06P_0/VREF_0	P98	VREF
0	IP_0	P97	IP
0	IP_0/VREF_0	P82	VREF
0	VCCO_0	P79	VCCO
0	VCCO_0	P96	VCCO
1	IO_L01N_1	P57	IO
1	IO_L01P_1	P56	IO
1	IO_L02N_1/RHCLK1	P60	CLK
1	IO_L02P_1/RHCLK0	P59	CLK
1	IO_L03N_1/TRDY1/RHCLK3	P62	CLK
1	IO_L03P_1/RHCLK2	P61	CLK
1	IO_L04N_1/RHCLK7	P65	CLK
1	IO_L04P_1/IRDY1/RHCLK6	P64	CLK
1	IO_L05N_1	P71	IO
1	IO_L05P_1	P70	IO
1	IO_L06N_1	P73	IO
1	IO_L06P_1	P72	IO
1	IP_1/VREF_1	P68	VREF
1	VCCO_1	P67	VCCO
2	IO_2/MOSI/CSI_B	P46	DUAL
2	IO_L01N_2/M0	P25	DUAL
2	IO_L01P_2/M1	P23	DUAL
2	IO_L02N_2/CSO_B	P27	DUAL
2	IO_L02P_2/M2	P24	DUAL
2	IO_L03N_2/VS1 (3S50A) IO_L04P_2/VS1 (3S200A)	P30	DUAL
2	IO_L03P_2/RDWR_B	P28	DUAL
2	IO_L04N_2/VS0	P31	DUAL
2	IO_L04P_2/VS2 (3S50A) IO_L03N_2/VS2 (3S200A)	P29	DUAL
2	IO_L05N_2/D7 (3S50A) IO_L06P_2/D7 (3S200A)	P34	DUAL
2	IO_L05P_2	P32	IO
2	IO_L06N_2/D6	P35	DUAL
2	IO_L06P_2 (3S50A) IO_L05N_2 (3S200A)	P33	IO
2	IO_L07N_2/D4	P37	DUAL
2	IO_L07P_2/D5	P36	DUAL
2	IO_L08N_2/GCLK15	P41	CLK
2	IO_L08P_2/GCLK14	P40	CLK
2	IO_L09N_2/GCLK1	P44	CLK
2	IO_L09P_2/GCLK0	P43	CLK
2	IO_L10N_2/D3	P49	DUAL
2	IO_L10P_2/INIT_B	P48	DUAL
2	IO_L11N_2/D0/DIN/MISO (3S50A) IO_L12P_2/D0/DIN/MISO (3S200A)	P51	DUAL
2	IO_L11P_2/D2	P50	DUAL
2	IO_L12N_2/CCLK	P53	DUAL

Table 63: **Spartan-3A VQ100 Pinout*(Continued)***

2	IO_L12P_2/D1 (3S50A) IO_L11N_2/D1 (3S200A)	P52	DUAL
2	IP_2/VREF_2	P39	VREF
2	VCCO_2	P26	VCCO
2	VCCO_2	P45	VCCO
3	IO_L01N_3	P4	IO
3	IO_L01P_3	P3	IO
3	IO_L02N_3	P6	IO
3	IO_L02P_3	P5	IO
3	IO_L03N_3/LHCLK1	P10	CLK
3	IO_L03P_3/LHCLK0	P9	CLK
3	IO_L04N_3/IRDY2/LHCLK3	P13	CLK
3	IO_L04P_3/LHCLK2	P12	CLK
3	IO_L05N_3/LHCLK7	P16	CLK
3	IO_L05P_3/TRDY2/LHCLK6	P15	CLK
3	IO_L06N_3	P20	IO
3	IO_L06P_3	P19	IO
3	IP_3	P21	IP
3	IP_3/VREF_3	P7	VREF
3	VCCO_3	P11	VCCO
GND	GND	P14	GND
GND	GND	P18	GND
GND	GND	P42	GND
GND	GND	P47	GND
GND	GND	P58	GND
GND	GND	P63	GND
GND	GND	P69	GND
GND	GND	P74	GND
GND	GND	P8	GND
GND	GND	P80	GND
GND	GND	P87	GND
GND	GND	P91	GND
GND	GND	P95	GND
VCCAUX	DONE	P54	CONFIG
VCCAUX	PROG_B	P100	CONFIG
VCCAUX	TCK	P76	JTAG
VCCAUX	TDI	P2	JTAG
VCCAUX	TDO	P75	JTAG
VCCAUX	TMS	P1	JTAG
VCCAUX	VCCAUX	P22	VCCAUX
VCCAUX	VCCAUX	P55	VCCAUX
VCCAUX	VCCAUX	P92	VCCAUX

Table 63: **Spartan-3A VQ100 Pinout*(Continued)***

VCCINT	VCCINT	P17	VCCINT
VCCINT	VCCINT	P38	VCCINT
VCCINT	VCCINT	P66	VCCINT
VCCINT	VCCINT	P81	VCCINT

Table 68: **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400) *(Continued)***

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
0	IO_L17P_0	IO_L17P_0	A5	I/O
0	IO_L18N_0	IO_L18N_0	B4	I/O
0	IO_L18P_0	IO_L18P_0	A4	I/O
0	IO_L19N_0	IO_L19N_0	B3	I/O
0	IO_L19P_0	IO_L19P_0	A3	I/O
0	IO_L20N_0/ PUDC_B	IO_L20N_0/ PUDC_B	D5	DUAL
0	IO_L20P_0/ VREF_0	IO_L20P_0/ VREF_0	C4	VREF
0	IP_0	IP_0	D6	INPUT
0	IP_0	IP_0	D12	INPUT
0	IP_0	IP_0	E6	INPUT
0	IP_0	IP_0	F7	INPUT
0	IP_0	IP_0	F9	INPUT
0	IP_0	IP_0	F10	INPUT
0	IP_0/VREF_0	IP_0/VREF_0	E9	VREF
0	VCCO_0	VCCO_0	B5	VCCO
0	VCCO_0	VCCO_0	B9	VCCO
0	VCCO_0	VCCO_0	B13	VCCO
0	VCCO_0	VCCO_0	E8	VCCO
1	IO_L01N_1/ LDC2	IO_L01N_1/ LDC2	N14	DUAL
1	IO_L01P_1/ HDC	IO_L01P_1/ HDC	N13	DUAL
1	IO_L02N_1/ LDC0	IO_L02N_1/ LDC0	P15	DUAL
1	IO_L02P_1/ LDC1	IO_L02P_1/ LDC1	R15	DUAL
1	IO_L03N_1	IO_L03N_1/A1	N16	DUAL
1	IO_L03P_1	IO_L03P_1/A0	P16	DUAL
1	N.C. (◆)	IO_L05N_1/ VREF_1	M14	VREF
1	N.C. (◆)	IO_L05P_1	M13	I/O
1	N.C. (◆)	IO_L06N_1/A3	K13	DUAL
1	N.C. (◆)	IO_L06P_1/A2	L13	DUAL
1	N.C. (◆)	IO_L07N_1/A5	M16	DUAL
1	N.C. (◆)	IO_L07P_1/A4	M15	DUAL
1	N.C. (◆)	IO_L08N_1/A7	L16	DUAL
1	N.C. (◆)	IO_L08P_1/A6	L14	DUAL
1	IO_L10N_1	IO_L10N_1/A9	J13	DUAL
1	IO_L10P_1	IO_L10P_1/A8	J12	DUAL
1	IO_L11N_1/ RHCLK1	IO_L11N_1/ RHCLK1	K14	RHCLK
1	IO_L11P_1/ RHCLK0	IO_L11P_1/ RHCLK0	K15	RHCLK

Table 68: **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400) *(Continued)***

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
1	IO_L12N_1/ TRDY1/RHCLK3	IO_L12N_1/ TRDY1/RHCLK3	J16	RHCLK
1	IO_L12P_1/ RHCLK2	IO_L12P_1/ RHCLK2	K16	RHCLK
1	IO_L14N_1/ RHCLK5	IO_L14N_1/ RHCLK5	H14	RHCLK
1	IO_L14P_1/ RHCLK4	IO_L14P_1/ RHCLK4	J14	RHCLK
1	IO_L15N_1/ RHCLK7	IO_L15N_1/ RHCLK7	H16	RHCLK
1	IO_L15P_1/ IRDY1/RHCLK6	IO_L15P_1/ IRDY1/RHCLK6	H15	RHCLK
1	N.C. (◆)	IO_L16N_1/A11	F16	DUAL
1	N.C. (◆)	IO_L16P_1/A10	G16	DUAL
1	N.C. (◆)	IO_L17N_1/A13	G14	DUAL
1	N.C. (◆)	IO_L17P_1/A12	H13	DUAL
1	N.C. (◆)	IO_L18N_1/A15	F15	DUAL
1	N.C. (◆)	IO_L18P_1/A14	E16	DUAL
1	N.C. (◆)	IO_L19N_1/A17	F14	DUAL
1	N.C. (◆)	IO_L19P_1/A16	G13	DUAL
1	IO_L20N_1	IO_L20N_1/A19	F13	DUAL
1	IO_L20P_1	IO_L20P_1/A18	E14	DUAL
1	IO_L22N_1	IO_L22N_1/A21	D15	DUAL
1	IO_L22P_1	IO_L22P_1/A20	D16	DUAL
1	IO_L23N_1	IO_L23N_1/A23	D14	DUAL
1	IO_L23P_1	IO_L23P_1/A22	E13	DUAL
1	IO_L24N_1	IO_L24N_1/A25	C15	DUAL
1	IO_L24P_1	IO_L24P_1/A24	C16	DUAL
1	IP_L04N_1/ VREF_1	IP_L04N_1/ VREF_1	K12	VREF
1	IP_L04P_1	IP_L04P_1	K11	INPUT
1	N.C. (◆)	IP_L09N_1	J11	INPUT
1	N.C. (◆)	IP_L09P_1/ VREF_1	J10	VREF
1	IP_L13N_1	IP_L13N_1	H11	INPUT
1	IP_L13P_1	IP_L13P_1	H10	INPUT
1	IP_L21N_1	IP_L21N_1	G11	INPUT
1	IP_L21P_1/ VREF_1	IP_L21P_1/ VREF_1	G12	VREF
1	IP_L25N_1	IP_L25N_1	F11	INPUT
1	IP_L25P_1/ VREF_1	IP_L25P_1/ VREF_1	F12	VREF
1	VCCO_1	VCCO_1	E15	VCCO
1	VCCO_1	VCCO_1	H12	VCCO
1	VCCO_1	VCCO_1	J15	VCCO
1	VCCO_1	VCCO_1	N15	VCCO

Table 69: **Spartan-3A FT256 Pinout (XC3S700A,**

Bank	XC3S700A XC3S1400A	FT256 Ball	Type
VCCAUX	VCCAUX	F5	VCCAUX
VCCAUX	VCCAUX	H14	VCCAUX
VCCAUX	VCCAUX	H4	VCCAUX
VCCAUX	VCCAUX	L12	VCCAUX
VCCAUX	VCCAUX	L5	VCCAUX
VCCAUX	VCCAUX	M10	VCCAUX
VCCAUX	VCCAUX	M6	VCCAUX
VCCINT	VCCINT	F10	VCCINT
VCCINT	VCCINT	G11	VCCINT
VCCINT	VCCINT	G7	VCCINT
VCCINT	VCCINT	G9	VCCINT
VCCINT	VCCINT	H10	VCCINT
VCCINT	VCCINT	H6	VCCINT
VCCINT	VCCINT	H8	VCCINT
VCCINT	VCCINT	J11	VCCINT
VCCINT	VCCINT	J7	VCCINT
VCCINT	VCCINT	J9	VCCINT
VCCINT	VCCINT	K10	VCCINT
VCCINT	VCCINT	K6	VCCINT
VCCINT	VCCINT	K8	VCCINT
VCCINT	VCCINT	L7	VCCINT
VCCINT	VCCINT	L9	VCCINT

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
2	IO_L02N_2/CSO_B	V3	DUAL
2	IO_L02P_2/M2	V2	DUAL
2	IO_L03N_2/VS2	U4	DUAL
2	IO_L03P_2/RDWR_B	T4	DUAL
2	IO_L04N_2	T5	I/O
2	IO_L04P_2	R5	I/O
2	IO_L05N_2/VS0	V5	DUAL
2	IO_L05P_2/VS1	V4	DUAL
2	IO_L06N_2	U6	I/O
2	IO_L06P_2	T6	I/O
2	IO_L07N_2	P8	I/O
2	IO_L07P_2	N8	I/O
2	IO_L08N_2/D6	T7	DUAL
2	IO_L08P_2/D7	R7	DUAL
2	IO_L09N_2	R9	I/O
2	IO_L09P_2	T8	I/O
2	IO_L10N_2/D4	V6	DUAL
2	IO_L10P_2/D5	U7	DUAL
2	IO_L11N_2/GCLK13	V8	GCLK
2	IO_L11P_2/GCLK12	U8	GCLK
2	IO_L12N_2/GCLK15	V9	GCLK
2	IO_L12P_2/GCLK14	U9	GCLK
2	IO_L13N_2/GCLK1	T10	GCLK
2	IO_L13P_2/GCLK0	U10	GCLK
2	IO_L14N_2/GCLK3	U11	GCLK
2	IO_L14P_2/GCLK2	V11	GCLK
2	IO_L15N_2	R10	I/O
2	IO_L15P_2	P10	I/O
2	IO_L16N_2/MOSI/CSI_B	T11	DUAL
2	IO_L16P_2	R11	I/O
2	IO_L17N_2	V13	I/O
2	IO_L17P_2	U12	I/O
2	IO_L18N_2/DOUT	U13	DUAL
2	IO_L18P_2/AWAKE	T12	PWR MGMT
2	IO_L19N_2	P12	I/O
2	IO_L19P_2	N12	I/O
2	IO_L20N_2/D3	R13	DUAL
2	IO_L20P_2/INIT_B	T13	DUAL
2	IO_L21N_2	T14	I/O

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
2	IO_L21P_2	V14	I/O
2	IO_L22N_2/D1	U15	DUAL
2	IO_L22P_2/D2	V15	DUAL
2	IO_L23N_2	T15	I/O
2	IO_L23P_2	R14	I/O
2	IO_L24N_2/CCLK	U16	DUAL
2	IO_L24P_2/D0/DIN/MISO	V16	DUAL
2	IP_2	M8	INPUT
2	IP_2	M9	INPUT
2	IP_2	M12	INPUT
2	***XC3S400A:*** IP_2 ***XC3S200A:*** N.C. (◆)	N7	INPUT
2	IP_2	N9	INPUT
2	IP_2	N11	INPUT
2	IP_2	R6	INPUT
2	IP_2/VREF_2	M11	VREF
2	IP_2/VREF_2	N10	VREF
2	IP_2/VREF_2	P6	VREF
2	IP_2/VREF_2	P7	VREF
2	IP_2/VREF_2	P9	VREF
2	IP_2/VREF_2	P13	VREF
2	***XC3S400A:*** IP_2/VREF_2 ***XC3S200A:*** N.C. (◆)	P14	VREF
2	VCCO_2	P11	VCCO
2	VCCO_2	R8	VCCO
2	VCCO_2	U5	VCCO
2	VCCO_2	U14	VCCO
3	IO_L01N_3	C1	I/O
3	IO_L01P_3	C2	I/O
3	IO_L02N_3	B1	I/O
3	IO_L02P_3	B2	I/O
3	IO_L03N_3	D2	I/O
3	IO_L03P_3	D3	I/O
3	IO_L05N_3	G5	I/O
3	IO_L05P_3	F5	I/O
3	IO_L06N_3	E3	I/O
3	IO_L06P_3	F4	I/O
3	IO_L07N_3	E1	I/O
3	IO_L07P_3	D1	I/O
3	IO_L09N_3	G4	I/O
3	IO_L09P_3	F3	I/O

Right Half of FG484 Package (Top View)

Figure 26:

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
2	IP_2	AD10	INPUT
2	IP_2	AD16	INPUT
2	IP_2	AF2	INPUT
2	IP_2	AF7	INPUT
2	IP_2	Y11	INPUT
2	IP_2/VREF_2	AA9	VREF
2	IP_2/VREF_2	AA20	VREF
2	IP_2/VREF_2	AB6	VREF
2	IP_2/VREF_2	AB10	VREF
2	IP_2/VREF_2	AC10	VREF
2	IP_2/VREF_2	AD12	VREF
2	IP_2/VREF_2	AF15	VREF
2	IP_2/VREF_2	AF17	VREF
2	IP_2/VREF_2	AF22	VREF
2	IP_2/VREF_2	Y16	VREF
2	N.C. (◆)	AA8	N.C.
2	N.C. (◆)	AC5	N.C.
2	N.C. (◆)	AC22	N.C.
2	N.C. (◆)	AD5	N.C.
2	N.C. (◆)	Y18	N.C.
2	N.C. (◆)	Y19	N.C.
2	N.C. (◆)	AD23	N.C.
2	N.C. (◆)	W18	N.C.
2	N.C. (◆)	Y8	N.C.
2	VCCO_2	AB8	VCCO
2	VCCO_2	AB14	VCCO
2	VCCO_2	AB19	VCCO
2	VCCO_2	AE5	VCCO
2	VCCO_2	AE11	VCCO
2	VCCO_2	AE16	VCCO
2	VCCO_2	AE22	VCCO
2	VCCO_2	W11	VCCO
2	VCCO_2	W16	VCCO
3	IO_L01N_3	J9	I/O
3	IO_L01P_3	J8	I/O
3	IO_L02N_3	B1	I/O
3	IO_L02P_3	B2	I/O
3	IO_L03N_3	H7	I/O
3	IO_L03P_3	G6	I/O
3	IO_L05N_3	K8	I/O

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
3	IO_L05P_3	K9	I/O
3	IO_L06N_3	E4	I/O
3	IO_L06P_3	D3	I/O
3	IO_L07N_3	F4	I/O
3	IO_L07P_3	E3	I/O
3	IO_L09N_3	G4	I/O
3	IO_L09P_3	F5	I/O
3	IO_L10N_3	H6	I/O
3	IO_L10P_3	J7	I/O
3	IO_L11N_3	F2	I/O
3	IO_L11P_3	E1	I/O
3	IO_L13N_3	J6	I/O
3	IO_L13P_3	K7	I/O
3	IO_L14N_3	F3	I/O
3	IO_L14P_3	G3	I/O
3	IO_L15N_3	L9	I/O
3	IO_L15P_3	L10	I/O
3	IO_L17N_3	H1	I/O
3	IO_L17P_3	H2	I/O
3	IO_L18N_3	L7	I/O
3	IO_L18P_3	K6	I/O
3	IO_L19N_3	J4	I/O
3	IO_L19P_3	J5	I/O
3	IO_L21N_3	M9	I/O
3	IO_L21P_3	M10	I/O
3	IO_L22N_3	K4	I/O
3	IO_L22P_3	K5	I/O
3	IO_L23N_3	K2	I/O
3	IO_L23P_3	K3	I/O
3	IO_L25N_3	L3	I/O
3	IO_L25P_3	L4	I/O
3	IO_L26N_3	M7	I/O
3	IO_L26P_3	M8	I/O
3	IO_L27N_3	M3	I/O
3	IO_L27P_3	M4	I/O
3	IO_L28N_3	M6	I/O
3	IO_L28P_3	M5	I/O
3	IO_L29N_3/VREF_3	M1	VREF
3	IO_L29P_3	M2	I/O
3	IO_L30N_3	N4	I/O