# AMD Xilinx - XC3S1400A-5FTG256C Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 2816 |
| Number of Logic Elements/Cells | 25344 |
| Total RAM Bits | 589824 |
| Number of I/O | 161 |
| Number of Gates | 1400000 |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FTBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc3s1400a-5ftg256c |

## Spartan-3A FPGA Design Documentation

The functionality of the Spartan®-3A FPGA Family is described in the following documents. The topics covered in each guide is listed below.

- **DS706: Extended Spartan-3A Family Overview**
  www.xilinx.com/support/documentation/data_sheets/ds706.pdf
- **UG331: Spartan-3 Generation FPGA User Guide**
  www.xilinx.com/support/documentation/user_guides/ug331.pdf
  - Clocking Resources
  - Digital Clock Managers (DCMs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
    - Distributed RAM
    - SRL16 Shift Registers
    - Carry and Arithmetic Logic
  - I/O Resources
  - Embedded Multiplier Blocks
  - Programmable Interconnect
  - ISE® Software Design Tools
  - IP Cores
  - Embedded Processing and Control Solutions
  - Pin Types and Package Overview
  - Package Drawings
  - Powering FPGAs
  - Power Management
- **UG332: Spartan-3 Generation Configuration User Guide**
  www.xilinx.com/support/documentation/user_guides/ug332.pdf
  - Configuration Overview
    - Configuration Pins and Behavior
    - Bitstream Sizes
  - Detailed Descriptions by Mode
    - Master Serial Mode using Xilinx® Platform Flash PROM
    - Master SPI Mode using Commodity SPI Serial Flash PROM
    - Master BPI Mode using Commodity Parallel NOR Flash PROM
    - Slave Parallel (SelectMAP) using a Processor
    - Slave Serial using a Processor
    - JTAG Mode
  - ISE iMPACT Programming Examples
  - MultiBoot Reconfiguration
  - Design Authentication using Device DNA

For application examples, see the Spartan-3A FPGA application notes.

- **Spartan-3A FPGA Application Notes**
  www.xilinx.com/support/documentation/spartan-3a_application_notes.htm

For specific hardware examples, please see the Spartan-3A FPGA Starter Kit board web page, which has links to various design examples and the user guide.

- **Spartan-3A/3AN FPGA Starter Kit Board Page**
  www.xilinx.com/s3astarter
- **UG334: Spartan-3A/3AN FPGA Starter Kit User Guide**
  www.xilinx.com/support/documentation/boards_and_kits/ug334.pdf

For information on the XA Automotive version of the Spartan-3A family, see the following data sheet.

- XA Spartan-3A Automotive FPGA Family Data Sheet
  www.xilinx.com/support/documentation/data_sheets/ds681.pdf

Create a Xilinx user account and sign up to receive automatic e-mail notification whenever this data sheet or the associated user guides are updated.

- Sign Up for Alerts
  www.xilinx.com/support/answers/18683.htm

*Table 22:* **Propagation Times for the IOB Input Path *(Continued)***

| Symbol | Description | Conditions | DELAY_VALUE | Device | Speed Grade | | Units |
|---|---|---|---|---|---|---|---|
| | | | | | -5 | -4 | |
| | | | | | Max | Max | |
| $T_{IOPID}$ | The time it takes for data to travel from the Input pin to the I output with the input delay programmed | LVCMOS25(2) | 15 | XC3S200A | 5.43 | 6.24 | ns |
| | | | 16 | | 5.75 | 6.59 | ns |
| | | | 1 | XC3S400A | 1.32 | 1.43 | ns |
| | | | 2 | | 1.67 | 1.83 | ns |
| | | | 3 | | 1.90 | 2.07 | ns |
| | | | 4 | | 2.33 | 2.52 | ns |
| | | | 5 | | 2.60 | 2.91 | ns |
| | | | 6 | | 2.94 | 3.20 | ns |
| | | | 7 | | 3.23 | 3.51 | ns |
| | | | 8 | | 3.50 | 3.85 | ns |
| | | | 9 | | 3.18 | 3.55 | ns |
| | | | 10 | | 3.53 | 3.95 | ns |
| | | | 11 | | 3.76 | 4.20 | ns |
| | | | 12 | | 4.26 | 4.67 | ns |
| | | | 13 | | 4.51 | 4.97 | ns |
| | | | 14 | | 4.85 | 5.32 | ns |
| | | | 15 | | 5.14 | 5.64 | ns |
| | | | 16 | | 5.40 | 5.95 | ns |
| | | | 1 | XC3S700A | 1.84 | 1.87 | ns |
| | | | 2 | | 2.20 | 2.27 | ns |
| | | | 3 | | 2.46 | 2.60 | ns |
| | | | 4 | | 2.93 | 3.15 | ns |
| | | | 5 | | 3.21 | 3.45 | ns |
| | | | 6 | | 3.54 | 3.80 | ns |
| | | | 7 | | 3.86 | 4.16 | ns |
| | | | 8 | | 4.13 | 4.48 | ns |
| | | | 9 | | 3.82 | 4.19 | ns |
| | | | 10 | | 4.17 | 4.58 | ns |
| | | | 11 | | 4.43 | 4.89 | ns |
| | | | 12 | | 4.95 | 5.49 | ns |
| | | | 13 | | 5.22 | 5.83 | ns |
| | | | 14 | | 5.57 | 6.21 | ns |
| | | | 15 | | 5.89 | 6.55 | ns |
| | | | 16 | | 6.16 | 6.89 | ns |
| | | | 1 | XC3S1400A | 1.95 | 2.18 | ns |
| | | | 2 | | 2.29 | 2.59 | ns |
| | | | 3 | | 2.54 | 2.84 | ns |
| | | | 4 | | 2.96 | 3.30 | ns |

## Output Timing Adjustments

*Table 26:* **Output Timing Adjustments for IOB**

| Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD) | | | Add the Adjustment Below | | Units |
|---|---|---|---|---|---|
| | | | Speed Grade | | |
| | | | -5 | -4 | |
| **Single-Ended Standards** | | | | | |
| LVTTL | Slow | 2 mA | 5.58 | 5.58 | ns |
| | | 4 mA | 3.16 | 3.16 | ns |
| | | 6 mA | 3.17 | 3.17 | ns |
| | | 8 mA | 2.09 | 2.09 | ns |
| | | 12 mA | 1.62 | 1.62 | ns |
| | | 16 mA | 1.24 | 1.24 | ns |
| | | 24 mA | 2.74(3) | 2.74(3) | ns |
| | Fast | 2 mA | 3.03 | 3.03 | ns |
| | | 4 mA | 1.71 | 1.71 | ns |
| | | 6 mA | 1.71 | 1.71 | ns |
| | | 8 mA | 0.53 | 0.53 | ns |
| | | 12 mA | 0.53 | 0.53 | ns |
| | | 16 mA | 0.59 | 0.59 | ns |
| | | 24 mA | 0.60 | 0.60 | ns |
| | QuietIO | 2 mA | 27.67 | 27.67 | ns |
| | | 4 mA | 27.67 | 27.67 | ns |
| | | 6 mA | 27.67 | 27.67 | ns |
| | | 8 mA | 16.71 | 16.71 | ns |
| | | 12 mA | 16.67 | 16.67 | ns |
| | | 16 mA | 16.22 | 16.22 | ns |
| | | 24 mA | 12.11 | 12.11 | ns |

*Table 26:* **Output Timing Adjustments for IOB*(Continued)***

| Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD) | | | Add the Adjustment Below | | Units |
|---|---|---|---|---|---|
| | | | Speed Grade | | |
| | | | -5 | -4 | |
| LVCMOS33 | Slow | 2 mA | 5.58 | 5.58 | ns |
| | | 4 mA | 3.17 | 3.17 | ns |
| | | 6 mA | 3.17 | 3.17 | ns |
| | | 8 mA | 2.09 | 2.09 | ns |
| | | 12 mA | 1.24 | 1.24 | ns |
| | | 16 mA | 1.15 | 1.15 | ns |
| | | 24 mA | 2.55(3) | 2.55(3) | ns |
| | Fast | 2 mA | 3.02 | 3.02 | ns |
| | | 4 mA | 1.71 | 1.71 | ns |
| | | 6 mA | 1.72 | 1.72 | ns |
| | | 8 mA | 0.53 | 0.53 | ns |
| | | 12 mA | 0.59 | 0.59 | ns |
| | | 16 mA | 0.59 | 0.59 | ns |
| | | 24 mA | 0.51 | 0.51 | ns |
| | QuietIO | 2 mA | 27.67 | 27.67 | ns |
| | | 4 mA | 27.67 | 27.67 | ns |
| | | 6 mA | 27.67 | 27.67 | ns |
| | | 8 mA | 16.71 | 16.71 | ns |
| | | 12 mA | 16.29 | 16.29 | ns |
| | | 16 mA | 16.18 | 16.18 | ns |
| | | 24 mA | 12.11 | 12.11 | ns |

## Block RAM Timing

*Table 35:* **Block RAM Timing**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -5 | | -4 | | |
| | | Min | Max | Min | Max | |
| **Clock-to-Output Times** | | | | | | |
| $T_{RCKO}$ | When reading from block RAM, the delay from the active transition at the CLK input to data appearing at the DOUT output | – | 2.06 | – | 2.49 | ns |
| **Setup Times** | | | | | | |
| $T_{RCCK\_ADDR}$ | Setup time for the ADDR inputs before the active transition at the CLK input of the block RAM | 0.32 | – | 0.36 | – | ns |
| $T_{RDCK\_DIB}$ | Setup time for data at the DIN inputs before the active transition at the CLK input of the block RAM | 0.28 | – | 0.31 | – | ns |
| $T_{RCCK\_ENB}$ | Setup time for the EN input before the active transition at the CLK input of the block RAM | 0.69 | – | 0.77 | – | ns |
| $T_{RCCK\_WEB}$ | Setup time for the WE input before the active transition at the CLK input of the block RAM | 1.12 | – | 1.26 | – | ns |
| **Hold Times** | | | | | | |
| $T_{RCKC\_ADDR}$ | Hold time on the ADDR inputs after the active transition at the CLK input | 0 | – | 0 | – | ns |
| $T_{RCKD\_DIB}$ | Hold time on the DIN inputs after the active transition at the CLK input | 0 | – | 0 | – | ns |
| $T_{RCKC\_ENB}$ | Hold time on the EN input after the active transition at the CLK input | 0 | – | 0 | – | ns |
| $T_{RCKC\_WEB}$ | Hold time on the WE input after the active transition at the CLK input | 0 | – | 0 | – | ns |
| **Clock Timing** | | | | | | |
| $T_{BPWH}$ | High pulse width of the CLK signal | 1.56 | – | 1.79 | – | ns |
| $T_{BPWL}$ | Low pulse width of the CLK signal | 1.56 | – | 1.79 | – | ns |
| **Clock Frequency** | | | | | | |
| $F_{BRAM}$ | Block RAM clock frequency | 0 | 320 | 0 | 280 | MHz |

**Notes:**

1. The numbers in this table are based on the operating conditions set forth in Table 8.

## Miscellaneous DCM Timing

*Table 42:* **Miscellaneous DCM Timing**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| DCM_RST_PW_MIN | Minimum duration of a RST pulse width | 3 | – | CLKIN cycles |
| DCM_RST_PW_MAX(2) | Maximum duration of a RST pulse width | N/A | N/A | seconds |
| | | N/A | N/A | seconds |
| DCM_CONFIG_LAG_TIME(3) | Maximum duration from $V_{CCINT}$ applied to FPGA configuration successfully completed (DONE pin goes High) and clocks applied to DCM DLL | N/A | N/A | minutes |
| | | N/A | N/A | minutes |

**Notes:**

1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFX180) are unaffected.
2. This specification is equivalent to the Virtex®-4 DCM_RESET specification. This specification does not apply for Spartan-3A FPGAs.
3. This specification is equivalent to the Virtex-4 TCONFIG specification. This specification does not apply for Spartan-3A FPGAs.

# DNA Port Timing

*Table 43:* **DNA_PORT Interface Timing**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{DNASSU}$ | Setup time on SHIFT before the rising edge of CLK | 1.0 | – | ns |
| $T_{DNASH}$ | Hold time on SHIFT after the rising edge of CLK | 0.5 | – | ns |
| $T_{DNADSU}$ | Setup time on DIN before the rising edge of CLK | 1.0 | – | ns |
| $T_{DNADH}$ | Hold time on DIN after the rising edge of CLK | 0.5 | – | ns |
| $T_{DNARSU}$ | Setup time on READ before the rising edge of CLK | 5.0 | 10,000 | ns |
| $T_{DNARH}$ | Hold time on READ after the rising edge of CLK | 0 | – | ns |
| $T_{DNADCKO}$ | Clock-to-output delay on DOUT after rising edge of CLK | 0.5 | 1.5 | ns |
| $T_{DNACLKF}$ | CLK frequency | 0 | 100 | MHz |
| $T_{DNACLKH}$ | CLK High time | 1.0 | ∞ | ns |
| $T_{DNACLKL}$ | CLK Low time | 1.0 | ∞ | ns |

**Notes:**

1. The minimum READ pulse width is 5 ns, the maximum READ pulse width is 10 µs.
2. The numbers in this table are based on the operating conditions set forth in Table 8.

## Configuration Clock (CCLK) Characteristics

*Table 46:* **Master Mode CCLK Output Period by *ConfigRate* Opti0on Setting**

| Symbol | Description | *ConfigRate* Setting | Temperature Range | Minimum | Maximum | Units |
|---|---|---|---|---|---|---|
| $T_{CCLK1}$ | CCLK clock period by ***ConfigRate*** setting | 1 *(power-on value)* | Commercial | 1,254 | 2,500 | ns |
| | | | Industrial | 1,180 | | ns |
| $T_{CCLK3}$ | | 3 | Commercial | 413 | 833 | ns |
| | | | Industrial | 390 | | ns |
| $T_{CCLK6}$ | | 6 (default) | Commercial | 207 | 417 | ns |
| | | | Industrial | 195 | | ns |
| $T_{CCLK7}$ | | 7 | Commercial | 178 | 357 | ns |
| | | | Industrial | 168 | | ns |
| $T_{CCLK8}$ | | 8 | Commercial | 156 | 313 | ns |
| | | | Industrial | 147 | | ns |
| $T_{CCLK10}$ | | 10 | Commercial | 123 | 250 | ns |
| | | | Industrial | 116 | | ns |
| $T_{CCLK12}$ | | 12 | Commercial | 103 | 208 | ns |
| | | | Industrial | 97 | | ns |
| $T_{CCLK13}$ | | 13 | Commercial | 93 | 192 | ns |
| | | | Industrial | 88 | | ns |
| $T_{CCLK17}$ | | 17 | Commercial | 72 | 147 | ns |
| | | | Industrial | 68 | | ns |
| $T_{CCLK22}$ | | 22 | Commercial | 54 | 114 | ns |
| | | | Industrial | 51 | | ns |
| $T_{CCLK25}$ | | 25 | Commercial | 47 | 100 | ns |
| | | | Industrial | 45 | | ns |
| $T_{CCLK27}$ | | 27 | Commercial | 44 | 93 | ns |
| | | | Industrial | 42 | | ns |
| $T_{CCLK33}$ | | 33 | Commercial | 36 | 76 | ns |
| | | | Industrial | 34 | | ns |
| $T_{CCLK44}$ | | 44 | Commercial | 26 | 57 | ns |
| | | | Industrial | 25 | | ns |
| $T_{CCLK50}$ | | 50 | Commercial | 22 | 50 | ns |
| | | | Industrial | 21 | | ns |
| $T_{CCLK100}$ | | 100 | Commercial | 11.2 | 25 | ns |
| | | | Industrial | 10.6 | | ns |

**Notes:**

1. Set the ***ConfigRate*** option value when generating a configuration bitstream.

*Table 47:* **Master Mode CCLK Output Frequency by *ConfigRate* Option Setting**

| Symbol | Description | *ConfigRate* Setting | Temperature Range | Minimum | Maximum | Units |
|---|---|---|---|---|---|---|
| $F_{CCLK1}$ | Equivalent CCLK clock frequency by ***ConfigRate*** setting | 1 *(power-on value)* | Commercial | 0.400 | 0.797 | MHz |
| | | | Industrial | | 0.847 | MHz |
| $F_{CCLK3}$ | | 3 | Commercial | 1.20 | 2.42 | MHz |
| | | | Industrial | | 2.57 | MHz |
| $F_{CCLK6}$ | | 6 (default) | Commercial | 2.40 | 4.83 | MHz |
| | | | Industrial | | 5.13 | MHz |
| $F_{CCLK7}$ | | 7 | Commercial | 2.80 | 5.61 | MHz |
| | | | Industrial | | 5.96 | MHz |
| $F_{CCLK8}$ | | 8 | Commercial | 3.20 | 6.41 | MHz |
| | | | Industrial | | 6.81 | MHz |
| $F_{CCLK10}$ | | 10 | Commercial | 4.00 | 8.12 | MHz |
| | | | Industrial | | 8.63 | MHz |
| $F_{CCLK12}$ | | 12 | Commercial | 4.80 | 9.70 | MHz |
| | | | Industrial | | 10.31 | MHz |
| $F_{CCLK13}$ | | 13 | Commercial | 5.20 | 10.69 | MHz |
| | | | Industrial | | 11.37 | MHz |
| $F_{CCLK17}$ | | 17 | Commercial | 6.80 | 13.74 | MHz |
| | | | Industrial | | 14.61 | MHz |
| $F_{CCLK22}$ | | 22 | Commercial | 8.80 | 18.44 | MHz |
| | | | Industrial | | 19.61 | MHz |
| $F_{CCLK25}$ | | 25 | Commercial | 10.00 | 20.90 | MHz |
| | | | Industrial | | 22.23 | MHz |
| $F_{CCLK27}$ | | 27 | Commercial | 10.80 | 22.39 | MHz |
| | | | Industrial | | 23.81 | MHz |
| $F_{CCLK33}$ | | 33 | Commercial | 13.20 | 27.48 | MHz |
| | | | Industrial | | 29.23 | MHz |
| $F_{CCLK44}$ | | 44 | Commercial | 17.60 | 37.60 | MHz |
| | | | Industrial | | 40.00 | MHz |
| $F_{CCLK50}$ | | 50 | Commercial | 20.00 | 44.80 | MHz |
| | | | Industrial | | 47.66 | MHz |
| $F_{CCLK100}$ | | 100 | Commercial | 40.00 | 88.68 | MHz |
| | | | Industrial | | 94.34 | MHz |

*Table 48:* **Master Mode CCLK Output Minimum Low and High Time**

| Symbol | Description | | *ConfigRate* Setting | | | | | | | | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1 | 3 | 6 | 7 | 8 | 10 | 12 | 13 | 17 | 22 | 25 | 27 | 33 | 44 | 50 | 100 | |
| $T_{MCCL}$, $T_{MCCH}$ | Master Mode CCLK Minimum Low and High Time | Commercial | 595 | 196 | 98.3 | 84.5 | 74.1 | 58.4 | 48.9 | 44.1 | 34.2 | 25.6 | 22.3 | 20.9 | 17.1 | 12.3 | 10.4 | 5.3 | ns |
| | | Industrial | 560 | 185 | 92.6 | 79.8 | 69.8 | 55.0 | 46.0 | 41.8 | 32.3 | 24.2 | 21.4 | 20.0 | 16.2 | 11.9 | 10.0 | 5.0 | ns |

*Table 49:* **Slave Mode CCLK Input Low and High Time**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{SCCL}$, $T_{SCCH}$ | CCLK Low and High time | 5 | ∞ | ns |

## IEEE 1149.1/1532 JTAG Test Access Port Timing

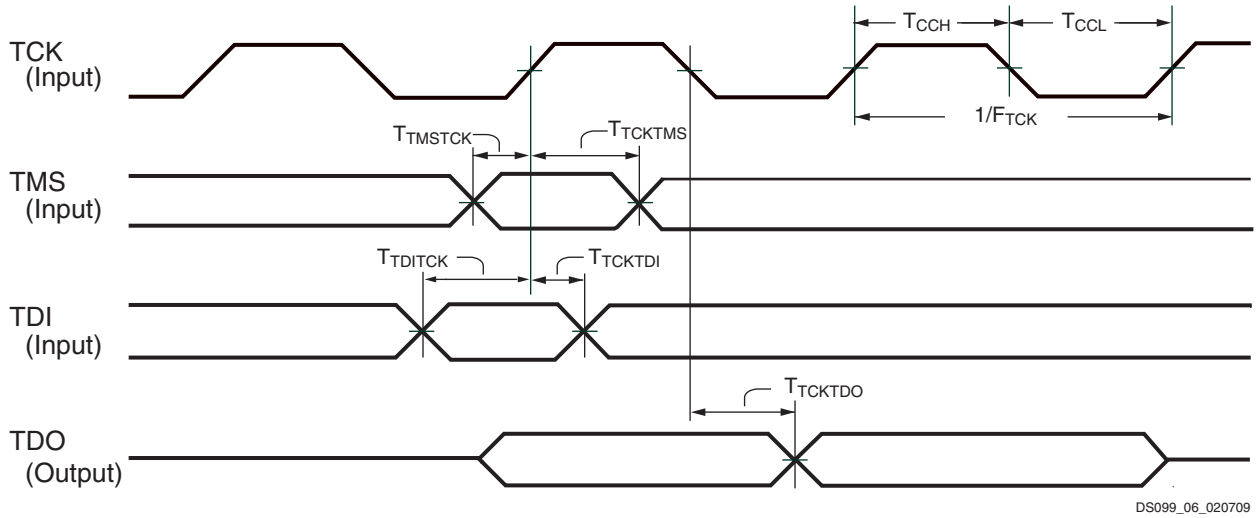


*Figure 16:* **JTAG Waveforms**

*Table 56:* **Timing for the JTAG Test Access Port**

| Symbol | Description | | All Speed Grades | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| **Clock-to-Output Times** | | | | | |
| $T_{TCKTDO}$ | The time from the falling transition on the TCK pin to data appearing at the TDO pin | | 1.0 | 11.0 | ns |
| **Setup Times** | | | | | |
| $T_{TDITCK}$ | The time from the setup of data at the TDI pin to the rising transition at the TCK pin | All devices and functions except those shown below | 7.0 | – | ns |
| | | Boundary scan commands (INTEST, EXTEST, SAMPLE) on XC3S700A and XC3S1400A FPGAs | 11.0 | | |
| $T_{TMSTCK}$ | The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin | | 7.0 | – | ns |
| **Hold Times** | | | | | |
| $T_{TCKTDI}$ | The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin | All functions except those shown below | 0 | – | ns |
| | | Configuration commands (CFG_IN, ISC_PROGRAM) | 2.0 | | |
| $T_{TCKTMS}$ | The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin | | 0 | – | ns |
| **Clock Timing** | | | | | |
| $T_{CCH}$ | The High pulse width at the TCK pin | All functions except ISC_DNA command | 5 | – | ns |
| $T_{CCL}$ | The Low pulse width at the TCK pin | | 5 | – | ns |
| $T_{CCHDNA}$ | The High pulse width at the TCK pin | During ISC_DNA command | 10 | 10,000 | ns |
| $T_{CCLDNA}$ | The Low pulse width at the TCK pin | | 10 | 10,000 | ns |
| $F_{TCK}$ | Frequency of the TCK signal | All operations on XC3S50A, XC3S200A, and XC3S400A FPGAs and for BYPASS or HIGHZ instructions on all FPGAs | 0 | 33 | MHz |
| | | All operations on XC3S700A and XC3S1400A FPGAs, except for BYPASS or HIGHZ instructions | | 20 | |

**Notes:**

1. The numbers in this table are based on the operating conditions set forth in Table 8.
2. For details on JTAG see Chapter 9 “JTAG Configuration Mode and Boundary-Scan” in UG332 *Spartan-3 Generation Configuration User Guide*.

## Introduction

This section describes how the various pins on a Spartan®-3A FPGA connect within the supported component packages, and provides device-specific thermal characteristics. For general information on the pin functions and the package characteristics, see the Packaging section of UG331: *Spartan-3 Generation FPGA User Guide*.

- **UG331: Spartan-3 Generation FPGA User Guide**
  www.xilinx.com/support/documentation/user_guides/ug331.pdf

Spartan-3A FPGAs are available in both standard and Pb-free, RoHS versions of each package, with the Pb-free version adding a "G" to the middle of the package code. Except for the thermal characteristics, all information for the standard package applies equally to the Pb-free package.

## Pin Types

Most pins on a Spartan-3A FPGA are general-purpose, user-defined I/O pins. There are, however, up to 12 different functional types of pins on Spartan-3A FPGA packages, as outlined in Table 57. In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

*Table 57:* **Types of Pins on Spartan-3A FPGAs**

| Type / Color Code | Description | Pin Name(s) in Type |
|---|---|---|
| I/O | Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os. | IO_#<br>IO_Lxxy_# |
| INPUT | Unrestricted, general-purpose input-only pin. This pin does not have an output structure, differential termination resistor, or PCI clamp diode. | IP_#<br>IP_Lxxy_# |
| DUAL | Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. See UG332: *Spartan-3 Generation Configuration User Guide* for additional information on these signals. | M[2:0]<br>PUDC_B<br>CCLK<br>MOSI/CSI_B<br>D[7:1]<br>D0/DIN<br>DOUT<br>CSO_B<br>RDWR_B<br>INIT_B<br>A[25:0]<br>VS[2:0]<br>LDC[2:0]<br>HDC |
| VREF | Dual-purpose pin that is either a user-I/O pin or Input-only pin, or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected. | IP/VREF_#<br>IP_Lxxy_#/VREF_#<br>IO/VREF_#<br>IO_Lxxy_#/VREF_# |
| CLK | Either a user-I/O pin or an input to a specific clock buffer driver. Most packages have 16 global clock inputs that optionally clock the entire device. The exceptions are the TQ144 and the XC3S50A in the FT256 package). The RHCLK inputs optionally clock the right half of the device. The LHCLK inputs optionally clock the left half of the device. See the Using Global Clock Resources chapter in UG331: *Spartan-3 Generation FPGA User Guide* for additional information on these signals. | IO_Lxxy_#/GCLK[15:0],<br>IO_Lxxy_#/LHCLK[7:0],<br>IO_Lxxy_#/RHCLK[7:0] |
| CONFIG | Dedicated configuration pin, two per device. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See the UG332: *Spartan-3 Generation Configuration User Guide* for additional information on the DONE and PROG_B signals. | DONE, PROG_B |

*Table 59:* **Maximum User I/O by Package**

| Device | Package | Maximum User I/Os and Input-Only | Maximum Input-Only | Maximum Differential Pairs | All Possible I/Os by Type | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | I/O | INPUT | DUAL | VREF | CLK | N.C. |
| XC3S50A | VQ100 | 68 | 6 | 60 | 17 | 2 | 20 | 6 | 23 | 0 |
| XC3S200A | | 68 | 6 | 60 | 17 | 2 | 20 | 6 | 23 | 0 |
| XC3S50A | TQ144 | 108 | 7 | 50 | 42 | 2 | 26 | 8 | 30 | 0 |
| XC3S50A | FT256 | 144 | 32 | 64 | 53 | 20 | 26 | 15 | 30 | 51 |
| XC3S200A | | 195 | 35 | 90 | 69 | 21 | 52 | 21 | 32 | 0 |
| XC3S400A | | 195 | 35 | 90 | 69 | 21 | 52 | 21 | 32 | 0 |
| XC3S700A | | 161 | 13 | 60 | 59 | 2 | 52 | 18 | 30 | 0 |
| XC3S1400A | | 161 | 13 | 60 | 59 | 2 | 52 | 18 | 30 | 0 |
| XC3S200A | FG320 | 248 | 56 | 112 | 101 | 40 | 52 | 23 | 32 | 3 |
| XC3S400A | | 251 | 59 | 112 | 101 | 42 | 52 | 24 | 32 | 0 |
| XC3S400A | FG400 | 311 | 63 | 142 | 155 | 46 | 52 | 26 | 32 | 0 |
| XC3S700A | | 311 | 63 | 142 | 155 | 46 | 52 | 26 | 32 | 0 |
| XC3S700A | FG484 | 372 | 84 | 165 | 194 | 61 | 52 | 33 | 32 | 3 |
| XC3S1400A | | 375 | 87 | 165 | 195 | 62 | 52 | 34 | 32 | 0 |
| XC3S1400A | FG676 | 502 | 94 | 227 | 313 | 67 | 52 | 38 | 32 | 17 |

**Notes:**

1. Some VREFs are on INPUT pins. See pinout tables for details.

Electronic versions of the package pinout tables and footprints are available for download from the Xilinx website. Using a spreadsheet program, the data can be sorted and reformatted according to any specific needs. Similarly, the ASCII-text file is easily parsed by most scripting programs.

http://www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip

*Table 63:* **Spartan-3A VQ100 Pinout*(Continued)***

| | | | |
|---|---|---|---|
| 2 | IO_L12P_2/D1 (3S50A)<br>IO_L11N_2/D1 (3S200A) | P52 | DUAL |
| 2 | IP_2/VREF_2 | P39 | VREF |
| 2 | VCCO_2 | P26 | VCCO |
| 2 | VCCO_2 | P45 | VCCO |
| 3 | IO_L01N_3 | P4 | IO |
| 3 | IO_L01P_3 | P3 | IO |
| 3 | IO_L02N_3 | P6 | IO |
| 3 | IO_L02P_3 | P5 | IO |
| 3 | IO_L03N_3/LHCLK1 | P10 | CLK |
| 3 | IO_L03P_3/LHCLK0 | P9 | CLK |
| 3 | IO_L04N_3/IRDY2/LHCLK3 | P13 | CLK |
| 3 | IO_L04P_3/LHCLK2 | P12 | CLK |
| 3 | IO_L05N_3/LHCLK7 | P16 | CLK |
| 3 | IO_L05P_3/TRDY2/LHCLK6 | P15 | CLK |
| 3 | IO_L06N_3 | P20 | IO |
| 3 | IO_L06P_3 | P19 | IO |
| 3 | IP_3 | P21 | IP |
| 3 | IP_3/VREF_3 | P7 | VREF |
| 3 | VCCO_3 | P11 | VCCO |
| GND | GND | P14 | GND |
| GND | GND | P18 | GND |
| GND | GND | P42 | GND |
| GND | GND | P47 | GND |
| GND | GND | P58 | GND |
| GND | GND | P63 | GND |
| GND | GND | P69 | GND |
| GND | GND | P74 | GND |
| GND | GND | P8 | GND |
| GND | GND | P80 | GND |
| GND | GND | P87 | GND |
| GND | GND | P91 | GND |
| GND | GND | P95 | GND |
| VCCAUX | DONE | P54 | CONFIG |
| VCCAUX | PROG_B | P100 | CONFIG |
| VCCAUX | TCK | P76 | JTAG |
| VCCAUX | TDI | P2 | JTAG |
| VCCAUX | TDO | P75 | JTAG |
| VCCAUX | TMS | P1 | JTAG |
| VCCAUX | VCCAUX | P22 | VCCAUX |
| VCCAUX | VCCAUX | P55 | VCCAUX |
| VCCAUX | VCCAUX | P92 | VCCAUX |

*Table 63:* **Spartan-3A VQ100 Pinout*(Continued)***

| | | | |
|---|---|---|---|
| VCCINT | VCCINT | P17 | VCCINT |
| VCCINT | VCCINT | P38 | VCCINT |
| VCCINT | VCCINT | P66 | VCCINT |
| VCCINT | VCCINT | P81 | VCCINT |

## VQ100 Footprint (XC3S50A)

Note pin 1 indicator in top-left corner and logo orientation.

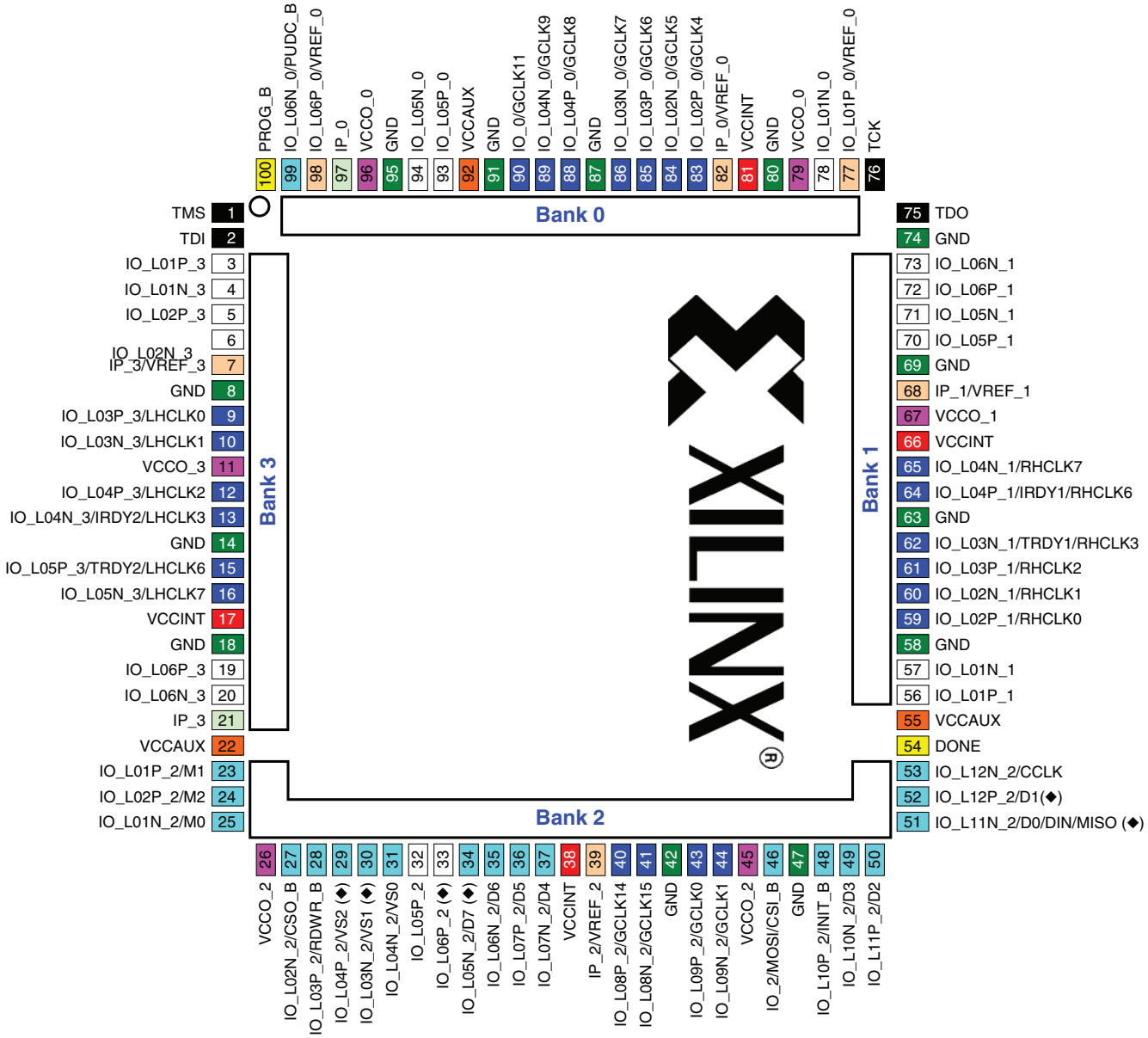


*Figure 17:* **VQ100 Package Footprint - XC3S50A (Top View)**

| | | | | | |
|---|---|---|---|---|---|
| 17 | **I/O:** Unrestricted, general-purpose user I/O | 20 | **DUAL:** Configuration pins, then possible user I/O | 6 | **VREF:** User I/O or input voltage reference for bank |
| 2 | **INPUT:** Unrestricted, general-purpose input pin | 23 | **CLK:** User I/O, input, or global buffer input | 6 | **VCCO:** Output voltage supply for bank |
| 2 | **CONFIG:** Dedicated configuration pins | 4 | **JTAG:** Dedicated JTAG port pins | 4 | **VCCINT:** Internal core supply voltage (+1.2V) |
| 0 | **N.C.:** Not connected | 13 | **GND:** Ground | 3 | **VCCAUX:** Auxiliary supply voltage |

## TQ144 Footprint

Note pin 1 indicator in top-left corner and logo orientation.

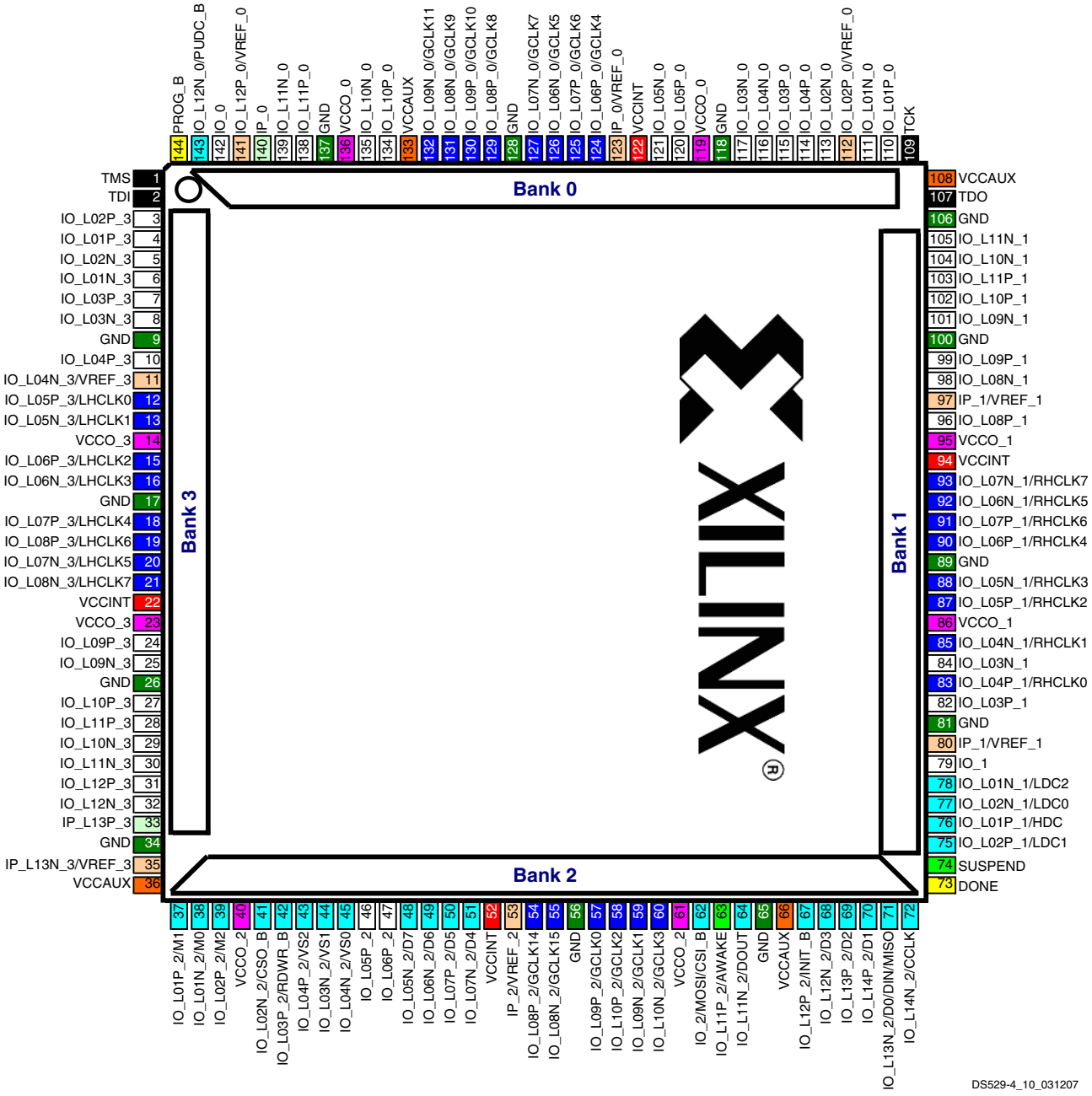


*Figure 19:* **TQ144 Package Footprint (Top View)**

| | | | | | |
|---|---|---|---|---|---|
| 42 | **I/O:** Unrestricted, general-purpose user I/O | 25 | **DUAL:** Configuration pins, then possible user I/O | 8 | **VREF:** User I/O or input voltage reference for bank |
| 2 | **INPUT:** Unrestricted, general-purpose input pin | 30 | **CLK:** User I/O, input, or global buffer input | 8 | **VCCO:** Output voltage supply for bank |
| 2 | **CONFIG:** Dedicated configuration pins | 4 | **JTAG:** Dedicated JTAG port pins | 4 | **VCCINT:** Internal core supply voltage (+1.2V) |
| 0 | **N.C.:** Not connected | 13 | **GND:** Ground | 4 | **VCCAUX:** Auxiliary supply voltage |
| 2 | **SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins | | | | |

*Table 68:* **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400) *(Continued)***

| Bank | XC3S50A | XC3S200A XC3S400A | FT256 Ball | Type |
|---|---|---|---|---|
| 0 | IO_L17P_0 | IO_L17P_0 | A5 | I/O |
| 0 | IO_L18N_0 | IO_L18N_0 | B4 | I/O |
| 0 | IO_L18P_0 | IO_L18P_0 | A4 | I/O |
| 0 | IO_L19N_0 | IO_L19N_0 | B3 | I/O |
| 0 | IO_L19P_0 | IO_L19P_0 | A3 | I/O |
| 0 | IO_L20N_0/ PUDC_B | IO_L20N_0/ PUDC_B | D5 | DUAL |
| 0 | IO_L20P_0/ VREF_0 | IO_L20P_0/ VREF_0 | C4 | VREF |
| 0 | IP_0 | IP_0 | D6 | INPUT |
| 0 | IP_0 | IP_0 | D12 | INPUT |
| 0 | IP_0 | IP_0 | E6 | INPUT |
| 0 | IP_0 | IP_0 | F7 | INPUT |
| 0 | IP_0 | IP_0 | F9 | INPUT |
| 0 | IP_0 | IP_0 | F10 | INPUT |
| 0 | IP_0/VREF_0 | IP_0/VREF_0 | E9 | VREF |
| 0 | VCCO_0 | VCCO_0 | B5 | VCCO |
| 0 | VCCO_0 | VCCO_0 | B9 | VCCO |
| 0 | VCCO_0 | VCCO_0 | B13 | VCCO |
| 0 | VCCO_0 | VCCO_0 | E8 | VCCO |
| 1 | IO_L01N_1/ LDC2 | IO_L01N_1/ LDC2 | N14 | DUAL |
| 1 | IO_L01P_1/ HDC | IO_L01P_1/ HDC | N13 | DUAL |
| 1 | IO_L02N_1/ LDC0 | IO_L02N_1/ LDC0 | P15 | DUAL |
| 1 | IO_L02P_1/ LDC1 | IO_L02P_1/ LDC1 | R15 | DUAL |
| 1 | IO_L03N_1 | IO_L03N_1/A1 | N16 | DUAL |
| 1 | IO_L03P_1 | IO_L03P_1/A0 | P16 | DUAL |
| 1 | N.C. (◆) | IO_L05N_1/ VREF_1 | M14 | VREF |
| 1 | N.C. (◆) | IO_L05P_1 | M13 | I/O |
| 1 | N.C. (◆) | IO_L06N_1/A3 | K13 | DUAL |
| 1 | N.C. (◆) | IO_L06P_1/A2 | L13 | DUAL |
| 1 | N.C. (◆) | IO_L07N_1/A5 | M16 | DUAL |
| 1 | N.C. (◆) | IO_L07P_1/A4 | M15 | DUAL |
| 1 | N.C. (◆) | IO_L08N_1/A7 | L16 | DUAL |
| 1 | N.C. (◆) | IO_L08P_1/A6 | L14 | DUAL |
| 1 | IO_L10N_1 | IO_L10N_1/A9 | J13 | DUAL |
| 1 | IO_L10P_1 | IO_L10P_1/A8 | J12 | DUAL |
| 1 | IO_L11N_1/ RHCLK1 | IO_L11N_1/ RHCLK1 | K14 | RHCLK |
| 1 | IO_L11P_1/ RHCLK0 | IO_L11P_1/ RHCLK0 | K15 | RHCLK |

*Table 68:* **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400) *(Continued)***

| Bank | XC3S50A | XC3S200A XC3S400A | FT256 Ball | Type |
|---|---|---|---|---|
| 1 | IO_L12N_1/ TRDY1/RHCLK3 | IO_L12N_1/ TRDY1/RHCLK3 | J16 | RHCLK |
| 1 | IO_L12P_1/ RHCLK2 | IO_L12P_1/ RHCLK2 | K16 | RHCLK |
| 1 | IO_L14N_1/ RHCLK5 | IO_L14N_1/ RHCLK5 | H14 | RHCLK |
| 1 | IO_L14P_1/ RHCLK4 | IO_L14P_1/ RHCLK4 | J14 | RHCLK |
| 1 | IO_L15N_1/ RHCLK7 | IO_L15N_1/ RHCLK7 | H16 | RHCLK |
| 1 | IO_L15P_1/ IRDY1/RHCLK6 | IO_L15P_1/ IRDY1/RHCLK6 | H15 | RHCLK |
| 1 | N.C. (◆) | IO_L16N_1/A11 | F16 | DUAL |
| 1 | N.C. (◆) | IO_L16P_1/A10 | G16 | DUAL |
| 1 | N.C. (◆) | IO_L17N_1/A13 | G14 | DUAL |
| 1 | N.C. (◆) | IO_L17P_1/A12 | H13 | DUAL |
| 1 | N.C. (◆) | IO_L18N_1/A15 | F15 | DUAL |
| 1 | N.C. (◆) | IO_L18P_1/A14 | E16 | DUAL |
| 1 | N.C. (◆) | IO_L19N_1/A17 | F14 | DUAL |
| 1 | N.C. (◆) | IO_L19P_1/A16 | G13 | DUAL |
| 1 | IO_L20N_1 | IO_L20N_1/A19 | F13 | DUAL |
| 1 | IO_L20P_1 | IO_L20P_1/A18 | E14 | DUAL |
| 1 | IO_L22N_1 | IO_L22N_1/A21 | D15 | DUAL |
| 1 | IO_L22P_1 | IO_L22P_1/A20 | D16 | DUAL |
| 1 | IO_L23N_1 | IO_L23N_1/A23 | D14 | DUAL |
| 1 | IO_L23P_1 | IO_L23P_1/A22 | E13 | DUAL |
| 1 | IO_L24N_1 | IO_L24N_1/A25 | C15 | DUAL |
| 1 | IO_L24P_1 | IO_L24P_1/A24 | C16 | DUAL |
| 1 | IP_L04N_1/ VREF_1 | IP_L04N_1/ VREF_1 | K12 | VREF |
| 1 | IP_L04P_1 | IP_L04P_1 | K11 | INPUT |
| 1 | N.C. (◆) | IP_L09N_1 | J11 | INPUT |
| 1 | N.C. (◆) | IP_L09P_1/ VREF_1 | J10 | VREF |
| 1 | IP_L13N_1 | IP_L13N_1 | H11 | INPUT |
| 1 | IP_L13P_1 | IP_L13P_1 | H10 | INPUT |
| 1 | IP_L21N_1 | IP_L21N_1 | G11 | INPUT |
| 1 | IP_L21P_1/ VREF_1 | IP_L21P_1/ VREF_1 | G12 | VREF |
| 1 | IP_L25N_1 | IP_L25N_1 | F11 | INPUT |
| 1 | IP_L25P_1/ VREF_1 | IP_L25P_1/ VREF_1 | F12 | VREF |
| 1 | VCCO_1 | VCCO_1 | E15 | VCCO |
| 1 | VCCO_1 | VCCO_1 | H12 | VCCO |
| 1 | VCCO_1 | VCCO_1 | J15 | VCCO |
| 1 | VCCO_1 | VCCO_1 | N15 | VCCO |

*Table 68:* **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400) *(Continued)***

| Bank | XC3S50A | XC3S200A XC3S400A | FT256 Ball | Type |
|---|---|---|---|---|
| 2 | IO_L01N_2/M0 | IO_L01N_2/M0 | P4 | DUAL |
| 2 | IO_L01P_2/M1 | IO_L01P_2/M1 | N4 | DUAL |
| 2 | IO_L02N_2/ CSO_B | IO_L02N_2/ CSO_B | T2 | DUAL |
| 2 | IO_L02P_2/M2 | IO_L02P_2/M2 | R2 | DUAL |
| 2 | IO_L04P_2/VS2 | IO_L03N_2/VS2 | T3 | DUAL |
| 2 | IO_L03P_2/ RDWR_B | IO_L03P_2/ RDWR_B | R3 | DUAL |
| 2 | IO_L04N_2/VS0 | IO_L04N_2/VS0 | P5 | DUAL |
| 2 | IO_L03N_2/VS1 | IO_L04P_2/VS1 | N6 | DUAL |
| 2 | IO_L06P_2 | IO_L05N_2 | R5 | I/O |
| 2 | IO_L05P_2 | IO_L05P_2 | T4 | I/O |
| 2 | IO_L06N_2/D6 | IO_L06N_2/D6 | T6 | DUAL |
| 2 | IO_L05N_2/D7 | IO_L06P_2/D7 | T5 | DUAL |
| 2 | N.C. (◆) | IO_L07N_2 | P6 | I/O |
| 2 | N.C. (◆) | IO_L07P_2 | N7 | I/O |
| 2 | IO_L08N_2/D4 | IO_L08N_2/D4 | N8 | DUAL |
| 2 | IO_L08P_2/D5 | IO_L08P_2/D5 | P7 | DUAL |
| 2 | N.C. (◆) | IO_L09N_2/ GCLK13 | T7 | GCLK |
| 2 | N.C. (◆) | IO_L09P_2/ GCLK12 | R7 | GCLK |
| 2 | IO_L10N_2/ GCLK15 | IO_L10N_2/ GCLK15 | T8 | GCLK |
| 2 | IO_L10P_2/ GCLK14 | IO_L10P_2/ GCLK14 | P8 | GCLK |
| 2 | IO_L11N_2/ GCLK1 | IO_L11N_2/ GCLK1 | P9 | GCLK |
| 2 | IO_L11P_2/ GCLK0 | IO_L11P_2/ GCLK0 | N9 | GCLK |
| 2 | IO_L12N_2/ GCLK3 | IO_L12N_2/ GCLK3 | T9 | GCLK |
| 2 | IO_L12P_2/ GCLK2 | IO_L12P_2/ GCLK2 | R9 | GCLK |
| 2 | N.C. (◆) | IO_L13N_2 | M10 | I/O |
| 2 | N.C. (◆) | IO_L13P_2 | N10 | I/O |
| 2 | IO_L14P_2/ MOSI/CSI_B | IO_L14N_2/ MOSI/CSI_B | P10 | DUAL |
| 2 | IO_L14N_2 | IO_L14P_2 | T10 | I/O |
| 2 | IO_L15N_2/ DOUT | IO_L15N_2/ DOUT | R11 | DUAL |
| 2 | IO_L15P_2/ AWAKE | IO_L15P_2/ AWAKE | T11 | PWR MGMT |
| 2 | IO_L16N_2 | IO_L16N_2 | N11 | I/O |
| 2 | IO_L16P_2 | IO_L16P_2 | P11 | I/O |
| 2 | IO_L17N_2/D3 | IO_L17N_2/D3 | P12 | DUAL |
| 2 | IO_L17P_2/ INIT_B | IO_L17P_2/ INIT_B | T12 | DUAL |

*Table 68:* **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400) *(Continued)***

| Bank | XC3S50A | XC3S200A XC3S400A | FT256 Ball | Type |
|---|---|---|---|---|
| 2 | IO_L20P_2/D1 | IO_L18N_2/D1 | R13 | DUAL |
| 2 | IO_L18P_2/D2 | IO_L18P_2/D2 | T13 | DUAL |
| 2 | N.C. (◆) | IO_L19N_2 | P13 | I/O |
| 2 | N.C. (◆) | IO_L19P_2 | N12 | I/O |
| 2 | IO_L20N_2/ CCLK | IO_L20N_2/ CCLK | R14 | DUAL |
| 2 | IO_L18N_2/D0/ DIN/MISO | IO_L20P_2/D0/ DIN/MISO | T14 | DUAL |
| 2 | IP_2 | IP_2 | L7 | INPUT |
| 2 | IP_2 | IP_2 | L8 | INPUT |
| 2 | IP_2/VREF_2 | IP_2/VREF_2 | L9 | VREF |
| 2 | IP_2/VREF_2 | IP_2/VREF_2 | L10 | VREF |
| 2 | IP_2/VREF_2 | IP_2/VREF_2 | M7 | VREF |
| 2 | IP_2/VREF_2 | IP_2/VREF_2 | M8 | VREF |
| 2 | IP_2/VREF_2 | IP_2/VREF_2 | M11 | VREF |
| 2 | IP_2/VREF_2 | IP_2/VREF_2 | N5 | VREF |
| 2 | VCCO_2 | VCCO_2 | M9 | VCCO |
| 2 | VCCO_2 | VCCO_2 | R4 | VCCO |
| 2 | VCCO_2 | VCCO_2 | R8 | VCCO |
| 2 | VCCO_2 | VCCO_2 | R12 | VCCO |
| 3 | IO_L01N_3 | IO_L01N_3 | C1 | I/O |
| 3 | IO_L01P_3 | IO_L01P_3 | C2 | I/O |
| 3 | IO_L02N_3 | IO_L02N_3 | D3 | I/O |
| 3 | IO_L02P_3 | IO_L02P_3 | D4 | I/O |
| 3 | IO_L03N_3 | IO_L03N_3 | E1 | I/O |
| 3 | IO_L03P_3 | IO_L03P_3 | D1 | I/O |
| 3 | N.C. (◆) | IO_L05N_3 | E2 | I/O |
| 3 | N.C. (◆) | IO_L05P_3 | E3 | I/O |
| 3 | N.C. (◆) | IO_L07N_3 | G4 | I/O |
| 3 | N.C. (◆) | IO_L07P_3 | F3 | I/O |
| 3 | IO_L08N_3/ VREF_3 | IO_L08N_3/ VREF_3 | G1 | VREF |
| 3 | IO_L08P_3 | IO_L08P_3 | F1 | I/O |
| 3 | N.C. (◆) | IO_L09N_3 | H4 | I/O |
| 3 | N.C. (◆) | IO_L09P_3 | G3 | I/O |
| 3 | N.C. (◆) | IO_L10N_3 | H5 | I/O |
| 3 | N.C. (◆) | IO_L10P_3 | H6 | I/O |
| 3 | IO_L11N_3/ LHCLK1 | IO_L11N_3/ LHCLK1 | H1 | LHCLK |
| 3 | IO_L11P_3/ LHCLK0 | IO_L11P_3/ LHCLK0 | G2 | LHCLK |
| 3 | IO_L12N_3/ IRDY2/LHCLK3 | IO_L12N_3/ IRDY2/LHCLK3 | J3 | LHCLK |
| 3 | IO_L12P_3/ LHCLK2 | IO_L12P_3/ LHCLK2 | H3 | LHCLK |

## XC3S50A Differential I/O Alignment Differences

Also, some differential I/O pairs on the XC3S50A FPGA are aligned differently than the corresponding pairs on the XC3S200A or XC3S400A FPGAs, as shown in Table 74. All the mismatched pairs are in I/O Bank 2. The shading highlights the N side of each pair.

*Table 74:* **Differential I/O Differences in FT256**

| FT256 Ball | Bank | XC3S50A | XC3S200A XC3S400A |
|---|---|---|---|
| T3 | 2 | IO_L04P_2/VS2 | IO_L03N_2/VS2 |
| N6 | | IO_L03N_2/VS1 | IO_L04P_2/VS1 |
| R5 | | IO_L06P_2 | IO_L05N_2 |
| T5 | | IO_L05N_2/D7 | IO_L06P_2/D7 |
| P10 | | IO_L14P_2/MOSI /CSI_B | IO_L14N_2/MOSI /CSI_B |
| T10 | | IO_L14N_2 | IO_L14P_2 |
| R13 | | IO_L20P_2 | IO_L18N_2 |
| T14 | | IO_L18N_2 | IO_L20P_2 |

## XC3S50A Does Not Have BPI Mode Address Outputs

The XC3S50A FPGA does not generate the BPI-mode address pins during configuration. Table 75 summarizes these differences.

*Table 75:* **XC3S50A BPI Functional Differences**

| FT256 Ball | Bank | XC3S50A | XC3S200A XC3S400A |
|---|---|---|---|
| N16 | 1 | IO_L03N_1 | IO_L03N_1/A1 |
| P16 | | IO_L03P_1 | IO_L03P_1/A0 |
| J13 | | IO_L10N_1 | IO_L10N_1/A9 |
| J12 | | IO_L10P_1 | IO_L10P_1/A8 |
| F13 | | IO_L20N_1 | IO_L20N_1/A19 |
| E14 | | IO_L20P_1 | IO_L20P_1/A18 |
| D15 | | IO_L22N_1 | IO_L22N_1/A21 |
| D16 | | IO_L22P_1 | IO_L22P_1/A20 |
| D14 | | IO_L23N_1 | IO_L23N_1/A23 |
| E13 | | IO_L23P_1 | IO_L23P_1/A22 |
| C15 | | IO_L24N_1 | IO_L24N_1/A25 |
| C16 | | IO_L24P_1 | IO_L24P_1/A24 |

*Table 77:* **Spartan-3A FG320 Pinout*(Continued)***

| Bank | Pin Name | FG320 Ball | Type |
|---|---|---|---|
| 3 | IO_L10N_3/VREF_3 | F1 | VREF |
| 3 | IO_L10P_3 | F2 | I/O |
| 3 | IO_L11N_3 | J6 | I/O |
| 3 | IO_L11P_3 | J7 | I/O |
| 3 | IO_L13N_3 | H1 | I/O |
| 3 | IO_L13P_3 | H2 | I/O |
| 3 | IO_L14N_3/LHCLK1 | J3 | LHCLK |
| 3 | IO_L14P_3/LHCLK0 | H3 | LHCLK |
| 3 | IO_L15N_3/IRDY2/LHCLK3 | J1 | LHCLK |
| 3 | IO_L15P_3/LHCLK2 | J2 | LHCLK |
| 3 | IO_L17N_3/LHCLK5 | K5 | LHCLK |
| 3 | IO_L17P_3/LHCLK4 | J4 | LHCLK |
| 3 | IO_L18N_3/LHCLK7 | K3 | LHCLK |
| 3 | IO_L18P_3/TRDY2/LHCLK6 | K2 | LHCLK |
| 3 | IO_L19N_3 | L2 | I/O |
| 3 | IO_L19P_3/VREF_3 | L1 | VREF |
| 3 | IO_L21N_3 | M2 | I/O |
| 3 | IO_L21P_3 | N1 | I/O |
| 3 | IO_L22N_3 | N2 | I/O |
| 3 | IO_L22P_3 | P1 | I/O |
| 3 | IO_L23N_3 | L4 | I/O |
| 3 | IO_L23P_3 | L3 | I/O |
| 3 | IO_L25N_3 | R2 | I/O |
| 3 | IO_L25P_3 | R1 | I/O |
| 3 | IO_L26N_3 | N4 | I/O |
| 3 | IO_L26P_3 | N3 | I/O |
| 3 | IO_L27N_3 | T2 | I/O |
| 3 | IO_L27P_3 | T1 | I/O |
| 3 | IO_L29N_3 | N6 | I/O |
| 3 | IO_L29P_3 | N5 | I/O |
| 3 | IO_L30N_3 | R3 | I/O |
| 3 | IO_L30P_3 | P3 | I/O |
| 3 | IO_L31N_3 | U2 | I/O |
| 3 | IO_L31P_3 | U1 | I/O |
| 3 | IP_L04N_3/VREF_3 | H7 | VREF |
| 3 | IP_L04P_3 | G6 | INPUT |
| 3 | IP_L08N_3/VREF_3 | H5 | VREF |
| 3 | IP_L08P_3 | H6 | INPUT |
| 3 | IP_L12N_3 | G2 | INPUT |
| 3 | IP_L12P_3 | G3 | INPUT |

*Table 77:* **Spartan-3A FG320 Pinout*(Continued)***

| Bank | Pin Name | FG320 Ball | Type |
|---|---|---|---|
| 3 | IP_L16N_3 | K6 | INPUT |
| 3 | IP_L16P_3 | J5 | INPUT |
| 3 | IP_L20N_3 | L6 | INPUT |
| 3 | IP_L20P_3 | L7 | INPUT |
| 3 | IP_L24N_3 | M4 | INPUT |
| 3 | IP_L24P_3 | M3 | INPUT |
| 3 | IP_L28N_3 | M5 | INPUT |
| 3 | IP_L28P_3 | M6 | INPUT |
| 3 | IP_L32N_3/VREF_3 | P4 | VREF |
| 3 | IP_L32P_3 | P5 | INPUT |
| 3 | VCCO_3 | E2 | VCCO |
| 3 | VCCO_3 | H4 | VCCO |
| 3 | VCCO_3 | L5 | VCCO |
| 3 | VCCO_3 | P2 | VCCO |
| GND | GND | A1 | GND |
| GND | GND | A7 | GND |
| GND | GND | A12 | GND |
| GND | GND | A18 | GND |
| GND | GND | C10 | GND |
| GND | GND | D4 | GND |
| GND | GND | D7 | GND |
| GND | GND | D15 | GND |
| GND | GND | F6 | GND |
| GND | GND | G1 | GND |
| GND | GND | G12 | GND |
| GND | GND | G18 | GND |
| GND | GND | H8 | GND |
| GND | GND | H10 | GND |
| GND | GND | J11 | GND |
| GND | GND | J15 | GND |
| GND | GND | K4 | GND |
| GND | GND | K8 | GND |
| GND | GND | L9 | GND |
| GND | GND | L11 | GND |
| GND | GND | M1 | GND |
| GND | GND | M7 | GND |
| GND | GND | M18 | GND |
| GND | GND | N13 | GND |
| GND | GND | R4 | GND |
| GND | GND | R12 | GND |

*Table 81:* **Spartan-3A FG400 Pinout*(Continued)***

| Bank | Pin Name | FG400 Ball | Type |
|---|---|---|---|
| 2 | IO_L28P_2 | Y16 | I/O |
| 2 | IO_L29N_2 | U16 | I/O |
| 2 | IO_L29P_2 | V16 | I/O |
| 2 | IO_L30N_2 | Y18 | I/O |
| 2 | IO_L30P_2 | Y17 | I/O |
| 2 | IO_L31N_2 | U17 | I/O |
| 2 | IO_L31P_2 | V17 | I/O |
| 2 | IO_L32N_2/CCLK | Y19 | DUAL |
| 2 | IO_L32P_2/D0/DIN/MISO | W18 | DUAL |
| 2 | IP_2 | P9 | INPUT |
| 2 | IP_2 | P12 | INPUT |
| 2 | IP_2 | P13 | INPUT |
| 2 | IP_2 | R8 | INPUT |
| 2 | IP_2 | R10 | INPUT |
| 2 | IP_2 | T11 | INPUT |
| 2 | IP_2/VREF_2 | N9 | VREF |
| 2 | IP_2/VREF_2 | N12 | VREF |
| 2 | IP_2/VREF_2 | P8 | VREF |
| 2 | IP_2/VREF_2 | P10 | VREF |
| 2 | IP_2/VREF_2 | P11 | VREF |
| 2 | IP_2/VREF_2 | R14 | VREF |
| 2 | VCCO_2 | R11 | VCCO |
| 2 | VCCO_2 | U8 | VCCO |
| 2 | VCCO_2 | U14 | VCCO |
| 2 | VCCO_2 | W5 | VCCO |
| 2 | VCCO_2 | W11 | VCCO |
| 2 | VCCO_2 | W17 | VCCO |
| 3 | IO_L01N_3 | D3 | I/O |
| 3 | IO_L01P_3 | D4 | I/O |
| 3 | IO_L02N_3 | C2 | I/O |
| 3 | IO_L02P_3 | B1 | I/O |
| 3 | IO_L03N_3 | D2 | I/O |
| 3 | IO_L03P_3 | C1 | I/O |
| 3 | IO_L05N_3 | E1 | I/O |
| 3 | IO_L05P_3 | D1 | I/O |
| 3 | IO_L06N_3 | G5 | I/O |
| 3 | IO_L06P_3 | F4 | I/O |
| 3 | IO_L07N_3 | J5 | I/O |
| 3 | IO_L07P_3 | J6 | I/O |
| 3 | IO_L08N_3 | H4 | I/O |

*Table 81:* **Spartan-3A FG400 Pinout*(Continued)***

| Bank | Pin Name | FG400 Ball | Type |
|---|---|---|---|
| 3 | IO_L08P_3 | H6 | I/O |
| 3 | IO_L09N_3 | G4 | I/O |
| 3 | IO_L09P_3 | F3 | I/O |
| 3 | IO_L10N_3 | F2 | I/O |
| 3 | IO_L10P_3 | E3 | I/O |
| 3 | IO_L12N_3 | H2 | I/O |
| 3 | IO_L12P_3 | G3 | I/O |
| 3 | IO_L13N_3/VREF_3 | G1 | VREF |
| 3 | IO_L13P_3 | F1 | I/O |
| 3 | IO_L14N_3 | H3 | I/O |
| 3 | IO_L14P_3 | J4 | I/O |
| 3 | IO_L16N_3 | J2 | I/O |
| 3 | IO_L16P_3 | J3 | I/O |
| 3 | IO_L17N_3/LHCLK1 | K2 | LHCLK |
| 3 | IO_L17P_3/LHCLK0 | J1 | LHCLK |
| 3 | IO_L18N_3/IRDY2/LHCLK3 | L3 | LHCLK |
| 3 | IO_L18P_3/LHCLK2 | K3 | LHCLK |
| 3 | IO_L20N_3/LHCLK5 | L5 | LHCLK |
| 3 | IO_L20P_3/LHCLK4 | K4 | LHCLK |
| 3 | IO_L21N_3/LHCLK7 | M1 | LHCLK |
| 3 | IO_L21P_3/TRDY2/LHCLK6 | L1 | LHCLK |
| 3 | IO_L22N_3 | M3 | I/O |
| 3 | IO_L22P_3/VREF_3 | M2 | VREF |
| 3 | IO_L24N_3 | M5 | I/O |
| 3 | IO_L24P_3 | M4 | I/O |
| 3 | IO_L25N_3 | N2 | I/O |
| 3 | IO_L25P_3 | N1 | I/O |
| 3 | IO_L26N_3 | N4 | I/O |
| 3 | IO_L26P_3 | N3 | I/O |
| 3 | IO_L28N_3 | R1 | I/O |
| 3 | IO_L28P_3 | P1 | I/O |
| 3 | IO_L29N_3 | P4 | I/O |
| 3 | IO_L29P_3 | P3 | I/O |
| 3 | IO_L30N_3 | R3 | I/O |
| 3 | IO_L30P_3 | R2 | I/O |
| 3 | IO_L32N_3 | T2 | I/O |
| 3 | IO_L32P_3/VREF_3 | T1 | VREF |
| 3 | IO_L33N_3 | R4 | I/O |
| 3 | IO_L33P_3 | T3 | I/O |
| 3 | IO_L34N_3 | U3 | I/O |

*Table 81:* **Spartan-3A FG400 Pinout*(Continued)***

| Bank | Pin Name | FG400 Ball | Type |
|---|---|---|---|
| 3 | IO_L34P_3 | U1 | I/O |
| 3 | IO_L36N_3 | T4 | I/O |
| 3 | IO_L36P_3 | R5 | I/O |
| 3 | IO_L37N_3 | V2 | I/O |
| 3 | IO_L37P_3 | V1 | I/O |
| 3 | IO_L38N_3 | W2 | I/O |
| 3 | IO_L38P_3 | W1 | I/O |
| 3 | IP_3 | H7 | INPUT |
| 3 | IP_L04N_3/VREF_3 | G6 | VREF |
| 3 | IP_L04P_3 | G7 | INPUT |
| 3 | IP_L11N_3/VREF_3 | J7 | VREF |
| 3 | IP_L11P_3 | J8 | INPUT |
| 3 | IP_L15N_3 | K7 | INPUT |
| 3 | IP_L15P_3 | K8 | INPUT |
| 3 | IP_L19N_3 | K5 | INPUT |
| 3 | IP_L19P_3 | K6 | INPUT |
| 3 | IP_L23N_3 | L6 | INPUT |
| 3 | IP_L23P_3 | L7 | INPUT |
| 3 | IP_L27N_3 | M7 | INPUT |
| 3 | IP_L27P_3 | M8 | INPUT |
| 3 | IP_L31N_3 | N7 | INPUT |
| 3 | IP_L31P_3 | M6 | INPUT |
| 3 | IP_L35N_3 | N6 | INPUT |
| 3 | IP_L35P_3 | P5 | INPUT |
| 3 | IP_L39N_3/VREF_3 | P7 | VREF |
| 3 | IP_L39P_3 | P6 | INPUT |
| 3 | VCCO_3 | E2 | VCCO |
| 3 | VCCO_3 | H5 | VCCO |
| 3 | VCCO_3 | L2 | VCCO |
| 3 | VCCO_3 | N5 | VCCO |
| 3 | VCCO_3 | U2 | VCCO |
| GND | GND | A1 | GND |
| GND | GND | A11 | GND |
| GND | GND | A20 | GND |
| GND | GND | B6 | GND |
| GND | GND | B14 | GND |
| GND | GND | C3 | GND |
| GND | GND | C18 | GND |
| GND | GND | D9 | GND |
| GND | GND | E5 | GND |

*Table 81:* **Spartan-3A FG400 Pinout*(Continued)***

| Bank | Pin Name | FG400 Ball | Type |
|---|---|---|---|
| GND | GND | E12 | GND |
| GND | GND | F15 | GND |
| GND | GND | G2 | GND |
| GND | GND | G19 | GND |
| GND | GND | H8 | GND |
| GND | GND | H13 | GND |
| GND | GND | J9 | GND |
| GND | GND | J11 | GND |
| GND | GND | K1 | GND |
| GND | GND | K10 | GND |
| GND | GND | K12 | GND |
| GND | GND | K17 | GND |
| GND | GND | L4 | GND |
| GND | GND | L9 | GND |
| GND | GND | L11 | GND |
| GND | GND | L20 | GND |
| GND | GND | M10 | GND |
| GND | GND | M12 | GND |
| GND | GND | N8 | GND |
| GND | GND | N11 | GND |
| GND | GND | N13 | GND |
| GND | GND | P2 | GND |
| GND | GND | P19 | GND |
| GND | GND | R6 | GND |
| GND | GND | R9 | GND |
| GND | GND | T16 | GND |
| GND | GND | U12 | GND |
| GND | GND | V3 | GND |
| GND | GND | V18 | GND |
| GND | GND | W7 | GND |
| GND | GND | W15 | GND |
| GND | GND | Y1 | GND |
| GND | GND | Y10 | GND |
| GND | GND | Y20 | GND |
| VCCAUX | SUSPEND | R15 | PWR MGMT |
| VCCAUX | DONE | W19 | CONFIG |
| VCCAUX | PROG_B | D5 | CONFIG |
| VCCAUX | TCK | A19 | JTAG |
| VCCAUX | TDI | F5 | JTAG |

*Table 87:* **Spartan-3A FG676 Pinout*(Continued)***

| Bank | Pin Name | FG676 Ball | Type |
|---|---|---|---|
| 2 | IP_2 | AD10 | INPUT |
| 2 | IP_2 | AD16 | INPUT |
| 2 | IP_2 | AF2 | INPUT |
| 2 | IP_2 | AF7 | INPUT |
| 2 | IP_2 | Y11 | INPUT |
| 2 | IP_2/VREF_2 | AA9 | VREF |
| 2 | IP_2/VREF_2 | AA20 | VREF |
| 2 | IP_2/VREF_2 | AB6 | VREF |
| 2 | IP_2/VREF_2 | AB10 | VREF |
| 2 | IP_2/VREF_2 | AC10 | VREF |
| 2 | IP_2/VREF_2 | AD12 | VREF |
| 2 | IP_2/VREF_2 | AF15 | VREF |
| 2 | IP_2/VREF_2 | AF17 | VREF |
| 2 | IP_2/VREF_2 | AF22 | VREF |
| 2 | IP_2/VREF_2 | Y16 | VREF |
| 2 | N.C. (◆) | AA8 | N.C. |
| 2 | N.C. (◆) | AC5 | N.C. |
| 2 | N.C. (◆) | AC22 | N.C. |
| 2 | N.C. (◆) | AD5 | N.C. |
| 2 | N.C. (◆) | Y18 | N.C. |
| 2 | N.C. (◆) | Y19 | N.C. |
| 2 | N.C. (◆) | AD23 | N.C. |
| 2 | N.C. (◆) | W18 | N.C. |
| 2 | N.C. (◆) | Y8 | N.C. |
| 2 | VCCO_2 | AB8 | VCCO |
| 2 | VCCO_2 | AB14 | VCCO |
| 2 | VCCO_2 | AB19 | VCCO |
| 2 | VCCO_2 | AE5 | VCCO |
| 2 | VCCO_2 | AE11 | VCCO |
| 2 | VCCO_2 | AE16 | VCCO |
| 2 | VCCO_2 | AE22 | VCCO |
| 2 | VCCO_2 | W11 | VCCO |
| 2 | VCCO_2 | W16 | VCCO |
| 3 | IO_L01N_3 | J9 | I/O |
| 3 | IO_L01P_3 | J8 | I/O |
| 3 | IO_L02N_3 | B1 | I/O |
| 3 | IO_L02P_3 | B2 | I/O |
| 3 | IO_L03N_3 | H7 | I/O |
| 3 | IO_L03P_3 | G6 | I/O |
| 3 | IO_L05N_3 | K8 | I/O |

*Table 87:* **Spartan-3A FG676 Pinout*(Continued)***

| Bank | Pin Name | FG676 Ball | Type |
|---|---|---|---|
| 3 | IO_L05P_3 | K9 | I/O |
| 3 | IO_L06N_3 | E4 | I/O |
| 3 | IO_L06P_3 | D3 | I/O |
| 3 | IO_L07N_3 | F4 | I/O |
| 3 | IO_L07P_3 | E3 | I/O |
| 3 | IO_L09N_3 | G4 | I/O |
| 3 | IO_L09P_3 | F5 | I/O |
| 3 | IO_L10N_3 | H6 | I/O |
| 3 | IO_L10P_3 | J7 | I/O |
| 3 | IO_L11N_3 | F2 | I/O |
| 3 | IO_L11P_3 | E1 | I/O |
| 3 | IO_L13N_3 | J6 | I/O |
| 3 | IO_L13P_3 | K7 | I/O |
| 3 | IO_L14N_3 | F3 | I/O |
| 3 | IO_L14P_3 | G3 | I/O |
| 3 | IO_L15N_3 | L9 | I/O |
| 3 | IO_L15P_3 | L10 | I/O |
| 3 | IO_L17N_3 | H1 | I/O |
| 3 | IO_L17P_3 | H2 | I/O |
| 3 | IO_L18N_3 | L7 | I/O |
| 3 | IO_L18P_3 | K6 | I/O |
| 3 | IO_L19N_3 | J4 | I/O |
| 3 | IO_L19P_3 | J5 | I/O |
| 3 | IO_L21N_3 | M9 | I/O |
| 3 | IO_L21P_3 | M10 | I/O |
| 3 | IO_L22N_3 | K4 | I/O |
| 3 | IO_L22P_3 | K5 | I/O |
| 3 | IO_L23N_3 | K2 | I/O |
| 3 | IO_L23P_3 | K3 | I/O |
| 3 | IO_L25N_3 | L3 | I/O |
| 3 | IO_L25P_3 | L4 | I/O |
| 3 | IO_L26N_3 | M7 | I/O |
| 3 | IO_L26P_3 | M8 | I/O |
| 3 | IO_L27N_3 | M3 | I/O |
| 3 | IO_L27P_3 | M4 | I/O |
| 3 | IO_L28N_3 | M6 | I/O |
| 3 | IO_L28P_3 | M5 | I/O |
| 3 | IO_L29N_3/VREF_3 | M1 | VREF |
| 3 | IO_L29P_3 | M2 | I/O |
| 3 | IO_L30N_3 | N4 | I/O |