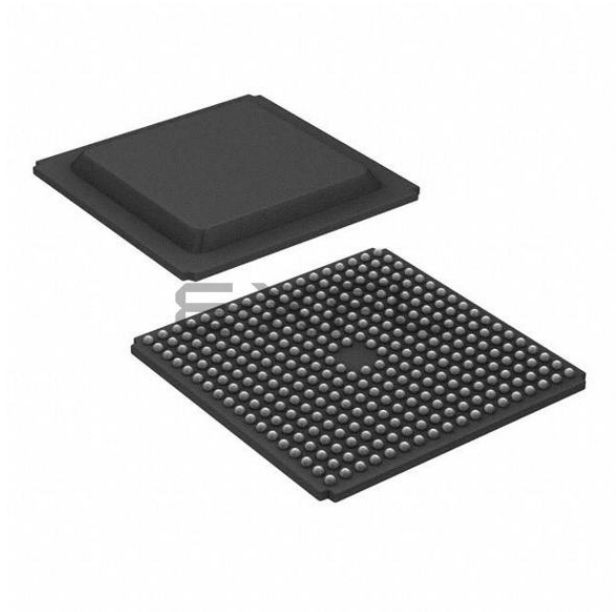

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	448
Number of Logic Elements/Cells	4032
Total RAM Bits	294912
Number of I/O	248
Number of Gates	200000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	320-BGA
Supplier Device Package	320-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s200a-4fgg320c

Configuration

Spartan-3A FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored externally in a PROM or some other non-volatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of seven different modes:

- Master Serial from a Xilinx Platform Flash PROM
- Serial Peripheral Interface (SPI) from an industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary Scan (JTAG), typically downloaded from a processor or system tester

Furthermore, Spartan-3A FPGAs support MultiBoot configuration, allowing two or more FPGA configuration bitstreams to be stored in a single SPI serial Flash or a BPI parallel NOR Flash. The FPGA application controls which configuration to load next and when to load it.

Additionally, each Spartan-3A FPGA contains a unique, factory-programmed Device DNA identifier useful for tracking purposes, anti-cloning designs, or IP protection.

I/O Capabilities

The Spartan-3A FPGA SelectIO interface supports many popular single-ended and differential standards. Table 2 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination. Some of the user I/Os are unidirectional input-only pins as indicated in Table 2.

Spartan-3A FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3.3V PCI at 33 MHz or 66 MHz
- HSTL I, II, and III at 1.5V and 1.8V, commonly used in memory applications
- SSTL I and II at 1.8V, 2.5V, and 3.3V, commonly used for memory applications

Spartan-3A FPGAs support the following differential standards:

- LVDS, mini-LVDS, RSDS, and PPDS I/O at 2.5V or 3.3V
- Bus LVDS I/O at 2.5V
- TMDS I/O at 3.3V
- Differential HSTL and SSTL I/O
- LVPECL inputs at 2.5V or 3.3V

Table 2: **Available User I/Os and Differential (Diff) I/O Pairs**

Package	VQ100 VQG100		TQ144 TQG144		FT256 FTG256		FG320 FGG320		FG400 FGG400		FG484 FGG484		FG676 FGG676	
Body Size (mm)	14 x 14(2)		20 x 20(2)		17 x 17		19 x 19		21 x 21		23 x 23		27 x 27	
Device	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff
XC3S50A	**68** *(13)*	**60** *(24)*	**108** *(7)*	**50** *(24)*	**144** *(32)*	**64** *(32)*	-	-	-	-	-	-	-	-
XC3S200A	**68** *(13)*	**60** *(24)*	-	-	**195** *(35)*	**90** *(50)*	**248** *(56)*	**112** *(64)*	-	-	-	-	-	-
XC3S400A	-	-	-	-	**195** *(35)*	**90** *(50)*	**251** *(59)*	**112** *(64)*	**311** *(63)*	**142** *(78)*	-	-	-	-
XC3S700A	-	-	-	-	**161** *(13)*	**74** *(36)*	-	-	**311** *(63)*	**142** *(78)*	**372** *(84)*	**165** *(93)*	-	-
XC3S1400A	-	-	-	-	**161** *(13)*	**74** *(36)*	-	-	-	-	**375** *(87)*	**165** *(93)*	**502** *(94)*	**227** *(131)*

Notes:

1. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in (*italics*) indicates the number of input-only pins. The differential (Diff) input-only pin count includes both differential pairs on input-only pins and differential pairs on I/O pins within I/O banks that are restricted to differential inputs.
2. The footprints for the VQ/TQ packages are larger than the package body. See the Package Drawings for details.

Table 22: **Propagation Times for the IOB Input Path *(Continued)***

Symbol	Description	Conditions	DELAY_VALUE	Device	Speed Grade		Units
					-5	-4	
					Max	Max	
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25(2)	5	XC3S400A	3.55	4.18	ns
			6		4.34	5.03	ns
			7		5.09	5.88	ns
			8		5.58	6.42	ns
			1	XC3S700A	1.96	2.18	ns
			2		2.76	3.06	ns
			3		3.45	3.95	ns
			4		3.97	4.54	ns
			5		3.83	4.37	ns
			6		4.74	5.42	ns
			7		5.53	6.33	ns
			8		6.06	6.96	ns
			1	XC3S1400A	1.93	2.40	ns
			2		2.69	3.15	ns
			3		3.52	3.99	ns
			4		3.89	4.55	ns
			5		3.95	4.42	ns
			6		4.53	5.32	ns
			7		5.30	6.21	ns
			8		5.83	6.80	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 23.

Table 26: **Output Timing Adjustments for IOB*(Continued)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Differential Standards			
LVDS_25	1.16	1.16	ns
LVDS_33	0.46	0.46	ns
BLVDS_25	0.11	0.11	ns
MINI_LVDS_25	0.75	0.75	ns
MINI_LVDS_33	0.40	0.40	ns
LVPECL_25	Input Only		
LVPECL_33			
RSDS_25	1.42	1.42	ns
RSDS_33	0.58	0.58	ns
TMDS_33	0.46	0.46	ns
PPDS_25	1.07	1.07	ns
PPDS_33	0.63	0.63	ns
DIFF_HSTL_I_18	0.43	0.43	ns
DIFF_HSTL_II_18	0.41	0.41	ns
DIFF_HSTL_III_18	0.36	0.36	ns
DIFF_HSTL_I	1.01	1.01	ns
DIFF_HSTL_III	0.54	0.54	ns
DIFF_SSTL18_I	0.49	0.49	ns
DIFF_SSTL18_II	0.41	0.41	ns
DIFF_SSTL2_I	0.82	0.82	ns
DIFF_SSTL2_II	0.09	0.09	ns
DIFF_SSTL3_I	1.16	1.16	ns
DIFF_SSTL3_II	0.28	0.28	ns

Notes:

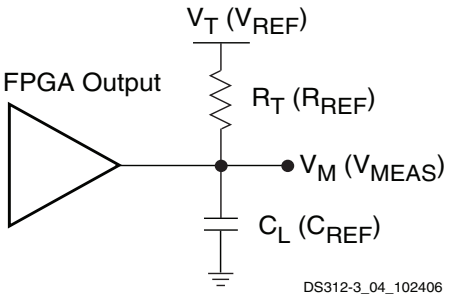
1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8, Table 11, and Table 13.
2. These adjustments are used to convert output- and three-state-path times originally specified for the LVCMOS25 standard with 12 mA drive and Fast slew rate to times that correspond to other signal standards. Do not adjust times that measure when outputs go into a high-impedance state.
3. Note that 16 mA drive is faster than 24 mA drive for the Slow slew rate.

Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 27 lists the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H.

The Output test setup is shown in Figure 9. A termination voltage V_T is applied to the termination resistor R_T, the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (for example, LVCMOS, LVTTL), then R_T is set to 1MΩ to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



Notes:

1. The names shown in parentheses are used in the IBIS file.

Figure 9: **Output Test Setup**

Table 27: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended							
LVTTL		-	0	3.3	1M	0	1.4
LVCMOS33		-	0	3.3	1M	0	1.65
LVCMOS25		-	0	2.5	1M	0	1.25
LVCMOS18		-	0	1.8	1M	0	0.9
LVCMOS15		-	0	1.5	1M	0	0.75
LVCMOS12		-	0	1.2	1M	0	0.6
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
PCI66_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
HSTL_I		0.75	V_{REF} – 0.5	V_{REF} + 0.5	50	0.75	V_{REF}
HSTL_III		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	1.5	V_{REF}
HSTL_I_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_II_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL18_II		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
SSTL2_II		1.25	V_{REF} – 0.75	V_{REF} + 0.75	25	1.25	V_{REF}
SSTL3_I		1.5	V_{REF} – 0.75	V_{REF} + 0.75	50	1.5	V_{REF}
SSTL3_II		1.5	V_{REF} – 0.75	V_{REF} + 0.75	25	1.5	V_{REF}

Using IBIS Models to Simulate Load Conditions in Application

IBIS models permit the most accurate prediction of timing delays for a given application. The parameters found in the IBIS model (V_{REF}, R_{REF}, and V_{MEAS}) correspond directly with the parameters used in Table 27 (V_T, R_T, and V_M). Do not confuse V_{REF} (the termination voltage) from the IBIS model with V_{REF} (the input-switching threshold) from the table. A fourth parameter, C_{REF}, is always zero. The four parameters describe all relevant output test conditions. IBIS models are found in the Xilinx development software as well as at the following link:

www.xilinx.com/support/download/index.htm

Delays for a given application are simulated according to its specific load conditions as follows:

1. Simulate the desired signal standard with the output driver connected to the test setup shown in Figure 9. Use parameter values V_T, R_T, and V_M from Table 27. C_{REF} is zero.
2. Record the time to V_M.
3. Simulate the same signal standard with the output driver connected to the PCB trace with load. Use the appropriate IBIS model (including V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} values) or capacitive value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. Add (or subtract) the increase (or decrease) in delay to (or from) the appropriate Output standard adjustment (Table 26) to yield the worst-case delay of the PCB trace.

Simultaneously Switching Output Guidelines

This section provides guidelines for the recommended maximum allowable number of Simultaneous Switching Outputs (SSOs). These guidelines describe the maximum number of user I/O pins of a given output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of ground and power bounce.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common voltage rail. Low-to-High transitions conduct to the V_{CCO} rail; High-to-Low transitions conduct to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the die pad and the power supply or ground return. The inductance is associated with bonding wires, the package lead frame, and any other signal routing inside the package. Other variables contribute to SSO noise levels, including stray inductance on the PCB as well as capacitive loading at receivers. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

Table 28 and Table 29 provide the essential SSO guidelines. For each device/package combination, Table 28 provides the number of equivalent V_{CCO}/GND pairs. The equivalent number of pairs is based on characterization and may not match the physical number of pairs. For each output signal standard and drive strength, Table 29 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The guidelines in Table 29 are categorized by package style, slew rate, and output drive current. Furthermore, the number of SSOs is specified by I/O bank. Generally, the left and right I/O banks (Banks 1 and 3) support higher output drive current.

Multiply the appropriate numbers from Table 28 and Table 29 to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines might result in increased power or ground bounce, degraded signal integrity, or increased system jitter.

SSO_{MAX}/IO Bank = Table 28 x Table 29

The recommended maximum SSO values assume that the FPGA is soldered on the printed circuit board and that the board uses sound design practices. The SSO values do not apply for FPGAs mounted in sockets, due to the lead inductance introduced by the socket.

The SSO values assume that the V_{CCAUX} is powered at 3.3V. Setting V_{CCAUX} to 2.5V provides better SSO characteristics.

The number of SSOs allowed for quad-flat packages (VQ/TQ) is lower than for ball grid array packages (FG) due to the larger lead inductance of the quad-flat packages. Ball grid array packages are recommended for applications with a large number of simultaneously switching outputs.

Table 29: **Recommended Number of Simultaneously Switching Outputs per VCCO-GND Pair (V_{CCAUX}=3.3V)*(Continued)***

Signal Standard (IOSTANDARD)	Package Type			
	VQ100, TQ144		FT256, FG320, FG400, FG484, FG676	
	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)
Differential Standards (Number of I/O *Pairs* or Channels)				
LVDS_25	8	–	22	–
LVDS_33	8	–	27	–
BLVDS_25	1	1	4	4
MINI_LVDS_25	8	–	22	–
MINI_LVDS_33	8	–	27	–
LVPECL_25	Input Only			
LVPECL_33	Input Only			
RSDS_25	8	–	22	–
RSDS_33	8	–	27	–
TMDS_33	8	–	27	–
PPDS_25	8	–	22	–
PPDS_33	8	–	27	–
DIFF_HSTL_I	–	5	–	10
DIFF_HSTL_III	–	3	–	4
DIFF_HSTL_I_18	6	6	8	8
DIFF_HSTL_II_18	–	2	–	2
DIFF_HSTL_III_18	4	4	5	4
DIFF_SSTL18_I	3	6	3	7
DIFF_SSTL18_II	–	4	–	4
DIFF_SSTL2_I	5	5	9	9
DIFF_SSTL2_II	–	3	–	4
DIFF_SSTL3_I	3	4	4	5
DIFF_SSTL3_II	2	3	3	3

Notes:

1. Not all I/O standards are supported on all I/O banks. The left and right banks (I/O banks 1 and 3) support higher output drive current than the top and bottom banks (I/O banks 0 and 2). Similarly, true differential output standards, such as LVDS, RSDS, PPDS, miniLVDS, and TMDS, are only supported in top or bottom banks (I/O banks 0 and 2). Refer to UG331: *Spartan-3 Generation FPGA User Guide* for additional information.
2. The numbers in this table are recommendations that assume sound board lay out practice. Test limits are the V_{IL}/V_{IH} voltage limits for the respective I/O standard.
3. If more than one signal standard is assigned to the I/Os of a given bank, refer to XAPP689: *Managing Ground Bounce in Large FPGAs* for information on how to perform weighted average SSO calculations.

Block RAM Timing

Table 35: **Block RAM Timing**

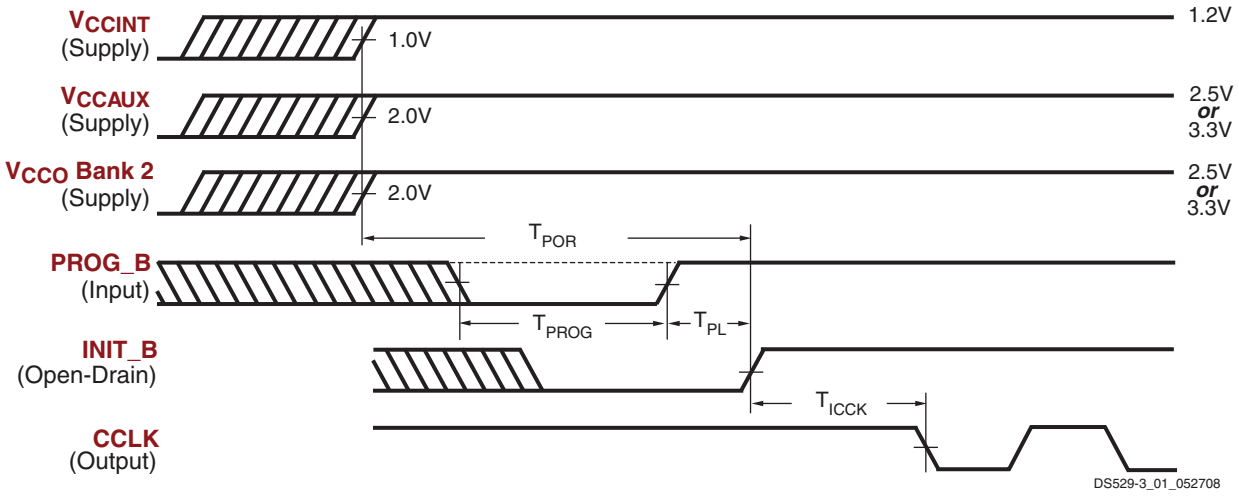
Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{RCKO}	When reading from block RAM, the delay from the active transition at the CLK input to data appearing at the DOUT output	–	2.06	–	2.49	ns
Setup Times						
T_{RCCK_ADDR}	Setup time for the ADDR inputs before the active transition at the CLK input of the block RAM	0.32	–	0.36	–	ns
T_{RDCK_DIB}	Setup time for data at the DIN inputs before the active transition at the CLK input of the block RAM	0.28	–	0.31	–	ns
T_{RCCK_ENB}	Setup time for the EN input before the active transition at the CLK input of the block RAM	0.69	–	0.77	–	ns
T_{RCCK_WEB}	Setup time for the WE input before the active transition at the CLK input of the block RAM	1.12	–	1.26	–	ns
Hold Times						
T_{RCKC_ADDR}	Hold time on the ADDR inputs after the active transition at the CLK input	0	–	0	–	ns
T_{RCKD_DIB}	Hold time on the DIN inputs after the active transition at the CLK input	0	–	0	–	ns
T_{RCKC_ENB}	Hold time on the EN input after the active transition at the CLK input	0	–	0	–	ns
T_{RCKC_WEB}	Hold time on the WE input after the active transition at the CLK input	0	–	0	–	ns
Clock Timing						
T_{BPWH}	High pulse width of the CLK signal	1.56	–	1.79	–	ns
T_{BPWL}	Low pulse width of the CLK signal	1.56	–	1.79	–	ns
Clock Frequency						
F_{BRAM}	Block RAM clock frequency	0	320	0	280	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.

Configuration and JTAG Timing

General Configuration Power-On/Reconfigure Timing



Notes:

1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies can be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 11: **Waveforms for Power-On and the Beginning of Configuration**

Table 45: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	All	–	18	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	-	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XC3S50A	–	0.5	ms
		XC3S200A	–	0.5	ms
		XC3S400A	–	1	ms
		XC3S700A	–	2	ms
		XC3S1400A	–	2	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	250	–	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, and BPI modes.
4. For details on configuration, see UG332 *Spartan-3 Generation Configuration User Guide*.

Serial Peripheral Interface (SPI) Configuration Timing

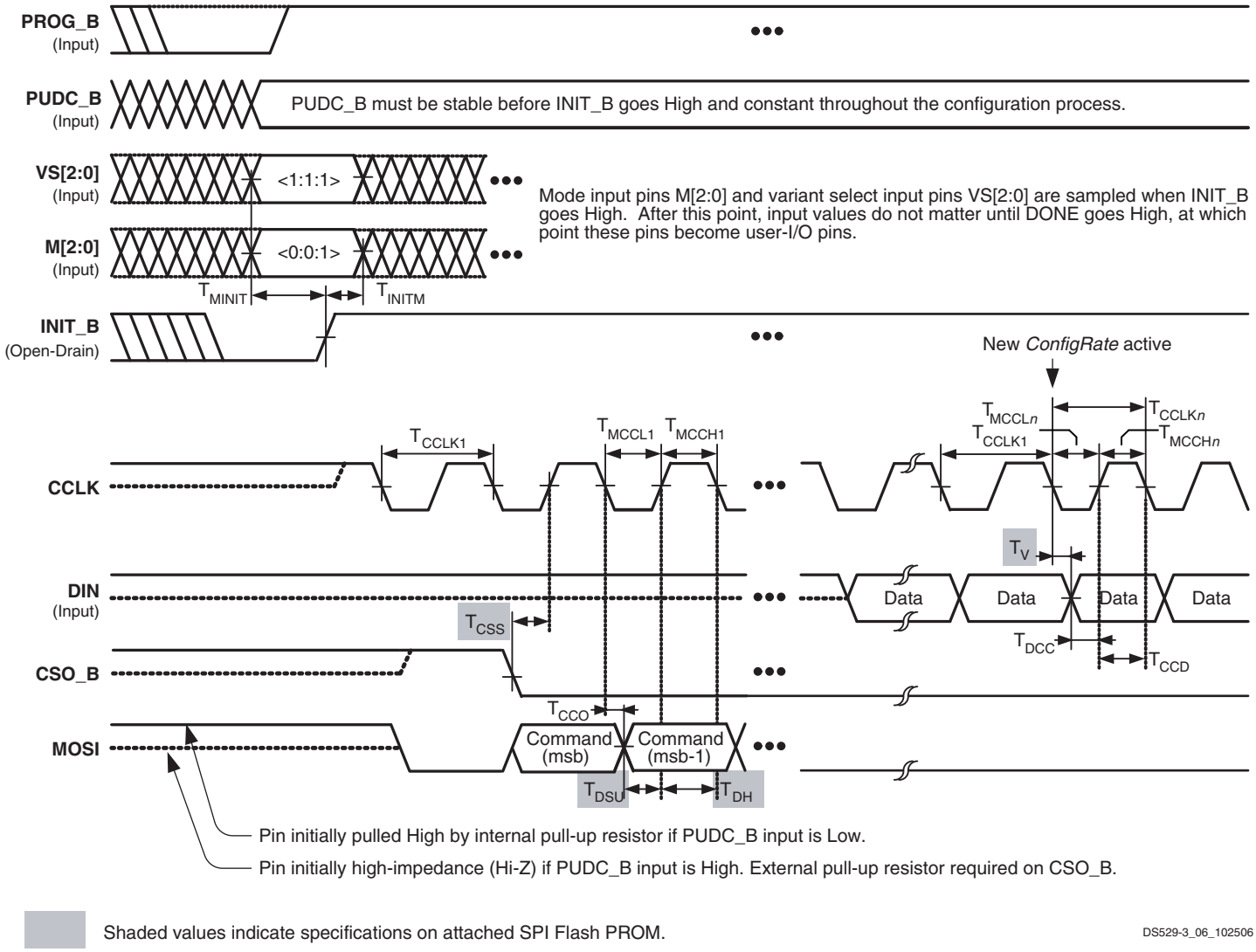


Figure 14: **Waveforms for Serial Peripheral Interface (SPI) Configuration**

Table 52: **Timing for Serial Peripheral Interface (SPI) Configuration Mode**

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	See Table 46		
T_{CCLKn}	CCLK clock period after FPGA loads ***ConfigRate*** bitstream option setting	See Table 46		
T_{MINIT}	Setup time on VS[2:0] variant-select pins and M[2:0] mode pins before the rising edge of INIT_B	50	–	ns
T_{INITM}	Hold time on VS[2:0] variant-select pins and M[2:0] mode pins after the rising edge of INIT_B	0	–	ns
T_{CCO}	MOSI output valid delay after CCLK falling clock edge	See Table 50		
T_{DCC}	Setup time on the DIN data input before CCLK rising clock edge	See Table 50		
T_{CCD}	Hold time on the DIN data input after CCLK rising clock edge	See Table 50		

Table 53: **Configuration Timing Requirements for Attached SPI Serial Flash**

Symbol	Description	Requirement	Units
T_{CCS}	SPI serial Flash PROM chip-select time	$T_{CCS} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DSU}	SPI serial Flash PROM data input setup time	$T_{DSU} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DH}	SPI serial Flash PROM data input hold time	$T_{DH} \leq T_{MCCH1}$	ns
T_V	SPI serial Flash PROM data clock-to-output time	$T_V \leq T_{MCCLn} - T_{DCC}$	ns
f_C or f_R	Maximum SPI serial Flash PROM clock frequency (also depends on specific read command used)	$f_C \geq \frac{1}{T_{CCLKn(min)}}$	MHz

Notes:

1. These requirements are for successful FPGA configuration in SPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.

Introduction

This section describes how the various pins on a Spartan®-3A FPGA connect within the supported component packages, and provides device-specific thermal characteristics. For general information on the pin functions and the package characteristics, see the Packaging section of UG331: *Spartan-3 Generation FPGA User Guide*.

- **UG331: Spartan-3 Generation FPGA User Guide**
  www.xilinx.com/support/documentation/user_guides/ug331.pdf

Spartan-3A FPGAs are available in both standard and Pb-free, RoHS versions of each package, with the Pb-free version adding a "G" to the middle of the package code. Except for the thermal characteristics, all information for the standard package applies equally to the Pb-free package.

Pin Types

Most pins on a Spartan-3A FPGA are general-purpose, user-defined I/O pins. There are, however, up to 12 different functional types of pins on Spartan-3A FPGA packages, as outlined in Table 57. In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Table 57: **Types of Pins on Spartan-3A FPGAs**

Type / Color Code	Description	Pin Name(s) in Type
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO_# IO_Lxxy_#
INPUT	Unrestricted, general-purpose input-only pin. This pin does not have an output structure, differential termination resistor, or PCI clamp diode.	IP_# IP_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. See UG332: *Spartan-3 Generation Configuration User Guide* for additional information on these signals.	M[2:0] PUDC_B CCLK MOSI/CSI_B D[7:1] D0/DIN DOUT CSO_B RDWR_B INIT_B A[25:0] VS[2:0] LDC[2:0] HDC
VREF	Dual-purpose pin that is either a user-I/O pin or Input-only pin, or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected.	IP/VREF_# IP_Lxxy_#/VREF_# IO/VREF_# IO_Lxxy_#/VREF_#
CLK	Either a user-I/O pin or an input to a specific clock buffer driver. Most packages have 16 global clock inputs that optionally clock the entire device. The exceptions are the TQ144 and the XC3S50A in the FT256 package). The RHCLK inputs optionally clock the right half of the device. The LHCLK inputs optionally clock the left half of the device. See the Using Global Clock Resources chapter in UG331: *Spartan-3 Generation FPGA User Guide* for additional information on these signals.	IO_Lxxy_#/GCLK[15:0], IO_Lxxy_#/LHCLK[7:0], IO_Lxxy_#/RHCLK[7:0]
CONFIG	Dedicated configuration pin, two per device. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See the UG332: *Spartan-3 Generation Configuration User Guide* for additional information on the DONE and PROG_B signals.	DONE, PROG_B

Table 59: **Maximum User I/O by Package**

Device	Package	Maximum User I/Os and Input-Only	Maximum Input-Only	Maximum Differential Pairs	All Possible I/Os by Type					
					I/O	INPUT	DUAL	VREF	CLK	N.C.
XC3S50A	VQ100	68	6	60	17	2	20	6	23	0
XC3S200A		68	6	60	17	2	20	6	23	0
XC3S50A	TQ144	108	7	50	42	2	26	8	30	0
XC3S50A	FT256	144	32	64	53	20	26	15	30	51
XC3S200A		195	35	90	69	21	52	21	32	0
XC3S400A		195	35	90	69	21	52	21	32	0
XC3S700A		161	13	60	59	2	52	18	30	0
XC3S1400A		161	13	60	59	2	52	18	30	0
XC3S200A	FG320	248	56	112	101	40	52	23	32	3
XC3S400A		251	59	112	101	42	52	24	32	0
XC3S400A	FG400	311	63	142	155	46	52	26	32	0
XC3S700A		311	63	142	155	46	52	26	32	0
XC3S700A	FG484	372	84	165	194	61	52	33	32	3
XC3S1400A		375	87	165	195	62	52	34	32	0
XC3S1400A	FG676	502	94	227	313	67	52	38	32	17

Notes:

1. Some VREFs are on INPUT pins. See pinout tables for details.

Electronic versions of the package pinout tables and footprints are available for download from the Xilinx website. Using a spreadsheet program, the data can be sorted and reformatted according to any specific needs. Similarly, the ASCII-text file is easily parsed by most scripting programs.

http://www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip

TQ144 Footprint

Note pin 1 indicator in top-left corner and logo orientation.

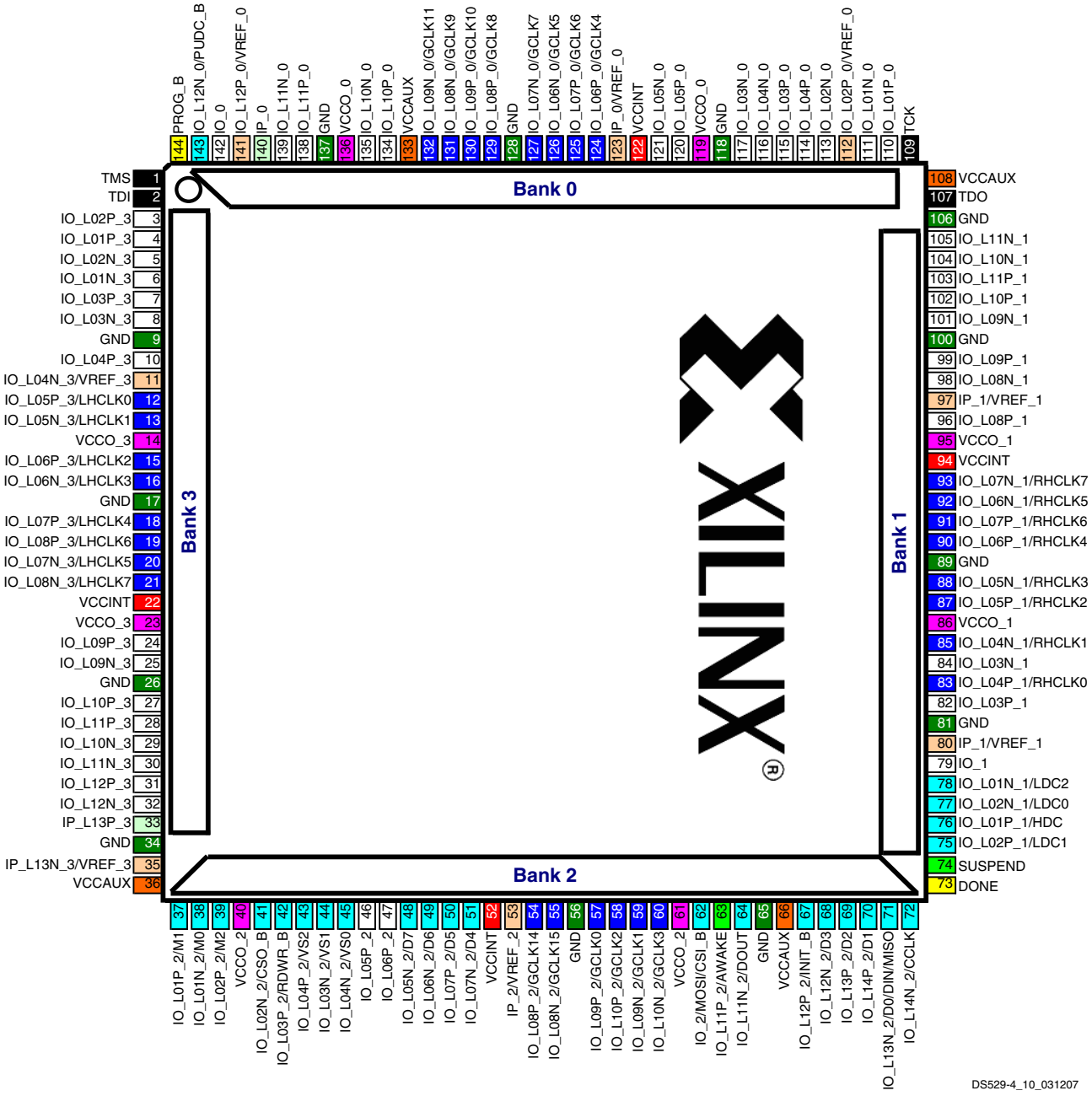


Figure 19: **TQ144 Package Footprint (Top View)**

42	**I/O:** Unrestricted, general-purpose user I/O	25	**DUAL:** Configuration pins, then possible user I/O	8	**VREF:** User I/O or input voltage reference for bank
2	**INPUT:** Unrestricted, general-purpose input pin	30	**CLK:** User I/O, input, or global buffer input	8	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core supply voltage (+1.2V)
0	**N.C.:** Not connected	13	**GND:** Ground	4	**VCCAUX:** Auxiliary supply voltage
2	**SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins				

FT256: 256-ball Fine-pitch, Thin Ball Grid Array

The 256-ball fine-pitch, thin ball grid array package, FT256, supports all five Spartan-3A FPGAs. The XC3S200A and XC3S400A have identical footprints, and the XC3S700A and XC3S1400A have identical footprints. The XC3S50A is compatible with the XC3S200A/XC3S400A but has 51 unconnected balls. The XC3S200A/XC3S400A is similar to the XC3S700A/XC3S1400A, but the XC3S700A/XC3S1400A adds more power and ground pins and therefore is not compatible.

Table 68 lists all the package pins for the XC3S50A, XC3S200A, and XC3S400A. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The highlighted rows indicate pinout differences between the XC3S50A, the XC3S200A, and the XC3S400A FPGAs. The XC3S50A has 51 unconnected balls, indicated as N.C. (No Connection) in Table 68 and Figure 20 and with the black diamond character (◆) in Table 68. Figure 21 provides the common footprint for the XC3S200A and XC3S400A.

Table 68 also indicates that some differential I/O pairs have different assignments between the XC3S50A and the XC3S200A/XC3S400A, highlighted in light blue. See "Footprint Migration Differences," page 99 for additional information.

All other balls have nearly identical functionality on all three devices. Table 73 summarizes the XC3S50A FPGA footprint migration differences for the FT256 package.

The XC3S50A does not support the address output pins for the Byte-wide Peripheral Interface (BPI) configuration mode.

Table 69 lists all the package pins for the XC3S700A and XC3S1400A. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier. Figure 22 provides the common footprint for the XC3S200A and XC3S400A.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 68: **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400)**

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
0	IO_L01N_0	IO_L01N_0	C13	I/O
0	IO_L01P_0	IO_L01P_0	D13	I/O
0	IO_L02N_0	IO_L02N_0	B14	I/O
0	IO_L02P_0/ VREF_0	IO_L02P_0/ VREF_0	B15	VREF
0	IO_L03N_0	IO_L03N_0	D11	I/O
0	IO_L03P_0	IO_L03P_0	C12	I/O
0	IO_L04N_0	IO_L04N_0	A13	I/O
0	IO_L04P_0	IO_L04P_0	A14	I/O
0	N.C. (◆)	IO_L05N_0	A12	I/O
0	IP_0	IO_L05P_0	B12	I/O
0	N.C. (◆)	IO_L06N_0/ VREF_0	E10	VREF
0	N.C. (◆)	IO_L06P_0	D10	I/O
0	IO_L07N_0	IO_L07N_0	A11	I/O
0	IO_L07P_0	IO_L07P_0	C11	I/O
0	IO_L08N_0	IO_L08N_0	A10	I/O
0	IO_L08P_0	IO_L08P_0	B10	I/O
0	IO_L09N_0/ GCLK5	IO_L09N_0/ GCLK5	D9	GCLK
0	IO_L09P_0/ GCLK4	IO_L09P_0/ GCLK4	C10	GCLK
0	IO_L10N_0/ GCLK7	IO_L10N_0/ GCLK7	A9	GCLK
0	IO_L10P_0/ GCLK6	IO_L10P_0/ GCLK6	C9	GCLK
0	IO_L11N_0/ GCLK9	IO_L11N_0/ GCLK9	D8	GCLK
0	IO_L11P_0/ GCLK8	IO_L11P_0/ GCLK8	C8	GCLK
0	IO_L12N_0/ GCLK11	IO_L12N_0/ GCLK11	B8	GCLK
0	IO_L12P_0/ GCLK10	IO_L12P_0/ GCLK10	A8	GCLK
0	N.C. (◆)	IO_L13N_0	C7	I/O
0	N.C. (◆)	IO_L13P_0	A7	I/O
0	N.C. (◆)	IO_L14N_0/ VREF_0	E7	VREF
0	N.C. (◆)	IO_L14P_0	F8	I/O
0	IO_L15N_0	IO_L15N_0	B6	I/O
0	IO_L15P_0	IO_L15P_0	A6	I/O
0	IO_L16N_0	IO_L16N_0	C6	I/O
0	IO_L16P_0	IO_L16P_0	D7	I/O
0	IO_L17N_0	IO_L17N_0	C5	I/O

FT256 Footprint (XC3S700A, XC3S1400A)

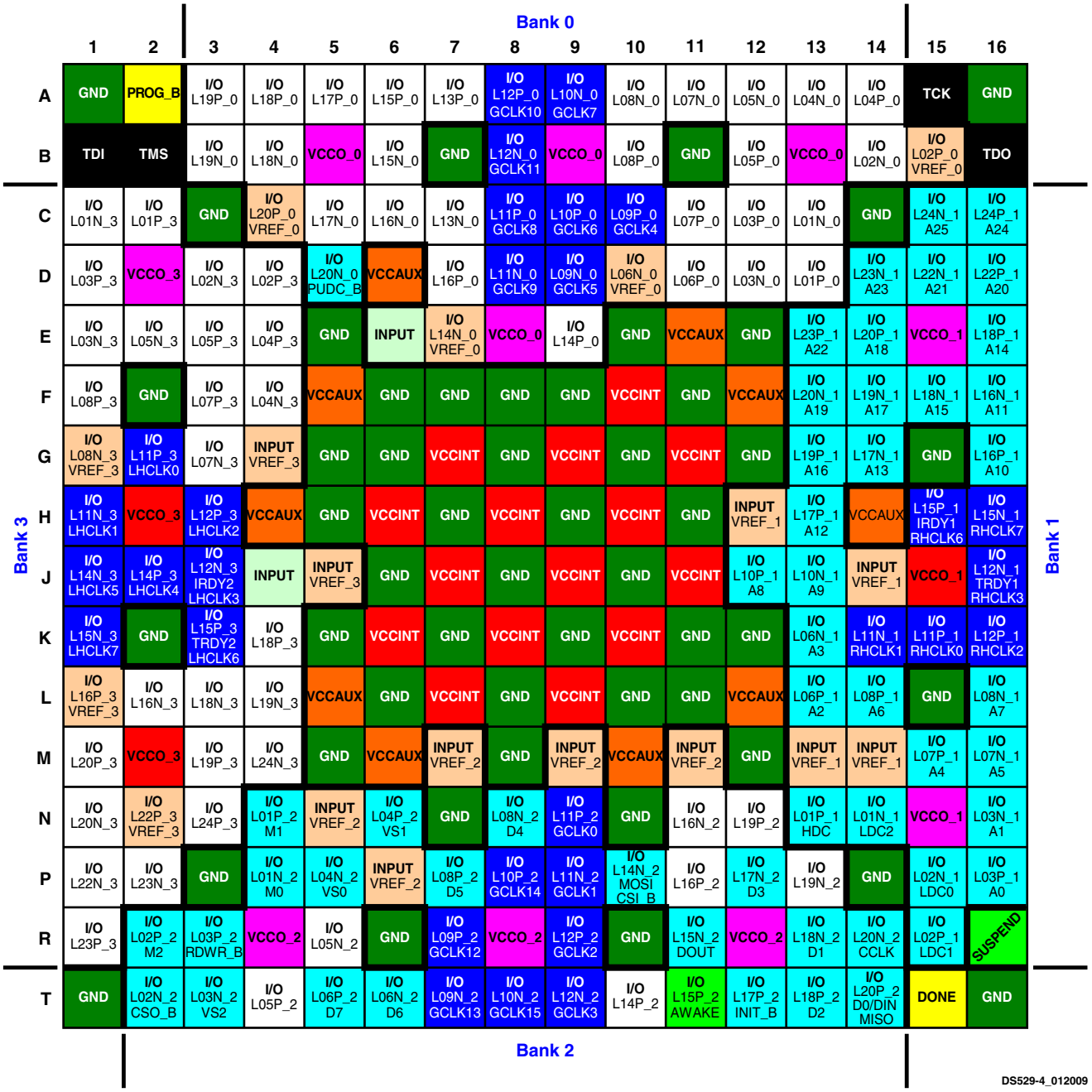


Figure 22: **XC3S700A and XC3S1400A FT256 Package Footprint (Top View)**

59 **I/O:** Unrestricted, general-purpose user I/O

2 **INPUT:** Unrestricted, general-purpose input pin

2 **CONFIG:** Dedicated configuration pins

0 **N.C.:** Not connected

51 **DUAL:** Configuration, then possible user I/O

30 **CLK:** User I/O, input, or global buffer input

4 **JTAG:** Dedicated JTAG port pins

50 **GND:** Ground

18 **VREF:** User I/O or input voltage reference for bank

13 **VCCO:** Output voltage supply for bank

15 **VCCINT:** Internal core supply voltage (+1.2V)

10 **VCCAUX:** Auxiliary supply voltage

2 **SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins

FG320: 320-ball Fine-pitch Ball Grid Array

The 320-ball fine-pitch ball grid array package, FG320, supports two Spartan-3A FPGAs, the XC3S200A and the XC3S400A, as shown in Table 77 and Figure 23.

The FG320 package is an 18 x 18 array of solder balls minus the four center balls.

Table 77 lists all the package pins. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The shaded rows indicate pinout differences between the XC3S200A and the XC3S400A FPGAs. The XC3S200A has three unconnected balls, indicated as N.C. (No Connection) in Table 77 and with the black diamond character (◆) in Table 77 and Figure 23.

All other balls have nearly identical functionality on all three devices. Table 80 summarizes the Spartan-3A FPGA footprint migration differences for the FG320 package.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 77: **Spartan-3A FG320 Pinout**

Bank	Pin Name	FG320 Ball	Type
0	IO_L01N_0	C15	I/O
0	IO_L01P_0	C16	I/O
0	IO_L02N_0	A16	I/O
0	IO_L02P_0/VREF_0	B16	VREF
0	IO_L03N_0	A14	I/O
0	IO_L03P_0	A15	I/O
0	IO_L04N_0	C14	I/O
0	IO_L04P_0	B15	I/O
0	IO_L05N_0	D12	I/O
0	IO_L05P_0	C13	I/O
0	IO_L06N_0/VREF_0	A13	VREF
0	IO_L06P_0	B13	I/O
0	IO_L07N_0	B12	I/O
0	IO_L07P_0	C12	I/O
0	IO_L08N_0	F11	I/O
0	IO_L08P_0	E11	I/O
0	IO_L09N_0	A11	I/O
0	IO_L09P_0	B11	I/O
0	IO_L10N_0	D10	I/O
0	IO_L10P_0	C11	I/O
0	IO_L11N_0/GCLK5	C9	GCLK
0	IO_L11P_0/GCLK4	B10	GCLK
0	IO_L12N_0/GCLK7	B9	GCLK
0	IO_L12P_0/GCLK6	A10	GCLK
0	IO_L13N_0/GCLK9	B7	GCLK
0	IO_L13P_0/GCLK8	A8	GCLK
0	IO_L14N_0/GCLK11	C8	GCLK
0	IO_L14P_0/GCLK10	B8	GCLK
0	IO_L15N_0	C7	I/O
0	IO_L15P_0	D8	I/O
0	IO_L16N_0	E9	I/O
0	IO_L16P_0	D9	I/O
0	IO_L17N_0	B6	I/O
0	IO_L17P_0	A6	I/O
0	IO_L18N_0/VREF_0	A4	VREF
0	IO_L18P_0	A5	I/O
0	IO_L19N_0	E7	I/O
0	IO_L19P_0	F8	I/O
0	IO_L20N_0	D6	I/O
0	IO_L20P_0	C6	I/O
0	IO_L21N_0	A3	I/O
0	IO_L21P_0	B4	I/O
0	IO_L22N_0	D5	I/O
0	IO_L22P_0	C5	I/O
0	IO_L23N_0	A2	I/O
0	IO_L23P_0	B3	I/O
0	IO_L24N_0/PUDC_B	E5	DUAL
0	IO_L24P_0/VREF_0	E6	VREF
0	IP_0	D13	INPUT
0	IP_0	D14	INPUT
0	IP_0	E12	INPUT
0	***XC3S400A:*** IP_0 ***XC3S200A:*** N.C. (◆)	E13	INPUT
0	IP_0	F7	INPUT
0	IP_0	F9	INPUT
0	IP_0	F10	INPUT

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
0	IP_0	F12	INPUT
0	IP_0	G7	INPUT
0	IP_0	G8	INPUT
0	IP_0	G9	INPUT
0	IP_0	G11	INPUT
0	IP_0/VREF_0	E10	VREF
0	VCCO_0	B5	VCCO
0	VCCO_0	B14	VCCO
0	VCCO_0	D11	VCCO
0	VCCO_0	E8	VCCO
1	IO_L01N_1/LDC2	T17	DUAL
1	IO_L01P_1/HDC	R16	DUAL
1	IO_L02N_1/LDC0	U18	DUAL
1	IO_L02P_1/LDC1	U17	DUAL
1	IO_L03N_1/A1	R17	DUAL
1	IO_L03P_1/A0	T18	DUAL
1	IO_L05N_1	N16	I/O
1	IO_L05P_1	P16	I/O
1	IO_L06N_1	M14	I/O
1	IO_L06P_1	N15	I/O
1	IO_L07N_1/VREF_1	P18	VREF
1	IO_L07P_1	R18	I/O
1	IO_L09N_1/A3	M17	DUAL
1	IO_L09P_1/A2	M16	DUAL
1	IO_L10N_1/A5	N18	DUAL
1	IO_L10P_1/A4	N17	DUAL
1	IO_L11N_1/A7	L12	DUAL
1	IO_L11P_1/A6	L13	DUAL
1	IO_L13N_1/A9	K16	DUAL
1	IO_L13P_1/A8	L17	DUAL
1	IO_L14N_1/RHCLK1	K17	RHCLK
1	IO_L14P_1/RHCLK0	L18	RHCLK
1	IO_L15N_1/TRDY1/RHCLK3	J17	RHCLK
1	IO_L15P_1/RHCLK2	K18	RHCLK
1	IO_L17N_1/RHCLK5	K15	RHCLK
1	IO_L17P_1/RHCLK4	J16	RHCLK
1	IO_L18N_1/RHCLK7	H17	RHCLK
1	IO_L18P_1/IRDY1/RHCLK6	H18	RHCLK
1	IO_L19N_1/A11	G16	DUAL
1	IO_L19P_1/A10	H16	DUAL

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
1	IO_L21N_1	F17	I/O
1	IO_L21P_1	G17	I/O
1	IO_L22N_1/A13	E18	DUAL
1	IO_L22P_1/A12	F18	DUAL
1	IO_L23N_1/A15	H15	DUAL
1	IO_L23P_1/A14	J14	DUAL
1	IO_L25N_1	D17	I/O
1	IO_L25P_1	D18	I/O
1	IO_L26N_1/A17	E16	DUAL
1	IO_L26P_1/A16	F16	DUAL
1	IO_L27N_1/A19	F15	DUAL
1	IO_L27P_1/A18	G15	DUAL
1	IO_L29N_1/A21	E15	DUAL
1	IO_L29P_1/A20	D16	DUAL
1	IO_L30N_1/A23	B18	DUAL
1	IO_L30P_1/A22	C18	DUAL
1	IO_L31N_1/A25	B17	DUAL
1	IO_L31P_1/A24	C17	DUAL
1	IP_L04N_1/VREF_1	N14	VREF
1	IP_L04P_1	P15	INPUT
1	IP_L08N_1/VREF_1	L14	VREF
1	IP_L08P_1	M13	INPUT
1	IP_L12N_1	L16	INPUT
1	IP_L12P_1/VREF_1	M15	VREF
1	IP_L16N_1	K14	INPUT
1	IP_L16P_1	K13	INPUT
1	IP_L20N_1	J13	INPUT
1	IP_L20P_1/VREF_1	K12	VREF
1	IP_L24N_1	G14	INPUT
1	IP_L24P_1	H13	INPUT
1	IP_L28N_1	G13	INPUT
1	IP_L28P_1/VREF_1	H12	VREF
1	IP_L32N_1	F13	INPUT
1	IP_L32P_1/VREF_1	F14	VREF
1	VCCO_1	E17	VCCO
1	VCCO_1	H14	VCCO
1	VCCO_1	L15	VCCO
1	VCCO_1	P17	VCCO
2	IO_L01N_2/M0	U3	DUAL
2	IO_L01P_2/M1	T3	DUAL

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
2	IO_L02N_2/CSO_B	V3	DUAL
2	IO_L02P_2/M2	V2	DUAL
2	IO_L03N_2/VS2	U4	DUAL
2	IO_L03P_2/RDWR_B	T4	DUAL
2	IO_L04N_2	T5	I/O
2	IO_L04P_2	R5	I/O
2	IO_L05N_2/VS0	V5	DUAL
2	IO_L05P_2/VS1	V4	DUAL
2	IO_L06N_2	U6	I/O
2	IO_L06P_2	T6	I/O
2	IO_L07N_2	P8	I/O
2	IO_L07P_2	N8	I/O
2	IO_L08N_2/D6	T7	DUAL
2	IO_L08P_2/D7	R7	DUAL
2	IO_L09N_2	R9	I/O
2	IO_L09P_2	T8	I/O
2	IO_L10N_2/D4	V6	DUAL
2	IO_L10P_2/D5	U7	DUAL
2	IO_L11N_2/GCLK13	V8	GCLK
2	IO_L11P_2/GCLK12	U8	GCLK
2	IO_L12N_2/GCLK15	V9	GCLK
2	IO_L12P_2/GCLK14	U9	GCLK
2	IO_L13N_2/GCLK1	T10	GCLK
2	IO_L13P_2/GCLK0	U10	GCLK
2	IO_L14N_2/GCLK3	U11	GCLK
2	IO_L14P_2/GCLK2	V11	GCLK
2	IO_L15N_2	R10	I/O
2	IO_L15P_2	P10	I/O
2	IO_L16N_2/MOSI/CSI_B	T11	DUAL
2	IO_L16P_2	R11	I/O
2	IO_L17N_2	V13	I/O
2	IO_L17P_2	U12	I/O
2	IO_L18N_2/DOUT	U13	DUAL
2	IO_L18P_2/AWAKE	T12	PWR MGMT
2	IO_L19N_2	P12	I/O
2	IO_L19P_2	N12	I/O
2	IO_L20N_2/D3	R13	DUAL
2	IO_L20P_2/INIT_B	T13	DUAL
2	IO_L21N_2	T14	I/O

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
2	IO_L21P_2	V14	I/O
2	IO_L22N_2/D1	U15	DUAL
2	IO_L22P_2/D2	V15	DUAL
2	IO_L23N_2	T15	I/O
2	IO_L23P_2	R14	I/O
2	IO_L24N_2/CCLK	U16	DUAL
2	IO_L24P_2/D0/DIN/MISO	V16	DUAL
2	IP_2	M8	INPUT
2	IP_2	M9	INPUT
2	IP_2	M12	INPUT
2	***XC3S400A:*** IP_2 ***XC3S200A:*** N.C. (◆)	N7	INPUT
2	IP_2	N9	INPUT
2	IP_2	N11	INPUT
2	IP_2	R6	INPUT
2	IP_2/VREF_2	M11	VREF
2	IP_2/VREF_2	N10	VREF
2	IP_2/VREF_2	P6	VREF
2	IP_2/VREF_2	P7	VREF
2	IP_2/VREF_2	P9	VREF
2	IP_2/VREF_2	P13	VREF
2	***XC3S400A:*** IP_2/VREF_2 ***XC3S200A:*** N.C. (◆)	P14	VREF
2	VCCO_2	P11	VCCO
2	VCCO_2	R8	VCCO
2	VCCO_2	U5	VCCO
2	VCCO_2	U14	VCCO
3	IO_L01N_3	C1	I/O
3	IO_L01P_3	C2	I/O
3	IO_L02N_3	B1	I/O
3	IO_L02P_3	B2	I/O
3	IO_L03N_3	D2	I/O
3	IO_L03P_3	D3	I/O
3	IO_L05N_3	G5	I/O
3	IO_L05P_3	F5	I/O
3	IO_L06N_3	E3	I/O
3	IO_L06P_3	F4	I/O
3	IO_L07N_3	E1	I/O
3	IO_L07P_3	D1	I/O
3	IO_L09N_3	G4	I/O
3	IO_L09P_3	F3	I/O

Table 81: **Spartan-3A FG400 Pinout *(Continued)***

Bank	Pin Name	FG400 Ball	Type
VCCAUX	TDO	E17	JTAG
VCCAUX	TMS	E4	JTAG
VCCAUX	VCCAUX	A13	VCCAUX
VCCAUX	VCCAUX	E16	VCCAUX
VCCAUX	VCCAUX	H1	VCCAUX
VCCAUX	VCCAUX	K13	VCCAUX
VCCAUX	VCCAUX	L8	VCCAUX
VCCAUX	VCCAUX	N20	VCCAUX
VCCAUX	VCCAUX	T5	VCCAUX
VCCAUX	VCCAUX	Y8	VCCAUX
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	J12	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	N10	VCCINT

User I/Os by Bank

Table 82 indicates how the 311 available user-I/O pins are distributed between the four I/O banks on the FG400 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 82: **User I/Os Per Bank for the XC3S400A and XC3S700A in the FG400 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	77	50	12	1	6	8
Right	1	79	21	12	30	8	8
Bottom	2	76	35	6	21	6	8
Left	3	79	49	16	0	6	8
TOTAL		**311**	**155**	**46**	**52**	**26**	**32**

Footprint Migration Differences

The XC3S400A and XC3S700A FPGAs have identical footprints in the FG400 package. Designs can migrate between the XC3S400A and XC3S700A FPGAs without further consideration.