AMD Xilinx - XC3S200A-4VQG100I Datasheet

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	448
Number of Logic Elements/Cells	4032
Total RAM Bits	294912
Number of I/O	68
Number of Gates	200000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s200a-4vqg100i

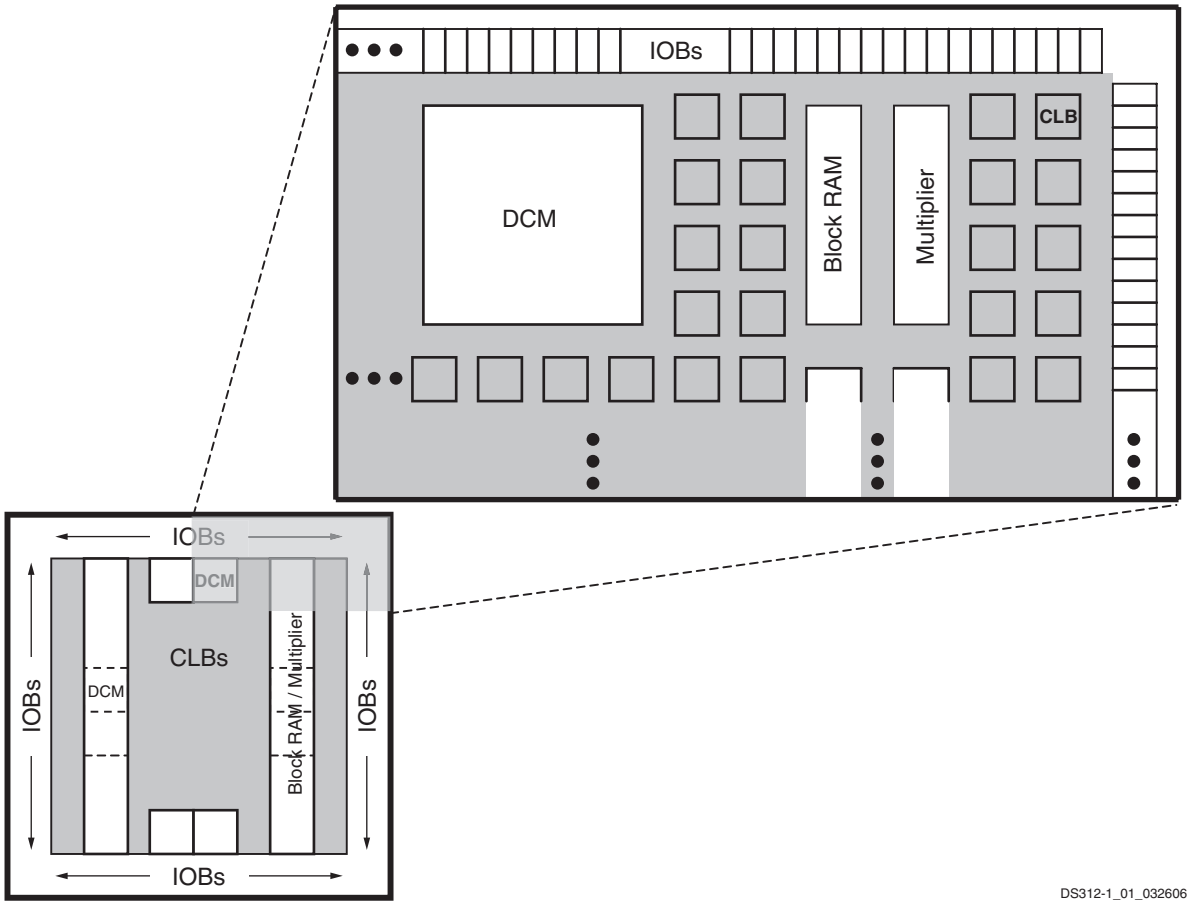
Architectural Overview

The Spartan-3A family architecture consists of five fundamental programmable functional elements:

- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. IOBs support bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including several high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A dual ring of staggered IOBs surrounds a regular array of CLBs. Each device has two columns of block RAM except for the XC3S50A, which has one column. Each RAM column consists of several 18-Kbit RAM blocks. Each block RAM is associated with a dedicated multiplier. The DCMs are positioned in the center with two at the top and two at the bottom of the device. The XC3S50A has DCMs only at the top, while the XC3S700A and XC3S1400A add two DCMs in the middle of the two columns of block RAM and multipliers.

The Spartan-3A family features a rich network of routing that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



Notes:

1. The XC3S700A and XC3S1400A have two additional DCMs on both the left and right sides as indicated by the dashed lines. The XC3S50A has only two DCMs at the top and only one Block RAM/Multiplier column.

Figure 1: **Spartan-3A FPGA Architecture**

Production Status

Table 3 indicates the production status of each Spartan-3A FPGA by temperature range and speed grade. The table also lists the earliest speed file version required for creating a production configuration bitstream. Later versions are also supported.

Table 3: **Spartan-3A FPGA Production Status (Production Speed File)**

Temperature Range		Commercial (C)		Industrial
Speed Grade		Standard (–4)	High-Performance (–5)	Standard (–4)
Part Number	XC3S50A	**Production** (v1.35)	**Production** (v1.35)	**Production** (v1.35)
	XC3S200A	**Production** (v1.35)	**Production** (v1.35)	**Production** (v1.35)
	XC3S400A	**Production** (v1.36)	**Production** (v1.36)	**Production** (v1.36)
	XC3S700A	**Production** (v1.34)	**Production** (v1.35)	**Production** (v1.34)
	XC3S1400A	**Production** (v1.34)	**Production** (v1.35)	**Production** (v1.34)

Package Marking

Figure 2 provides a top marking example for Spartan-3A FPGAs in the quad-flat packages. Figure 3 shows the top marking for Spartan-3A FPGAs in BGA packages. The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator.

The "5C" and "4I" Speed Grade/Temperature Range part combinations may be dual marked as "5C/4I". Devices with a single mark are only guaranteed for the marked speed grade and temperature range.

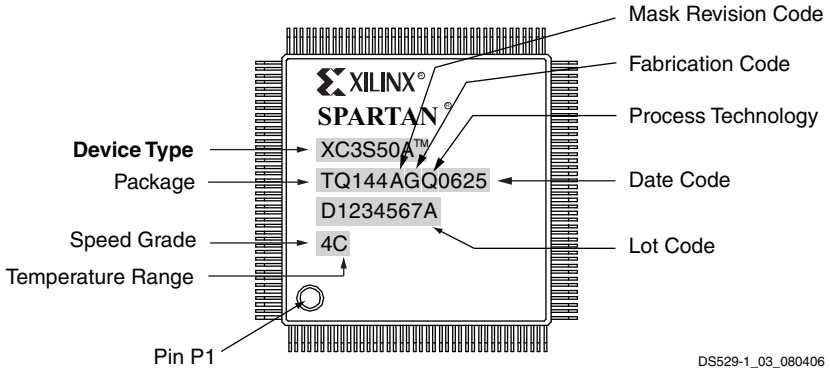


Figure 2: **Spartan-3A QFP Package Marking Example**

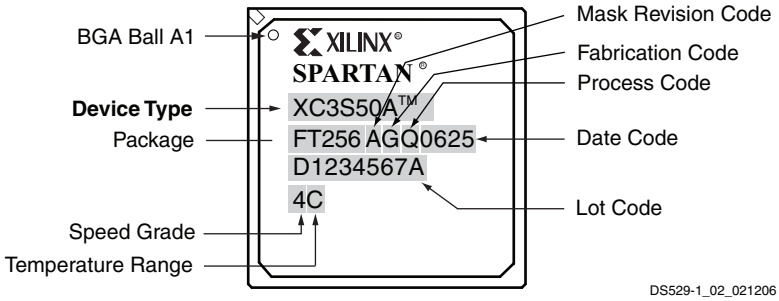


Figure 3: **Spartan-3A BGA Package Marking Example**

Spartan-3A FPGA Design Documentation

The functionality of the Spartan®-3A FPGA Family is described in the following documents. The topics covered in each guide is listed below.

- **DS706: Extended Spartan-3A Family Overview**
  www.xilinx.com/support/documentation/data_sheets/ds706.pdf
- **UG331: Spartan-3 Generation FPGA User Guide**
  www.xilinx.com/support/documentation/user_guides/ug331.pdf
  - Clocking Resources
  - Digital Clock Managers (DCMs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
    - Distributed RAM
    - SRL16 Shift Registers
    - Carry and Arithmetic Logic
  - I/O Resources
  - Embedded Multiplier Blocks
  - Programmable Interconnect
  - ISE® Software Design Tools
  - IP Cores
  - Embedded Processing and Control Solutions
  - Pin Types and Package Overview
  - Package Drawings
  - Powering FPGAs
  - Power Management
- **UG332: Spartan-3 Generation Configuration User Guide**
  www.xilinx.com/support/documentation/user_guides/ug332.pdf
  - Configuration Overview
    - Configuration Pins and Behavior
    - Bitstream Sizes
  - Detailed Descriptions by Mode
    - Master Serial Mode using Xilinx® Platform Flash PROM
    - Master SPI Mode using Commodity SPI Serial Flash PROM
    - Master BPI Mode using Commodity Parallel NOR Flash PROM
    - Slave Parallel (SelectMAP) using a Processor
    - Slave Serial using a Processor
    - JTAG Mode
  - ISE iMPACT Programming Examples
  - MultiBoot Reconfiguration
  - Design Authentication using Device DNA

For application examples, see the Spartan-3A FPGA application notes.

- **Spartan-3A FPGA Application Notes**
  www.xilinx.com/support/documentation/spartan-3a_application_notes.htm

For specific hardware examples, please see the Spartan-3A FPGA Starter Kit board web page, which has links to various design examples and the user guide.

- **Spartan-3A/3AN FPGA Starter Kit Board Page**
  www.xilinx.com/s3astarter
- **UG334: Spartan-3A/3AN FPGA Starter Kit User Guide**
  www.xilinx.com/support/documentation/boards_and_kits/ug334.pdf

For information on the XA Automotive version of the Spartan-3A family, see the following data sheet.

- XA Spartan-3A Automotive FPGA Family Data Sheet
  www.xilinx.com/support/documentation/data_sheets/ds681.pdf

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Output Timing Adjustments

Table 26: **Output Timing Adjustments for IOB**

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
Single-Ended Standards					
LVTTL	Slow	2 mA	5.58	5.58	ns
		4 mA	3.16	3.16	ns
		6 mA	3.17	3.17	ns
		8 mA	2.09	2.09	ns
		12 mA	1.62	1.62	ns
		16 mA	1.24	1.24	ns
		24 mA	2.74(3)	2.74(3)	ns
	Fast	2 mA	3.03	3.03	ns
		4 mA	1.71	1.71	ns
		6 mA	1.71	1.71	ns
		8 mA	0.53	0.53	ns
		12 mA	0.53	0.53	ns
		16 mA	0.59	0.59	ns
		24 mA	0.60	0.60	ns
	QuietIO	2 mA	27.67	27.67	ns
		4 mA	27.67	27.67	ns
		6 mA	27.67	27.67	ns
		8 mA	16.71	16.71	ns
		12 mA	16.67	16.67	ns
		16 mA	16.22	16.22	ns
		24 mA	12.11	12.11	ns

Table 26: **Output Timing Adjustments for IOB*(Continued)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS33	Slow	2 mA	5.58	5.58	ns
		4 mA	3.17	3.17	ns
		6 mA	3.17	3.17	ns
		8 mA	2.09	2.09	ns
		12 mA	1.24	1.24	ns
		16 mA	1.15	1.15	ns
		24 mA	2.55(3)	2.55(3)	ns
	Fast	2 mA	3.02	3.02	ns
		4 mA	1.71	1.71	ns
		6 mA	1.72	1.72	ns
		8 mA	0.53	0.53	ns
		12 mA	0.59	0.59	ns
		16 mA	0.59	0.59	ns
		24 mA	0.51	0.51	ns
	QuietIO	2 mA	27.67	27.67	ns
		4 mA	27.67	27.67	ns
		6 mA	27.67	27.67	ns
		8 mA	16.71	16.71	ns
		12 mA	16.29	16.29	ns
		16 mA	16.18	16.18	ns
		24 mA	12.11	12.11	ns

Table 27: **Test Methods for Timing Measurement at I/Os*(Continued)***

Signal Standard (IOSTANDARD)	Inputs			Outputs		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Differential						
LVDS_25	-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDS_33	-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
BLVDS_25	-	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
MINI_LVDS_25	-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
MINI_LVDS_33	-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVPECL_25	-	V_{ICM} – 0.3	V_{ICM} + 0.3	N/A	N/A	V_{ICM}
LVPECL_33	-	V_{ICM} – 0.3	V_{ICM} + 0.3	N/A	N/A	V_{ICM}
RSDS_25	-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
RSDS_33	-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
TMDS_33	-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	3.3	V_{ICM}
PPDS_25	-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	0.8	V_{ICM}
PPDS_33	-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	0.8	V_{ICM}
DIFF_HSTL_I	-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.75	V_{ICM}
DIFF_HSTL_III	-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.5	V_{ICM}
DIFF_HSTL_I_18	-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_HSTL_II_18	-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_HSTL_III_18	-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.8	V_{ICM}
DIFF_SSTL18_I	-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_SSTL18_II	-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_SSTL2_I	-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.25	V_{ICM}
DIFF_SSTL2_II	-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.25	V_{ICM}
DIFF_SSTL3_I	-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.5	V_{ICM}
DIFF_SSTL3_II	-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.5	V_{ICM}

Notes:

1. Descriptions of the relevant symbols are as follows:
   V_{REF} – The reference voltage for setting the input switching threshold
   V_{ICM} – The common mode input voltage
   V_M – Voltage of measurement point on signal transition
   V_L – Low-level test voltage at Input pin
   V_H – High-level test voltage at Input pin
   R_T – Effective termination resistance, which takes on a value of 1 MΩ when no parallel termination is required
   V_T – Termination voltage
2. The load capacitance (C_L) at the Output pin is 0 pF for all signal standards.
3. According to the PCI specification.

The capacitive load (C_L) is connected between the output and GND. *The Output timing for all standards, as published in the speed files and the data sheet, is always based on a C_L value of zero*. High-impedance probes (less than 1 pF) are used for all measurements. Any delay that the test fixture might contribute to test measurements is subtracted from those measurements to produce the final timing numbers as published in the speed files and data sheet.

Digital Clock Manager (DCM) Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables (Table 36 and Table 37) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables (Table 38 through Table 41) supersede any corresponding ones in the DLL tables. DLL specifications that do not change with the addition of DFS or PS functions are presented in Table 36 and Table 37.

Period jitter and cycle-cycle jitter are two of many different ways of specifying clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the ideal clock period over a collection of millions of samples. In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

Spread Spectrum

DCMs accept typical spread spectrum clocks as long as they meet the input requirements. The DLL will track the frequency changes created by the spread spectrum clock to drive the global clocks to the FPGA logic. See XAPP469, *Spread-Spectrum Clocking Reception for Displays* for details.

Delay-Locked Loop (DLL)

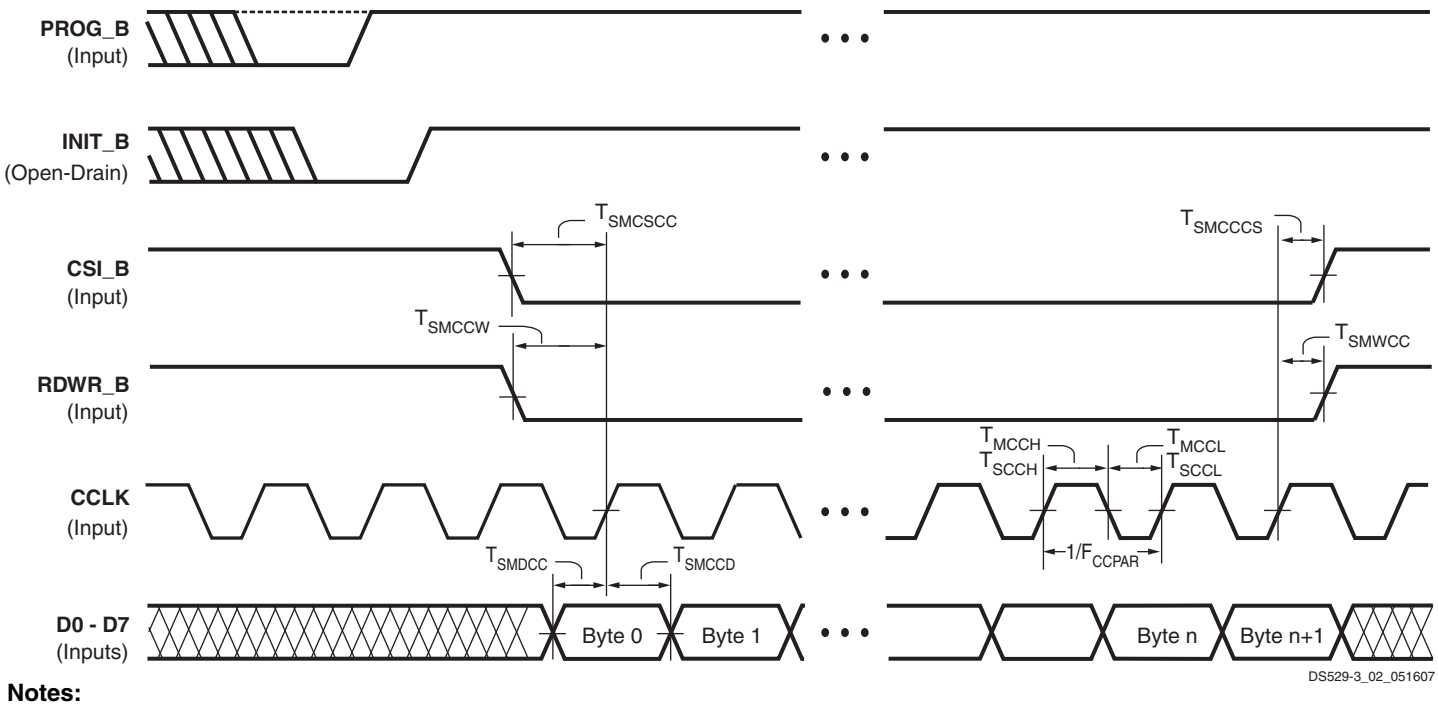
Table 36: **Recommended Operating Conditions for the DLL**

Symbol		Description		Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges								
F_{CLKIN}	CLKIN_FREQ_DLL	Frequency of the CLKIN clock input		5(2)	280(3)	5(2)	250(3)	MHz
Input Pulse Requirements								
CLKIN_PULSE		CLKIN pulse width as a percentage of the CLKIN period	$F_{CLKIN} \leq 150$ MHz	40%	60%	40%	60%	–
			$F_{CLKIN} > 150$ MHz	45%	55%	45%	55%	–
Input Clock Jitter Tolerance and Delay Path Variation(4)								
CLKIN_CYC_JITT_DLL_LF		Cycle-to-cycle jitter at the CLKIN input	$F_{CLKIN} \leq 150$ MHz	–	±300	–	±300	ps
CLKIN_CYC_JITT_DLL_HF			$F_{CLKIN} > 150$ MHz	–	±150	–	±150	ps
CLKIN_PER_JITT_DLL		Period jitter at the CLKIN input		–	±1	–	±1	ns
CLKFB_DELAY_VAR_EXT		Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input		–	±1	–	±1	ns

Notes:

1. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
2. The DFS, when operating independently of the DLL, supports lower FCLKIN frequencies. See Table 38.
3. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM. The CLK2X output reproduces the clock frequency provided on the CLKIN input.
4. CLKIN input jitter beyond these limits might cause the DCM to lose lock.
5. The DCM specifications are guaranteed when both adjacent DCMs are locked.

Slave Parallel Mode Timing



Notes:

1. It is possible to abort configuration by pulling CSI_B Low in a given CCLK cycle, then switching RDWR_B Low or High in any subsequent cycle for which CSI_B remains Low. The RDWR_B pin asynchronously controls the driver impedance of the D0 - D7 bus. When RDWR_B switches High, be careful to avoid contention on the D0 - D7 bus.
2. To pause configuration, pause CCLK instead of de-asserting CSI_B. See UG332 Chapter 7 section “Non-Continuous SelectMAP Data Loading” for more details.

Figure 13: **Waveforms for Slave Parallel Configuration**

Table 51: **Timing for the Slave Parallel Configuration Mode**

Symbol	Description		All Speed Grades		Units
			Min	Max	
Setup Times					
T_{SMDCC}(2)	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin		7	–	ns
T_{SMCSCC}	Setup time on the CSI_B pin before the rising transition at the CCLK pin		7	–	ns
T_{SMCCW}	Setup time on the RDWR_B pin before the rising transition at the CCLK pin		15	–	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins		1.0	–	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CSO_B pin		0	–	ns
T_{SMWCC}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	–	ns
Clock Timing					
T_{CCH}	The High pulse width at the CCLK input pin		5	–	ns
T_{CCL}	The Low pulse width at the CCLK input pin		5	–	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	0	80	MHz
		With bitstream compression	0	80	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.
2. Some Xilinx documents refer to Parallel modes as “SelectMAP” modes.

Byte Peripheral Interface (BPI) Configuration Timing

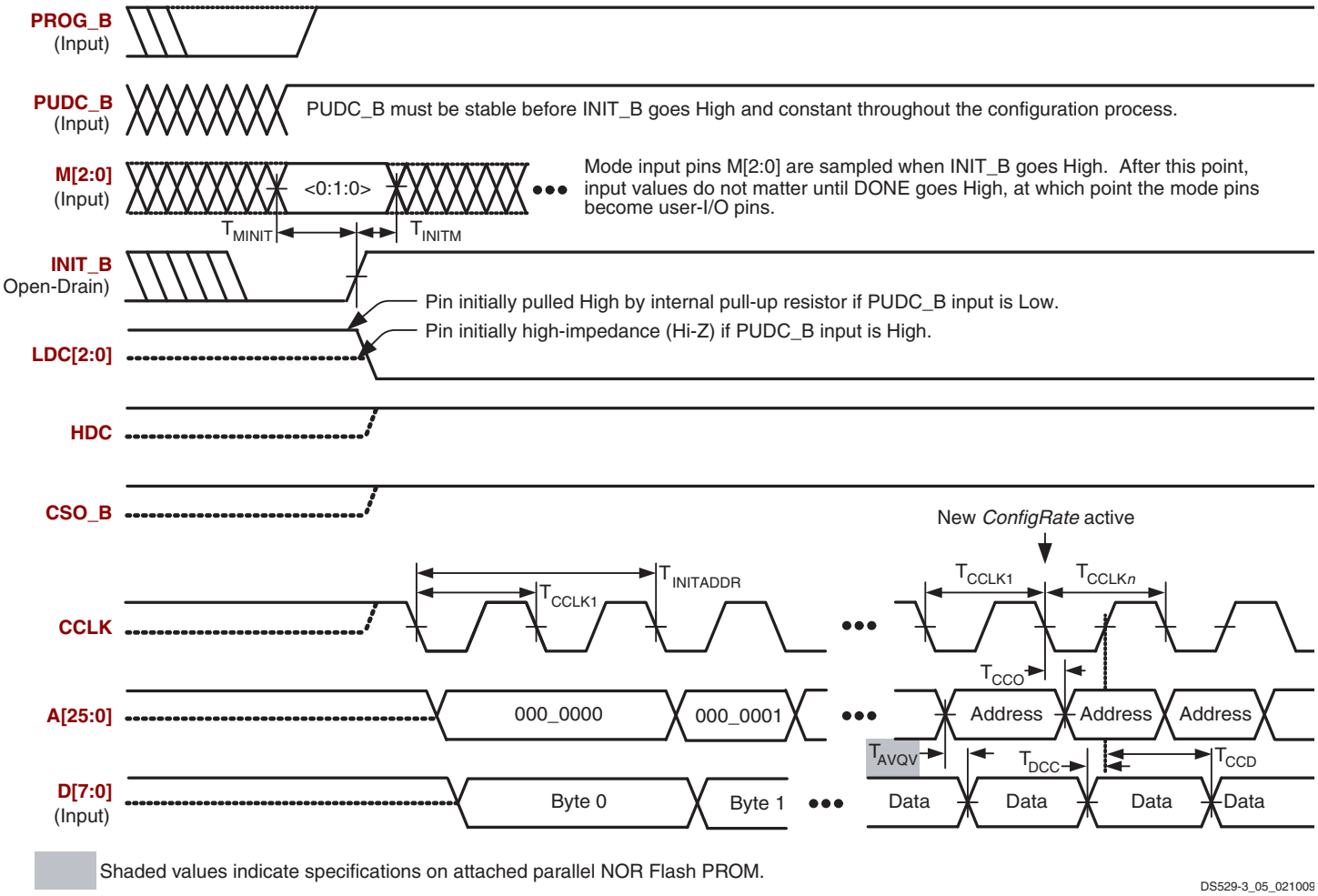


Figure 15: **Waveforms for Byte-wide Peripheral Interface (BPI) Configuration**

Table 54: **Timing for Byte-wide Peripheral Interface (BPI) Configuration Mode**

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	See Table 46		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting	See Table 46		
T_{MINIT}	Setup time on M[2:0] mode pins before the rising edge of INIT_B	50	–	ns
T_{INITM}	Hold time on M[2:0] mode pins after the rising edge of INIT_B	0	–	ns
$T_{INITADDR}$	Minimum period of initial A[25:0] address cycle; LDC[2:0] and HDC are asserted and valid	5	5	T_{CCLK1} cycles
T_{CCO}	Address A[25:0] outputs valid after CCLK falling edge	See Table 50		
T_{DCC}	Setup time on D[7:0] data inputs before CCLK rising edge	See T_{SMDCC} in Table 51		
T_{CCD}	Hold time on D[7:0] data inputs after CCLK rising edge	0	–	ns

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/05/06	1.0	Initial release.
02/02/07	1.1	Promoted to Preliminary status. Moved Table 15 to under "DC Electrical Characteristics" section. Updated all timing specifications for the v1.32 speed files. Added recommended Simultaneous Switching Output (SSO) limits in Table 29. Set a 10 µs maximum pulse width for the DNA_PORT READ signal and the JTAG clock input during the ISC_DNA command, affecting both Table 43 and Table 56. Described "External Termination Requirements for Differential I/O." Added separate DIN hold time for Slave mode in Table 50. Corrected wording in Table 52 and Table 54; no specifications affected.
03/16/07	1.2	Updated all AC timing specifications to the v1.34 speeds file. Promoted the XC3S700A and XC3S1400A FPGAs offered in the -4 speed grade to Production status, as shown in Table 16. Added Note 2 to Table 39 regarding the extra logic (one LUT) automatically added by ISE 9.1i and later software revisions for any DCM application that leverages the Digital Frequency Synthesizer (DFS). Separated some JTAG specifications by array size or function, as shown in Table 56. Updated quiescent current limits in Table 10.
04/23/07	1.3	Updated all AC timing specifications to the v1.35 speeds file. Promoted all devices except the XC3S400A to Production status, as shown in Table 16.
05/08/07	1.4	Updated XC3S400A to Production and v1.36 speeds file. Added banking rules and other explanatory footnotes to Table 12 and Table 13. Corrected DIFF_SSTL3_II V_{OL} Max in Table 14. Improved XC3S400A Pin-to-Pin Clock-to-Output times in Table 18. Updated XC3S400A Pin-to-Pin Setup Times in Table 19. Updated TIOICKPD for -5 in Table 20. Added SSO numbers to Table 28 and Table 29. Removed invalid Embedded Multiplier Hold Times in Table 34. Improved CLKOUT_FREQ_CLK90 in Table 37. Improved T_{TDITCK} and F_{TCK} performance for XC3S400A in Table 56.
07/10/07	1.5	Added DIFF_HSTL_I and DIFF_HSTL_III to Table 13, Table 14, Table 27, and Table 29. Updated TMDS DC characteristics in Table 14. Updated for speed file v1.37 in ISE 9.2.01i as shown in Table 17. Updated pin-to-pin setup and hold times in Table 19. Updated TMDS output adjustment in Table 26. Updated I/O Test Method values in Table 27. Added BLVDS SSO numbers inTable 29. For Multiplier block, updated setup times and added hold times to Table 34. Updated block RAM clock width in Table 35. Updated CLKOUT_PER_JITT_2X and CLKOUT_PER_JITT_DV2 in Table 37. Added CCLK specifications for Commercial in Table 46 through Table 48.
04/15/08	1.6	Added V_{IN} to Recommended Operating Conditions in Table 8 and added reference to XAPP459, "Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins." Reduced typical I_{CCINTQ} and I_{CCAUXQ} quiescent current values by 12%-58% in Table 10. Increased V_{IL} max to 0.4V for LVCMOS12/15/18 and improved V_{IH} min to 0.7V for LVCMOS12 in Table 11. Changed V_{OL} max to 0.4V and V_{OH} min to V_{CCO}-0.4V for LVCMOS15/18 in Table 12. Noted latest speed file v1.39 in ISE 10.1 software in Table 16. Added new packages to SSO limits in Table 28 and Table 29. Improved SSTL18_II SSO limit for FG packages in Table 29. Improved F_{BUFG} for -4 to 334 MHz in Table 33. Added references to 375 MHz performance via SCD 4103 in Table 33,Table 38, Table 39, and Table 40. Restored Units column to Table 44. Updated CCLK output maximum period in Table 46 to match minimum frequency in Table 47. Corrected BPI active clock edge in Figure 15 and Table 54.
05/28/08	1.7	Improved V_{CCAUXT} and V_{CCO2T} POR minimum in Table 5 and updated V_{CCO} POR levels in Figure 11. Clarified recommended V_{IN} in Table 8. Added reference to V_{CCAUX} in "Simultaneously Switching Output Guidelines". Added reference to Sample Window in Table 21. Removed DNA_RETENTION limit of 10 years in Table 15 since number of Read cycles is the only unique limit. Added references to UG332.
03/06/09	1.8	Changed typical quiescent current temperature from ambient to junction. Updated BPI configuration waveforms in Figure 15 and updated Table 55. Updated selected I/O standard DC characteristics. Added TIOPI and TIOPID in Table 22. Removed references to SCD 4103.
08/19/10	2.0	Added I_{IK} to Table 4. Updated V_{IN} in Table 8 and footnoted I_L in Table 9 to note potential leakage between pins of a differential pair. Clarified LVPECL notes to Table 13. Corrected symbols for TSUSPEND_GTS and TSUSPEND_GWE in Table 44.

Introduction

This section describes how the various pins on a Spartan®-3A FPGA connect within the supported component packages, and provides device-specific thermal characteristics. For general information on the pin functions and the package characteristics, see the Packaging section of UG331: *Spartan-3 Generation FPGA User Guide*.

- **UG331: Spartan-3 Generation FPGA User Guide**
  www.xilinx.com/support/documentation/user_guides/ug331.pdf

Spartan-3A FPGAs are available in both standard and Pb-free, RoHS versions of each package, with the Pb-free version adding a "G" to the middle of the package code. Except for the thermal characteristics, all information for the standard package applies equally to the Pb-free package.

Pin Types

Most pins on a Spartan-3A FPGA are general-purpose, user-defined I/O pins. There are, however, up to 12 different functional types of pins on Spartan-3A FPGA packages, as outlined in Table 57. In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Table 57: **Types of Pins on Spartan-3A FPGAs**

Type / Color Code	Description	Pin Name(s) in Type
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO_# IO_Lxxy_#
INPUT	Unrestricted, general-purpose input-only pin. This pin does not have an output structure, differential termination resistor, or PCI clamp diode.	IP_# IP_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. See UG332: *Spartan-3 Generation Configuration User Guide* for additional information on these signals.	M[2:0] PUDC_B CCLK MOSI/CSI_B D[7:1] D0/DIN DOUT CSO_B RDWR_B INIT_B A[25:0] VS[2:0] LDC[2:0] HDC
VREF	Dual-purpose pin that is either a user-I/O pin or Input-only pin, or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected.	IP/VREF_# IP_Lxxy_#/VREF_# IO/VREF_# IO_Lxxy_#/VREF_#
CLK	Either a user-I/O pin or an input to a specific clock buffer driver. Most packages have 16 global clock inputs that optionally clock the entire device. The exceptions are the TQ144 and the XC3S50A in the FT256 package). The RHCLK inputs optionally clock the right half of the device. The LHCLK inputs optionally clock the left half of the device. See the Using Global Clock Resources chapter in UG331: *Spartan-3 Generation FPGA User Guide* for additional information on these signals.	IO_Lxxy_#/GCLK[15:0], IO_Lxxy_#/LHCLK[7:0], IO_Lxxy_#/RHCLK[7:0]
CONFIG	Dedicated configuration pin, two per device. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See the UG332: *Spartan-3 Generation Configuration User Guide* for additional information on the DONE and PROG_B signals.	DONE, PROG_B

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Table 59: **Maximum User I/O by Package**

Device	Package	Maximum User I/Os and Input-Only	Maximum Input-Only	Maximum Differential Pairs	All Possible I/Os by Type					
					I/O	INPUT	DUAL	VREF	CLK	N.C.
XC3S50A	VQ100	68	6	60	17	2	20	6	23	0
XC3S200A		68	6	60	17	2	20	6	23	0
XC3S50A	TQ144	108	7	50	42	2	26	8	30	0
XC3S50A	FT256	144	32	64	53	20	26	15	30	51
XC3S200A		195	35	90	69	21	52	21	32	0
XC3S400A		195	35	90	69	21	52	21	32	0
XC3S700A		161	13	60	59	2	52	18	30	0
XC3S1400A		161	13	60	59	2	52	18	30	0
XC3S200A	FG320	248	56	112	101	40	52	23	32	3
XC3S400A		251	59	112	101	42	52	24	32	0
XC3S400A	FG400	311	63	142	155	46	52	26	32	0
XC3S700A		311	63	142	155	46	52	26	32	0
XC3S700A	FG484	372	84	165	194	61	52	33	32	3
XC3S1400A		375	87	165	195	62	52	34	32	0
XC3S1400A	FG676	502	94	227	313	67	52	38	32	17

Notes:

1. Some VREFs are on INPUT pins. See pinout tables for details.

Electronic versions of the package pinout tables and footprints are available for download from the Xilinx website. Using a spreadsheet program, the data can be sorted and reformatted according to any specific needs. Similarly, the ASCII-text file is easily parsed by most scripting programs.

http://www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip

User I/Os by Bank

Table 67 indicates how the 108 available user-I/O pins are distributed between the four I/O banks on the TQ144 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 67: **User I/Os Per Bank for the XC3S50A in the TQ144 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	27	14	1	1	3	8
Right	1	25	11	0	4	2	8
Bottom	2	30	2	0	21	1	6
Left	3	26	15	1	0	2	8
TOTAL		**108**	**42**	**2**	**26**	**8**	**30**

Footprint Migration Differences

The XC3S50A FPGA is the only Spartan-3A device offered in the TQ144 package.

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
0	IP_0	F12	INPUT
0	IP_0	G7	INPUT
0	IP_0	G8	INPUT
0	IP_0	G9	INPUT
0	IP_0	G11	INPUT
0	IP_0/VREF_0	E10	VREF
0	VCCO_0	B5	VCCO
0	VCCO_0	B14	VCCO
0	VCCO_0	D11	VCCO
0	VCCO_0	E8	VCCO
1	IO_L01N_1/LDC2	T17	DUAL
1	IO_L01P_1/HDC	R16	DUAL
1	IO_L02N_1/LDC0	U18	DUAL
1	IO_L02P_1/LDC1	U17	DUAL
1	IO_L03N_1/A1	R17	DUAL
1	IO_L03P_1/A0	T18	DUAL
1	IO_L05N_1	N16	I/O
1	IO_L05P_1	P16	I/O
1	IO_L06N_1	M14	I/O
1	IO_L06P_1	N15	I/O
1	IO_L07N_1/VREF_1	P18	VREF
1	IO_L07P_1	R18	I/O
1	IO_L09N_1/A3	M17	DUAL
1	IO_L09P_1/A2	M16	DUAL
1	IO_L10N_1/A5	N18	DUAL
1	IO_L10P_1/A4	N17	DUAL
1	IO_L11N_1/A7	L12	DUAL
1	IO_L11P_1/A6	L13	DUAL
1	IO_L13N_1/A9	K16	DUAL
1	IO_L13P_1/A8	L17	DUAL
1	IO_L14N_1/RHCLK1	K17	RHCLK
1	IO_L14P_1/RHCLK0	L18	RHCLK
1	IO_L15N_1/TRDY1/RHCLK3	J17	RHCLK
1	IO_L15P_1/RHCLK2	K18	RHCLK
1	IO_L17N_1/RHCLK5	K15	RHCLK
1	IO_L17P_1/RHCLK4	J16	RHCLK
1	IO_L18N_1/RHCLK7	H17	RHCLK
1	IO_L18P_1/IRDY1/RHCLK6	H18	RHCLK
1	IO_L19N_1/A11	G16	DUAL
1	IO_L19P_1/A10	H16	DUAL

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
1	IO_L21N_1	F17	I/O
1	IO_L21P_1	G17	I/O
1	IO_L22N_1/A13	E18	DUAL
1	IO_L22P_1/A12	F18	DUAL
1	IO_L23N_1/A15	H15	DUAL
1	IO_L23P_1/A14	J14	DUAL
1	IO_L25N_1	D17	I/O
1	IO_L25P_1	D18	I/O
1	IO_L26N_1/A17	E16	DUAL
1	IO_L26P_1/A16	F16	DUAL
1	IO_L27N_1/A19	F15	DUAL
1	IO_L27P_1/A18	G15	DUAL
1	IO_L29N_1/A21	E15	DUAL
1	IO_L29P_1/A20	D16	DUAL
1	IO_L30N_1/A23	B18	DUAL
1	IO_L30P_1/A22	C18	DUAL
1	IO_L31N_1/A25	B17	DUAL
1	IO_L31P_1/A24	C17	DUAL
1	IP_L04N_1/VREF_1	N14	VREF
1	IP_L04P_1	P15	INPUT
1	IP_L08N_1/VREF_1	L14	VREF
1	IP_L08P_1	M13	INPUT
1	IP_L12N_1	L16	INPUT
1	IP_L12P_1/VREF_1	M15	VREF
1	IP_L16N_1	K14	INPUT
1	IP_L16P_1	K13	INPUT
1	IP_L20N_1	J13	INPUT
1	IP_L20P_1/VREF_1	K12	VREF
1	IP_L24N_1	G14	INPUT
1	IP_L24P_1	H13	INPUT
1	IP_L28N_1	G13	INPUT
1	IP_L28P_1/VREF_1	H12	VREF
1	IP_L32N_1	F13	INPUT
1	IP_L32P_1/VREF_1	F14	VREF
1	VCCO_1	E17	VCCO
1	VCCO_1	H14	VCCO
1	VCCO_1	L15	VCCO
1	VCCO_1	P17	VCCO
2	IO_L01N_2/M0	U3	DUAL
2	IO_L01P_2/M1	T3	DUAL

Table 77: **Spartan-3A FG320 Pinout *(Continued)***

Bank	Pin Name	FG320 Ball	Type
GND	GND	R15	GND
GND	GND	T9	GND
GND	GND	V1	GND
GND	GND	V7	GND
GND	GND	V12	GND
GND	GND	V18	GND
VCCAUX	SUSPEND	T16	PWR MGMT
VCCAUX	DONE	V17	CONFIG
VCCAUX	PROG_B	C4	CONFIG
VCCAUX	TCK	A17	JTAG
VCCAUX	TDI	E4	JTAG
VCCAUX	TDO	E14	JTAG
VCCAUX	TMS	C3	JTAG
VCCAUX	VCCAUX	A9	VCCAUX
VCCAUX	VCCAUX	G10	VCCAUX
VCCAUX	VCCAUX	J12	VCCAUX
VCCAUX	VCCAUX	J18	VCCAUX
VCCAUX	VCCAUX	K1	VCCAUX
VCCAUX	VCCAUX	K7	VCCAUX
VCCAUX	VCCAUX	M10	VCCAUX
VCCAUX	VCCAUX	V10	VCCAUX
VCCINT	VCCINT	H9	VCCINT
VCCINT	VCCINT	H11	VCCINT
VCCINT	VCCINT	J8	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	L8	VCCINT
VCCINT	VCCINT	L10	VCCINT

User I/Os by Bank

Table 78 and Table 79 indicate how the available user-I/O pins are distributed between the four I/O banks on the FG320 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 78: **User I/Os Per Bank for XC3S200A in the FG320 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	60	35	11	1	5	8
Right	1	64	9	10	30	7	8
Bottom	2	60	19	6	21	6	8
Left	3	64	38	13	0	5	8
TOTAL		**248**	**101**	**40**	**52**	**23**	**32**

Table 79: **User I/Os Per Bank for XC3S400A in the FG320 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	61	35	12	1	5	8
Right	1	64	9	10	30	7	8
Bottom	2	62	19	7	21	7	8
Left	3	64	38	13	0	5	8
TOTAL		**251**	**101**	**42**	**52**	**24**	**32**

Footprint Migration Differences

Table 80 summarizes any footprint and functionality differences between the XC3S200A and the XC3S400A FPGAs that might affect easy migration between devices available in the FG320 package. There are three such balls. All other pins not listed in Table 80 unconditionally migrate between Spartan-3A devices available in the FG320 package.

The arrows indicate the direction for easy migration.

Table 80: **FG320 Footprint Migration Differences**

Pin	Bank	XC3S200A	Migration	XC3S400A
E13	0	N.C.	→	INPUT
N7	2	N.C.	→	INPUT
P14	2	N.C.	→	INPUT/VREF
DIFFERENCES			**3**	

Legend:

→ This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction is possible depending on how the pin is configured for the device on the right.

FG400: 400-ball Fine-pitch Ball Grid Array

The 400-ball fine-pitch ball grid array, FG400, supports two different Spartan-3A FPGAs, the XC3S400A and the XC3S700A. Both devices share a common footprint for this package as shown in Table 81 and Figure 24.

Table 81 lists all the FG400 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 81: **Spartan-3A FG400 Pinout**

Bank	Pin Name	FG400 Ball	Type
0	IO_L01N_0	A18	I/O
0	IO_L01P_0	B18	I/O
0	IO_L02N_0	C17	I/O
0	IO_L02P_0/VREF_0	D17	VREF
0	IO_L03N_0	E15	I/O
0	IO_L03P_0	D16	I/O
0	IO_L04N_0	A17	I/O
0	IO_L04P_0/VREF_0	B17	VREF
0	IO_L05N_0	A16	I/O
0	IO_L05P_0	C16	I/O
0	IO_L06N_0	C15	I/O
0	IO_L06P_0	D15	I/O
0	IO_L07N_0	A14	I/O
0	IO_L07P_0	C14	I/O
0	IO_L08N_0	A15	I/O
0	IO_L08P_0	B15	I/O
0	IO_L09N_0	F13	I/O
0	IO_L09P_0	E13	I/O
0	IO_L10N_0/VREF_0	C13	VREF
0	IO_L10P_0	D14	I/O
0	IO_L11N_0	C12	I/O
0	IO_L11P_0	B13	I/O
0	IO_L12N_0	F12	I/O
0	IO_L12P_0	D12	I/O
0	IO_L13N_0	A12	I/O

Table 81: **Spartan-3A FG400 Pinout *(Continued)***

Bank	Pin Name	FG400 Ball	Type
0	IO_L13P_0	B12	I/O
0	IO_L14N_0	C11	I/O
0	IO_L14P_0	B11	I/O
0	IO_L15N_0/GCLK5	E11	GCLK
0	IO_L15P_0/GCLK4	D11	GCLK
0	IO_L16N_0/GCLK7	C10	GCLK
0	IO_L16P_0/GCLK6	A10	GCLK
0	IO_L17N_0/GCLK9	E10	GCLK
0	IO_L17P_0/GCLK8	D10	GCLK
0	IO_L18N_0/GCLK11	A8	GCLK
0	IO_L18P_0/GCLK10	A9	GCLK
0	IO_L19N_0	C9	I/O
0	IO_L19P_0	B9	I/O
0	IO_L20N_0	C8	I/O
0	IO_L20P_0	B8	I/O
0	IO_L21N_0	D8	I/O
0	IO_L21P_0	C7	I/O
0	IO_L22N_0/VREF_0	F9	VREF
0	IO_L22P_0	E9	I/O
0	IO_L23N_0	F8	I/O
0	IO_L23P_0	E8	I/O
0	IO_L24N_0	A7	I/O
0	IO_L24P_0	B7	I/O
0	IO_L25N_0	C6	I/O
0	IO_L25P_0	A6	I/O
0	IO_L26N_0	B5	I/O
0	IO_L26P_0	A5	I/O
0	IO_L27N_0	F7	I/O
0	IO_L27P_0	E7	I/O
0	IO_L28N_0	D6	I/O
0	IO_L28P_0	C5	I/O
0	IO_L29N_0	C4	I/O
0	IO_L29P_0	A4	I/O
0	IO_L30N_0	B3	I/O
0	IO_L30P_0	A3	I/O
0	IO_L31N_0	F6	I/O
0	IO_L31P_0	E6	I/O
0	IO_L32N_0/PUDC_B	B2	DUAL

FG484: 484-ball Fine-pitch Ball Grid Array

The 484-ball fine-pitch ball grid array, FG484, supports both the XC3S700A and the XC3S1400A FPGAs. There are three pinout differences, as described in Table 86.

Table 83 lists all the FG484 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The shaded rows indicate pinout differences between the XC3S700A and the XC3S1400A FPGAs. The XC3S700A has three unconnected balls, indicated as N.C. (No Connection) in Table 83 and with the black diamond character (◆) in Table 83 and Figure 25.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 83: **Spartan-3A FG484 Pinout**

Bank	Pin Name	FG484 Ball	Type
0	IO_L01N_0	D18	I/O
0	IO_L01P_0	E17	I/O
0	IO_L02N_0	C19	I/O
0	IO_L02P_0/VREF_0	D19	VREF
0	IO_L03N_0	A20	I/O
0	IO_L03P_0	B20	I/O
0	IO_L04N_0	F15	I/O
0	IO_L04P_0	E15	I/O
0	IO_L05N_0	A18	I/O
0	IO_L05P_0	C18	I/O
0	IO_L06N_0	A19	I/O
0	IO_L06P_0/VREF_0	B19	VREF
0	IO_L07N_0	C17	I/O
0	IO_L07P_0	D17	I/O
0	IO_L08N_0	C16	I/O
0	IO_L08P_0	D16	I/O
0	IO_L09N_0	E14	I/O
0	IO_L09P_0	C14	I/O
0	IO_L10N_0	A17	I/O
0	IO_L10P_0	B17	I/O
0	IO_L11N_0	C15	I/O
0	IO_L11P_0	D15	I/O
0	IO_L12N_0/VREF_0	A15	VREF
0	IO_L12P_0	A16	I/O
0	IO_L13N_0	A14	I/O
0	IO_L13P_0	B15	I/O
0	IO_L14N_0	E13	I/O
0	IO_L14P_0	F13	I/O
0	IO_L15N_0	C13	I/O
0	IO_L15P_0	D13	I/O
0	IO_L16N_0	A13	I/O
0	IO_L16P_0	B13	I/O
0	IO_L17N_0/GCLK5	E12	GCLK
0	IO_L17P_0/GCLK4	C12	GCLK
0	IO_L18N_0/GCLK7	A11	GCLK
0	IO_L18P_0/GCLK6	A12	GCLK
0	IO_L19N_0/GCLK9	C11	GCLK
0	IO_L19P_0/GCLK8	B11	GCLK
0	IO_L20N_0/GCLK11	E11	GCLK
0	IO_L20P_0/GCLK10	D11	GCLK
0	IO_L21N_0	C10	I/O
0	IO_L21P_0	A10	I/O
0	IO_L22N_0	A8	I/O
0	IO_L22P_0	A9	I/O
0	IO_L23N_0	E10	I/O
0	IO_L23P_0	D10	I/O
0	IO_L24N_0/VREF_0	C9	VREF
0	IO_L24P_0	B9	I/O
0	IO_L25N_0	C8	I/O
0	IO_L25P_0	B8	I/O
0	IO_L26N_0	A6	I/O
0	IO_L26P_0	A7	I/O
0	IO_L27N_0	C7	I/O
0	IO_L27P_0	D7	I/O
0	IO_L28N_0	A5	I/O
0	IO_L28P_0	B6	I/O
0	IO_L29N_0	D6	I/O
0	IO_L29P_0	C6	I/O
0	IO_L30N_0	D8	I/O

Table 83: **Spartan-3A FG484 Pinout *(Continued)***

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
2	IP_2	AD10	INPUT
2	IP_2	AD16	INPUT
2	IP_2	AF2	INPUT
2	IP_2	AF7	INPUT
2	IP_2	Y11	INPUT
2	IP_2/VREF_2	AA9	VREF
2	IP_2/VREF_2	AA20	VREF
2	IP_2/VREF_2	AB6	VREF
2	IP_2/VREF_2	AB10	VREF
2	IP_2/VREF_2	AC10	VREF
2	IP_2/VREF_2	AD12	VREF
2	IP_2/VREF_2	AF15	VREF
2	IP_2/VREF_2	AF17	VREF
2	IP_2/VREF_2	AF22	VREF
2	IP_2/VREF_2	Y16	VREF
2	N.C. (◆)	AA8	N.C.
2	N.C. (◆)	AC5	N.C.
2	N.C. (◆)	AC22	N.C.
2	N.C. (◆)	AD5	N.C.
2	N.C. (◆)	Y18	N.C.
2	N.C. (◆)	Y19	N.C.
2	N.C. (◆)	AD23	N.C.
2	N.C. (◆)	W18	N.C.
2	N.C. (◆)	Y8	N.C.
2	VCCO_2	AB8	VCCO
2	VCCO_2	AB14	VCCO
2	VCCO_2	AB19	VCCO
2	VCCO_2	AE5	VCCO
2	VCCO_2	AE11	VCCO
2	VCCO_2	AE16	VCCO
2	VCCO_2	AE22	VCCO
2	VCCO_2	W11	VCCO
2	VCCO_2	W16	VCCO
3	IO_L01N_3	J9	I/O
3	IO_L01P_3	J8	I/O
3	IO_L02N_3	B1	I/O
3	IO_L02P_3	B2	I/O
3	IO_L03N_3	H7	I/O
3	IO_L03P_3	G6	I/O
3	IO_L05N_3	K8	I/O

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
3	IO_L05P_3	K9	I/O
3	IO_L06N_3	E4	I/O
3	IO_L06P_3	D3	I/O
3	IO_L07N_3	F4	I/O
3	IO_L07P_3	E3	I/O
3	IO_L09N_3	G4	I/O
3	IO_L09P_3	F5	I/O
3	IO_L10N_3	H6	I/O
3	IO_L10P_3	J7	I/O
3	IO_L11N_3	F2	I/O
3	IO_L11P_3	E1	I/O
3	IO_L13N_3	J6	I/O
3	IO_L13P_3	K7	I/O
3	IO_L14N_3	F3	I/O
3	IO_L14P_3	G3	I/O
3	IO_L15N_3	L9	I/O
3	IO_L15P_3	L10	I/O
3	IO_L17N_3	H1	I/O
3	IO_L17P_3	H2	I/O
3	IO_L18N_3	L7	I/O
3	IO_L18P_3	K6	I/O
3	IO_L19N_3	J4	I/O
3	IO_L19P_3	J5	I/O
3	IO_L21N_3	M9	I/O
3	IO_L21P_3	M10	I/O
3	IO_L22N_3	K4	I/O
3	IO_L22P_3	K5	I/O
3	IO_L23N_3	K2	I/O
3	IO_L23P_3	K3	I/O
3	IO_L25N_3	L3	I/O
3	IO_L25P_3	L4	I/O
3	IO_L26N_3	M7	I/O
3	IO_L26P_3	M8	I/O
3	IO_L27N_3	M3	I/O
3	IO_L27P_3	M4	I/O
3	IO_L28N_3	M6	I/O
3	IO_L28P_3	M5	I/O
3	IO_L29N_3/VREF_3	M1	VREF
3	IO_L29P_3	M2	I/O
3	IO_L30N_3	N4	I/O

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
3	IP_L58P_3	AA4	INPUT
3	IP_L62N_3	AB4	INPUT
3	IP_L62P_3	AB3	INPUT
3	IP_L66N_3/VREF_3	AE2	VREF
3	IP_L66P_3	AE1	INPUT
3	VCCO_3	AB2	VCCO
3	VCCO_3	E2	VCCO
3	VCCO_3	H5	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	L8	VCCO
3	VCCO_3	P5	VCCO
3	VCCO_3	T2	VCCO
3	VCCO_3	T8	VCCO
3	VCCO_3	W5	VCCO
GND	GND	A1	GND
GND	GND	A6	GND
GND	GND	A11	GND
GND	GND	A16	GND
GND	GND	A21	GND
GND	GND	A26	GND
GND	GND	AA1	GND
GND	GND	AA6	GND
GND	GND	AA11	GND
GND	GND	AA16	GND
GND	GND	AA21	GND
GND	GND	AA26	GND
GND	GND	AD3	GND
GND	GND	AD8	GND
GND	GND	AD13	GND
GND	GND	AD18	GND
GND	GND	AD24	GND
GND	GND	AF1	GND
GND	GND	AF6	GND
GND	GND	AF11	GND
GND	GND	AF16	GND
GND	GND	AF21	GND
GND	GND	AF26	GND
GND	GND	C3	GND
GND	GND	C9	GND
GND	GND	C14	GND

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
GND	GND	C19	GND
GND	GND	C24	GND
GND	GND	F1	GND
GND	GND	F6	GND
GND	GND	F11	GND
GND	GND	F16	GND
GND	GND	F21	GND
GND	GND	F26	GND
GND	GND	H3	GND
GND	GND	H8	GND
GND	GND	H14	GND
GND	GND	H19	GND
GND	GND	J24	GND
GND	GND	K10	GND
GND	GND	K17	GND
GND	GND	L1	GND
GND	GND	L6	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L15	GND
GND	GND	L21	GND
GND	GND	L26	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M16	GND
GND	GND	N3	GND
GND	GND	N8	GND
GND	GND	N11	GND
GND	GND	N15	GND
GND	GND	P12	GND
GND	GND	P16	GND
GND	GND	P19	GND
GND	GND	P24	GND
GND	GND	R11	GND
GND	GND	R13	GND
GND	GND	R15	GND
GND	GND	T1	GND
GND	GND	T6	GND
GND	GND	T12	GND
GND	GND	T14	GND