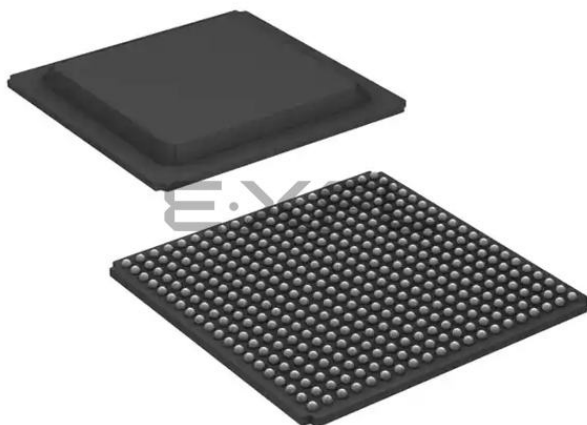




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	896
Number of Logic Elements/Cells	8064
Total RAM Bits	368640
Number of I/O	311
Number of Gates	400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	400-BGA
Supplier Device Package	400-FBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s400a-4fgg400i

Power Supply Specifications

Table 5: Supply Voltage Thresholds for Power-On Reset

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	1.0	2.0	V
V_{CCO2T}	Threshold for the V_{CCO} Bank 2 supply	1.0	2.0	V

Notes:

1. V_{CCINT} , V_{CCAUX} , and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. Apply V_{CCINT} last for lowest overall power consumption (see [UG331](#) chapter "Powering Spartan-3 Generation FPGAs" for more information).
2. To ensure successful power-on, V_{CCINT} , V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 6: Supply Voltage Ramp Rate

Symbol	Description	Min	Max	Units
V_{CCINTR}	Ramp rate from GND to valid V_{CCINT} supply level	0.2	100	ms
V_{CCAUXR}	Ramp rate from GND to valid V_{CCAUX} supply level	0.2	100	ms
V_{CCO2R}	Ramp rate from GND to valid V_{CCO} Bank 2 supply level	0.2	100	ms

Notes:

1. V_{CCINT} , V_{CCAUX} , and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. Apply V_{CCINT} last for lowest overall power consumption (see [UG331](#) chapter "Powering Spartan-3 Generation FPGAs" for more information).
2. To ensure successful power-on, V_{CCINT} , V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 7: Supply Voltage Levels Necessary for Preserving CMOS Configuration Latch (CCL) Contents and RAM Data

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain CMOS Configuration Latch (CCL) and RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain CMOS Configuration Latch (CCL) and RAM data	2.0	V

External Termination Requirements for Differential I/O

LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards

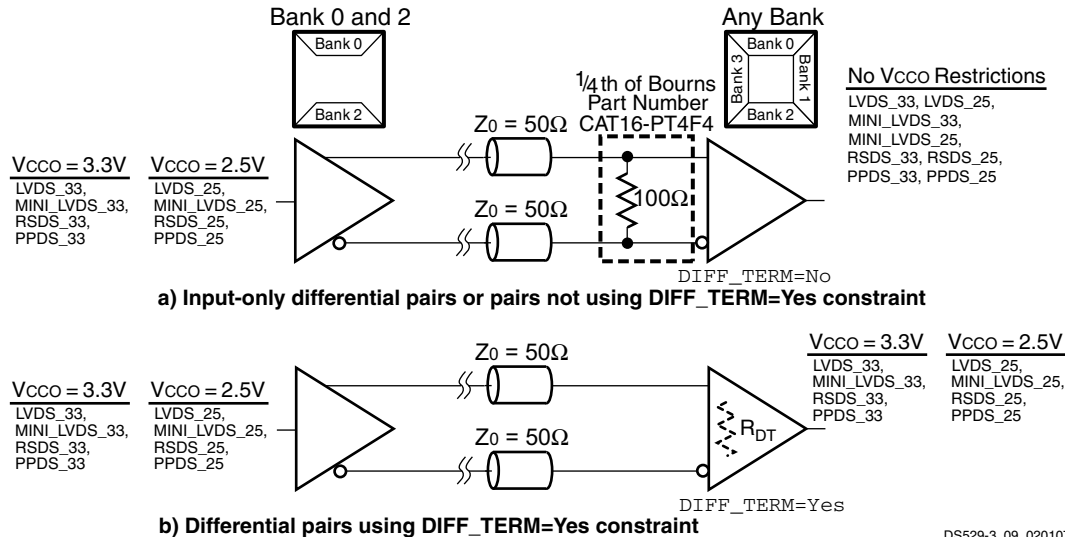


Figure 6: External Input Termination for LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards

BLVDS_25 I/O Standard

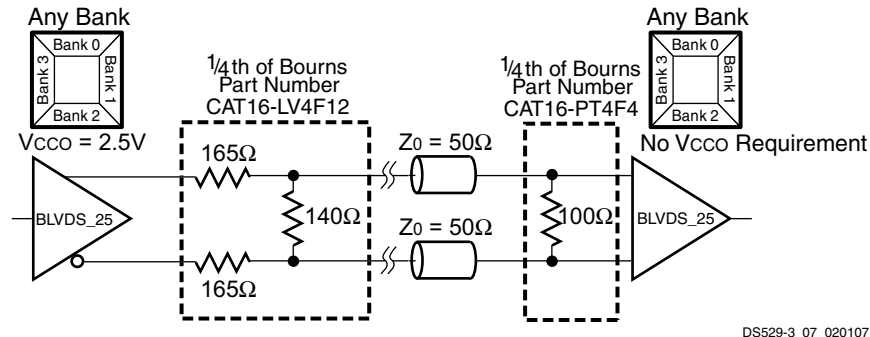


Figure 7: External Output and Input Termination Resistors for BLVDS_25 I/O Standard

TMDS_33 I/O Standard

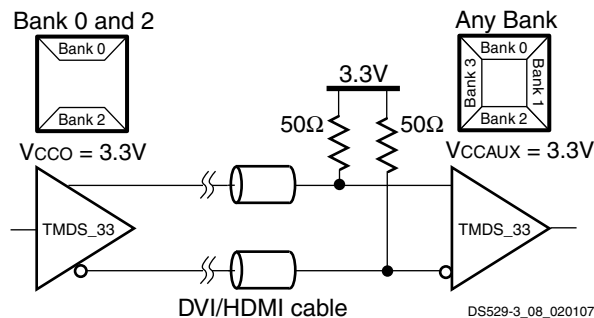


Figure 8: External Input Resistors Required for TMDS_33 I/O Standard

Device DNA Read Endurance

Table 15: Device DNA Identifier Memory Characteristics

Symbol	Description	Minimum	Units
DNA_CYCLES	Number of READ operations or JTAG ISC_DNA read operations. Unaffected by HOLD or SHIFT operations.	30,000,000	Read cycles

Table 20: Setup and Hold Times for the IOB Input Path(Continued)

Symbol	Description	Conditions	IFD_ DELAY_ VALUE	Device	Speed Grade		Units
					-5	-4	
					Min	Min	
T _{IOICKD}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). The Input Delay is programmed.	LVCMOS25 ⁽²⁾	1	XC3S700A	1.82	1.95	ns
			2		2.62	2.83	ns
			3		3.32	3.72	ns
			4		3.83	4.31	ns
			5		3.69	4.14	ns
			6		4.60	5.19	ns
			7		5.39	6.10	ns
			8		5.92	6.73	ns
			1	XC3S1400A	1.79	2.17	ns
			2		2.55	2.92	ns
			3		3.38	3.76	ns
			4		3.75	4.32	ns
			5		3.81	4.19	ns
			6		4.39	5.09	ns
			7		5.16	5.98	ns
			8		5.69	6.57	ns
Hold Times							
T _{IOICKP}	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. No Input Delay is programmed.	LVCMOS25 ⁽³⁾	0	XC3S50A	−0.66	−0.64	ns
				XC3S200A	−0.85	−0.65	ns
				XC3S400A	−0.42	−0.42	ns
				XC3S700A	−0.81	−0.67	ns
				XC3S1400A	−0.71	−0.71	ns
T _{IOICKPD}	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25 ⁽³⁾	1	XC3S50A	−0.88	−0.88	ns
			2		−1.33	−1.33	ns
			3		−2.05	−2.05	ns
			4		−2.43	−2.43	ns
			5		−2.34	−2.34	ns
			6		−2.81	−2.81	ns
			7		−3.03	−3.03	ns
			8		−3.83	−3.57	ns
			1	XC3S200A	−1.51	−1.51	ns
			2		−2.09	−2.09	ns
			3		−2.40	−2.40	ns
			4		−2.68	−2.68	ns
			5		−2.56	−2.56	ns
			6		−2.99	−2.99	ns
			7		−3.29	−3.29	ns
			8		−3.61	−3.61	ns

Table 26: Output Timing Adjustments for IOB(Continued)

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Differential Standards			
LVDS_25	1.16	1.16	ns
LVDS_33	0.46	0.46	ns
BLVDS_25	0.11	0.11	ns
MINI_LVDS_25	0.75	0.75	ns
MINI_LVDS_33	0.40	0.40	ns
LVPECL_25	Input Only		
LVPECL_33			
RSDS_25	1.42	1.42	ns
RSDS_33	0.58	0.58	ns
TMDS_33	0.46	0.46	ns
PPDS_25	1.07	1.07	ns
PPDS_33	0.63	0.63	ns
DIFF_HSTL_I_18	0.43	0.43	ns
DIFF_HSTL_II_18	0.41	0.41	ns
DIFF_HSTL_III_18	0.36	0.36	ns
DIFF_HSTL_I	1.01	1.01	ns
DIFF_HSTL_III	0.54	0.54	ns
DIFF_SSTL18_I	0.49	0.49	ns
DIFF_SSTL18_II	0.41	0.41	ns
DIFF_SSTL2_I	0.82	0.82	ns
DIFF_SSTL2_II	0.09	0.09	ns
DIFF_SSTL3_I	1.16	1.16	ns
DIFF_SSTL3_II	0.28	0.28	ns

Notes:

1. The numbers in this table are tested using the methodology presented in [Table 27](#) and are based on the operating conditions set forth in [Table 8](#), [Table 11](#), and [Table 13](#).
2. These adjustments are used to convert output- and three-state-path times originally specified for the LVCMOS25 standard with 12 mA drive and Fast slew rate to times that correspond to other signal standards. Do not adjust times that measure when outputs go into a high-impedance state.
3. Note that 16 mA drive is faster than 24 mA drive for the Slow slew rate.

Table 28: Equivalent V_{CCO}/GND Pairs per Bank

Device	Package Style (including Pb-free)						
	VQ100	TQ144	FT256	FG320	FG400	FG484	FG676
XC3S50A	1	2	3	—	—	—	—
XC3S200A	1	—	4	4	—	—	—
XC3S400A	—	—	4	4	5	—	—
XC3S700A	—	—	4	—	5	5	—
XC3S1400A	—	—	4	—	—	6	9

Table 29: Recommended Number of Simultaneously Switching Outputs per VCCO-GND Pair (V_{CCAUX}=3.3V)

Signal Standard (IOSTANDARD)			Package Type				
			VQ100, TQ144		FT256, FG320, FG400, FG484, FG676		
			Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)	
Single-Ended Standards							
LVTTTL	Slow	2	20	20	60	60	
		4	10	10	41	41	
		6	10	10	29	29	
		8	6	6	22	22	
		12	6	6	13	13	
		16	5	5	11	11	
		24	4	4	9	9	
	Fast	2	10	10	10	10	
		4	6	6	6	6	
		6	5	5	5	5	
		8	3	3	3	3	
		12	3	3	3	3	
		16	3	3	3	3	
		24	2	2	2	2	
	QuietIO	2	40	40	80	80	
		4	24	24	48	48	
		6	20	20	36	36	
		8	16	16	27	27	
		12	12	12	16	16	
		16	9	9	13	13	
		24	9	9	12	12	

Table 29: Recommended Number of Simultaneously Switching Outputs per VCCO-GND Pair (V_{CCAUX}=3.3V)(Continued)

Signal Standard (IOSTANDARD)			Package Type				
			VQ100, TQ144		FT256, FG320, FG400, FG484, FG676		
			Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)	
LVCMOS33	Slow	2	24	24	76	76	
		4	14	14	46	46	
		6	11	11	27	27	
		8	10	10	20	20	
		12	9	9	13	13	
		16	8	8	10	10	
		24	—	8	—	9	
	Fast	2	10	10	10	10	
		4	8	8	8	8	
		6	5	5	5	5	
		8	4	4	4	4	
		12	4	4	4	4	
		16	2	2	2	2	
		24	—	2	—	2	
	QuietIO	2	36	36	76	76	
		4	32	32	46	46	
		6	24	24	32	32	
		8	16	16	26	26	
		12	16	16	18	18	
		16	12	12	14	14	
		24	—	10	—	10	

Table 29: Recommended Number of Simultaneously Switching Outputs per VCCO-GND Pair ($V_{CCAUX}=3.3V$)(Continued)

Signal Standard (IOSTANDARD)	Package Type			
	VQ100, TQ144		FT256, FG320, FG400, FG484, FG676	
	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)
Differential Standards (Number of I/O <i>Pairs</i> or Channels)				
LVDS_25	8	—	22	—
LVDS_33	8	—	27	—
BLVDS_25	1	1	4	4
MINI_LVDS_25	8	—	22	—
MINI_LVDS_33	8	—	27	—
LVPECL_25	Input Only			
LVPECL_33	Input Only			
RSDS_25	8	—	22	—
RSDS_33	8	—	27	—
TMDS_33	8	—	27	—
PPDS_25	8	—	22	—
PPDS_33	8	—	27	—
DIFF_HSTL_I	—	5	—	10
DIFF_HSTL_III	—	3	—	4
DIFF_HSTL_I_18	6	6	8	8
DIFF_HSTL_II_18	—	2	—	2
DIFF_HSTL_III_18	4	4	5	4
DIFF_SSTL18_I	3	6	3	7
DIFF_SSTL18_II	—	4	—	4
DIFF_SSTL2_I	5	5	9	9
DIFF_SSTL2_II	—	3	—	4
DIFF_SSTL3_I	3	4	4	5
DIFF_SSTL3_II	2	3	3	3

Notes:

- Not all I/O standards are supported on all I/O banks. The left and right banks (I/O banks 1 and 3) support higher output drive current than the top and bottom banks (I/O banks 0 and 2). Similarly, true differential output standards, such as LVDS, RSDS, PPDS, miniLVDS, and TMDS, are only supported in top or bottom banks (I/O banks 0 and 2). Refer to [UG331: Spartan-3 Generation FPGA User Guide](#) for additional information.
- The numbers in this table are recommendations that assume sound board lay out practice. Test limits are the V_{IL}/V_{IH} voltage limits for the respective I/O standard.
- If more than one signal standard is assigned to the I/Os of a given bank, refer to [XAPP689: Managing Ground Bounce in Large FPGAs](#) for information on how to perform weighted average SSO calculations.

Table 31: CLB Distributed RAM Switching Characteristics

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T _{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output	–	1.69	–	2.01	ns
Setup Times						
T _{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	–0.07	–	–0.02	–	ns
T _{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.18	–	0.36	–	ns
T _{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.30	–	0.59	–	ns
Hold Times						
T _{DH}	Hold time of the BX and BY data inputs after the active transition at the CLK input of the distributed RAM	0.13	–	0.13	–	ns
T _{AH} , T _{WH}	Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM	0.01	–	0.01	–	ns
Clock Pulse Width						
T _{WPH} , T _{WPL}	Minimum High or Low pulse width at CLK input	0.88	–	1.01	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in [Table 8](#).

Table 32: CLB Shift Register Switching Characteristics

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T _{REG}	Time from the active edge at the CLK input to data appearing on the shift register output	–	4.11	–	4.82	ns
Setup Times						
T _{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.13	–	0.18	–	ns
Hold Times						
T _{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0.16	–	0.16	–	ns
Clock Pulse Width						
T _{WPH} , T _{WPL}	Minimum High or Low pulse width at CLK input	0.90	–	1.01	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in [Table 8](#).

Table 37: Switching Characteristics for the DLL

Symbol	Description	Device	Speed Grade				Units	
			-5		-4			
			Min	Max	Min	Max		
Output Frequency Ranges								
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs	All	5	280	5	250	MHz	
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs		5	200	5	200	MHz	
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs		10	334	10	334	MHz	
CLKOUT_FREQ_DV	Frequency for the CLKDV output		0.3125	186	0.3125	166	MHz	
Output Clock Jitter ^(2,3,4)								
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output	All	—	±100	—	±100	ps	
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output		—	±150	—	±150	ps	
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output		—	±150	—	±150	ps	
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output		—	±150	—	±150	ps	
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs		—	±[0.5% of CLKIN period + 100]	—	±[0.5% of CLKIN period + 100]	ps	
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division		—	±150	—	±150	ps	
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division		—	±[0.5% of CLKIN period + 100]	—	±[0.5% of CLKIN period + 100]	ps	
Duty Cycle ⁽⁴⁾								
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion	All	—	±[1% of CLKIN period + 350]	—	±[1% of CLKIN period + 350]	ps	
Phase Alignment ⁽⁴⁾								
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs	All	—	±150	—	±150	ps	
CLKOUT_PHASE_DLL	Phase offset between DLL outputs		CLK0 to CLK2X (not CLK2X180)	—	±[1% of CLKIN period + 100]	—	±[1% of CLKIN period + 100]	ps
			All others	—	±[1% of CLKIN period + 150]	—	±[1% of CLKIN period + 150]	ps
Lock Time								
LOCK_DLL ⁽³⁾	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	5 MHz ≤ F _{CLKIN} ≤ 15 MHz	All	—	5	—	5	ms
		F _{CLKIN} > 15 MHz		—	600	—	600	μs
Delay Lines								
DCM_DELAY_STEP ⁽⁵⁾	Finest delay resolution, averaged over all steps	All	15	35	15	35	ps	

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8 and Table 36.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, the data sheet specifies a maximum jitter of "±[1% of CLKIN period + 150]". Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250ps.
5. The typical delay step size is 23 ps.

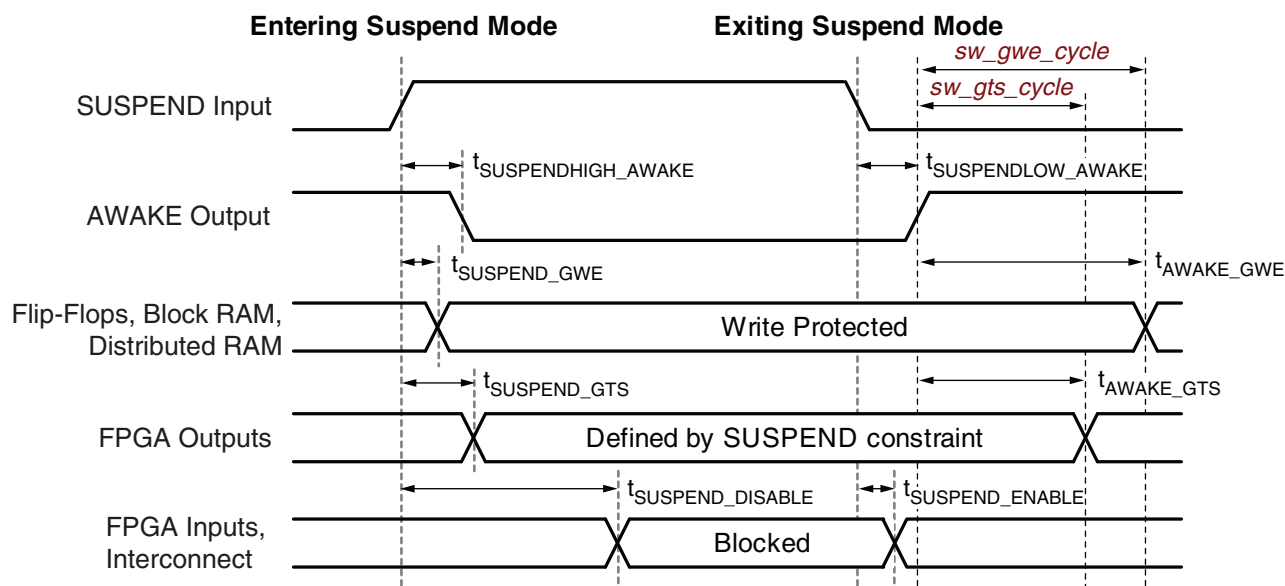
Table 39: Switching Characteristics for the DFS(Continued)

Symbol	Description	Device	Speed Grade				Units	
			-5		-4			
			Min	Max	Min	Max		
Lock Time								
LOCK_FX ^(2, 3)	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. If using both the DLL and the DFS, use the longer locking time.	$5\text{ MHz} \leq F_{\text{CLKIN}} \leq 15\text{ MHz}$	All	—	5	—	5	ms
		$F_{\text{CLKIN}} > 15\text{ MHz}$		—	450	—	450	μs

Notes:

1. The numbers in this table are based on the operating conditions set forth in [Table 8](#) and [Table 38](#).
2. DFS performance requires the additional logic automatically added by ISE 9.1i and later software revisions.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Maximum output jitter is characterized within a reasonable noise environment (150 ps input period jitter, 40 SSOs and 25% CLB switching) on an XC3S1400A FPGA. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply and PCB design. The actual maximum output jitter depends on the system application.
5. The CLKFX and CLKFX180 outputs always have an approximate 50% duty cycle.
6. Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, the data sheet specifies a maximum CLKFX jitter of “±[1% of CLKFX period + 200]”. Assume the CLKFX output frequency is 100 MHz. The equivalent CLKFX period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 200 ps] = ±300 ps.

Suspend Mode Timing



DS610-3_08_061207

Figure 10: Suspend Mode Timing

Table 44: Suspend Mode Timing Parameters

Symbol	Description	Min	Typ	Max	Units
Entering Suspend Mode					
$T_{\text{SUSPENDHIGH_AWAKE}}$	Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter (<i>suspend_filter:No</i>)	—	7	—	ns
$T_{\text{SUSPENDFILTER}}$	Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled (<i>suspend_filter:Yes</i>)	+160	+300	+600	ns
$T_{\text{SUSPEND_GTS}}$	Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior	—	10	—	ns
$T_{\text{SUSPEND_GWE}}$	Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements	—	<5	—	ns
$T_{\text{SUSPEND_DISABLE}}$	Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled	—	340	—	ns
Exiting Suspend Mode					
$T_{\text{SUSPENDLOW_AWAKE}}$	Falling edge of the SUSPEND pin to rising edge of the AWAKE pin. Does not include DCM lock time.	—	4 to 108	—	μs
$T_{\text{SUSPEND_ENABLE}}$	Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled	—	3.7 to 109	—	μs
$T_{\text{AWAKE_GWE1}}$	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using <i>sw_clk:InternalClock</i> and <i>sw_gwe_cycle:1</i> .	—	67	—	ns
$T_{\text{AWAKE_GWE512}}$	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using <i>sw_clk:InternalClock</i> and <i>sw_gwe_cycle:512</i> .	—	14	—	μs
$T_{\text{AWAKE_GTS1}}$	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using <i>sw_clk:InternalClock</i> and <i>sw_gts_cycle:1</i> .	—	57	—	ns
$T_{\text{AWAKE_GTS512}}$	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using <i>sw_clk:InternalClock</i> and <i>sw_gts_cycle:512</i> .	—	14	—	μs

Notes:

- These parameters based on characterization.
- For information on using the Spartan-3A Suspend feature, see [XAPP480: Using Suspend Mode in Spartan-3 Generation FPGAs](#).

Table 53: Configuration Timing Requirements for Attached SPI Serial Flash

Symbol	Description	Requirement	Units
T_{CCS}	SPI serial Flash PROM chip-select time	$T_{CCS} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DSU}	SPI serial Flash PROM data input setup time	$T_{DSU} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DH}	SPI serial Flash PROM data input hold time	$T_{DH} \leq T_{MCCH1}$	ns
T_V	SPI serial Flash PROM data clock-to-output time	$T_V \leq T_{MCCLn} - T_{DCC}$	ns
f_C or f_R	Maximum SPI serial Flash PROM clock frequency (also depends on specific read command used)	$f_C \geq \frac{1}{T_{CCLKn(min)}}$	MHz

Notes:

1. These requirements are for successful FPGA configuration in SPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.

Table 59: Maximum User I/O by Package

Device	Package	Maximum User I/Os and Input-Only	Maximum Input-Only	Maximum Differential Pairs	All Possible I/Os by Type					
					I/O	INPUT	DUAL	VREF	CLK	N.C.
XC3S50A	VQ100	68	6	60	17	2	20	6	23	0
XC3S200A		68	6	60	17	2	20	6	23	0
XC3S50A	TQ144	108	7	50	42	2	26	8	30	0
XC3S50A	FT256	144	32	64	53	20	26	15	30	51
XC3S200A		195	35	90	69	21	52	21	32	0
XC3S400A		195	35	90	69	21	52	21	32	0
XC3S700A		161	13	60	59	2	52	18	30	0
XC3S1400A		161	13	60	59	2	52	18	30	0
XC3S200A	FG320	248	56	112	101	40	52	23	32	3
XC3S400A		251	59	112	101	42	52	24	32	0
XC3S400A	FG400	311	63	142	155	46	52	26	32	0
XC3S700A		311	63	142	155	46	52	26	32	0
XC3S700A	FG484	372	84	165	194	61	52	33	32	3
XC3S1400A		375	87	165	195	62	52	34	32	0
XC3S1400A	FG676	502	94	227	313	67	52	38	32	17

Notes:

1. Some VREFs are on INPUT pins. See pinout tables for details.

Electronic versions of the package pinout tables and footprints are available for download from the Xilinx website. Using a spreadsheet program, the data can be sorted and reformatted according to any specific needs. Similarly, the ASCII-text file is easily parsed by most scripting programs.

http://www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip

VQ100: 100-lead Very Thin Quad Flat Package

The XC3S50A and XC3S200 are available in the 100-lead very thin quad flat package, VQ100.

Table 63 lists all the package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The VQ100 does not support Suspend mode (SUSPEND and AWAKE are not connected), the address output pins for the Byte-wide Peripheral Interface (BPI) configuration mode, or daisy chain configuration (DOUT is not connected).

Table 63 also indicates that some differential I/O pairs have different assignments between the XC3S50A and the XC3S200A, highlighted in light blue. See "[Footprint Migration Differences](#)," [page 72](#) for additional information.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 63: Spartan-3A VQ100 Pinout

Bank	Pin Name	Pin	Type
0	IO_0/GCLK11	P90	CLK
0	IO_L01N_0	P78	IO
0	IO_L01P_0/VREF_0	P77	VREF
0	IO_L02N_0/GCLK5	P84	CLK
0	IO_L02P_0/GCLK4	P83	CLK
0	IO_L03N_0/GCLK7	P86	CLK
0	IO_L03P_0/GCLK6	P85	CLK
0	IO_L04N_0/GCLK9	P89	CLK
0	IO_L04P_0/GCLK8	P88	CLK
0	IO_L05N_0	P94	IO
0	IO_L05P_0	P93	IO
0	IO_L06N_0/PUDC_B	P99	DUAL
0	IO_L06P_0/VREF_0	P98	VREF
0	IP_0	P97	IP
0	IP_0/VREF_0	P82	VREF
0	VCCO_0	P79	VCCO
0	VCCO_0	P96	VCCO
1	IO_L01N_1	P57	IO
1	IO_L01P_1	P56	IO
1	IO_L02N_1/RHCLK1	P60	CLK

Table 63: Spartan-3A VQ100 Pinout(Continued)

1	IO_L02P_1/RHCLK0	P59	CLK
1	IO_L03N_1/TRDY1/RHCLK3	P62	CLK
1	IO_L03P_1/RHCLK2	P61	CLK
1	IO_L04N_1/RHCLK7	P65	CLK
1	IO_L04P_1/IRDY1/RHCLK6	P64	CLK
1	IO_L05N_1	P71	IO
1	IO_L05P_1	P70	IO
1	IO_L06N_1	P73	IO
1	IO_L06P_1	P72	IO
1	IP_1/VREF_1	P68	VREF
1	VCCO_1	P67	VCCO
2	IO_2/MOSI/CSI_B	P46	DUAL
2	IO_L01N_2/M0	P25	DUAL
2	IO_L01P_2/M1	P23	DUAL
2	IO_L02N_2/CSO_B	P27	DUAL
2	IO_L02P_2/M2	P24	DUAL
2	IO_L03N_2/VS1 (3S50A) IO_L04P_2/VS1 (3S200A)	P30	DUAL
2	IO_L03P_2/RDWR_B	P28	DUAL
2	IO_L04N_2/VS0	P31	DUAL
2	IO_L04P_2/VS2 (3S50A) IO_L03N_2/VS2 (3S200A)	P29	DUAL
2	IO_L05N_2/D7 (3S50A) IO_L06P_2/D7 (3S200A)	P34	DUAL
2	IO_L05P_2	P32	IO
2	IO_L06N_2/D6	P35	DUAL
2	IO_L06P_2 (3S50A) IO_L05N_2 (3S200A)	P33	IO
2	IO_L07N_2/D4	P37	DUAL
2	IO_L07P_2/D5	P36	DUAL
2	IO_L08N_2/GCLK15	P41	CLK
2	IO_L08P_2/GCLK14	P40	CLK
2	IO_L09N_2/GCLK1	P44	CLK
2	IO_L09P_2/GCLK0	P43	CLK
2	IO_L10N_2/D3	P49	DUAL
2	IO_L10P_2/INIT_B	P48	DUAL
2	IO_L11N_2/D0/DIN/MISO (3S50A) IO_L12P_2/D0/DIN/MISO (3S200A)	P51	DUAL
2	IO_L11P_2/D2	P50	DUAL
2	IO_L12N_2/CCLK	P53	DUAL

Table 66: Spartan-3A TQ144 Pinout(Continued)

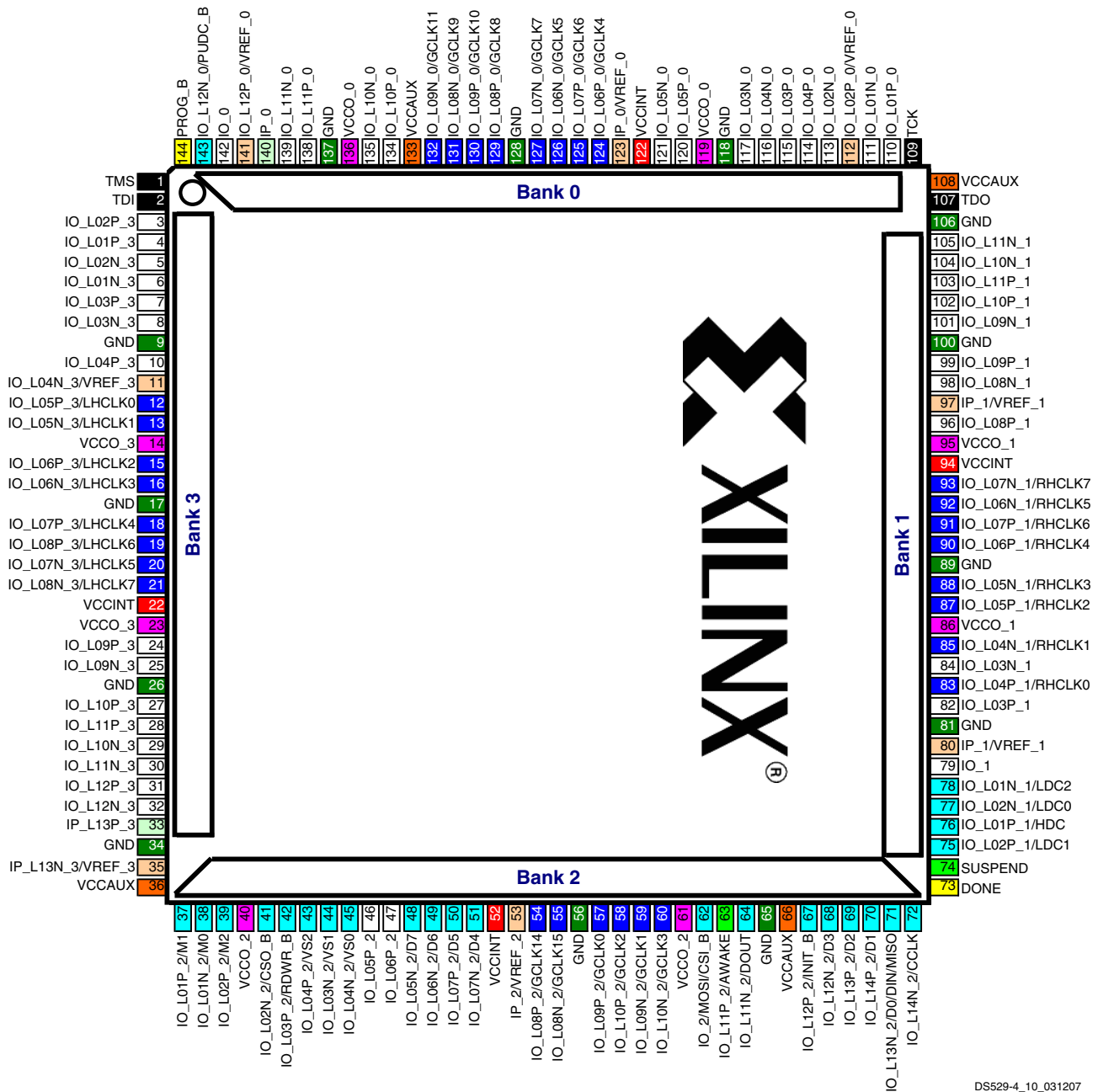
Bank	Pin Name	Pin	Type
2	IO_L05P_2	P46	I/O
2	IO_L06N_2/D6	P49	DUAL
2	IO_L06P_2	P47	I/O
2	IO_L07N_2/D4	P51	DUAL
2	IO_L07P_2/D5	P50	DUAL
2	IO_L08N_2/GCLK15	P55	GCLK
2	IO_L08P_2/GCLK14	P54	GCLK
2	IO_L09N_2/GCLK1	P59	GCLK
2	IO_L09P_2/GCLK0	P57	GCLK
2	IO_L10N_2/GCLK3	P60	GCLK
2	IO_L10P_2/GCLK2	P58	GCLK
2	IO_L11N_2/DOOUT	P64	DUAL
2	IO_L11P_2/AWAKE	P63	PWR MGMT
2	IO_L12N_2/D3	P68	DUAL
2	IO_L12P_2/INIT_B	P67	DUAL
2	IO_L13N_2/D0/DIN/MISO	P71	DUAL
2	IO_L13P_2/D2	P69	DUAL
2	IO_L14N_2/CCLK	P72	DUAL
2	IO_L14P_2/D1	P70	DUAL
2	IP_2/VREF_2	P53	VREF
2	VCCO_2	P40	VCCO
2	VCCO_2	P61	VCCO
3	IO_L01N_3	P6	I/O
3	IO_L01P_3	P4	I/O
3	IO_L02N_3	P5	I/O
3	IO_L02P_3	P3	I/O
3	IO_L03N_3	P8	I/O
3	IO_L03P_3	P7	I/O
3	IO_L04N_3/VREF_3	P11	VREF
3	IO_L04P_3	P10	I/O
3	IO_L05N_3/LHCLK1	P13	LHCLK
3	IO_L05P_3/LHCLK0	P12	LHCLK
3	IO_L06N_3/IRDY2/LHCLK3	P16	LHCLK
3	IO_L06P_3/LHCLK2	P15	LHCLK
3	IO_L07N_3/LHCLK5	P20	LHCLK
3	IO_L07P_3/LHCLK4	P18	LHCLK
3	IO_L08N_3/LHCLK7	P21	LHCLK
3	IO_L08P_3/TRDY2/LHCLK6	P19	LHCLK
3	IO_L09N_3	P25	I/O
3	IO_L09P_3	P24	I/O
3	IO_L10N_3	P29	I/O

Table 66: Spartan-3A TQ144 Pinout(Continued)

Bank	Pin Name	Pin	Type
3	IO_L10P_3	P27	I/O
3	IO_L11N_3	P30	I/O
3	IO_L11P_3	P28	I/O
3	IO_L12N_3	P32	I/O
3	IO_L12P_3	P31	I/O
3	IP_L13N_3/VREF_3	P35	VREF
3	IP_L13P_3	P33	INPUT
3	VCCO_3	P14	VCCO
3	VCCO_3	P23	VCCO
GND	GND	P9	GND
GND	GND	P17	GND
GND	GND	P26	GND
GND	GND	P34	GND
GND	GND	P56	GND
GND	GND	P65	GND
GND	GND	P81	GND
GND	GND	P89	GND
GND	GND	P100	GND
GND	GND	P106	GND
GND	GND	P118	GND
GND	GND	P128	GND
GND	GND	P137	GND
VCCAUX	SUSPEND	P74	PWR MGMT
VCCAUX	DONE	P73	CONFIG
VCCAUX	PROG_B	P144	CONFIG
VCCAUX	TCK	P109	JTAG
VCCAUX	TDI	P2	JTAG
VCCAUX	TDO	P107	JTAG
VCCAUX	TMS	P1	JTAG
VCCAUX	VCCAUX	P36	VCCAUX
VCCAUX	VCCAUX	P66	VCCAUX
VCCAUX	VCCAUX	P108	VCCAUX
VCCAUX	VCCAUX	P133	VCCAUX
VCCINT	VCCINT	P22	VCCINT
VCCINT	VCCINT	P52	VCCINT
VCCINT	VCCINT	P94	VCCINT
VCCINT	VCCINT	P122	VCCINT

TQ144 Footprint

Note pin 1 indicator in top-left corner and logo orientation.



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Figure 19: TQ144 Package Footprint (Top View)

42	I/O: Unrestricted, general-purpose user I/O	25	DUAL: Configuration pins, then possible user I/O	8	VREF: User I/O or input voltage reference for bank
2	INPUT: Unrestricted, general-purpose input pin	30	CLK: User I/O, input, or global buffer input	8	VCCO: Output voltage supply for bank
2	CONFIG: Dedicated configuration pins	4	JTAG: Dedicated JTAG port pins	4	VCCINT: Internal core supply voltage (+1.2V)
0	N.C.: Not connected	13	GND: Ground	4	VCCAUX: Auxiliary supply voltage
2	SUSPEND: Dedicated SUSPEND and dual-purpose AWAKE Power Management pins				

Table 69: Spartan-3A FT256 Pinout (XC3S700A,

Bank	XC3S700A XC3S1400A	FT256 Ball	Type
1	IO_L20P_1/A18	E14	DUAL
1	IO_L22N_1/A21	D15	DUAL
1	IO_L22P_1/A20	D16	DUAL
1	IO_L23N_1/A23	D14	DUAL
1	IO_L23P_1/A22	E13	DUAL
1	IO_L24N_1/A25	C15	DUAL
1	IO_L24P_1/A24	C16	DUAL
1	IP_1/VREF_1	H12	VREF
1	IP_1/VREF_1	J14	VREF
1	IP_1/VREF_1	M13	VREF
1	IP_1/VREF_1	M14	VREF
1	VCCO_1	E15	VCCO
1	VCCO_1	J15	VCCO
1	VCCO_1	N15	VCCO
2	IO_L01N_2/M0	P4	DUAL
2	IO_L01P_2/M1	N4	DUAL
2	IO_L02N_2/CSO_B	T2	DUAL
2	IO_L02P_2/M2	R2	DUAL
2	IO_L03N_2/VS2	T3	DUAL
2	IO_L03P_2/RDWR_B	R3	DUAL
2	IO_L04N_2/VS0	P5	DUAL
2	IO_L04P_2/VS1	N6	DUAL
2	IO_L05N_2	R5	I/O
2	IO_L05P_2	T4	I/O
2	IO_L06N_2/D6	T6	DUAL
2	IO_L06P_2/D7	T5	DUAL
2	IO_L08N_2/D4	N8	DUAL
2	IO_L08P_2/D5	P7	DUAL
2	IO_L09N_2/GCLK13	T7	GCLK
2	IO_L09P_2/GCLK12	R7	GCLK
2	IO_L10N_2/GCLK15	T8	GCLK
2	IO_L10P_2/GCLK14	P8	GCLK
2	IO_L11N_2/GCLK1	P9	GCLK
2	IO_L11P_2/GCLK0	N9	GCLK
2	IO_L12N_2/GCLK3	T9	GCLK
2	IO_L12P_2/GCLK2	R9	GCLK
2	IO_L14N_2/MOSI/CSI_B	P10	DUAL
2	IO_L14P_2	T10	I/O
2	IO_L15N_2/DOUT	R11	DUAL
2	IO_L15P_2/AWAKE	T11	PWRMGT

Table 69: Spartan-3A FT256 Pinout (XC3S700A,

Bank	XC3S700A XC3S1400A	FT256 Ball	Type
2	IO_L16N_2	N11	I/O
2	IO_L16P_2	P11	I/O
2	IO_L17N_2/D3	P12	DUAL
2	IO_L17P_2/INIT_B	T12	DUAL
2	IO_L18N_2/D1	R13	DUAL
2	IO_L18P_2/D2	T13	DUAL
2	IO_L19N_2	P13	I/O
2	IO_L19P_2	N12	I/O
2	IO_L20N_2/CCLK	R14	DUAL
2	IO_L20P_2/D0/DIN/MISO	T14	DUAL
2	IP_2/VREF_2	M11	VREF
2	IP_2/VREF_2	M7	VREF
2	IP_2/VREF_2	M9	VREF
2	IP_2/VREF_2	N5	VREF
2	IP_2/VREF_2	P6	VREF
2	VCCO_2	R12	VCCO
2	VCCO_2	R4	VCCO
2	VCCO_2	R8	VCCO
3	IO_L01N_3	C1	I/O
3	IO_L01P_3	C2	I/O
3	IO_L02N_3	D3	I/O
3	IO_L02P_3	D4	I/O
3	IO_L03N_3	E1	I/O
3	IO_L03P_3	D1	I/O
3	IO_L04N_3	F4	I/O
3	IO_L04P_3	E4	I/O
3	IO_L05N_3	E2	I/O
3	IO_L05P_3	E3	I/O
3	IO_L07N_3	G3	I/O
3	IO_L07P_3	F3	I/O
3	IO_L08N_3/VREF_3	G1	VREF
3	IO_L08P_3	F1	I/O
3	IO_L11N_3/LHCLK1	H1	LHCLK
3	IO_L11P_3/LHCLK0	G2	LHCLK
3	IO_L12N_3/IRDY2/LHCLK3	J3	LHCLK
3	IO_L12P_3/LHCLK2	H3	LHCLK
3	IO_L14N_3/LHCLK5	J1	LHCLK
3	IO_L14P_3/LHCLK4	J2	LHCLK
3	IO_L15N_3/LHCLK7	K1	LHCLK
3	IO_L15P_3/TRDY2/LHCLK6	K3	LHCLK

FT256 Footprint (XC3S200A, XC3S400A)

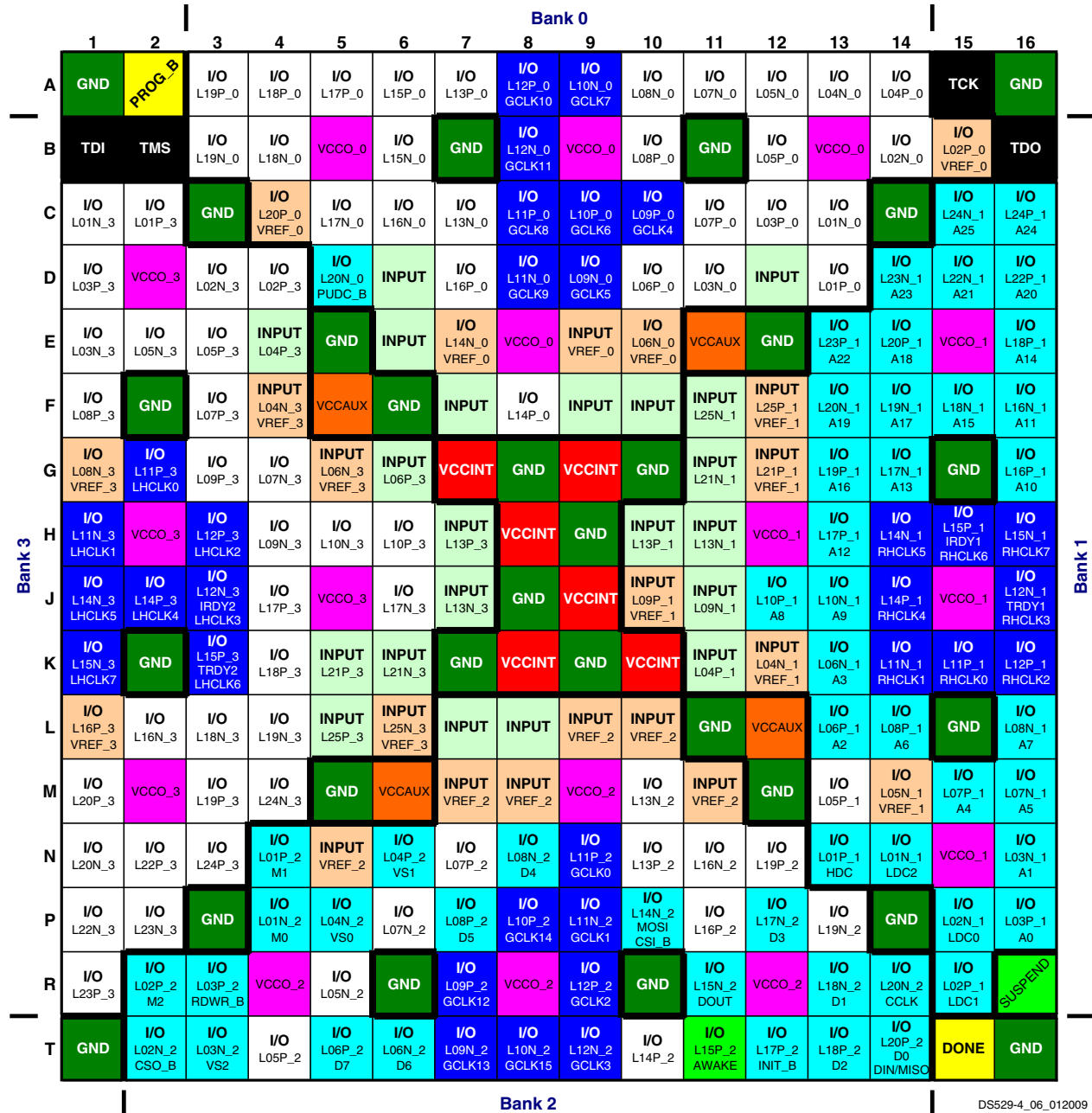


Figure 21: XC3S200A and XC3S400A FT256 Package Footprint (Top View)

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69	I/O: Unrestricted, general-purpose user I/O	51	DUAL: Configuration pins, then possible user I/O	21	VREF: User I/O or input voltage reference for bank	2	SUSPEND: Dedicated SUSPEND and dual-purpose AWAKE Power Management pins
21	INPUT: Unrestricted, general-purpose input pin	32	CLK: User I/O, input, or global buffer input	16	VCCO: Output voltage supply for bank		
2	CONFIG: Dedicated configuration pins	4	JTAG: Dedicated JTAG port pins	6	VCCINT: Internal core supply voltage (+1.2V)		
0	N.C.: Not connected	28	GND: Ground	4	VCCAUX: Auxiliary supply voltage		

Table 77: Spartan-3A FG320 Pinout(Continued)

Bank	Pin Name	FG320 Ball	Type
2	IO_L02N_2/CSO_B	V3	DUAL
2	IO_L02P_2/M2	V2	DUAL
2	IO_L03N_2/VS2	U4	DUAL
2	IO_L03P_2/RDWR_B	T4	DUAL
2	IO_L04N_2	T5	I/O
2	IO_L04P_2	R5	I/O
2	IO_L05N_2/VS0	V5	DUAL
2	IO_L05P_2/VS1	V4	DUAL
2	IO_L06N_2	U6	I/O
2	IO_L06P_2	T6	I/O
2	IO_L07N_2	P8	I/O
2	IO_L07P_2	N8	I/O
2	IO_L08N_2/D6	T7	DUAL
2	IO_L08P_2/D7	R7	DUAL
2	IO_L09N_2	R9	I/O
2	IO_L09P_2	T8	I/O
2	IO_L10N_2/D4	V6	DUAL
2	IO_L10P_2/D5	U7	DUAL
2	IO_L11N_2/GCLK13	V8	GCLK
2	IO_L11P_2/GCLK12	U8	GCLK
2	IO_L12N_2/GCLK15	V9	GCLK
2	IO_L12P_2/GCLK14	U9	GCLK
2	IO_L13N_2/GCLK1	T10	GCLK
2	IO_L13P_2/GCLK0	U10	GCLK
2	IO_L14N_2/GCLK3	U11	GCLK
2	IO_L14P_2/GCLK2	V11	GCLK
2	IO_L15N_2	R10	I/O
2	IO_L15P_2	P10	I/O
2	IO_L16N_2/MOSI/CSI_B	T11	DUAL
2	IO_L16P_2	R11	I/O
2	IO_L17N_2	V13	I/O
2	IO_L17P_2	U12	I/O
2	IO_L18N_2/DOUT	U13	DUAL
2	IO_L18P_2/AWAKE	T12	PWR MGMT
2	IO_L19N_2	P12	I/O
2	IO_L19P_2	N12	I/O
2	IO_L20N_2/D3	R13	DUAL
2	IO_L20P_2/INIT_B	T13	DUAL
2	IO_L21N_2	T14	I/O

Table 77: Spartan-3A FG320 Pinout(Continued)

Bank	Pin Name	FG320 Ball	Type
2	IO_L21P_2	V14	I/O
2	IO_L22N_2/D1	U15	DUAL
2	IO_L22P_2/D2	V15	DUAL
2	IO_L23N_2	T15	I/O
2	IO_L23P_2	R14	I/O
2	IO_L24N_2/CCLK	U16	DUAL
2	IO_L24P_2/D0/DIN/MISO	V16	DUAL
2	IP_2	M8	INPUT
2	IP_2	M9	INPUT
2	IP_2	M12	INPUT
2	XC3S400A: IP_2 XC3S200A: N.C. (◆)	N7	INPUT
2	IP_2	N9	INPUT
2	IP_2	N11	INPUT
2	IP_2	R6	INPUT
2	IP_2/VREF_2	M11	VREF
2	IP_2/VREF_2	N10	VREF
2	IP_2/VREF_2	P6	VREF
2	IP_2/VREF_2	P7	VREF
2	IP_2/VREF_2	P9	VREF
2	IP_2/VREF_2	P13	VREF
2	XC3S400A: IP_2/VREF_2 XC3S200A: N.C. (◆)	P14	VREF
2	VCCO_2	P11	VCCO
2	VCCO_2	R8	VCCO
2	VCCO_2	U5	VCCO
2	VCCO_2	U14	VCCO
3	IO_L01N_3	C1	I/O
3	IO_L01P_3	C2	I/O
3	IO_L02N_3	B1	I/O
3	IO_L02P_3	B2	I/O
3	IO_L03N_3	D2	I/O
3	IO_L03P_3	D3	I/O
3	IO_L05N_3	G5	I/O
3	IO_L05P_3	F5	I/O
3	IO_L06N_3	E3	I/O
3	IO_L06P_3	F4	I/O
3	IO_L07N_3	E1	I/O
3	IO_L07P_3	D1	I/O
3	IO_L09N_3	G4	I/O
3	IO_L09P_3	F3	I/O

Table 83: Spartan-3A FG484 Pinout(Continued)

Bank	Pin Name	FG484 Ball	Type
3	IP_L04P_3	H8	INPUT
3	IP_L11N_3	K8	INPUT
3	IP_L11P_3	J7	INPUT
3	IP_L15N_3/VREF_3	L8	VREF
3	IP_L15P_3	K7	INPUT
3	IP_L19N_3	M8	INPUT
3	IP_L19P_3	L7	INPUT
3	IP_L23N_3	M6	INPUT
3	IP_L23P_3	M7	INPUT
3	IP_L27N_3	N9	INPUT
3	IP_L27P_3	N8	INPUT
3	IP_L31N_3	N5	INPUT
3	IP_L31P_3	N6	INPUT
3	IP_L35N_3	P8	INPUT
3	IP_L35P_3	N7	INPUT
3	IP_L39N_3	R8	INPUT
3	IP_L39P_3	P7	INPUT
3	IP_L46N_3/VREF_3	T6	VREF
3	IP_L46P_3	R7	INPUT
3	VCCO_3	E2	VCCO
3	VCCO_3	J2	VCCO
3	VCCO_3	J6	VCCO
3	VCCO_3	N2	VCCO
3	VCCO_3	P6	VCCO
3	VCCO_3	V2	VCCO
GND	GND	A1	GND
GND	GND	A22	GND
GND	GND	AA11	GND
GND	GND	AA16	GND
GND	GND	AA7	GND
GND	GND	AB1	GND
GND	GND	AB22	GND
GND	GND	B12	GND
GND	GND	B16	GND
GND	GND	B7	GND
GND	GND	C20	GND
GND	GND	C3	GND
GND	GND	D14	GND
GND	GND	D9	GND
GND	GND	F11	GND

Table 83: Spartan-3A FG484 Pinout(Continued)

Bank	Pin Name	FG484 Ball	Type
GND	GND	F17	GND
GND	GND	F6	GND
GND	GND	G2	GND
GND	GND	G21	GND
GND	GND	J11	GND
GND	GND	J13	GND
GND	GND	J14	GND
GND	GND	J19	GND
GND	GND	J4	GND
GND	GND	J9	GND
GND	GND	K10	GND
GND	GND	K12	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L17	GND
GND	GND	L2	GND
GND	GND	L6	GND
GND	GND	L9	GND
GND	GND	M10	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M21	GND
GND	GND	N11	GND
GND	GND	N13	GND
GND	GND	P10	GND
GND	GND	P14	GND
GND	GND	P19	GND
GND	GND	P4	GND
GND	GND	P9	GND
GND	GND	T12	GND
GND	GND	T2	GND
GND	GND	T21	GND
GND	GND	U17	GND
GND	GND	U6	GND
GND	GND	W10	GND
GND	GND	W14	GND
GND	GND	Y20	GND
GND	GND	Y3	GND
VCCAUX	SUSPEND	U18	PWR MGMT

