AMD Xilinx - XC3S400A-4FT256I Datasheet

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	896
Number of Logic Elements/Cells	8064
Total RAM Bits	368640
Number of I/O	195
Number of Gates	400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s400a-4ft256i

Quiescent Current Requirements

Table 10: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Typical(2)	Commercial Maximum(2)	Industrial Maximum(2)	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC3S50A	2	20	30	mA
		XC3S200A	7	50	70	mA
		XC3S400A	10	85	125	mA
		XC3S700A	13	120	185	mA
		XC3S1400A	24	220	310	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC3S50A	0.2	2	3	mA
		XC3S200A	0.2	2	3	mA
		XC3S400A	0.3	3	4	mA
		XC3S700A	0.3	3	4	mA
		XC3S1400A	0.3	3	4	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC3S50A	3	8	10	mA
		XC3S200A	5	12	15	mA
		XC3S400A	5	18	24	mA
		XC3S700A	6	28	34	mA
		XC3S1400A	10	50	58	mA

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8.
2. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using typical devices at room temperature (T_J of 25°C at V_{CCINT} = 1.2V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.6V, and V_{CCAUX} = 3.6V. The FPGA is programmed with a "blank" configuration data file (that is, a design with no functional elements instantiated). For conditions other than those described above (for example, a design including functional elements), measured quiescent current levels will be different than the values in the table.
3. For more accurate estimates for a specific design, use the Xilinx XPower tools. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3A FPGA XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer uses a netlist as input to provide maximum estimates as well as more accurate typical estimates.
4. The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.
5. For information on the power-saving Suspend mode, see XAPP480: *Using Suspend Mode in Spartan-3 Generation FPGAs*. Suspend mode typically saves 40% total power consumption compared to quiescent current.

Table 22: **Propagation Times for the IOB Input Path *(Continued)***

Symbol	Description	Conditions	DELAY_VALUE	Device	Speed Grade		Units
					-5	-4	
					Max	Max	
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25(2)	5	XC3S400A	3.55	4.18	ns
			6		4.34	5.03	ns
			7		5.09	5.88	ns
			8		5.58	6.42	ns
			1	XC3S700A	1.96	2.18	ns
			2		2.76	3.06	ns
			3		3.45	3.95	ns
			4		3.97	4.54	ns
			5		3.83	4.37	ns
			6		4.74	5.42	ns
			7		5.53	6.33	ns
			8		6.06	6.96	ns
			1	XC3S1400A	1.93	2.40	ns
			2		2.69	3.15	ns
			3		3.52	3.99	ns
			4		3.89	4.55	ns
			5		3.95	4.42	ns
			6		4.53	5.32	ns
			7		5.30	6.21	ns
			8		5.83	6.80	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 23.

Input Timing Adjustments

Table 23: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Single-Ended Standards			
LVTTL	0.62	0.62	ns
LVCMOS33	0.54	0.54	ns
LVCMOS25	0	0	ns
LVCMOS18	0.83	0.83	ns
LVCMOS15	0.60	0.60	ns
LVCMOS12	0.31	0.31	ns
PCI33_3	0.41	0.41	ns
PCI66_3	0.41	0.41	ns
HSTL_I	0.72	0.72	ns
HSTL_III	0.77	0.77	ns
HSTL_I_18	0.69	0.69	ns
HSTL_II_18	0.69	0.69	ns
HSTL_III_18	0.79	0.79	ns
SSTL18_I	0.71	0.71	ns
SSTL18_II	0.71	0.71	ns
SSTL2_I	0.68	0.68	ns
SSTL2_II	0.68	0.68	ns
SSTL3_I	0.78	0.78	ns
SSTL3_II	0.78	0.78	ns

Table 23: **Input Timing Adjustments by IOSTANDARD*(Continued)***

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Differential Standards			
LVDS_25	0.76	0.76	ns
LVDS_33	0.79	0.79	ns
BLVDS_25	0.79	0.79	ns
MINI_LVDS_25	0.78	0.78	ns
MINI_LVDS_33	0.79	0.79	ns
LVPECL_25	0.78	0.78	ns
LVPECL_33	0.79	0.79	ns
RSDS_25	0.79	0.79	ns
RSDS_33	0.77	0.77	ns
TMDS_33	0.79	0.79	ns
PPDS_25	0.79	0.79	ns
PPDS_33	0.79	0.79	ns
DIFF_HSTL_I_18	0.74	0.74	ns
DIFF_HSTL_II_18	0.72	0.72	ns
DIFF_HSTL_III_18	1.05	1.05	ns
DIFF_HSTL_I	0.72	0.72	ns
DIFF_HSTL_III	1.05	1.05	ns
DIFF_SSTL18_I	0.71	0.71	ns
DIFF_SSTL18_II	0.71	0.71	ns
DIFF_SSTL2_I	0.74	0.74	ns
DIFF_SSTL2_II	0.75	0.75	ns
DIFF_SSTL3_I	1.06	1.06	ns
DIFF_SSTL3_II	1.06	1.06	ns

Notes:

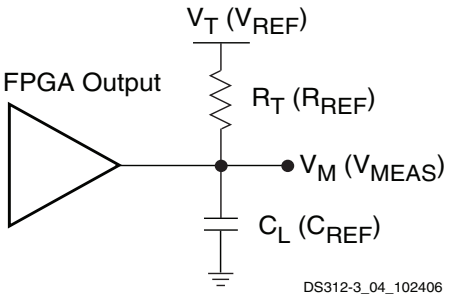
1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8, Table 11, and Table 13.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 27 lists the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H.

The Output test setup is shown in Figure 9. A termination voltage V_T is applied to the termination resistor R_T, the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (for example, LVCMOS, LVTTL), then R_T is set to 1MΩ to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



Notes:

1. The names shown in parentheses are used in the IBIS file.

Figure 9: **Output Test Setup**

Table 27: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended							
LVTTL		-	0	3.3	1M	0	1.4
LVCMOS33		-	0	3.3	1M	0	1.65
LVCMOS25		-	0	2.5	1M	0	1.25
LVCMOS18		-	0	1.8	1M	0	0.9
LVCMOS15		-	0	1.5	1M	0	0.75
LVCMOS12		-	0	1.2	1M	0	0.6
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
PCI66_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
HSTL_I		0.75	V_{REF} – 0.5	V_{REF} + 0.5	50	0.75	V_{REF}
HSTL_III		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	1.5	V_{REF}
HSTL_I_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_II_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL18_II		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
SSTL2_II		1.25	V_{REF} – 0.75	V_{REF} + 0.75	25	1.25	V_{REF}
SSTL3_I		1.5	V_{REF} – 0.75	V_{REF} + 0.75	50	1.5	V_{REF}
SSTL3_II		1.5	V_{REF} – 0.75	V_{REF} + 0.75	25	1.5	V_{REF}

Table 29: **Recommended Number of Simultaneously Switching Outputs per VCCO-GND Pair (V_{CCAUX}=3.3V)*(Continued)***

Signal Standard (IOSTANDARD)			Package Type			
			VQ100, TQ144		FT256, FG320, FG400, FG484, FG676	
			Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)
LVCMOS25	Slow	2	16	16	76	76
		4	10	10	46	46
		6	8	8	33	33
		8	7	7	24	24
		12	6	6	18	18
		16	–	6	–	11
		24	–	5	–	7
	Fast	2	12	12	18	18
		4	10	10	14	14
		6	8	8	6	6
		8	6	6	6	6
		12	3	3	3	3
		16	–	3	–	3
		24	–	2	–	2
	QuietIO	2	36	36	76	76
		4	30	30	60	60
		6	24	24	48	48
		8	20	20	36	36
		12	12	12	36	36
		16	–	12	–	36
		24	–	8	–	8
LVCMOS18	Slow	2	13	13	64	64
		4	8	8	34	34
		6	8	8	22	22
		8	7	7	18	18
		12	–	5	–	13
		16	–	5	–	10
	Fast	2	13	13	18	18
		4	8	8	9	9
		6	7	7	7	7
		8	4	4	4	4
		12	–	4	–	4
		16	–	3	–	3
	QuietIO	2	30	30	64	64
		4	24	24	64	64
		6	20	20	48	48
		8	16	16	36	36
		12	–	12	–	36
		16	–	12	–	24

Table 29: **Recommended Number of Simultaneously Switching Outputs per VCCO-GND Pair (V_{CCAUX}=3.3V)*(Continued)***

Signal Standard (IOSTANDARD)			Package Type			
			VQ100, TQ144		FT256, FG320, FG400, FG484, FG676	
			Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)
LVCMOS15	Slow	2	12	12	55	55
		4	7	7	31	31
		6	7	7	18	18
		8	–	6	–	15
		12	–	5	–	10
	Fast	2	10	10	25	25
		4	7	7	10	10
		6	6	6	6	6
		8	–	4	–	4
		12	–	3	–	3
	QuietIO	2	30	30	70	70
		4	21	21	40	40
		6	18	18	31	31
		8	–	12	–	31
		12	–	12	–	20
LVCMOS12	Slow	2	17	17	40	40
		4	–	13	–	25
		6	–	10	–	18
	Fast	2	12	9	31	31
		4	–	9	–	13
		6	–	9	–	9
	QuietIO	2	36	36	55	55
		4	–	33	–	36
		6	–	27	–	36
PCI33_3			9	9	16	16
PCI66_3			–	9	–	13
HSTL_I			–	11	–	20
HSTL_III			–	7	–	8
HSTL_I_18			13	13	17	17
HSTL_II_18			–	5	–	5
HSTL_III_18			8	8	10	8
SSTL18_I			7	13	7	15
SSTL18_II			–	9	–	9
SSTL2_I			10	10	18	18
SSTL2_II			–	6	–	9
SSTL3_I			7	8	8	10
SSTL3_II			5	6	6	7

Configurable Logic Block (CLB) Timing

Table 30: **CLB (SLICEM) Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{CKO}	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	–	0.60	–	0.68	ns
Setup Times						
T_{AS}	Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB	0.18	–	0.36	–	ns
T_{DICK}	Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB	1.58	–	1.88	–	ns
Hold Times						
T_{AH}	Time from the active transition at the CLK input to the point where data is last held at the F or G input	0	–	0	–	ns
T_{CKDI}	Time from the active transition at the CLK input to the point where data is last held at the BX or BY input	0	–	0	–	ns
Clock Timing						
T_{CH}	The High pulse width of the CLB's CLK signal	0.63	–	0.75	–	ns
T_{CL}	The Low pulse width of the CLK signal	0.63	–	0.75	–	ns
F_{TOG}	Toggle frequency (for export control)	0	770	0	667	MHz
Propagation Times						
T_{ILO}	The time it takes for data to travel from the CLB's F (G) input to the X (Y) output	–	0.62	–	0.71	ns
Set/Reset Pulse Width						
T_{RPW_CLB}	The minimum allowable pulse width, High or Low, to the CLB's SR input	1.33	–	1.61	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.

Suspend Mode Timing

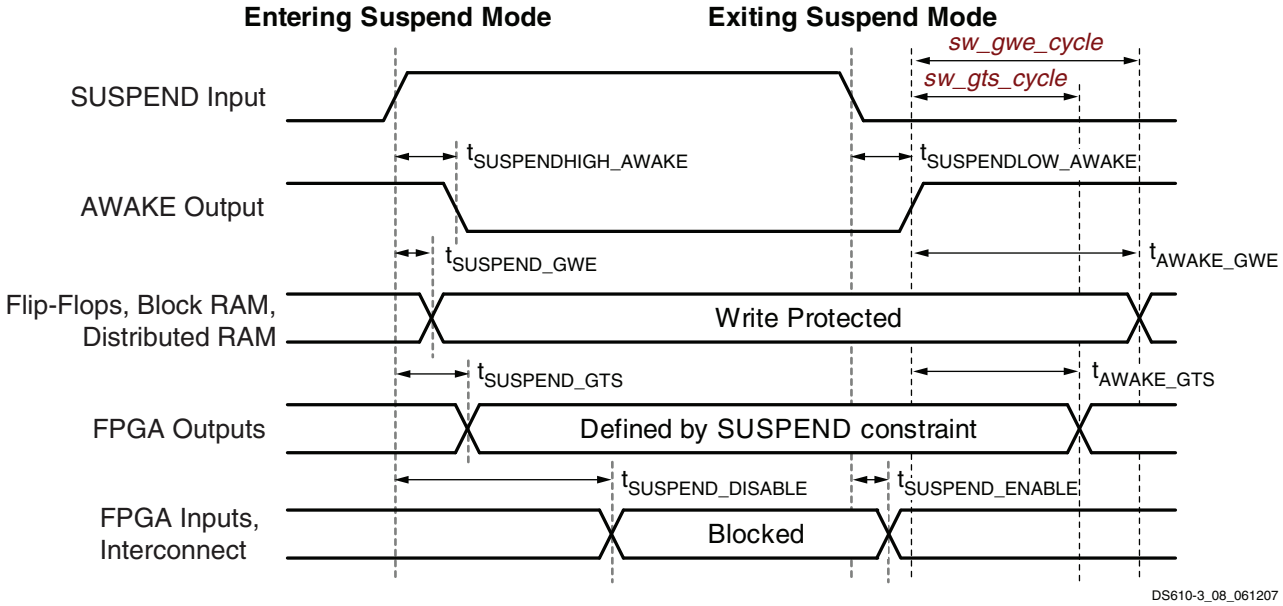


Figure 10: **Suspend Mode Timing**

Table 44: **Suspend Mode Timing Parameters**

Symbol	Description	Min	Typ	Max	Units
Entering Suspend Mode					
$T_{SUSPENDHIGH\_AWAKE}$	Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter (***suspend_filter:No***)	–	7	–	ns
$T_{SUSPENDFILTER}$	Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled (***suspend_filter:Yes***)	+160	+300	+600	ns
$T_{SUSPEND\_GTS}$	Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior	–	10	–	ns
$T_{SUSPEND\_GWE}$	Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements	–	<5	–	ns
$T_{SUSPEND\_DISABLE}$	Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled	–	340	–	ns
Exiting Suspend Mode					
$T_{SUSPENDLOW\_AWAKE}$	Falling edge of the SUSPEND pin to rising edge of the AWAKE pin. Does not include DCM lock time.	–	4 to 108	–	µs
$T_{SUSPEND\_ENABLE}$	Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled	–	3.7 to 109	–	µs
T_{AWAKE_GWE1}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using ***sw_clk:InternalClock*** and ***sw_gwe_cycle:1***.	–	67	–	ns
T_{AWAKE_GWE512}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using ***sw_clk:InternalClock*** and ***sw_gwe_cycle:512***.	–	14	–	µs
T_{AWAKE_GTS1}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using ***sw_clk:InternalClock*** and ***sw_gts_cycle:1***.	–	57	–	ns
T_{AWAKE_GTS512}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using ***sw_clk:InternalClock*** and ***sw_gts_cycle:512***.	–	14	–	µs

Notes:

1. These parameters based on characterization.
2. For information on using the Spartan-3A Suspend feature, see XAPP480: *Using Suspend Mode in Spartan-3 Generation FPGAs*.

Table 55: **Configuration Timing Requirements for Attached Parallel NOR BPI Flash**

Symbol	Description	Requirement	Units
T_{CE} (t_{ELQV})	Parallel NOR Flash PROM chip-select time	$T_{CE} \leq T_{INITADDR}$	ns
T_{OE} (t_{GLQV})	Parallel NOR Flash PROM output-enable time	$T_{OE} \leq T_{INITADDR}$	ns
T_{ACC} (t_{AVQV})	Parallel NOR Flash PROM read access time	$T_{ACC} \leq 50\% T_{CCLKn(min)} - T_{CCO} - T_{DCC} - PCB$	ns
T_{BYTE} (t_{FLQV}, t_{FHQV})	For x8/x16 PROMs only: BYTE# to output valid time(3)	$T_{BYTE} \leq T_{INITADDR}$	ns

Notes:

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's PUDC_B pin is High or Low.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/05/06	1.0	Initial release.
02/02/07	1.1	Promoted to Preliminary status. Moved Table 15 to under "DC Electrical Characteristics" section. Updated all timing specifications for the v1.32 speed files. Added recommended Simultaneous Switching Output (SSO) limits in Table 29. Set a 10 µs maximum pulse width for the DNA_PORT READ signal and the JTAG clock input during the ISC_DNA command, affecting both Table 43 and Table 56. Described "External Termination Requirements for Differential I/O." Added separate DIN hold time for Slave mode in Table 50. Corrected wording in Table 52 and Table 54; no specifications affected.
03/16/07	1.2	Updated all AC timing specifications to the v1.34 speeds file. Promoted the XC3S700A and XC3S1400A FPGAs offered in the -4 speed grade to Production status, as shown in Table 16. Added Note 2 to Table 39 regarding the extra logic (one LUT) automatically added by ISE 9.1i and later software revisions for any DCM application that leverages the Digital Frequency Synthesizer (DFS). Separated some JTAG specifications by array size or function, as shown in Table 56. Updated quiescent current limits in Table 10.
04/23/07	1.3	Updated all AC timing specifications to the v1.35 speeds file. Promoted all devices except the XC3S400A to Production status, as shown in Table 16.
05/08/07	1.4	Updated XC3S400A to Production and v1.36 speeds file. Added banking rules and other explanatory footnotes to Table 12 and Table 13. Corrected DIFF_SSTL3_II V_{OL} Max in Table 14. Improved XC3S400A Pin-to-Pin Clock-to-Output times in Table 18. Updated XC3S400A Pin-to-Pin Setup Times in Table 19. Updated TIOICKPD for -5 in Table 20. Added SSO numbers to Table 28 and Table 29. Removed invalid Embedded Multiplier Hold Times in Table 34. Improved CLKOUT_FREQ_CLK90 in Table 37. Improved T_{TDITCK} and F_{TCK} performance for XC3S400A in Table 56.
07/10/07	1.5	Added DIFF_HSTL_I and DIFF_HSTL_III to Table 13, Table 14, Table 27, and Table 29. Updated TMDS DC characteristics in Table 14. Updated for speed file v1.37 in ISE 9.2.01i as shown in Table 17. Updated pin-to-pin setup and hold times in Table 19. Updated TMDS output adjustment in Table 26. Updated I/O Test Method values in Table 27. Added BLVDS SSO numbers inTable 29. For Multiplier block, updated setup times and added hold times to Table 34. Updated block RAM clock width in Table 35. Updated CLKOUT_PER_JITT_2X and CLKOUT_PER_JITT_DV2 in Table 37. Added CCLK specifications for Commercial in Table 46 through Table 48.
04/15/08	1.6	Added V_{IN} to Recommended Operating Conditions in Table 8 and added reference to XAPP459, "Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins." Reduced typical I_{CCINTQ} and I_{CCAUXQ} quiescent current values by 12%-58% in Table 10. Increased V_{IL} max to 0.4V for LVCMOS12/15/18 and improved V_{IH} min to 0.7V for LVCMOS12 in Table 11. Changed V_{OL} max to 0.4V and V_{OH} min to V_{CCO}-0.4V for LVCMOS15/18 in Table 12. Noted latest speed file v1.39 in ISE 10.1 software in Table 16. Added new packages to SSO limits in Table 28 and Table 29. Improved SSTL18_II SSO limit for FG packages in Table 29. Improved F_{BUFG} for -4 to 334 MHz in Table 33. Added references to 375 MHz performance via SCD 4103 in Table 33,Table 38, Table 39, and Table 40. Restored Units column to Table 44. Updated CCLK output maximum period in Table 46 to match minimum frequency in Table 47. Corrected BPI active clock edge in Figure 15 and Table 54.
05/28/08	1.7	Improved V_{CCAUXT} and V_{CCO2T} POR minimum in Table 5 and updated V_{CCO} POR levels in Figure 11. Clarified recommended V_{IN} in Table 8. Added reference to V_{CCAUX} in "Simultaneously Switching Output Guidelines". Added reference to Sample Window in Table 21. Removed DNA_RETENTION limit of 10 years in Table 15 since number of Read cycles is the only unique limit. Added references to UG332.
03/06/09	1.8	Changed typical quiescent current temperature from ambient to junction. Updated BPI configuration waveforms in Figure 15 and updated Table 55. Updated selected I/O standard DC characteristics. Added TIOPI and TIOPID in Table 22. Removed references to SCD 4103.
08/19/10	2.0	Added I_{IK} to Table 4. Updated V_{IN} in Table 8 and footnoted I_L in Table 9 to note potential leakage between pins of a differential pair. Clarified LVPECL notes to Table 13. Corrected symbols for TSUSPEND_GTS and TSUSPEND_GWE in Table 44.

Package Overview

Table 60 shows the six low-cost, space-saving production package styles for the Spartan-3A family.

Table 60: **Spartan-3A Family Package Options**

Package	Leads	Type	Maximum I/O	Lead Pitch (mm)	Body Area (mm)	Height (mm)	Mass[1] (g)
VQ100 / VQG100	100	Very Thin Quad Flat Pack (VQFP)	68	0.5	14 x 14	1.20	0.6
TQ144 / TQG144	144	Thin Quad Flat Pack (TQFP)	108	0.5	20 x 20	1.60	1.4
FT256 / FTG256	256	Fine-pitch Thin Ball Grid Array (FBGA)	195	1.0	17 x 17	1.55	0.9
FG320 / FGG320	320	Fine-pitch Ball Grid Array (FBGA)	251	1.0	19 x 19	2.00	1.4
FG400 / FGG400	400	Fine-pitch Ball Grid Array (FBGA)	311	1.0	21 x 21	2.43	2.2
FG484 / FGG484	484	Fine-pitch Ball Grid Array (FBGA)	375	1.0	23 x 23	2.60	2.2
FG676 / FGG676	676	Fine-pitch Ball Grid Array (FBGA)	502	1.0	27 x 27	2.60	3.4

Notes:

1. Package mass is ±10%.

Each package style is available in an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra 'G' in the package style name. For example, the standard "CS484" package becomes "CSG484" when ordered as the Pb-free option. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 61.

For additional package information, see UG112: *Device Package User Guide*.

Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx web site at the specified location in Table 61.

Material Declaration Data Sheets (MDDS) are also available on the **Xilinx web site** for each package.

Table 61: **Xilinx Package Documentation**

Package	Drawing	MDDS
VQ100	Package Drawing	PK173_VQ100
VQG100		PK130_VQG100
TQ144	Package Drawing	PK169_TQ144
TQG144		PK126_TQG144
FT256	Package Drawing	PK158_FT256
FTG256		PK115_FTG256
FG320	Package Drawing	PK152_FG320
FGG320		PK106_FGG320
FG400	Package Drawing	PK182_FG400
FGG400		PK108_FGG400
FG484	Package Drawing	PK183_FG484
FGG484		PK110_FGG484
FG676	Package Drawing	PK155_FG676
FGG676		PK111_FGG676

FT256 Footprint (XC3S200A, XC3S400A)

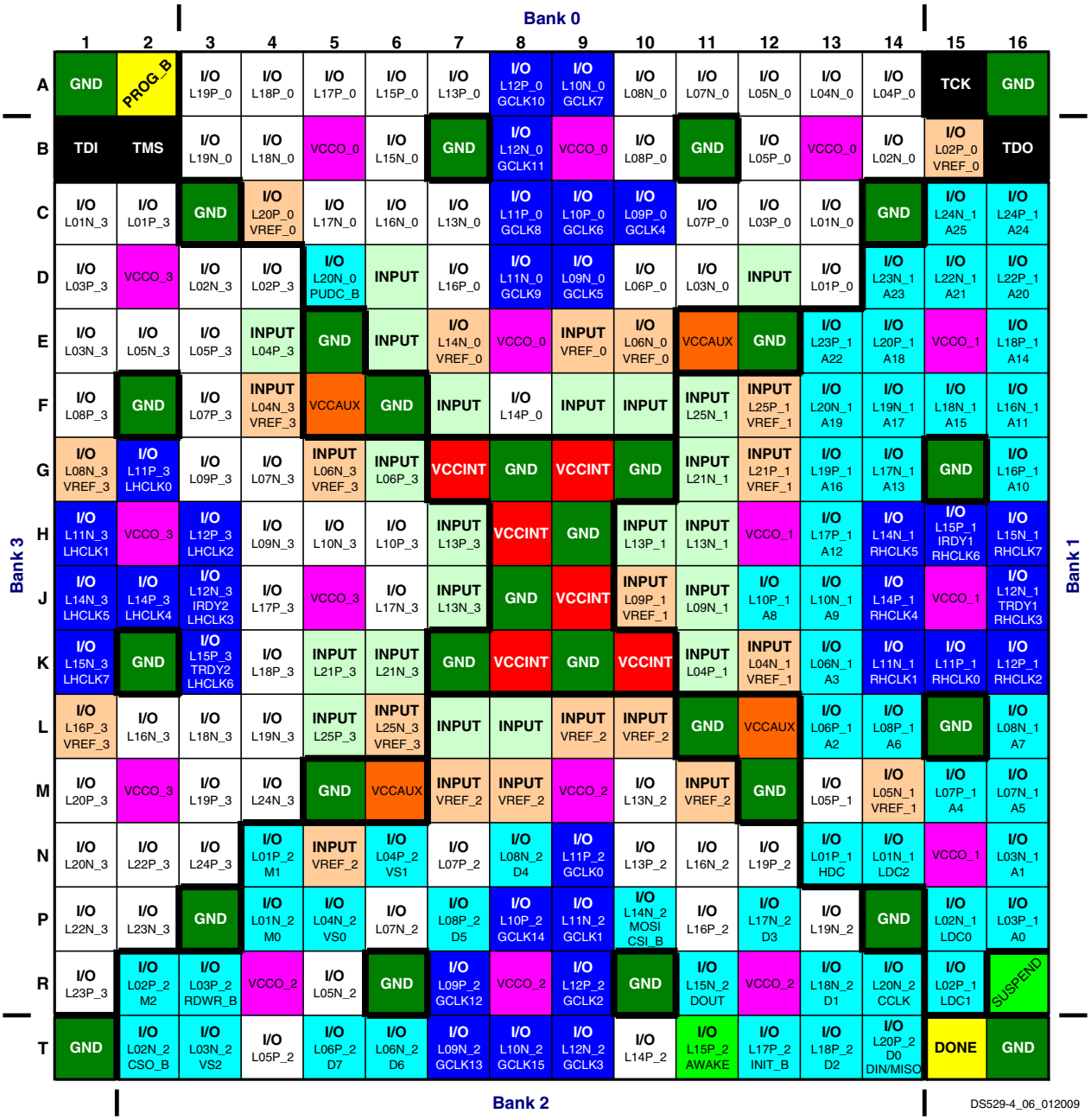


Figure 21: **XC3S200A and XC3S400A FT256 Package Footprint (Top View)**

69	**I/O:** Unrestricted, general-purpose user I/O	51	**DUAL:** Configuration pins, then possible user I/O	21	**VREF:** User I/O or input voltage reference for bank	2	**SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins
21	**INPUT:** Unrestricted, general-purpose input pin	32	**CLK:** User I/O, input, or global buffer input	16	**VCCO:** Output voltage supply for bank		
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	6	**VCCINT:** Internal core supply voltage (+1.2V)		
0	**N.C.:** Not connected	28	**GND:** Ground	4	**VCCAUX:** Auxiliary supply voltage		

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
0	IP_0	F12	INPUT
0	IP_0	G7	INPUT
0	IP_0	G8	INPUT
0	IP_0	G9	INPUT
0	IP_0	G11	INPUT
0	IP_0/VREF_0	E10	VREF
0	VCCO_0	B5	VCCO
0	VCCO_0	B14	VCCO
0	VCCO_0	D11	VCCO
0	VCCO_0	E8	VCCO
1	IO_L01N_1/LDC2	T17	DUAL
1	IO_L01P_1/HDC	R16	DUAL
1	IO_L02N_1/LDC0	U18	DUAL
1	IO_L02P_1/LDC1	U17	DUAL
1	IO_L03N_1/A1	R17	DUAL
1	IO_L03P_1/A0	T18	DUAL
1	IO_L05N_1	N16	I/O
1	IO_L05P_1	P16	I/O
1	IO_L06N_1	M14	I/O
1	IO_L06P_1	N15	I/O
1	IO_L07N_1/VREF_1	P18	VREF
1	IO_L07P_1	R18	I/O
1	IO_L09N_1/A3	M17	DUAL
1	IO_L09P_1/A2	M16	DUAL
1	IO_L10N_1/A5	N18	DUAL
1	IO_L10P_1/A4	N17	DUAL
1	IO_L11N_1/A7	L12	DUAL
1	IO_L11P_1/A6	L13	DUAL
1	IO_L13N_1/A9	K16	DUAL
1	IO_L13P_1/A8	L17	DUAL
1	IO_L14N_1/RHCLK1	K17	RHCLK
1	IO_L14P_1/RHCLK0	L18	RHCLK
1	IO_L15N_1/TRDY1/RHCLK3	J17	RHCLK
1	IO_L15P_1/RHCLK2	K18	RHCLK
1	IO_L17N_1/RHCLK5	K15	RHCLK
1	IO_L17P_1/RHCLK4	J16	RHCLK
1	IO_L18N_1/RHCLK7	H17	RHCLK
1	IO_L18P_1/IRDY1/RHCLK6	H18	RHCLK
1	IO_L19N_1/A11	G16	DUAL
1	IO_L19P_1/A10	H16	DUAL

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
1	IO_L21N_1	F17	I/O
1	IO_L21P_1	G17	I/O
1	IO_L22N_1/A13	E18	DUAL
1	IO_L22P_1/A12	F18	DUAL
1	IO_L23N_1/A15	H15	DUAL
1	IO_L23P_1/A14	J14	DUAL
1	IO_L25N_1	D17	I/O
1	IO_L25P_1	D18	I/O
1	IO_L26N_1/A17	E16	DUAL
1	IO_L26P_1/A16	F16	DUAL
1	IO_L27N_1/A19	F15	DUAL
1	IO_L27P_1/A18	G15	DUAL
1	IO_L29N_1/A21	E15	DUAL
1	IO_L29P_1/A20	D16	DUAL
1	IO_L30N_1/A23	B18	DUAL
1	IO_L30P_1/A22	C18	DUAL
1	IO_L31N_1/A25	B17	DUAL
1	IO_L31P_1/A24	C17	DUAL
1	IP_L04N_1/VREF_1	N14	VREF
1	IP_L04P_1	P15	INPUT
1	IP_L08N_1/VREF_1	L14	VREF
1	IP_L08P_1	M13	INPUT
1	IP_L12N_1	L16	INPUT
1	IP_L12P_1/VREF_1	M15	VREF
1	IP_L16N_1	K14	INPUT
1	IP_L16P_1	K13	INPUT
1	IP_L20N_1	J13	INPUT
1	IP_L20P_1/VREF_1	K12	VREF
1	IP_L24N_1	G14	INPUT
1	IP_L24P_1	H13	INPUT
1	IP_L28N_1	G13	INPUT
1	IP_L28P_1/VREF_1	H12	VREF
1	IP_L32N_1	F13	INPUT
1	IP_L32P_1/VREF_1	F14	VREF
1	VCCO_1	E17	VCCO
1	VCCO_1	H14	VCCO
1	VCCO_1	L15	VCCO
1	VCCO_1	P17	VCCO
2	IO_L01N_2/M0	U3	DUAL
2	IO_L01P_2/M1	T3	DUAL

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
2	IO_L02N_2/CSO_B	V3	DUAL
2	IO_L02P_2/M2	V2	DUAL
2	IO_L03N_2/VS2	U4	DUAL
2	IO_L03P_2/RDWR_B	T4	DUAL
2	IO_L04N_2	T5	I/O
2	IO_L04P_2	R5	I/O
2	IO_L05N_2/VS0	V5	DUAL
2	IO_L05P_2/VS1	V4	DUAL
2	IO_L06N_2	U6	I/O
2	IO_L06P_2	T6	I/O
2	IO_L07N_2	P8	I/O
2	IO_L07P_2	N8	I/O
2	IO_L08N_2/D6	T7	DUAL
2	IO_L08P_2/D7	R7	DUAL
2	IO_L09N_2	R9	I/O
2	IO_L09P_2	T8	I/O
2	IO_L10N_2/D4	V6	DUAL
2	IO_L10P_2/D5	U7	DUAL
2	IO_L11N_2/GCLK13	V8	GCLK
2	IO_L11P_2/GCLK12	U8	GCLK
2	IO_L12N_2/GCLK15	V9	GCLK
2	IO_L12P_2/GCLK14	U9	GCLK
2	IO_L13N_2/GCLK1	T10	GCLK
2	IO_L13P_2/GCLK0	U10	GCLK
2	IO_L14N_2/GCLK3	U11	GCLK
2	IO_L14P_2/GCLK2	V11	GCLK
2	IO_L15N_2	R10	I/O
2	IO_L15P_2	P10	I/O
2	IO_L16N_2/MOSI/CSI_B	T11	DUAL
2	IO_L16P_2	R11	I/O
2	IO_L17N_2	V13	I/O
2	IO_L17P_2	U12	I/O
2	IO_L18N_2/DOUT	U13	DUAL
2	IO_L18P_2/AWAKE	T12	PWR MGMT
2	IO_L19N_2	P12	I/O
2	IO_L19P_2	N12	I/O
2	IO_L20N_2/D3	R13	DUAL
2	IO_L20P_2/INIT_B	T13	DUAL
2	IO_L21N_2	T14	I/O

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
2	IO_L21P_2	V14	I/O
2	IO_L22N_2/D1	U15	DUAL
2	IO_L22P_2/D2	V15	DUAL
2	IO_L23N_2	T15	I/O
2	IO_L23P_2	R14	I/O
2	IO_L24N_2/CCLK	U16	DUAL
2	IO_L24P_2/D0/DIN/MISO	V16	DUAL
2	IP_2	M8	INPUT
2	IP_2	M9	INPUT
2	IP_2	M12	INPUT
2	***XC3S400A:*** IP_2 ***XC3S200A:*** N.C. (◆)	N7	INPUT
2	IP_2	N9	INPUT
2	IP_2	N11	INPUT
2	IP_2	R6	INPUT
2	IP_2/VREF_2	M11	VREF
2	IP_2/VREF_2	N10	VREF
2	IP_2/VREF_2	P6	VREF
2	IP_2/VREF_2	P7	VREF
2	IP_2/VREF_2	P9	VREF
2	IP_2/VREF_2	P13	VREF
2	***XC3S400A:*** IP_2/VREF_2 ***XC3S200A:*** N.C. (◆)	P14	VREF
2	VCCO_2	P11	VCCO
2	VCCO_2	R8	VCCO
2	VCCO_2	U5	VCCO
2	VCCO_2	U14	VCCO
3	IO_L01N_3	C1	I/O
3	IO_L01P_3	C2	I/O
3	IO_L02N_3	B1	I/O
3	IO_L02P_3	B2	I/O
3	IO_L03N_3	D2	I/O
3	IO_L03P_3	D3	I/O
3	IO_L05N_3	G5	I/O
3	IO_L05P_3	F5	I/O
3	IO_L06N_3	E3	I/O
3	IO_L06P_3	F4	I/O
3	IO_L07N_3	E1	I/O
3	IO_L07P_3	D1	I/O
3	IO_L09N_3	G4	I/O
3	IO_L09P_3	F3	I/O

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
3	IO_L10N_3/VREF_3	F1	VREF
3	IO_L10P_3	F2	I/O
3	IO_L11N_3	J6	I/O
3	IO_L11P_3	J7	I/O
3	IO_L13N_3	H1	I/O
3	IO_L13P_3	H2	I/O
3	IO_L14N_3/LHCLK1	J3	LHCLK
3	IO_L14P_3/LHCLK0	H3	LHCLK
3	IO_L15N_3/IRDY2/LHCLK3	J1	LHCLK
3	IO_L15P_3/LHCLK2	J2	LHCLK
3	IO_L17N_3/LHCLK5	K5	LHCLK
3	IO_L17P_3/LHCLK4	J4	LHCLK
3	IO_L18N_3/LHCLK7	K3	LHCLK
3	IO_L18P_3/TRDY2/LHCLK6	K2	LHCLK
3	IO_L19N_3	L2	I/O
3	IO_L19P_3/VREF_3	L1	VREF
3	IO_L21N_3	M2	I/O
3	IO_L21P_3	N1	I/O
3	IO_L22N_3	N2	I/O
3	IO_L22P_3	P1	I/O
3	IO_L23N_3	L4	I/O
3	IO_L23P_3	L3	I/O
3	IO_L25N_3	R2	I/O
3	IO_L25P_3	R1	I/O
3	IO_L26N_3	N4	I/O
3	IO_L26P_3	N3	I/O
3	IO_L27N_3	T2	I/O
3	IO_L27P_3	T1	I/O
3	IO_L29N_3	N6	I/O
3	IO_L29P_3	N5	I/O
3	IO_L30N_3	R3	I/O
3	IO_L30P_3	P3	I/O
3	IO_L31N_3	U2	I/O
3	IO_L31P_3	U1	I/O
3	IP_L04N_3/VREF_3	H7	VREF
3	IP_L04P_3	G6	INPUT
3	IP_L08N_3/VREF_3	H5	VREF
3	IP_L08P_3	H6	INPUT
3	IP_L12N_3	G2	INPUT
3	IP_L12P_3	G3	INPUT

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
3	IP_L16N_3	K6	INPUT
3	IP_L16P_3	J5	INPUT
3	IP_L20N_3	L6	INPUT
3	IP_L20P_3	L7	INPUT
3	IP_L24N_3	M4	INPUT
3	IP_L24P_3	M3	INPUT
3	IP_L28N_3	M5	INPUT
3	IP_L28P_3	M6	INPUT
3	IP_L32N_3/VREF_3	P4	VREF
3	IP_L32P_3	P5	INPUT
3	VCCO_3	E2	VCCO
3	VCCO_3	H4	VCCO
3	VCCO_3	L5	VCCO
3	VCCO_3	P2	VCCO
GND	GND	A1	GND
GND	GND	A7	GND
GND	GND	A12	GND
GND	GND	A18	GND
GND	GND	C10	GND
GND	GND	D4	GND
GND	GND	D7	GND
GND	GND	D15	GND
GND	GND	F6	GND
GND	GND	G1	GND
GND	GND	G12	GND
GND	GND	G18	GND
GND	GND	H8	GND
GND	GND	H10	GND
GND	GND	J11	GND
GND	GND	J15	GND
GND	GND	K4	GND
GND	GND	K8	GND
GND	GND	L9	GND
GND	GND	L11	GND
GND	GND	M1	GND
GND	GND	M7	GND
GND	GND	M18	GND
GND	GND	N13	GND
GND	GND	R4	GND
GND	GND	R12	GND

Table 77: **Spartan-3A FG320 Pinout *(Continued)***

Bank	Pin Name	FG320 Ball	Type
GND	GND	R15	GND
GND	GND	T9	GND
GND	GND	V1	GND
GND	GND	V7	GND
GND	GND	V12	GND
GND	GND	V18	GND
VCCAUX	SUSPEND	T16	PWR MGMT
VCCAUX	DONE	V17	CONFIG
VCCAUX	PROG_B	C4	CONFIG
VCCAUX	TCK	A17	JTAG
VCCAUX	TDI	E4	JTAG
VCCAUX	TDO	E14	JTAG
VCCAUX	TMS	C3	JTAG
VCCAUX	VCCAUX	A9	VCCAUX
VCCAUX	VCCAUX	G10	VCCAUX
VCCAUX	VCCAUX	J12	VCCAUX
VCCAUX	VCCAUX	J18	VCCAUX
VCCAUX	VCCAUX	K1	VCCAUX
VCCAUX	VCCAUX	K7	VCCAUX
VCCAUX	VCCAUX	M10	VCCAUX
VCCAUX	VCCAUX	V10	VCCAUX
VCCINT	VCCINT	H9	VCCINT
VCCINT	VCCINT	H11	VCCINT
VCCINT	VCCINT	J8	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	L8	VCCINT
VCCINT	VCCINT	L10	VCCINT

FG400: 400-ball Fine-pitch Ball Grid Array

The 400-ball fine-pitch ball grid array, FG400, supports two different Spartan-3A FPGAs, the XC3S400A and the XC3S700A. Both devices share a common footprint for this package as shown in Table 81 and Figure 24.

Table 81 lists all the FG400 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 81: **Spartan-3A FG400 Pinout**

Bank	Pin Name	FG400 Ball	Type
0	IO_L01N_0	A18	I/O
0	IO_L01P_0	B18	I/O
0	IO_L02N_0	C17	I/O
0	IO_L02P_0/VREF_0	D17	VREF
0	IO_L03N_0	E15	I/O
0	IO_L03P_0	D16	I/O
0	IO_L04N_0	A17	I/O
0	IO_L04P_0/VREF_0	B17	VREF
0	IO_L05N_0	A16	I/O
0	IO_L05P_0	C16	I/O
0	IO_L06N_0	C15	I/O
0	IO_L06P_0	D15	I/O
0	IO_L07N_0	A14	I/O
0	IO_L07P_0	C14	I/O
0	IO_L08N_0	A15	I/O
0	IO_L08P_0	B15	I/O
0	IO_L09N_0	F13	I/O
0	IO_L09P_0	E13	I/O
0	IO_L10N_0/VREF_0	C13	VREF
0	IO_L10P_0	D14	I/O
0	IO_L11N_0	C12	I/O
0	IO_L11P_0	B13	I/O
0	IO_L12N_0	F12	I/O
0	IO_L12P_0	D12	I/O
0	IO_L13N_0	A12	I/O

Table 81: **Spartan-3A FG400 Pinout *(Continued)***

Bank	Pin Name	FG400 Ball	Type
0	IO_L13P_0	B12	I/O
0	IO_L14N_0	C11	I/O
0	IO_L14P_0	B11	I/O
0	IO_L15N_0/GCLK5	E11	GCLK
0	IO_L15P_0/GCLK4	D11	GCLK
0	IO_L16N_0/GCLK7	C10	GCLK
0	IO_L16P_0/GCLK6	A10	GCLK
0	IO_L17N_0/GCLK9	E10	GCLK
0	IO_L17P_0/GCLK8	D10	GCLK
0	IO_L18N_0/GCLK11	A8	GCLK
0	IO_L18P_0/GCLK10	A9	GCLK
0	IO_L19N_0	C9	I/O
0	IO_L19P_0	B9	I/O
0	IO_L20N_0	C8	I/O
0	IO_L20P_0	B8	I/O
0	IO_L21N_0	D8	I/O
0	IO_L21P_0	C7	I/O
0	IO_L22N_0/VREF_0	F9	VREF
0	IO_L22P_0	E9	I/O
0	IO_L23N_0	F8	I/O
0	IO_L23P_0	E8	I/O
0	IO_L24N_0	A7	I/O
0	IO_L24P_0	B7	I/O
0	IO_L25N_0	C6	I/O
0	IO_L25P_0	A6	I/O
0	IO_L26N_0	B5	I/O
0	IO_L26P_0	A5	I/O
0	IO_L27N_0	F7	I/O
0	IO_L27P_0	E7	I/O
0	IO_L28N_0	D6	I/O
0	IO_L28P_0	C5	I/O
0	IO_L29N_0	C4	I/O
0	IO_L29P_0	A4	I/O
0	IO_L30N_0	B3	I/O
0	IO_L30P_0	A3	I/O
0	IO_L31N_0	F6	I/O
0	IO_L31P_0	E6	I/O
0	IO_L32N_0/PUDC_B	B2	DUAL

FG484: 484-ball Fine-pitch Ball Grid Array

The 484-ball fine-pitch ball grid array, FG484, supports both the XC3S700A and the XC3S1400A FPGAs. There are three pinout differences, as described in Table 86.

Table 83 lists all the FG484 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The shaded rows indicate pinout differences between the XC3S700A and the XC3S1400A FPGAs. The XC3S700A has three unconnected balls, indicated as N.C. (No Connection) in Table 83 and with the black diamond character (◆) in Table 83 and Figure 25.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 83: **Spartan-3A FG484 Pinout**

Bank	Pin Name	FG484 Ball	Type
0	IO_L01N_0	D18	I/O
0	IO_L01P_0	E17	I/O
0	IO_L02N_0	C19	I/O
0	IO_L02P_0/VREF_0	D19	VREF
0	IO_L03N_0	A20	I/O
0	IO_L03P_0	B20	I/O
0	IO_L04N_0	F15	I/O
0	IO_L04P_0	E15	I/O
0	IO_L05N_0	A18	I/O
0	IO_L05P_0	C18	I/O
0	IO_L06N_0	A19	I/O
0	IO_L06P_0/VREF_0	B19	VREF
0	IO_L07N_0	C17	I/O
0	IO_L07P_0	D17	I/O
0	IO_L08N_0	C16	I/O
0	IO_L08P_0	D16	I/O
0	IO_L09N_0	E14	I/O
0	IO_L09P_0	C14	I/O
0	IO_L10N_0	A17	I/O
0	IO_L10P_0	B17	I/O
0	IO_L11N_0	C15	I/O
0	IO_L11P_0	D15	I/O
0	IO_L12N_0/VREF_0	A15	VREF
0	IO_L12P_0	A16	I/O
0	IO_L13N_0	A14	I/O
0	IO_L13P_0	B15	I/O
0	IO_L14N_0	E13	I/O
0	IO_L14P_0	F13	I/O
0	IO_L15N_0	C13	I/O
0	IO_L15P_0	D13	I/O
0	IO_L16N_0	A13	I/O
0	IO_L16P_0	B13	I/O
0	IO_L17N_0/GCLK5	E12	GCLK
0	IO_L17P_0/GCLK4	C12	GCLK
0	IO_L18N_0/GCLK7	A11	GCLK
0	IO_L18P_0/GCLK6	A12	GCLK
0	IO_L19N_0/GCLK9	C11	GCLK
0	IO_L19P_0/GCLK8	B11	GCLK
0	IO_L20N_0/GCLK11	E11	GCLK
0	IO_L20P_0/GCLK10	D11	GCLK
0	IO_L21N_0	C10	I/O
0	IO_L21P_0	A10	I/O
0	IO_L22N_0	A8	I/O
0	IO_L22P_0	A9	I/O
0	IO_L23N_0	E10	I/O
0	IO_L23P_0	D10	I/O
0	IO_L24N_0/VREF_0	C9	VREF
0	IO_L24P_0	B9	I/O
0	IO_L25N_0	C8	I/O
0	IO_L25P_0	B8	I/O
0	IO_L26N_0	A6	I/O
0	IO_L26P_0	A7	I/O
0	IO_L27N_0	C7	I/O
0	IO_L27P_0	D7	I/O
0	IO_L28N_0	A5	I/O
0	IO_L28P_0	B6	I/O
0	IO_L29N_0	D6	I/O
0	IO_L29P_0	C6	I/O
0	IO_L30N_0	D8	I/O

Table 83: **Spartan-3A FG484 Pinout *(Continued)***

Table 83: **Spartan-3A FG484 Pinout*(Continued)***

Bank	Pin Name	FG484 Ball	Type
2	VCCO_2	AA18	VCCO
2	VCCO_2	AA5	VCCO
2	VCCO_2	AA9	VCCO
2	VCCO_2	U14	VCCO
2	VCCO_2	U9	VCCO
3	IO_L01N_3	D2	I/O
3	IO_L01P_3	C1	I/O
3	IO_L02N_3	C2	I/O
3	IO_L02P_3	B1	I/O
3	IO_L03N_3	E4	I/O
3	IO_L03P_3	D3	I/O
3	IO_L05N_3	G5	I/O
3	IO_L05P_3	G6	I/O
3	IO_L06N_3	E1	I/O
3	IO_L06P_3	D1	I/O
3	IO_L07N_3	E3	I/O
3	IO_L07P_3	F4	I/O
3	IO_L08N_3	G4	I/O
3	IO_L08P_3	F3	I/O
3	IO_L09N_3	H6	I/O
3	IO_L09P_3	H5	I/O
3	IO_L10N_3	J5	I/O
3	IO_L10P_3	K6	I/O
3	IO_L12N_3	F1	I/O
3	IO_L12P_3	F2	I/O
3	IO_L13N_3	G1	I/O
3	IO_L13P_3	G3	I/O
3	IO_L14N_3	H3	I/O
3	IO_L14P_3	H4	I/O
3	IO_L16N_3	H1	I/O
3	IO_L16P_3	H2	I/O
3	IO_L17N_3/VREF_3	J1	VREF
3	IO_L17P_3	J3	I/O
3	IO_L18N_3	K4	I/O
3	IO_L18P_3	K5	I/O
3	IO_L20N_3	K2	I/O
3	IO_L20P_3	K3	I/O
3	IO_L21N_3/LHCLK1	L3	LHCLK
3	IO_L21P_3/LHCLK0	L5	LHCLK
3	IO_L22N_3/IRDY2/LHCLK3	L1	LHCLK

Table 83: **Spartan-3A FG484 Pinout*(Continued)***

Bank	Pin Name	FG484 Ball	Type
3	IO_L22P_3/LHCLK2	K1	LHCLK
3	IO_L24N_3/LHCLK5	M2	LHCLK
3	IO_L24P_3/LHCLK4	M1	LHCLK
3	IO_L25N_3/LHCLK7	M4	LHCLK
3	IO_L25P_3/TRDY2/LHCLK6	M3	LHCLK
3	IO_L26N_3	N3	I/O
3	IO_L26P_3/VREF_3	N1	VREF
3	IO_L28N_3	P2	I/O
3	IO_L28P_3	P1	I/O
3	IO_L29N_3	P5	I/O
3	IO_L29P_3	P3	I/O
3	IO_L30N_3	N4	I/O
3	IO_L30P_3	M5	I/O
3	IO_L32N_3	R2	I/O
3	IO_L32P_3	R1	I/O
3	IO_L33N_3	R4	I/O
3	IO_L33P_3	R3	I/O
3	IO_L34N_3	T4	I/O
3	IO_L34P_3	R5	I/O
3	IO_L36N_3	T3	I/O
3	IO_L36P_3/VREF_3	T1	VREF
3	IO_L37N_3	U2	I/O
3	IO_L37P_3	U1	I/O
3	IO_L38N_3	V3	I/O
3	IO_L38P_3	V1	I/O
3	IO_L40N_3	U5	I/O
3	IO_L40P_3	T5	I/O
3	IO_L41N_3	U4	I/O
3	IO_L41P_3	U3	I/O
3	IO_L42N_3	W2	I/O
3	IO_L42P_3	W1	I/O
3	IO_L43N_3	W3	I/O
3	IO_L43P_3	V4	I/O
3	IO_L44N_3	Y2	I/O
3	IO_L44P_3	Y1	I/O
3	IO_L45N_3	AA2	I/O
3	IO_L45P_3	AA1	I/O
3	IP_3/VREF_3	J8	VREF
3	IP_3/VREF_3	R6	VREF
3	IP_L04N_3/VREF_3	H7	VREF

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
0	IO_L34N_0	D10	I/O
0	IO_L34P_0	C10	I/O
0	IO_L35N_0	H12	I/O
0	IO_L35P_0	G12	I/O
0	IO_L36N_0	B9	I/O
0	IO_L36P_0	A9	I/O
0	IO_L37N_0	D9	I/O
0	IO_L37P_0	E10	I/O
0	IO_L38N_0	B8	I/O
0	IO_L38P_0	A8	I/O
0	IO_L39N_0	K12	I/O
0	IO_L39P_0	J12	I/O
0	IO_L40N_0	D8	I/O
0	IO_L40P_0	C8	I/O
0	IO_L41N_0	C6	I/O
0	IO_L41P_0	B6	I/O
0	IO_L42N_0	C7	I/O
0	IO_L42P_0	B7	I/O
0	IO_L43N_0	K11	I/O
0	IO_L43P_0	J11	I/O
0	IO_L44N_0	D6	I/O
0	IO_L44P_0	C5	I/O
0	IO_L45N_0	B4	I/O
0	IO_L45P_0	A4	I/O
0	IO_L46N_0	H10	I/O
0	IO_L46P_0	G10	I/O
0	IO_L47N_0	H9	I/O
0	IO_L47P_0	G9	I/O
0	IO_L48N_0	E7	I/O
0	IO_L48P_0	F7	I/O
0	IO_L51N_0	B3	I/O
0	IO_L51P_0	A3	I/O
0	IO_L52N_0/PUDC_B	G8	DUAL
0	IO_L52P_0/VREF_0	F8	VREF
0	IP_0	A5	INPUT
0	IP_0	A7	INPUT
0	IP_0	A13	INPUT
0	IP_0	A17	INPUT
0	IP_0	A23	INPUT
0	IP_0	C4	INPUT

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
0	IP_0	D12	INPUT
0	IP_0	D15	INPUT
0	IP_0	D19	INPUT
0	IP_0	E11	INPUT
0	IP_0	E18	INPUT
0	IP_0	E20	INPUT
0	IP_0	F10	INPUT
0	IP_0	G14	INPUT
0	IP_0	G16	INPUT
0	IP_0	H13	INPUT
0	IP_0	H18	INPUT
0	IP_0	J10	INPUT
0	IP_0	J13	INPUT
0	IP_0	J15	INPUT
0	IP_0/VREF_0	D7	VREF
0	IP_0/VREF_0	D14	VREF
0	IP_0/VREF_0	G11	VREF
0	IP_0/VREF_0	J17	VREF
0	N.C. (◆)	A24	N.C.
0	N.C. (◆)	B24	N.C.
0	N.C. (◆)	D5	N.C.
0	N.C. (◆)	E9	N.C.
0	N.C. (◆)	F18	N.C.
0	N.C. (◆)	E6	N.C.
0	N.C. (◆)	F9	N.C.
0	N.C. (◆)	G18	N.C.
0	VCCO_0	B5	VCCO
0	VCCO_0	B11	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	B22	VCCO
0	VCCO_0	E8	VCCO
0	VCCO_0	E13	VCCO
0	VCCO_0	E19	VCCO
0	VCCO_0	H11	VCCO
0	VCCO_0	H16	VCCO
1	IO_L01N_1/LDC2	Y21	DUAL
1	IO_L01P_1/HDC	Y20	DUAL
1	IO_L02N_1/LDC0	AD25	DUAL
1	IO_L02P_1/LDC1	AE26	DUAL
1	IO_L03N_1/A1	AC24	DUAL

FG676 Footprint

Left Half of FG676 Package (Top View)

313 **I/O:** Unrestricted, general-purpose user I/O

67 **INPUT:** Unrestricted, general-purpose input pin

51 **DUAL:** Configuration pins, then possible user I/O

2 **SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins

38 **VREF:** User I/O or input voltage reference for bank

32 **CLK:** User I/O, input, or clock buffer input

2 **CONFIG:** Dedicated configuration pins

4 **JTAG:** Dedicated JTAG port pins

77 **GND:** Ground

36 **VCCO:** Output voltage supply for bank

23 **VCCINT:** Internal core supply voltage (+1.2V)

14 **VCCAUX:** Auxiliary supply voltage

17 ◆ **N.C.:** Not connected

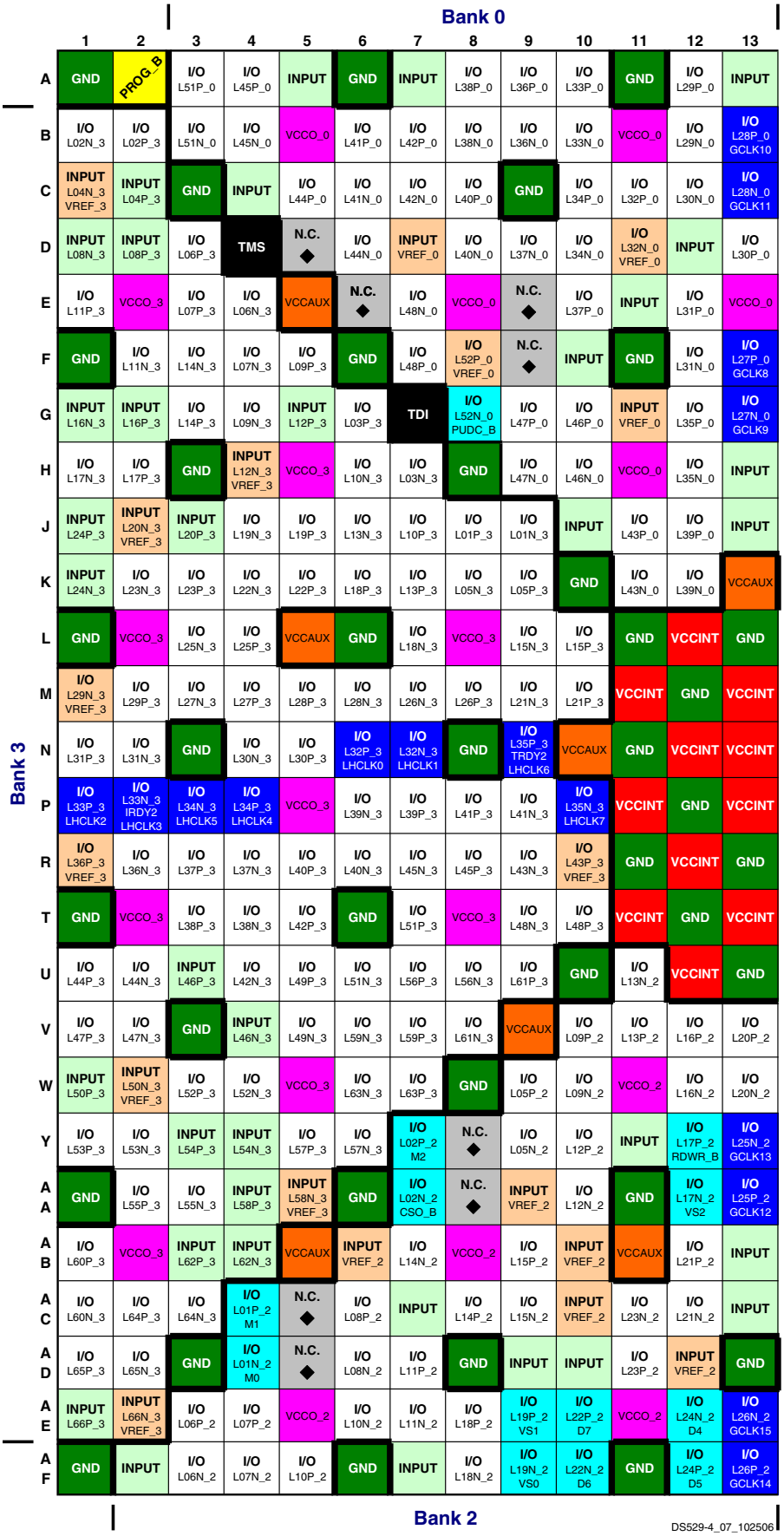


Figure 27: **FG676 Package Footprint (Top View)**