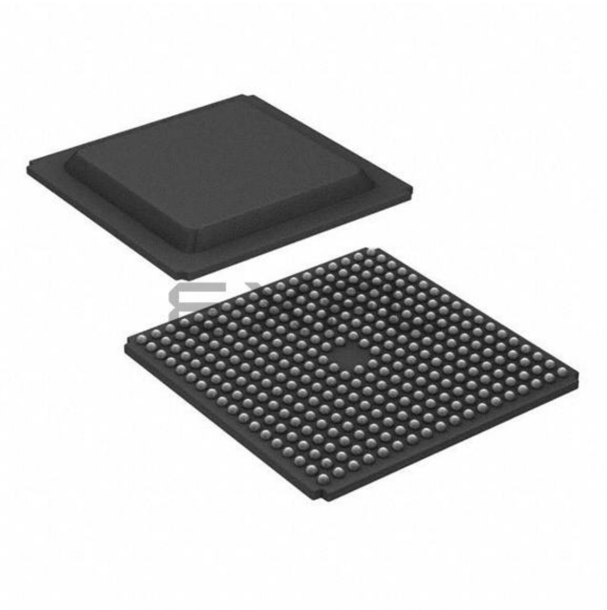

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	896
Number of Logic Elements/Cells	8064
Total RAM Bits	368640
Number of I/O	251
Number of Gates	400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	320-BGA
Supplier Device Package	320-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s400a-5fgg320c

Introduction

The Spartan®-3A family of Field-Programmable Gate Arrays (FPGAs) solves the design challenges in most high-volume, cost-sensitive, I/O-intensive electronic applications. The five-member family offers densities ranging from 50,000 to 1.4 million system gates, as shown in Table 1.

The Spartan-3A FPGAs are part of the Extended Spartan-3A family, which also include the non-volatile Spartan-3AN and the higher density Spartan-3A DSP FPGAs. The Spartan-3A family builds on the success of the earlier Spartan-3E and Spartan-3 FPGA families. New features improve system performance and reduce the cost of configuration. These Spartan-3A family enhancements, combined with proven 90 nm process technology, deliver more functionality and bandwidth per dollar than ever before, setting the new standard in the programmable logic industry.

Because of their exceptionally low cost, Spartan-3A FPGAs are ideally suited to a wide range of consumer electronics applications, including broadband access, home networking, display/projection, and digital television equipment.

The Spartan-3A family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, lengthy development cycles, and the inherent inflexibility of conventional ASICs, and permit field design upgrades.

Features

- Very low cost, high-performance logic solution for high-volume, cost-conscious applications
- Dual-range V_{CCAUX} supply simplifies 3.3V-only design
- Suspend, Hibernate modes reduce system power
- Multi-voltage, multi-standard SelectIO™ interface pins
  - Up to 502 I/O pins or 227 differential signal pairs
  - LVCMOS, LVTTL, HSTL, and SSTL single-ended I/O
  - 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V signaling
  - Selectable output drive, up to 24 mA per pin
  - QUIETIO standard reduces I/O switching noise
  - Full 3.3V ± 10% compatibility and hot swap compliance
  - 640+ Mb/s data transfer rate per differential I/O
  - LVDS, RSDS, mini-LVDS, HSTL/SSTL differential I/O with integrated differential termination resistors
  - Enhanced Double Data Rate (DDR) support
  - DDR/DDR2 SDRAM support up to 400 Mb/s
  - Fully compliant 32-/64-bit, 33/66 MHz PCI® technology support
- Abundant, flexible logic resources
  - Densities up to 25,344 logic cells, including optional shift register or distributed RAM support
  - Efficient wide multiplexers, wide logic
  - Fast look-ahead carry logic
  - Enhanced 18 x 18 multipliers with optional pipeline
  - IEEE 1149.1/1532 JTAG programming/debug port
- Hierarchical SelectRAM™ memory architecture
  - Up to 576 Kbits of fast block RAM with byte write enables for processor applications
  - Up to 176 Kbits of efficient distributed RAM
- Up to eight Digital Clock Managers (DCMs)
  - Clock skew elimination (delay locked loop)
  - Frequency synthesis, multiplication, division
  - High-resolution phase shifting
  - Wide frequency range (5 MHz to over 320 MHz)
- Eight low-skew global clock networks, eight additional clocks per half device, plus abundant low-skew routing
- Configuration interface to industry-standard PROMs
  - Low-cost, space-saving SPI serial Flash PROM
  - x8 or x8/x16 BPI parallel NOR Flash PROM
  - Low-cost Xilinx® Platform Flash with JTAG
  - Unique Device DNA identifier for design authentication
  - Load multiple bitstreams under FPGA control
  - Post-configuration CRC checking
- Complete Xilinx ISE® and WebPACK™ development system software support plus Spartan-3A Starter Kit
- MicroBlaze™ and PicoBlaze™ embedded processors
- Low-cost QFP and BGA packaging, Pb-free options
  - Common footprints support easy density migration
  - Compatible with select Spartan-3AN nonvolatile FPGAs
  - Compatible with higher density Spartan-3A DSP FPGAs
- XA Automotive version available

Table 1: **Summary of Spartan-3A FPGA Attributes**

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM bits(1)	Block RAM bits(1)	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	CLBs	Slices						
XC3S50A	50K	1,584	16	12	176	704	11K	54K	3	2	144	64
XC3S200A	200K	4,032	32	16	448	1,792	28K	288K	16	4	248	112
XC3S400A	400K	8,064	40	24	896	3,584	56K	360K	20	4	311	142
XC3S700A	700K	13,248	48	32	1,472	5,888	92K	360K	20	8	372	165
XC3S1400A	1400K	25,344	72	40	2,816	11,264	176K	576K	32	8	502	227

Notes:
1. By convention, one Kb is equivalent to 1,024 bits.

Spartan-3A FPGA Design Documentation

The functionality of the Spartan®-3A FPGA Family is described in the following documents. The topics covered in each guide is listed below.

- **DS706: Extended Spartan-3A Family Overview**
  www.xilinx.com/support/documentation/data_sheets/ds706.pdf
- **UG331: Spartan-3 Generation FPGA User Guide**
  www.xilinx.com/support/documentation/user_guides/ug331.pdf
  - Clocking Resources
  - Digital Clock Managers (DCMs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
    - Distributed RAM
    - SRL16 Shift Registers
    - Carry and Arithmetic Logic
  - I/O Resources
  - Embedded Multiplier Blocks
  - Programmable Interconnect
  - ISE® Software Design Tools
  - IP Cores
  - Embedded Processing and Control Solutions
  - Pin Types and Package Overview
  - Package Drawings
  - Powering FPGAs
  - Power Management
- **UG332: Spartan-3 Generation Configuration User Guide**
  www.xilinx.com/support/documentation/user_guides/ug332.pdf
  - Configuration Overview
    - Configuration Pins and Behavior
    - Bitstream Sizes
  - Detailed Descriptions by Mode
    - Master Serial Mode using Xilinx® Platform Flash PROM
    - Master SPI Mode using Commodity SPI Serial Flash PROM
    - Master BPI Mode using Commodity Parallel NOR Flash PROM
    - Slave Parallel (SelectMAP) using a Processor
    - Slave Serial using a Processor
    - JTAG Mode
  - ISE iMPACT Programming Examples
  - MultiBoot Reconfiguration
  - Design Authentication using Device DNA

For application examples, see the Spartan-3A FPGA application notes.

- **Spartan-3A FPGA Application Notes**
  www.xilinx.com/support/documentation/spartan-3a_application_notes.htm

For specific hardware examples, please see the Spartan-3A FPGA Starter Kit board web page, which has links to various design examples and the user guide.

- **Spartan-3A/3AN FPGA Starter Kit Board Page**
  www.xilinx.com/s3astarter
- **UG334: Spartan-3A/3AN FPGA Starter Kit User Guide**
  www.xilinx.com/support/documentation/boards_and_kits/ug334.pdf

For information on the XA Automotive version of the Spartan-3A family, see the following data sheet.

- XA Spartan-3A Automotive FPGA Family Data Sheet
  www.xilinx.com/support/documentation/data_sheets/ds681.pdf

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- Sign Up for Alerts

  www.xilinx.com/support/answers/18683.htm

DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

Advance: Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

Production: These specifications are approved once the silicon has been characterized over numerous production lots. Parameter values are considered stable with no future changes expected.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan®-3A devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Absolute Maximum Ratings

Stresses beyond those listed under Table 4: Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 4: **Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Max	Units
V_{CCINT}	Internal supply voltage		–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage		–0.5	3.75	V
V_{CCO}	Output driver supply voltage		–0.5	3.75	V
V_{REF}	Input reference voltage		–0.5	$V_{CCO} + 0.5$	V
V_{IN}	Voltage applied to all User I/O pins and dual-purpose pins	Driver in a high-impedance state	–0.95	4.6	V
	Voltage applied to all Dedicated pins		–0.5	4.6	V
I_{IK}	Input clamp current per I/O pin	$-0.5V < V_{IN} < (V_{CCO} + 0.5V)$ (1)	–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model	–	±2000	V
		Charged device model	–	±500	V
		Machine model	–	±200	V
T_J	Junction temperature		–	125	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:
1. Upper clamp applies only when using PCI IOSTANDARDs.
2. For soldering guidelines, see UG112: *Device Packaging and Thermal Characteristics* and XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

Single-Ended I/O Standards

Table 11: **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers(2)			V_{REF}			V_{IL}	V_{IH}
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
LVTTL	3.0	3.3	3.6	V_{REF} is not used for these I/O standards			0.8	2.0
LVCMOS33(4)	3.0	3.3	3.6				0.8	2.0
LVCMOS25(4,5)	2.3	2.5	2.7				0.7	1.7
LVCMOS18	1.65	1.8	1.95				0.4	0.8
LVCMOS15	1.4	1.5	1.6				0.4	0.8
LVCMOS12	1.1	1.2	1.3				0.4	0.7
PCI33_3(6)	3.0	3.3	3.6				$0.3 \bullet V_{CCO}$	$0.5 \bullet V_{CCO}$
PCI66_3(6)	3.0	3.3	3.6				$0.3 \bullet V_{CCO}$	$0.5 \bullet V_{CCO}$
HSTL_I	1.4	1.5	1.6	0.68	0.75	0.9	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_III	1.4	1.5	1.6	–	0.9	-	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_II_18	1.7	1.8	1.9	–	0.9	–	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_III_18	1.7	1.8	1.9	–	1.1	–	$V_{REF} - 0.1$	$V_{REF} + 0.1$
SSTL18_I	1.7	1.8	1.9	0.833	0.900	0.969	$V_{REF} - 0.125$	$V_{REF} + 0.125$
SSTL18_II	1.7	1.8	1.9	0.833	0.900	0.969	$V_{REF} - 0.125$	$V_{REF} + 0.125$
SSTL2_I	2.3	2.5	2.7	1.13	1.25	1.38	$V_{REF} - 0.150$	$V_{REF} + 0.150$
SSTL2_II	2.3	2.5	2.7	1.13	1.25	1.38	$V_{REF} - 0.150$	$V_{REF} + 0.150$
SSTL3_I	3.0	3.3	3.6	1.3	1.5	1.7	$V_{REF} - 0.2$	$V_{REF} + 0.2$
SSTL3_II	3.0	3.3	3.6	1.3	1.5	1.7	$V_{REF} - 0.2$	$V_{REF} + 0.2$

Notes:

1. Descriptions of the symbols used in this table are as follows:
   V_{CCO} – the supply voltage for output drivers
   V_{REF} – the reference voltage for setting the input switching threshold
   V_{IL} – the input voltage that indicates a Low logic level
   V_{IH} – the input voltage that indicates a High logic level
2. In general, the V_{CCO} rails supply only output drivers, not input circuits. The exceptions are for LVCMOS25 inputs when V_{CCAUX} = 3.3V range and for PCI I/O standards.
3. For device operation, the maximum signal voltage (V_{IH} max) can be as high as V_{IN} max. See Table 8.
4. There is approximately 100 mV of hysteresis on inputs using LVCMOS33 and LVCMOS25 I/O standards.
5. All Dedicated pins (PROG_B, DONE, SUSPEND, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail and use the LVCMOS25 or LVCMOS33 standard depending on V_{CCAUX}. The dual-purpose configuration pins use the LVCMOS standard before the User mode. When using these pins as part of a standard 2.5V configuration interface, apply 2.5V to the V_{CCO} lines of Banks 0, 1, and 2 at power-on as well as throughout configuration.
6. For information on PCI IP solutions, see www.xilinx.com/pci. The PCI IOSTANDARD is not supported on input-only pins. The PCIX IOSTANDARD is available and has equivalent characteristics but no PCI-X IP is supported.

Table 12: **DC Characteristics of User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute		Test Conditions I_{OL} (mA)	Test Conditions I_{OH} (mA)	Logic Level Characteristics V_{OL} Max (V)	Logic Level Characteristics V_{OH} Min (V)
LVTTL(3)	2	2	–2	0.4	2.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
LVCMOS33(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24(4)	24	–24		
LVCMOS25(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16(4)	16	–16		
	24(4)	24	–24		
LVCMOS18(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12(4)	12	–12		
	16(4)	16	–16		
LVCMOS15(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8(4)	8	–8		
	12(4)	12	–12		
LVCMOS12(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4(4)	4	–4		
	6(4)	6	–6		

Table 12: **DC Characteristics of User I/Os Using Single-Ended Standards *(Continued)***

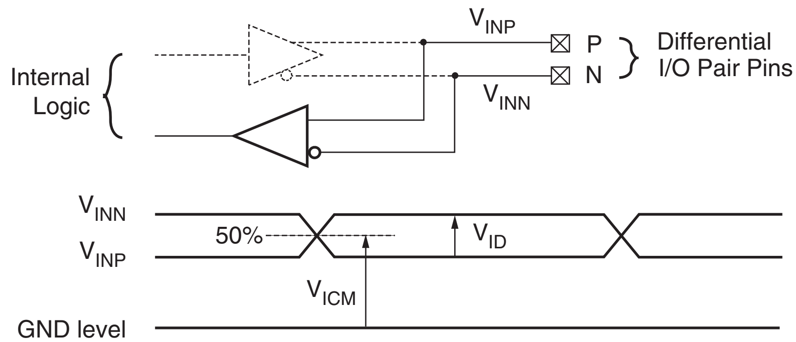
IOSTANDARD Attribute	Test Conditions I_{OL} (mA)	Test Conditions I_{OH} (mA)	Logic Level Characteristics V_{OL} Max (V)	Logic Level Characteristics V_{OH} Min (V)
PCI33_3(5)	1.5	–0.5	10% V_{CCO}	90% V_{CCO}
PCI66_3(5)	1.5	–0.5	10% V_{CCO}	90% V_{CCO}
HSTL_I(4)	8	–8	0.4	V_{CCO} - 0.4
HSTL_III(4)	24	–8	0.4	V_{CCO} - 0.4
HSTL_I_18	8	–8	0.4	V_{CCO} - 0.4
HSTL_II_18(4)	16	–16	0.4	V_{CCO} - 0.4
HSTL_III_18	24	–8	0.4	V_{CCO} - 0.4
SSTL18_I	6.7	–6.7	V_{TT} – 0.475	V_{TT} + 0.475
SSTL18_II(4)	13.4	–13.4	V_{TT} – 0.603	V_{TT} + 0.603
SSTL2_I	8.1	–8.1	V_{TT} – 0.61	V_{TT} + 0.61
SSTL2_II(4)	16.2	–16.2	V_{TT} – 0.81	V_{TT} + 0.81
SSTL3_I	8	–8	V_{TT} – 0.6	V_{TT} + 0.6
SSTL3_II	16	–16	V_{TT} – 0.8	V_{TT} + 0.8

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8 and Table 11.
2. Descriptions of the symbols used in this table are as follows:
   I_{OL} — the output current condition under which V_{OL} is tested
   I_{OH} — the output current condition under which V_{OH} is tested
   V_{OL} — the output voltage that indicates a Low logic level
   V_{OH} — the output voltage that indicates a High logic level
   V_{CCO} — the supply voltage for output drivers
   V_{TT} — the voltage applied to a resistor termination
3. For the LVCMOS and LVTTL standards: the same V_{OL} and V_{OH} limits apply for the Fast, Slow, and QUIETIO slew attributes.
4. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
5. Tested according to the relevant PCI specifications. For information on PCI IP solutions, see www.xilinx.com/pci. The PCIX IOSTANDARD is available and has equivalent characteristics but no PCI-X IP is supported.

Differential I/O Standards

Differential Input Pairs



$$V_{ICM} = \text{Input common mode voltage} = \frac{V_{INP} + V_{INN}}{2}$$

$$V_{ID} = \text{Differential input voltage} = \left| V_{INP} - V_{INN} \right|$$

DS529-3_10_012907

Figure 4: **Differential Input Voltages**

Table 13: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers(1)			V_{ID}			V_{ICM}(2)		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LVDS_25(3)	2.25	2.5	2.75	100	350	600	0.3	1.25	2.35
LVDS_33(3)	3.0	3.3	3.6	100	350	600	0.3	1.25	2.35
BLVDS_25(4)	2.25	2.5	2.75	100	300	–	0.3	1.3	2.35
MINI_LVDS_25(3)	2.25	2.5	2.75	200	–	600	0.3	1.2	1.95
MINI_LVDS_33(3)	3.0	3.3	3.6	200	–	600	0.3	1.2	1.95
LVPECL_25(5)	Inputs Only			100	800	1000	0.3	1.2	1.95
LVPECL_33(5)	Inputs Only			100	800	1000	0.3	1.2	2.8(6)
RSDS_25(3)	2.25	2.5	2.75	100	200	–	0.3	1.2	1.5
RSDS_33(3)	3.0	3.3	3.6	100	200	–	0.3	1.2	1.5
TMDS_33(3, 4, 7)	3.14	3.3	3.47	150	–	1200	2.7	–	3.23
PPDS_25(3)	2.25	2.5	2.75	100	–	400	0.2	–	2.3
PPDS_33(3)	3.0	3.3	3.6	100	–	400	0.2	–	2.3
DIFF_HSTL_I_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_II_18(8)	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_III_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_I	1.4	1.5	1.6	100	–	–	0.68		0.9
DIFF_HSTL_III	1.4	1.5	1.6	100	–	–	–	0.9	–
DIFF_SSTL18_I	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL18_II(8)	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL2_I	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL2_II(8)	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL3_I	3.0	3.3	3.6	100	–	–	1.1	–	1.9
DIFF_SSTL3_II	3.0	3.3	3.6	100	–	–	1.1	–	1.9

Notes:

1. The V_{CCO} rails supply only differential output drivers, not input circuits.
2. V_{ICM} must be less than V_{CCAUX}.
3. These true differential output standards are supported only on FPGA banks 0 and 2. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
4. See "External Termination Requirements for Differential I/O," page 20.
5. LVPECL is supported on inputs only, not outputs. LVPECL_33 requires V_{CCAUX}=3.3V ± 10%.
6. LVPECL_33 maximum V_{ICM} = the lower of 2.8V or $V_{CCAUX} – (V_{ID} / 2)$
7. Requires V_{CCAUX} = 3.3V ± 10% for inputs. (V_{CCAUX} – 300 mV) ≤ V_{ICM} ≤ (V_{CCAUX} – 37 mV)
8. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
9. All standards except for LVPECL and TMDS can have V_{CCAUX} at either 2.5V or 3.3V. Define your V_{CCAUX} level using the CONFIG VCCAUX constraint.

Switching Characteristics

All Spartan-3A FPGAs ship in two speed grades: –4 and the higher performance –5. Switching characteristics in this document are designated as Advance, Preliminary, or Production, as shown in Table 16. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGA designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Advance or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx® ISE® software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan-3A devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

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  www.xilinx.com/support/answers/18683.htm

Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3A FPGA speed files (v1.41), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in Table 16. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 16: **Spartan-3A v1.41 Speed Grade Designation**

Device	Advance	Preliminary	Production
XC3S50A			-4, -5
XC3S200A			-4, -5
XC3S400A			-4, -5
XC3S700A			-4, -5
XC3S1400A			-4, -5

Table 17 provides the recent history of the Spartan-3A FPGA speed files.

Table 17: **Spartan-3A Speed File Version History**

Version	ISE Release	Description
1.41	ISE 10.1.03	Updated Automotive output delays
1.40	ISE 10.1.02	Updated Automotive input delays.
1.39	ISE 10.1.01	Added Automotive parts.
1.38	ISE 9.2.03i	Added Absolute Minimum values.
1.37	ISE 9.2.01i	Updated pin-to-pin setup and hold times (Table 19), TMDS output adjustment (Table 26) multiplier setup/hold times (Table 34), and block RAM clock width (Table 35).
1.36	ISE 9.2i; previously available via Answer Record AR24992	XC3S400A, all speed grades and all temperature grades, upgraded to Production
1.35	Answer Record AR24992	XC3S50A, XC3S200A, XC3S700A, XC3S1400A, all speed grades and all temperature grades, upgraded to Production.
1.34	ISE 9.1.03i	XC3S700A and XC3S1400A -4 speed grade upgraded to Production. Updated pin-to-pin timing numbers.

Input Propagation Times

Table 22: **Propagation Times for the IOB Input Path**

Symbol	Description	Conditions	DELAY_VALUE	Device	Speed Grade -5 Max	Speed Grade -4 Max	Units
Propagation Times							
T_{IOPI}	The time it takes for data to travel from the Input pin to the I output with no input delay programmed	LVCMOS25(2)	IBUF_DELAY_VALUE=0	XC3S50A	1.04	1.12	ns
				XC3S200A	0.87	0.87	ns
				XC3S400A	0.65	0.72	ns
				XC3S700A	0.92	0.92	ns
				XC3S1400A	0.96	1.21	ns
T_{IOPID}	The time it takes for data to travel from the Input pin to the I output with the input delay programmed	LVCMOS25(2)	1	XC3S50A	1.79	2.07	ns
			2		2.13	2.46	ns
			3		2.36	2.71	ns
			4		2.88	3.21	ns
			5		3.11	3.46	ns
			6		3.45	3.84	ns
			7		3.75	4.19	ns
			8		4.00	4.47	ns
			9		3.61	4.11	ns
			10		3.95	4.50	ns
			11		4.18	4.67	ns
			12		4.75	5.20	ns
			13		4.98	5.44	ns
			14		5.31	5.95	ns
			15		5.62	6.28	ns
			16		5.86	6.57	ns
			1	XC3S200A	1.57	1.65	ns
			2		1.87	1.97	ns
			3		2.16	2.33	ns
			4		2.68	2.96	ns
			5		2.87	3.19	ns
			6		3.20	3.60	ns
			7		3.57	4.02	ns
			8		3.79	4.26	ns
			9		3.42	3.86	ns
			10		3.79	4.25	ns
			11		4.02	4.55	ns
			12		4.62	5.24	ns
			13		4.86	5.53	ns
			14		5.18	5.94	ns

Input Timing Adjustments

Table 23: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below Speed Grade -5	Add the Adjustment Below Speed Grade -4	Units
Single-Ended Standards			
LVTTL	0.62	0.62	ns
LVCMOS33	0.54	0.54	ns
LVCMOS25	0	0	ns
LVCMOS18	0.83	0.83	ns
LVCMOS15	0.60	0.60	ns
LVCMOS12	0.31	0.31	ns
PCI33_3	0.41	0.41	ns
PCI66_3	0.41	0.41	ns
HSTL_I	0.72	0.72	ns
HSTL_III	0.77	0.77	ns
HSTL_I_18	0.69	0.69	ns
HSTL_II_18	0.69	0.69	ns
HSTL_III_18	0.79	0.79	ns
SSTL18_I	0.71	0.71	ns
SSTL18_II	0.71	0.71	ns
SSTL2_I	0.68	0.68	ns
SSTL2_II	0.68	0.68	ns
SSTL3_I	0.78	0.78	ns
SSTL3_II	0.78	0.78	ns

Table 23: **Input Timing Adjustments by IOSTANDARD*(Continued)***

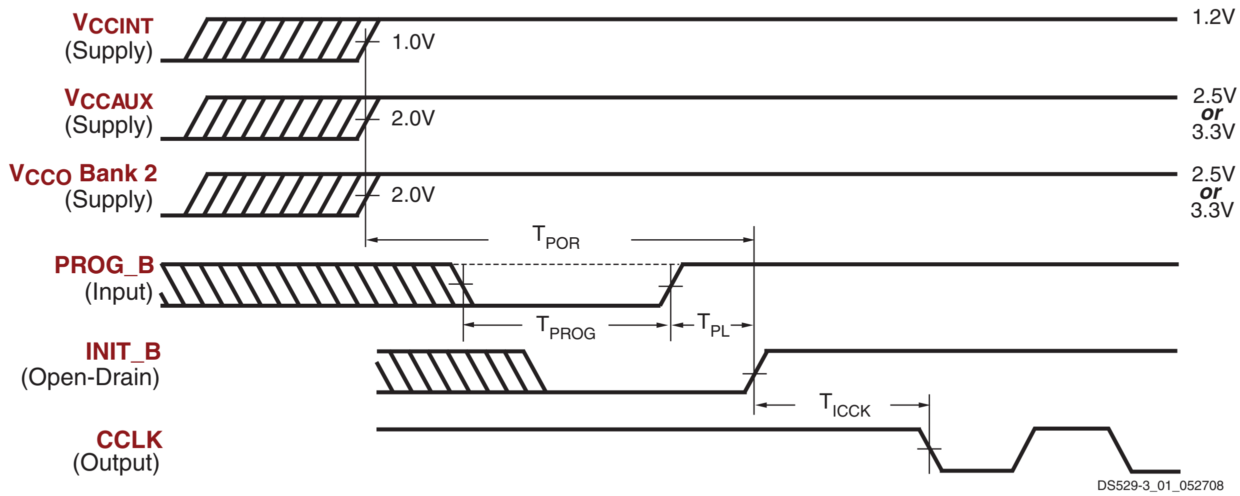
Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below Speed Grade -5	Add the Adjustment Below Speed Grade -4	Units
Differential Standards			
LVDS_25	0.76	0.76	ns
LVDS_33	0.79	0.79	ns
BLVDS_25	0.79	0.79	ns
MINI_LVDS_25	0.78	0.78	ns
MINI_LVDS_33	0.79	0.79	ns
LVPECL_25	0.78	0.78	ns
LVPECL_33	0.79	0.79	ns
RSDS_25	0.79	0.79	ns
RSDS_33	0.77	0.77	ns
TMDS_33	0.79	0.79	ns
PPDS_25	0.79	0.79	ns
PPDS_33	0.79	0.79	ns
DIFF_HSTL_I_18	0.74	0.74	ns
DIFF_HSTL_II_18	0.72	0.72	ns
DIFF_HSTL_III_18	1.05	1.05	ns
DIFF_HSTL_I	0.72	0.72	ns
DIFF_HSTL_III	1.05	1.05	ns
DIFF_SSTL18_I	0.71	0.71	ns
DIFF_SSTL18_II	0.71	0.71	ns
DIFF_SSTL2_I	0.74	0.74	ns
DIFF_SSTL2_II	0.75	0.75	ns
DIFF_SSTL3_I	1.06	1.06	ns
DIFF_SSTL3_II	1.06	1.06	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8, Table 11, and Table 13.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Configuration and JTAG Timing

General Configuration Power-On/Reconfigure Timing



Notes:

1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies can be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 11: **Waveforms for Power-On and the Beginning of Configuration**

Table 45: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	All	–	18	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	-	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XC3S50A	–	0.5	ms
		XC3S200A	–	0.5	ms
		XC3S400A	–	1	ms
		XC3S700A	–	2	ms
		XC3S1400A	–	2	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	250	–	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, and BPI modes.
4. For details on configuration, see UG332 *Spartan-3 Generation Configuration User Guide*.

Master Serial and Slave Serial Mode Timing

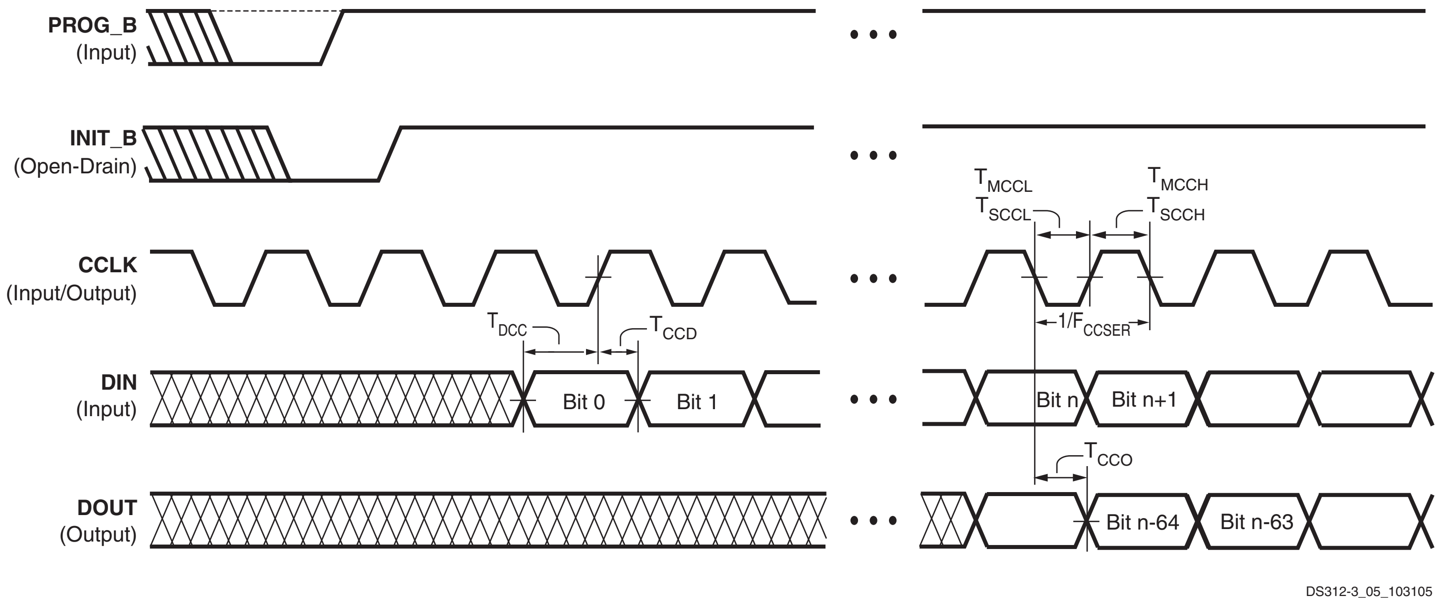


Figure 12: **Waveforms for Master Serial and Slave Serial Configuration**

Table 50: **Timing for the Master Serial and Slave Serial Configuration Modes**

Symbol	Description		Slave/ Master	All Speed Grades Min	All Speed Grades Max	Units
Clock-to-Output Times						
T_{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin		Both	1.5	10	ns
Setup Times						
T_{DCC}	The time from the setup of data at the DIN pin to the rising transition at the CCLK pin		Both	7	–	ns
Hold Times						
T_{CCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin		Master	0	–	ns
			Slave	1.0		
Clock Timing						
T_{CCH}	High pulse width at the CCLK input pin		Master	See Table 48		
			Slave	See Table 49		
T_{CCL}	Low pulse width at the CCLK input pin		Master	See Table 48		
			Slave	See Table 49		
F_{CCSER}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	Slave	0	100	MHz
		With bitstream compression		0	100	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Table 66: **Spartan-3A TQ144 Pinout*(Continued)***

Bank	Pin Name	Pin	Type
2	IO_L05P_2	P46	I/O
2	IO_L06N_2/D6	P49	DUAL
2	IO_L06P_2	P47	I/O
2	IO_L07N_2/D4	P51	DUAL
2	IO_L07P_2/D5	P50	DUAL
2	IO_L08N_2/GCLK15	P55	GCLK
2	IO_L08P_2/GCLK14	P54	GCLK
2	IO_L09N_2/GCLK1	P59	GCLK
2	IO_L09P_2/GCLK0	P57	GCLK
2	IO_L10N_2/GCLK3	P60	GCLK
2	IO_L10P_2/GCLK2	P58	GCLK
2	IO_L11N_2/DOUT	P64	DUAL
2	IO_L11P_2/AWAKE	P63	PWR MGMT
2	IO_L12N_2/D3	P68	DUAL
2	IO_L12P_2/INIT_B	P67	DUAL
2	IO_L13N_2/D0/DIN/MISO	P71	DUAL
2	IO_L13P_2/D2	P69	DUAL
2	IO_L14N_2/CCLK	P72	DUAL
2	IO_L14P_2/D1	P70	DUAL
2	IP_2/VREF_2	P53	VREF
2	VCCO_2	P40	VCCO
2	VCCO_2	P61	VCCO
3	IO_L01N_3	P6	I/O
3	IO_L01P_3	P4	I/O
3	IO_L02N_3	P5	I/O
3	IO_L02P_3	P3	I/O
3	IO_L03N_3	P8	I/O
3	IO_L03P_3	P7	I/O
3	IO_L04N_3/VREF_3	P11	VREF
3	IO_L04P_3	P10	I/O
3	IO_L05N_3/LHCLK1	P13	LHCLK
3	IO_L05P_3/LHCLK0	P12	LHCLK
3	IO_L06N_3/IRDY2/LHCLK3	P16	LHCLK
3	IO_L06P_3/LHCLK2	P15	LHCLK
3	IO_L07N_3/LHCLK5	P20	LHCLK
3	IO_L07P_3/LHCLK4	P18	LHCLK
3	IO_L08N_3/LHCLK7	P21	LHCLK
3	IO_L08P_3/TRDY2/LHCLK6	P19	LHCLK
3	IO_L09N_3	P25	I/O
3	IO_L09P_3	P24	I/O
3	IO_L10N_3	P29	I/O

Table 66: **Spartan-3A TQ144 Pinout*(Continued)***

Bank	Pin Name	Pin	Type
3	IO_L10P_3	P27	I/O
3	IO_L11N_3	P30	I/O
3	IO_L11P_3	P28	I/O
3	IO_L12N_3	P32	I/O
3	IO_L12P_3	P31	I/O
3	IP_L13N_3/VREF_3	P35	VREF
3	IP_L13P_3	P33	INPUT
3	VCCO_3	P14	VCCO
3	VCCO_3	P23	VCCO
GND	GND	P9	GND
GND	GND	P17	GND
GND	GND	P26	GND
GND	GND	P34	GND
GND	GND	P56	GND
GND	GND	P65	GND
GND	GND	P81	GND
GND	GND	P89	GND
GND	GND	P100	GND
GND	GND	P106	GND
GND	GND	P118	GND
GND	GND	P128	GND
GND	GND	P137	GND
VCCAUX	SUSPEND	P74	PWR MGMT
VCCAUX	DONE	P73	CONFIG
VCCAUX	PROG_B	P144	CONFIG
VCCAUX	TCK	P109	JTAG
VCCAUX	TDI	P2	JTAG
VCCAUX	TDO	P107	JTAG
VCCAUX	TMS	P1	JTAG
VCCAUX	VCCAUX	P36	VCCAUX
VCCAUX	VCCAUX	P66	VCCAUX
VCCAUX	VCCAUX	P108	VCCAUX
VCCAUX	VCCAUX	P133	VCCAUX
VCCINT	VCCINT	P22	VCCINT
VCCINT	VCCINT	P52	VCCINT
VCCINT	VCCINT	P94	VCCINT
VCCINT	VCCINT	P122	VCCINT

Table 69: **Spartan-3A FT256 Pinout (XC3S700A,**

Bank	XC3S700A XC3S1400A	FT256 Ball	Type
3	IO_L16N_3	L2	I/O
3	IO_L16P_3/VREF_3	L1	VREF
3	IO_L18N_3	L3	I/O
3	IO_L18P_3	K4	I/O
3	IO_L19N_3	L4	I/O
3	IO_L19P_3	M3	I/O
3	IO_L20N_3	N1	I/O
3	IO_L20P_3	M1	I/O
3	IO_L22N_3	P1	I/O
3	IO_L22P_3/VREF_3	N2	VREF
3	IO_L23N_3	P2	I/O
3	IO_L23P_3	R1	I/O
3	IO_L24N_3	M4	I/O
3	IO_L24P_3	N3	I/O
3	IP_3	J4	INPUT
3	IP_3/VREF_3	G4	VREF
3	IP_3/VREF_3	J5	VREF
3	VCCO_3	D2	VCCO
3	VCCO_3	H2	VCCO
3	VCCO_3	M2	VCCO
GND	GND	A1	GND
GND	GND	A16	GND
GND	GND	B11	GND
GND	GND	B7	GND
GND	GND	C14	GND
GND	GND	C3	GND
GND	GND	E10	GND
GND	GND	E12	GND
GND	GND	E5	GND
GND	GND	F11	GND
GND	GND	F2	GND
GND	GND	F6	GND
GND	GND	F7	GND
GND	GND	F8	GND
GND	GND	F9	GND
GND	GND	G10	GND
GND	GND	G12	GND
GND	GND	G15	GND
GND	GND	G5	GND
GND	GND	G6	GND

Table 69: **Spartan-3A FT256 Pinout (XC3S700A,**

Bank	XC3S700A XC3S1400A	FT256 Ball	Type
GND	GND	G8	GND
GND	GND	H11	GND
GND	GND	H5	GND
GND	GND	H7	GND
GND	GND	H9	GND
GND	GND	J10	GND
GND	GND	J6	GND
GND	GND	J8	GND
GND	GND	K11	GND
GND	GND	K12	GND
GND	GND	K2	GND
GND	GND	K5	GND
GND	GND	K7	GND
GND	GND	K9	GND
GND	GND	L10	GND
GND	GND	L11	GND
GND	GND	L15	GND
GND	GND	L6	GND
GND	GND	L8	GND
GND	GND	M12	GND
GND	GND	M5	GND
GND	GND	M8	GND
GND	GND	N10	GND
GND	GND	N7	GND
GND	GND	P14	GND
GND	GND	P3	GND
GND	GND	R10	GND
GND	GND	R6	GND
GND	GND	T1	GND
GND	GND	T16	GND
VCCAUX	SUSPEND	R16	PWRMGT
VCCAUX	DONE	T15	CONFIG
VCCAUX	PROG_B	A2	CONFIG
VCCAUX	TCK	A15	JTAG
VCCAUX	TDI	B1	JTAG
VCCAUX	TDO	B16	JTAG
VCCAUX	TMS	B2	JTAG
VCCAUX	VCCAUX	D6	VCCAUX
VCCAUX	VCCAUX	E11	VCCAUX
VCCAUX	VCCAUX	F12	VCCAUX

User I/Os by Bank

Table 70, Table 71, and Table 72 indicate how the available user-I/O pins are distributed between the four I/O banks on the FT256 package. The AWAKE pin is counted as a dual-purpose I/O.

The XC3S50A FPGA in the FT256 package has 51 unconnected balls, labeled with an "N.C." type. These pins are also indicated in Figure 20.

Table 70: **User I/Os Per Bank on XC3S50A in the FT256 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	40	21	7	1	3	8
Right	1	32	12	5	4	3	8
Bottom	2	40	5	2	21	6	6
Left	3	32	15	6	0	3	8
TOTAL		**144**	**53**	**20**	**26**	**15**	**30**

Table 71: **User I/Os Per Bank on XC3S200A and XC3S400A in the FT256 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	47	27	6	1	5	8
Right	1	50	1	6	30	5	8
Bottom	2	48	11	2	21	6	8
Left	3	50	30	7	0	5	8
TOTAL		**195**	**69**	**21**	**52**	**21**	**32**

Table 72: **User I/Os Per Bank on XC3S700A and XC3S1400A in the FT256 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	41	27	1	1	4	8
Right	1	40	0	0	30	4	6
Bottom	2	41	7	0	21	5	8
Left	3	39	25	1	0	5	8
TOTAL		**161**	**59**	**2**	**52**	**18**	**30**

Footprint Migration Differences

Unconnected Balls on XC3S50A

Table 73 summarizes any footprint and functionality differences between the XC3S50A and the XC3S200A or XC3S400A FPGAs that might affect easy migration between these devices in the FT256 package. The XC3S200A and XC3S400A have identical pinouts. The XC3S50A pinout is compatible, but there are 52 balls that are different. Generally, designs easily migrate upward from the XC3S50A to either the XC3S200A or XC3S400A. If using differential I/O, see Table 74. If using the BPI configuration mode (parallel Flash), see Table 75.

Table 73: **FT256 XC3S50A Footprint Migration Difference**

FT256 Ball	Bank	XC3S50A Type	Migration	XC3S200A/ XC3S400A Type
A7	0	N.C.	→	I/O
A12	0	N.C.	→	I/O
B12	0	INPUT	→	I/O
C7	0	N.C.	→	I/O
D10	0	N.C.	→	I/O
E2	3	N.C.	→	I/O
E3	3	N.C.	→	I/O
E7	0	N.C.	→	I/O
E10	0	N.C.	→	I/O
E16	1	N.C.	→	I/O
F3	3	N.C.	→	I/O
F8	0	N.C.	→	I/O
F14	1	N.C.	→	I/O
F15	1	N.C.	→	I/O
F16	1	N.C.	→	I/O
G3	3	N.C.	→	I/O
G4	3	N.C.	→	I/O
G5	3	N.C.	→	INPUT
G6	3	N.C.	→	INPUT
G13	1	N.C.	→	I/O
G14	1	N.C.	→	I/O
G16	1	N.C.	→	I/O
H4	3	N.C.	→	I/O
H5	3	N.C.	→	I/O
H6	3	N.C.	→	I/O
H13	1	N.C.	→	I/O
J4	3	N.C.	→	I/O
J6	3	N.C.	→	I/O
J10	1	N.C.	→	INPUT
J11	1	N.C.	→	INPUT
K4	3	N.C.	→	I/O
K13	1	N.C.	→	I/O
L1	3	N.C.	→	I/O
L2	3	N.C.	→	I/O
L3	3	N.C.	→	I/O
L4	3	N.C.	→	I/O
L13	1	N.C.	→	I/O
L14	1	N.C.	→	I/O
L16	1	N.C.	→	I/O
M3	3	N.C.	→	I/O
M10	2	N.C.	→	I/O
M13	1	N.C.	→	I/O
M14	1	N.C.	→	I/O
M15	1	N.C.	→	I/O
M16	1	N.C.	→	I/O
N7	2	N.C.	→	I/O
N10	2	N.C.	→	I/O
N12	2	N.C.	→	I/O
P6	2	N.C.	→	I/O
P13	2	N.C.	→	I/O
R7	2	N.C.	→	I/O
T7	2	N.C.	→	I/O
DIFFERENCES			52	

Legend:

→ This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction is possible depending on how the pin is configured for the device on the right.

FT256 Footprint (XC3S200A, XC3S400A)

Bank 0

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	GND	PROG_B	I/O L19P_0	I/O L18P_0	I/O L17P_0	I/O L15P_0	I/O L13P_0	I/O L12P_0 GCLK10	I/O L10N_0 GCLK7	I/O L08N_0	I/O L07N_0	I/O L05N_0	I/O L04N_0	I/O L04P_0	TCK	GND
B	TDI	TMS	I/O L19N_0	I/O L18N_0	VCCO_0	I/O L15N_0	GND	I/O L12N_0 GCLK11	VCCO_0	I/O L08P_0	GND	I/O L05P_0	VCCO_0	I/O L02N_0	I/O L02P_0 VREF_0	TDO
C	I/O L01N_3	I/O L01P_3	GND	I/O L20P_0 VREF_0	I/O L17N_0	I/O L16N_0	I/O L13N_0	I/O L11P_0 GCLK8	I/O L10P_0 GCLK6	I/O L09P_0 GCLK4	I/O L07P_0	I/O L03P_0	I/O L01N_0	GND	I/O L24N_1 A25	I/O L24P_1 A24
D	I/O L03P_3	VCCO_3	I/O L02N_3	I/O L02P_3	I/O L20N_0 PUDC_B	INPUT	I/O L16P_0	I/O L11N_0 GCLK9	I/O L09N_0 GCLK5	I/O L06P_0	I/O L03N_0	INPUT	I/O L01P_0	I/O L23N_1 A23	I/O L22N_1 A21	I/O L22P_1 A20
E	I/O L03N_3	I/O L05N_3	I/O L05P_3	INPUT L04P_3	GND	INPUT	I/O L14N_0 VREF_0	VCCO_0	INPUT VREF_0	I/O L06N_0 VREF_0	VCCAUX	GND	I/O L23P_1 A22	I/O L20P_1 A18	VCCO_1	I/O L18P_1 A14
F	I/O L08P_3	GND	I/O L07P_3	INPUT L04N_3 VREF_3	VCCAUX	GND	INPUT	I/O L14P_0	INPUT	INPUT	INPUT L25N_1	INPUT L25P_1 VREF_1	I/O L20N_1 A19	I/O L19N_1 A17	I/O L18N_1 A15	I/O L16N_1 A11
G	I/O L08N_3 VREF_3	I/O L11P_3 LHCLK0	I/O L09P_3	I/O L07N_3	INPUT L06N_3 VREF_3	INPUT L06P_3	VCCINT	GND	VCCINT	GND	INPUT L21N_1	INPUT L21P_1 VREF_1	I/O L19P_1 A16	I/O L17N_1 A13	GND	I/O L16P_1 A10
H	I/O L11N_3 LHCLK1	VCCO_3	I/O L12P_3 LHCLK2	I/O L09N_3	I/O L10N_3	I/O L10P_3	INPUT L13P_3	VCCINT	GND	INPUT L13P_1	INPUT L13N_1	VCCO_1	I/O L17P_1 A12	I/O L14N_1 RHCLK5	I/O L15P_1 IRDY1 RHCLK6	I/O L15N_1 RHCLK7
J	I/O L14N_3 LHCLK5	I/O L14P_3 LHCLK4	I/O L12N_3 IRDY2 LHCLK3	I/O L17P_3	VCCO_3	I/O L17N_3	INPUT L13N_3	GND	VCCINT	INPUT L09P_1 VREF_1	INPUT L09N_1	I/O L10P_1 A8	I/O L10N_1 A9	I/O L14P_1 RHCLK4	VCCO_1	I/O L12N_1 TRDY1 RHCLK3
K	I/O L15N_3 LHCLK7	GND	I/O L15P_3 TRDY2 LHCLK6	I/O L18P_3	INPUT L21P_3	INPUT L21N_3	GND	VCCINT	GND	VCCINT	INPUT L04P_1	INPUT L04N_1 VREF_1	I/O L06N_1 A3	I/O L11N_1 RHCLK1	I/O L11P_1 RHCLK0	I/O L12P_1 RHCLK2
L	I/O L16P_3 VREF_3	I/O L16N_3	I/O L18N_3	I/O L19N_3	INPUT L25P_3	INPUT L25N_3 VREF_3	INPUT	INPUT	INPUT VREF_2	INPUT VREF_2	GND	VCCAUX	I/O L06P_1 A2	I/O L08P_1 A6	GND	I/O L08N_1 A7
M	I/O L20P_3	VCCO_3	I/O L19P_3	I/O L24N_3	GND	VCCAUX	INPUT VREF_2	INPUT VREF_2	VCCO_2	I/O L13N_2	INPUT VREF_2	GND	I/O L05P_1	I/O L05N_1 VREF_1	I/O L07P_1 A4	I/O L07N_1 A5
N	I/O L20N_3	I/O L22P_3	I/O L24P_3	I/O L01P_2 M1	INPUT VREF_2	I/O L04P_2 VS1	I/O L07P_2	I/O L08N_2 D4	I/O L11P_2 GCLK0	I/O L13P_2	I/O L16N_2	I/O L19P_2	I/O L01P_1 HDC	I/O L01N_1 LDC2	VCCO_1	I/O L03N_1 A1
P	I/O L22N_3	I/O L23N_3	GND	I/O L01N_2 M0	I/O L04N_2 VS0	I/O L07N_2	I/O L08P_2 D5	I/O L10P_2 GCLK14	I/O L11N_2 GCLK1	I/O L14N_2 MOSI CSI_B	I/O L16P_2	I/O L17N_2 D3	I/O L19N_2	GND	I/O L02N_1 LDC0	I/O L03P_1 A0
R	I/O L23P_3	I/O L02P_2 M2	I/O L03P_2 RDWR_B	VCCO_2	I/O L05N_2	GND	I/O L09P_2 GCLK12	VCCO_2	I/O L12P_2 GCLK2	GND	I/O L15N_2 DOUT	VCCO_2	I/O L18N_2 D1	I/O L20N_2 CCLK	I/O L02P_1 LDC1	SUSPEND
T	GND	I/O L02N_2 CSO_B	I/O L03N_2 VS2	I/O L05P_2	I/O L06P_2 D7	I/O L06N_2 D6	I/O L09N_2 GCLK13	I/O L10N_2 GCLK15	I/O L12N_2 GCLK3	I/O L14P_2	I/O L15P_2 AWAKE	I/O L17P_2 INIT_B	I/O L18P_2 D2	I/O L20P_2 D0 DIN/MISO	DONE	GND

Bank 3 (left) Bank 1 (right)

Bank 2

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Figure 21: **XC3S200A and XC3S400A FT256 Package Footprint (Top View)**

- 69 **I/O:** Unrestricted, general-purpose user I/O
- 21 **INPUT:** Unrestricted, general-purpose input pin
- 2 **CONFIG:** Dedicated configuration pins
- 0 **N.C.:** Not connected
- 51 **DUAL:** Configuration pins, then possible user I/O
- 32 **CLK:** User I/O, input, or global buffer input
- 4 **JTAG:** Dedicated JTAG port pins
- 28 **GND:** Ground
- 21 **VREF:** User I/O or input voltage reference for bank
- 16 **VCCO:** Output voltage supply for bank
- 6 **VCCINT:** Internal core supply voltage (+1.2V)
- 4 **VCCAUX:** Auxiliary supply voltage
- 2 **SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins

FG400: 400-ball Fine-pitch Ball Grid Array

The 400-ball fine-pitch ball grid array, FG400, supports two different Spartan-3A FPGAs, the XC3S400A and the XC3S700A. Both devices share a common footprint for this package as shown in Table 81 and Figure 24.

Table 81 lists all the FG400 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 81: **Spartan-3A FG400 Pinout**

Bank	Pin Name	FG400 Ball	Type
0	IO_L01N_0	A18	I/O
0	IO_L01P_0	B18	I/O
0	IO_L02N_0	C17	I/O
0	IO_L02P_0/VREF_0	D17	VREF
0	IO_L03N_0	E15	I/O
0	IO_L03P_0	D16	I/O
0	IO_L04N_0	A17	I/O
0	IO_L04P_0/VREF_0	B17	VREF
0	IO_L05N_0	A16	I/O
0	IO_L05P_0	C16	I/O
0	IO_L06N_0	C15	I/O
0	IO_L06P_0	D15	I/O
0	IO_L07N_0	A14	I/O
0	IO_L07P_0	C14	I/O
0	IO_L08N_0	A15	I/O
0	IO_L08P_0	B15	I/O
0	IO_L09N_0	F13	I/O
0	IO_L09P_0	E13	I/O
0	IO_L10N_0/VREF_0	C13	VREF
0	IO_L10P_0	D14	I/O
0	IO_L11N_0	C12	I/O
0	IO_L11P_0	B13	I/O
0	IO_L12N_0	F12	I/O
0	IO_L12P_0	D12	I/O
0	IO_L13N_0	A12	I/O

Table 81: **Spartan-3A FG400 Pinout *(Continued)***

Bank	Pin Name	FG400 Ball	Type
0	IO_L13P_0	B12	I/O
0	IO_L14N_0	C11	I/O
0	IO_L14P_0	B11	I/O
0	IO_L15N_0/GCLK5	E11	GCLK
0	IO_L15P_0/GCLK4	D11	GCLK
0	IO_L16N_0/GCLK7	C10	GCLK
0	IO_L16P_0/GCLK6	A10	GCLK
0	IO_L17N_0/GCLK9	E10	GCLK
0	IO_L17P_0/GCLK8	D10	GCLK
0	IO_L18N_0/GCLK11	A8	GCLK
0	IO_L18P_0/GCLK10	A9	GCLK
0	IO_L19N_0	C9	I/O
0	IO_L19P_0	B9	I/O
0	IO_L20N_0	C8	I/O
0	IO_L20P_0	B8	I/O
0	IO_L21N_0	D8	I/O
0	IO_L21P_0	C7	I/O
0	IO_L22N_0/VREF_0	F9	VREF
0	IO_L22P_0	E9	I/O
0	IO_L23N_0	F8	I/O
0	IO_L23P_0	E8	I/O
0	IO_L24N_0	A7	I/O
0	IO_L24P_0	B7	I/O
0	IO_L25N_0	C6	I/O
0	IO_L25P_0	A6	I/O
0	IO_L26N_0	B5	I/O
0	IO_L26P_0	A5	I/O
0	IO_L27N_0	F7	I/O
0	IO_L27P_0	E7	I/O
0	IO_L28N_0	D6	I/O
0	IO_L28P_0	C5	I/O
0	IO_L29N_0	C4	I/O
0	IO_L29P_0	A4	I/O
0	IO_L30N_0	B3	I/O
0	IO_L30P_0	A3	I/O
0	IO_L31N_0	F6	I/O
0	IO_L31P_0	E6	I/O
0	IO_L32N_0/PUDC_B	B2	DUAL

Right Half of FG400 Package (Top View)

Bank 0

	11	12	13	14	15	16	17	18	19	20
A	GND	I/O L13N_0	VCCAUX	I/O L07N_0	I/O L08N_0	I/O L05N_0	I/O L04N_0	I/O L01N_0	TCK	GND
B	I/O L14P_0	I/O L13P_0	I/O L11P_0	GND	I/O L08P_0	VCCO_0	I/O L04P_0 VREF_0	I/O L01P_0	I/O L38N_1 A25	I/O L38P_1 A24
C	I/O L14N_0	I/O L11N_0	I/O L10N_0 VREF_0	I/O L07P_0	I/O L06N_0	I/O L05P_0	I/O L02N_0	GND	I/O L37N_1 A23	I/O L37P_1 A22
D	I/O L15P_0 GCLK4	I/O L12P_0	VCCO_0	I/O L10P_0	I/O L06P_0	I/O L03P_0	I/O L02P_0 VREF_0	I/O L34N_1	VCCO_1	I/O L34P_1
E	I/O L15N_0 GCLK5	GND	I/O L09P_0	INPUT	I/O L03N_0	VCCAUX	TDO	I/O L33P_1	I/O L32N_1	I/O L32P_1
F	INPUT	I/O L12N_0	I/O L09N_0	INPUT	GND	I/O L36N_1 A21	I/O L33N_1	I/O L30N_1 A19	I/O L29N_1 A17	I/O L29P_1 A16
G	INPUT VREF_0	INPUT	INPUT	INPUT L39N_1	INPUT L39P_1 VREF_1	I/O L36P_1 A20	I/O L30P_1 A18	I/O L28P_1	GND	I/O L26N_1 A15
H	INPUT	INPUT	GND	INPUT L35N_1	INPUT L35P_1	VCCO_1	I/O L28N_1	I/O L25N_1 A13	I/O L25P_1 A12	I/O L26P_1 A14
J	GND	VCCINT	INPUT L31N_1	INPUT L31P_1 VREF_1	INPUT L27N_1	INPUT L27P_1	I/O L24P_1	I/O L22N_1 A11	I/O L22P_1 A10	I/O L21N_1 RHCLK7
K	VCCINT	GND	VCCAUX	INPUT L23N_1	INPUT L23P_1 VREF_1	I/O L24N_1	GND	I/O L20P_1 RHCLK4	VCCO_1	I/O L21P_1 IRDY1 RHCLK6
L	GND	VCCINT	INPUT L19N_1	INPUT L19P_1	I/O L16P_1 A8	I/O L16N_1 A9	I/O L20N_1 RHCLK5	I/O L18N_1 TRDY1 RHCLK3	I/O L18P_1 RHCLK2	GND
M	VCCINT	GND	INPUT L15N_1	INPUT L15P_1 VREF_1	INPUT L11N_1 VREF_1	INPUT L11P_1	I/O L14P_1 A6	I/O L14N_1 A7	I/O L17P_1 RHCLK0	I/O L17N_1 RHCLK1
N	GND	INPUT VREF_2	GND	INPUT VREF_1	I/O L12P_1 A2	VCCO_1	I/O L12N_1 A3	I/O L13P_1 A4	I/O L13N_1 A5	VCCAUX
P	INPUT VREF_2	INPUT	INPUT	INPUT L04P_1	INPUT L04N_1 VREF_1	I/O L07P_1	I/O L07N_1	I/O L10P_1	GND	I/O L10N_1 VREF_1
R	VCCO_2	I/O L19N_2	I/O L23N_2	INPUT VREF_2	SUSPEND	I/O L03N_1 A1	I/O L08N_1	I/O L08P_1	I/O L09P_1	I/O L09N_1
T	INPUT	I/O L19P_2	I/O L23P_2	I/O L25N_2	I/O L27N_2	GND	I/O L03P_1 A0	I/O L05P_1	VCCO_1	I/O L05N_1
U	I/O L18P_2 GCLK2	GND	I/O L22P_2 AWAKE	VCCO_2	I/O L27P_2	I/O L29N_2	I/O L31N_2	I/O L02N_1 LDC0	I/O L06P_1	I/O L06N_1
V	I/O L17N_2 GCLK1	I/O L18N_2 GCLK3	I/O L22N_2 DOUT	I/O L25P_2	I/O L26N_2 D1	I/O L29P_2	I/O L31P_2	GND	I/O L02P_1 LDC1	I/O L01N_1 LDC2
W	VCCO_2	I/O L20N_2 MOSI CSI_B	I/O L21N_2	I/O L24N_2 D3	GND	I/O L28N_2	VCCO_2	I/O L32P_2 D0 DIN/MISO	DONE	I/O L01P_1 HDC
Y	I/O L17P_2 GCLK0	I/O L20P_2	I/O L21P_2	I/O L24P_2 INIT_B	I/O L26P_2 D2	I/O L28P_2	I/O L30P_2	I/O L30N_2	I/O L32N_2 CCLK	GND

Bank 1

Bank 2

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Right Half of FG676 Package (Top View)

Bank 0

	14	15	16	17	18	19	20	21	22	23	24	25	26
A	I/O L26N_0 GCLK7	I/O L23N_0	GND	INPUT	I/O L18N_0	I/O L15N_0	I/O L14N_0	GND	I/O L07N_0	INPUT	N.C. ◆	TCK	GND
B	I/O L26P_0 GCLK6	I/O L23P_0	VCCO_0	I/O L19N_0	I/O L18P_0	I/O L15P_0	I/O L14P_0 VREF_0	I/O L09N_0	VCCO_0	I/O L07P_0	N.C. ◆	INPUT L65N_1	INPUT L65P_1 VREF_1
C	GND	I/O L22N_0	I/O L21N_0	I/O L19P_0	I/O L17N_0	GND	I/O L11N_0	I/O L09P_0	I/O L05N_0	I/O L06N_0	GND	I/O L63N_1 A23	I/O L63P_1 A22
D	INPUT VREF_0	INPUT	I/O L22P_0	I/O L21P_0	I/O L17P_0	INPUT	I/O L11P_0	I/O L10N_0	I/O L05P_0	I/O L06P_0	I/O L61N_1	I/O L61P_1	I/O L60N_1
E	I/O L24P_0	I/O L20N_0 VREF_0	VCCAUX	I/O L13N_0	INPUT	VCCO_0	INPUT	I/O L10P_0	VCCAUX	TDO	I/O L56P_1	VCCO_1	I/O L60P_1
F	I/O L24N_0	I/O L20P_0	GND	I/O L13P_0	N.C. ◆	I/O L02N_0	I/O L01N_0	GND	I/O L58P_1 VREF_1	I/O L56N_1	I/O L54N_1	I/O L54P_1	GND
G	INPUT	I/O L16P_0	INPUT	I/O L08N_0	N.C. ◆	I/O L02P_0 VREF_0	I/O L01P_0	I/O L64N_1 A25	I/O L58N_1	I/O L51P_1	I/O L51N_1	INPUT L52N_1 VREF_1	INPUT L52P_1
H	GND	I/O L16N_0	VCCO_0	I/O L08P_0	INPUT	GND	I/O L64P_1 A24	I/O L62N_1 A21	VCCO_1	INPUT L48P_1	INPUT L48N_1	INPUT L44N_1	INPUT L44P_1 VREF_1
J	I/O L25N_0 GCLK5	INPUT	I/O L12P_0	INPUT VREF_0	VCCAUX	I/O L59P_1	I/O L59N_1	I/O L62P_1 A20	I/O L49N_1	I/O L49P_1	GND	I/O L43N_1 A19	I/O L43P_1 A18
K	I/O L25P_0 GCLK4	VCCINT	I/O L12N_0	GND	I/O L57N_1	I/O L57P_1	I/O L53N_1	I/O L50N_1	I/O L46N_1	I/O L46P_1	INPUT L40P_1	I/O L41P_1	I/O L41N_1
L	VCCINT	GND	VCCINT	I/O L55N_1	I/O L55P_1	VCCO_1	I/O L53P_1	GND	I/O L50P_1	INPUT L40N_1	I/O L38P_1 A12	VCCO_1	GND
M	GND	VCCINT	GND	VCCINT	I/O L47N_1	I/O L47P_1	I/O L42N_1 A17	I/O L45P_1	I/O L45N_1	I/O L38N_1 A13	INPUT L36P_1 VREF_1	I/O L35N_1 A11	I/O L35P_1 A10
N	VCCINT	GND	VCCINT	I/O L39N_1 A15	I/O L39P_1 A14	I/O L34N_1 RHCLK7	I/O L42P_1 A16	I/O L37N_1	VCCO_1	INPUT L36N_1	I/O L33N_1 RHCLK5	INPUT L32N_1	INPUT L32P_1
P	VCCINT	VCCINT	GND	VCCAUX	I/O L34P_1 IRDY1 RHCLK6	GND	I/O L30N_1 RHCLK1	I/O L30P_1 RHCLK0	I/O L37P_1	I/O L33P_1 RHCLK4	GND	I/O L31N_1 TRDY1 RHCLK3	I/O L31P_1 RHCLK2
R	VCCINT	GND	VCCINT	I/O L27N_1 A7	I/O L27P_1 A6	I/O L22P_1	I/O L22N_1	I/O L25P_1 A2	I/O L25N_1 A3	INPUT L28P_1 VREF_1	INPUT L28N_1	I/O L29P_1 A8	I/O L29N_1 A9
T	GND	VCCINT	GND	I/O L17N_1	I/O L17P_1	VCCO_1	I/O L14N_1	GND	VCCAUX	I/O L26P_1 A4	I/O L26N_1 A5	VCCO_1	GND
U	VCCAUX	I/O L35N_2	I/O L42N_2	GND	I/O L12N_1	I/O L12P_1	I/O L10N_1	I/O L14P_1	I/O L21N_1	I/O L23P_1	I/O L23N_1 VREF_1	INPUT L24P_1	INPUT L24N_1 VREF_1
V	I/O L31P_2	I/O L35P_2	I/O L42P_2	I/O L46N_2	I/O L08P_1	I/O L08N_1	SUSPEND	I/O L10P_1	I/O L18N_1	I/O L21P_1	I/O L19P_1	I/O L19N_1	INPUT L20N_1 VREF_1
W	GND	I/O L31N_2	VCCO_2	I/O L46P_2	N.C. ◆	GND	I/O L04P_1	I/O L04N_1	VCCO_1	I/O L18P_1	GND	INPUT L16P_1	INPUT L20P_1
Y	I/O L27P_2 GCLK0	I/O L34N_2 D3	INPUT 2 VREF_2	I/O L43N_2	N.C. ◆	N.C. ◆	I/O L01P_1 HDC	I/O L01N_1 LDC2	I/O L13P_1	I/O L13N_1	I/O L15P_1	I/O L15N_1	INPUT L16N_1
AA	I/O L27N_2 GCLK1	I/O L34P_2 INIT_B	GND	I/O L43P_2	I/O L47N_2	INPUT	INPUT VREF_2	GND	I/O L09P_1	I/O L09N_1	I/O L11P_1	I/O L11N_1	GND
AB	VCCO_2	I/O L30N_2 MOSI CSI_B	I/O L38N_2	INPUT	I/O L47P_2	VCCO_2	INPUT	DONE	VCCAUX	I/O L07P_1	I/O L07N_1 VREF_1	VCCO_1	I/O L06N_1
AC	I/O L29N_2	I/O L30P_2	I/O L38P_2	INPUT	INPUT	I/O L40N_2	I/O L41N_2	I/O L45N_2	N.C. ◆	I/O L03P_1 A0	I/O L03N_1 A1	I/O L05N_1	I/O L06P_1
AD	I/O L29P_2	I/O L32P_2 AWAKE	INPUT	I/O L33N_2	GND	I/O L40P_2	I/O L41P_2	I/O L44N_2	I/O L45P_2	N.C. ◆	GND	I/O L02N_1 LDC0	I/O L05P_1
AE	I/O L28N_2 GCLK3	I/O L32N_2 DOUT	VCCO_2	I/O L33P_2	I/O L36N_2 D1	I/O L37N_2	I/O L39N_2	I/O L44P_2	VCCO_2	I/O L48N_2	I/O L52N_2 CCLK	I/O L51N_2	I/O L02P_1 LDC1
AF	I/O L28P_2 GCLK2	INPUT VREF_2	GND	INPUT VREF_2	I/O L36P_2 D2	I/O L37P_2	I/O L39P_2	GND	INPUT VREF_2	I/O L48P_2	I/O L52P_2 D0 DIN/MISO	I/O L51P_2	GND

Bank 1

Bank 2

DS529-4_08_012009

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/05/06	1.0	Initial release.
02/02/07	1.1	Promoted to Preliminary status. Added DOUT pin to DUAL-type pins in Table 57. Corrected counts for DUAL pins and differential pairs in Table 59. Corrected minor typographical error on pin names for pin numbers P24 and P25 in Table 66. Highlighted the differences in differential I/O pairs between the XC3S50A and XC3S200A in the FT256 package, shown in Table 68 and added Table 74 and Table 75 to summarize the differences.
03/16/07	1.2	Corrected minor typographical error in Figure 19.
04/23/07	1.3	Added reference to compatible Spartan-3A DSP family.
05/08/07	1.4	Added note regarding banking rules.
07/10/07	1.5	Updated Thermal Characteristics in Table 62.
04/15/08	1.6	Added VQ100 for XC3S50A and XC3S200A and added FT256 for XC3S700A and XCS1400A to Table 58, Table 59, and Table 62. Updated Thermal Characteristics with latest data in Table 62. Corrected bank for T8 and type for U16 in Table 86. Removed VREF name on 6 unconnected N.C. pins for XC3S1400A FG676 in Table 87 and Figure 27. These pins are noted as VREF if migrating up to the XC3SD1800A in Table 89.
05/28/08	1.7	Added "Package Overview" section.
03/06/09	1.8	Corrected bank designation for SUSPEND to VCCAUX. Corrected bank designation for JTAG pins in XC3S700A and XC3S1400A FT256 to VCCAUX.
08/19/10	2.0	Corrected pin 36 number in Figure 17 and Figure 18. Noted difference in FT256 P10/T10 function between XC3S50A and larger devices in Table 68 and Table 74.