# AMD Xilinx - XC3S50A-4FT256C Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 176 |
| Number of Logic Elements/Cells | 1584 |
| Total RAM Bits | 55296 |
| Number of I/O | 144 |
| Number of Gates | 50000 |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FTBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc3s50a-4ft256c |

## DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

**Advance:** Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

**Preliminary:** Based on characterization. Further changes are not expected.

**Production:** These specifications are approved once the silicon has been characterized over numerous production lots. Parameter values are considered stable with no future changes expected.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan®-3A devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

### Absolute Maximum Ratings

Stresses beyond those listed under Table 4: Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

*Table 4:* **Absolute Maximum Ratings**

| Symbol | Description | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Internal supply voltage | | –0.5 | 1.32 | V |
| $V_{CCAUX}$ | Auxiliary supply voltage | | –0.5 | 3.75 | V |
| $V_{CCO}$ | Output driver supply voltage | | –0.5 | 3.75 | V |
| $V_{REF}$ | Input reference voltage | | –0.5 | $V_{CCO}$ + 0.5 | V |
| $V_{IN}$ | Voltage applied to all User I/O pins and dual-purpose pins | Driver in a high-impedance state | –0.95 | 4.6 | V |
| | Voltage applied to all Dedicated pins | | –0.5 | 4.6 | V |
| $I_{IK}$ | Input clamp current per I/O pin | $-0.5V < V_{IN} < (V_{CCO} + 0.5V)$ (1) | – | ±100 | mA |
| $V_{ESD}$ | Electrostatic Discharge Voltage | Human body model | – | ±2000 | V |
| | | Charged device model | – | ±500 | V |
| | | Machine model | – | ±200 | V |
| $T_J$ | Junction temperature | | – | 125 | °C |
| $T_{STG}$ | Storage temperature | | –65 | 150 | °C |

**Notes:**

1. Upper clamp applies only when using PCI IOSTANDARDs.
2. For soldering guidelines, see UG112: *Device Packaging and Thermal Characteristics* and XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

## General DC Characteristics for I/O Pins

*Table 9:* **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins**(1)

| Symbol | Description | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $I_L$(2) | Leakage current at User I/O, input-only, dual-purpose, and dedicated pins, FPGA powered | Driver is in a high-impedance state, $V_{IN}$ = 0V or $V_{CCO}$ max, sample-tested | | –10 | – | +10 | µA |
| $I_{HS}$ | Leakage current on pins during hot socketing, FPGA unpowered | All pins except INIT_B, PROG_B, DONE, and JTAG pins when PUDC_B = 1. | | –10 | – | +10 | µA |
| | | INIT_B, PROG_B, DONE, and JTAG pins or other pins when PUDC_B = 0. | | Add $I_{HS}$ + $I_{RPU}$ | | | µA |
| $I_{RPU}$(3) | Current through pull-up resistor at User I/O, dual-purpose, input-only, and dedicated pins. Dedicated pins are powered by $V_{CCAUX}$. | $V_{IN}$ = GND | $V_{CCO}$ or $V_{CCAUX}$ = 3.0V to 3.6V | –151 | –315 | –710 | µA |
| | | | $V_{CCO}$ or $V_{CCAUX}$ = 2.3V to 2.7V | –82 | –182 | –437 | µA |
| | | | $V_{CCO}$ = 1.7V to 1.9V | –36 | –88 | –226 | µA |
| | | | $V_{CCO}$ = 1.4V to 1.6V | –22 | –56 | –148 | µA |
| | | | $V_{CCO}$ = 1.14V to 1.26V | –11 | –31 | –83 | µA |
| $R_{PU}$(3) | Equivalent pull-up resistor value at User I/O, dual-purpose, input-only, and dedicated pins (based on $I_{RPU}$ per Note 3) | $V_{IN}$ = GND | $V_{CCO}$ = 3.0V to 3.6V | 5.1 | 11.4 | 23.9 | kΩ |
| | | | $V_{CCO}$ = 2.3V to 2.7V | 6.2 | 14.8 | 33.1 | kΩ |
| | | | $V_{CCO}$ = 1.7V to 1.9V | 8.4 | 21.6 | 52.6 | kΩ |
| | | | $V_{CCO}$ = 1.4V to 1.6V | 10.8 | 28.4 | 74.0 | kΩ |
| | | | $V_{CCO}$ = 1.14V to 1.26V | 15.3 | 41.1 | 119.4 | kΩ |
| $I_{RPD}$(3) | Current through pull-down resistor at User I/O, dual-purpose, input-only, and dedicated pins. Dedicated pins are powered by $V_{CCAUX}$. | $V_{IN}$ = $V_{CCO}$ | $V_{CCAUX}$ = 3.0V to 3.6V | 167 | 346 | 659 | µA |
| | | | $V_{CCAUX}$ = 2.25V to 2.75V | 100 | 225 | 457 | µA |
| $R_{PD}$(3) | Equivalent pull-down resistor value at User I/O, dual-purpose, input-only, and dedicated pins (based on $I_{RPD}$ per Note 3) | $V_{CCAUX}$ = 3.0V to 3.6V | $V_{IN}$ = 3.0V to 3.6V | 5.5 | 10.4 | 20.8 | kΩ |
| | | | $V_{IN}$ = 2.3V to 2.7V | 4.1 | 7.8 | 15.7 | kΩ |
| | | | $V_{IN}$ = 1.7V to 1.9V | 3.0 | 5.7 | 11.1 | kΩ |
| | | | $V_{IN}$ = 1.4V to 1.6V | 2.7 | 5.1 | 9.6 | kΩ |
| | | | $V_{IN}$ = 1.14V to 1.26V | 2.4 | 4.5 | 8.1 | kΩ |
| | | $V_{CCAUX}$ = 2.25V to 2.75V | $V_{IN}$ = 3.0V to 3.6V | 7.9 | 16.0 | 35.0 | kΩ |
| | | | $V_{IN}$ = 2.3V to 2.7V | 5.9 | 12.0 | 26.3 | kΩ |
| | | | $V_{IN}$ = 1.7V to 1.9V | 4.2 | 8.5 | 18.6 | kΩ |
| | | | $V_{IN}$ = 1.4V to 1.6V | 3.6 | 7.2 | 15.7 | kΩ |
| | | | $V_{IN}$ = 1.14V to 1.26V | 3.0 | 6.0 | 12.5 | kΩ |
| $I_{REF}$ | $V_{REF}$ current per pin | All $V_{CCO}$ levels | | –10 | – | +10 | µA |
| $C_{IN}$ | Input capacitance | – | | – | – | 10 | pF |
| $R_{DT}$ | Resistance of optional differential termination circuit within a differential I/O pair. Not available on Input-only pairs. | $V_{CCO}$ = 3.3V ± 10% | LVDS_33, MINI_LVDS_33, RSDS_33 | 90 | 100 | 115 | Ω |
| | | $V_{CCO}$ = 2.5V ± 10% | LVDS_25, MINI_LVDS_25, RSDS_25 | 90 | 110 | – | Ω |

**Notes:**

1. The numbers in this table are based on the conditions set forth in Table 8.
2. For single-ended signals that are placed on a differential-capable I/O, $V_{IN}$ of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See "Parasitic Leakage" in UG331, *Spartan-3 Generation FPGA User Guide*.
3. This parameter is based on characterization. The pull-up resistance $R_{PU}$ = $V_{CCO}$ / $I_{RPU}$. The pull-down resistance $R_{PD}$ = $V_{IN}$ / $I_{RPD}$.

# Differential I/O Standards

## Differential Input Pairs

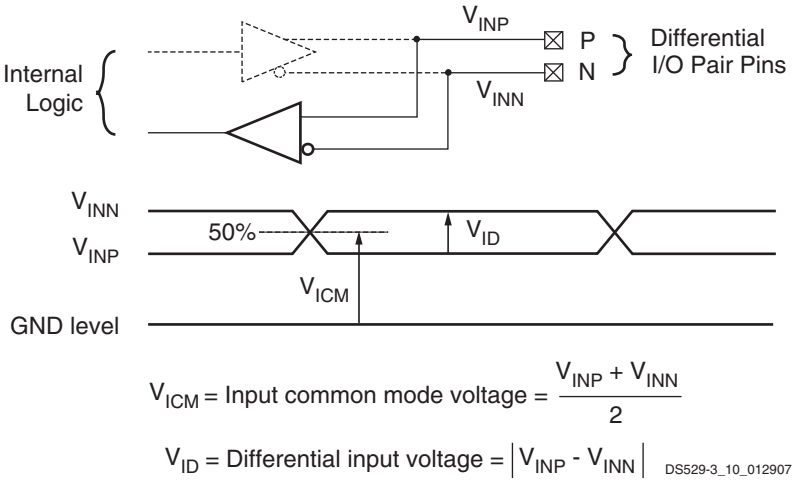


*Figure 4:* **Differential Input Voltages**

*Table 13:* **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

| IOSTANDARD Attribute | $V_{CCO}$ for Drivers(1) | | | $V_{ID}$ | | | $V_{ICM}$(2) | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min (V) | Nom (V) | Max (V) | Min (mV) | Nom (mV) | Max (mV) | Min (V) | Nom (V) | Max (V) |
| LVDS_25(3) | 2.25 | 2.5 | 2.75 | 100 | 350 | 600 | 0.3 | 1.25 | 2.35 |
| LVDS_33(3) | 3.0 | 3.3 | 3.6 | 100 | 350 | 600 | 0.3 | 1.25 | 2.35 |
| BLVDS_25(4) | 2.25 | 2.5 | 2.75 | 100 | 300 | – | 0.3 | 1.3 | 2.35 |
| MINI_LVDS_25(3) | 2.25 | 2.5 | 2.75 | 200 | – | 600 | 0.3 | 1.2 | 1.95 |
| MINI_LVDS_33(3) | 3.0 | 3.3 | 3.6 | 200 | – | 600 | 0.3 | 1.2 | 1.95 |
| LVPECL_25(5) | Inputs Only | | | 100 | 800 | 1000 | 0.3 | 1.2 | 1.95 |
| LVPECL_33(5) | Inputs Only | | | 100 | 800 | 1000 | 0.3 | 1.2 | 2.8(6) |
| RSDS_25(3) | 2.25 | 2.5 | 2.75 | 100 | 200 | – | 0.3 | 1.2 | 1.5 |
| RSDS_33(3) | 3.0 | 3.3 | 3.6 | 100 | 200 | – | 0.3 | 1.2 | 1.5 |
| TMDS_33(3, 4, 7) | 3.14 | 3.3 | 3.47 | 150 | – | 1200 | 2.7 | – | 3.23 |
| PPDS_25(3) | 2.25 | 2.5 | 2.75 | 100 | – | 400 | 0.2 | – | 2.3 |
| PPDS_33(3) | 3.0 | 3.3 | 3.6 | 100 | – | 400 | 0.2 | – | 2.3 |
| DIFF_HSTL_I_18 | 1.7 | 1.8 | 1.9 | 100 | – | – | 0.8 | – | 1.1 |
| DIFF_HSTL_II_18(8) | 1.7 | 1.8 | 1.9 | 100 | – | – | 0.8 | – | 1.1 |
| DIFF_HSTL_III_18 | 1.7 | 1.8 | 1.9 | 100 | – | – | 0.8 | – | 1.1 |
| DIFF_HSTL_I | 1.4 | 1.5 | 1.6 | 100 | – | – | 0.68 | | 0.9 |
| DIFF_HSTL_III | 1.4 | 1.5 | 1.6 | 100 | – | – | – | 0.9 | – |
| DIFF_SSTL18_I | 1.7 | 1.8 | 1.9 | 100 | – | – | 0.7 | – | 1.1 |
| DIFF_SSTL18_II(8) | 1.7 | 1.8 | 1.9 | 100 | – | – | 0.7 | – | 1.1 |
| DIFF_SSTL2_I | 2.3 | 2.5 | 2.7 | 100 | – | – | 1.0 | – | 1.5 |
| DIFF_SSTL2_II(8) | 2.3 | 2.5 | 2.7 | 100 | – | – | 1.0 | – | 1.5 |
| DIFF_SSTL3_I | 3.0 | 3.3 | 3.6 | 100 | – | – | 1.1 | – | 1.9 |
| DIFF_SSTL3_II | 3.0 | 3.3 | 3.6 | 100 | – | – | 1.1 | – | 1.9 |

**Notes:**

1. The $V_{CCO}$ rails supply only differential output drivers, not input circuits.
2. $V_{ICM}$ must be less than $V_{CCAUX}$.
3. These true differential output standards are supported only on FPGA banks 0 and 2. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
4. See "External Termination Requirements for Differential I/O," page 20.
5. LVPECL is supported on inputs only, not outputs. LVPECL_33 requires $V_{CCAUX}$=3.3V ± 10%.
6. LVPECL_33 maximum $V_{ICM}$ = the lower of 2.8V or $V_{CCAUX} - (V_{ID} / 2)$
7. Requires $V_{CCAUX}$ = 3.3V ± 10% for inputs. $(V_{CCAUX} - 300\ mV) \leq V_{ICM} \leq (V_{CCAUX} - 37\ mV)$
8. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
9. All standards except for LVPECL and TMDS can have $V_{CCAUX}$ at either 2.5V or 3.3V. Define your $V_{CCAUX}$ level using the CONFIG VCCAUX constraint.

## External Termination Requirements for Differential I/O

### *LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards*

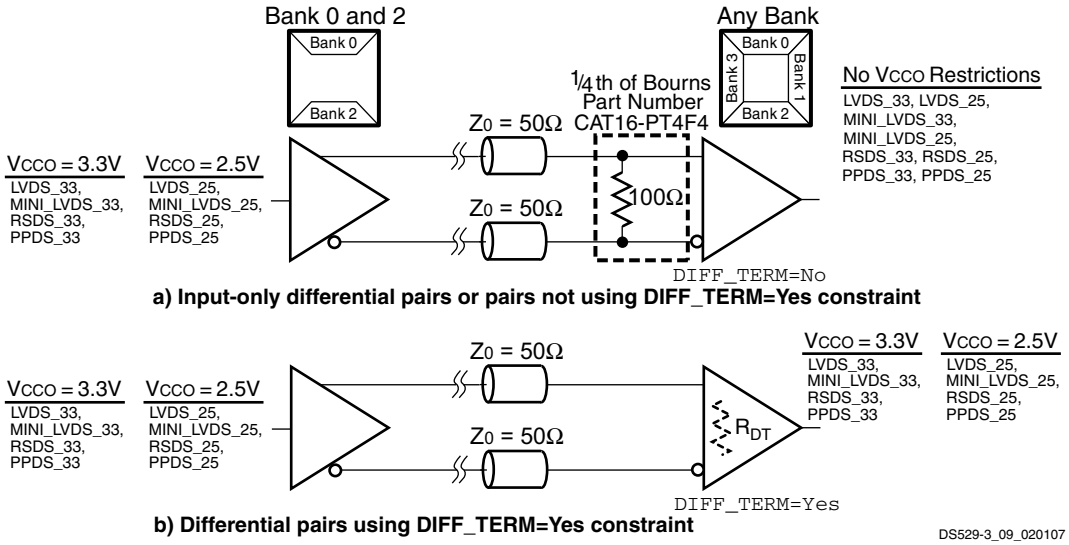


*Figure 6:* **External Input Termination for LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards**

### *BLVDS_25 I/O Standard*

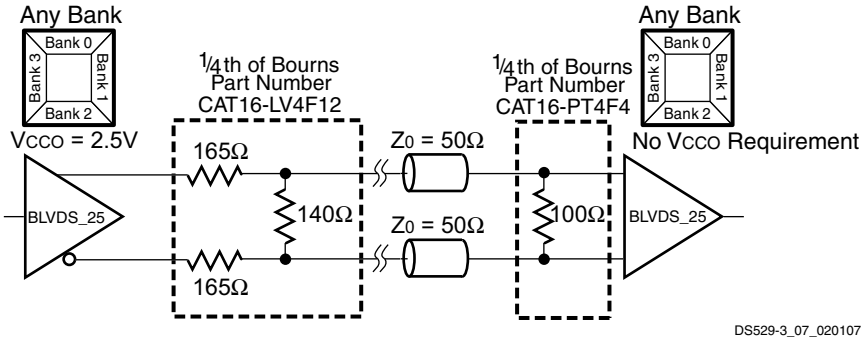


*Figure 7:* **External Output and Input Termination Resistors for BLVDS_25 I/O Standard**

### *TMDS_33 I/O Standard*

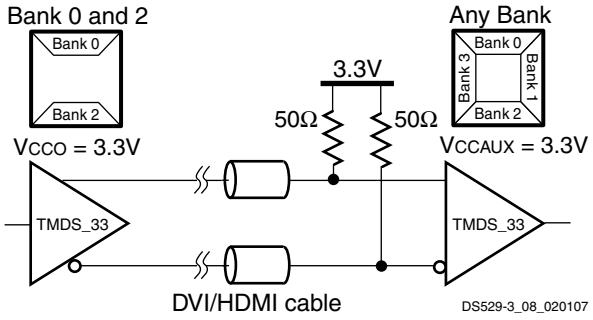


*Figure 8:* **External Input Resistors Required for TMDS_33 I/O Standard**

## Device DNA Read Endurance

*Table 15:* **Device DNA Identifier Memory Characteristics**

| Symbol | Description | Minimum | Units |
|---|---|---|---|
| DNA_CYCLES | Number of READ operations or JTAG ISC_DNA read operations. Unaffected by HOLD or SHIFT operations. | 30,000,000 | Read cycles |

## Switching Characteristics

All Spartan-3A FPGAs ship in two speed grades: –4 and the higher performance –5. Switching characteristics in this document are designated as Advance, Preliminary, or Production, as shown in Table 16. Each category is defined as follows:

**Advance**: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

**Preliminary**: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

**Production**: These specifications are approved once enough production silicon of a particular device has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

### Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGA designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Advance or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx® ISE® software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan-3A devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

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Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3A FPGA speed files (v1.41), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in Table 16. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

*Table 16:* **Spartan-3A v1.41 Speed Grade Designation**

| Device | Advance | Preliminary | Production |
|---|---|---|---|
| XC3S50A | | | -4, -5 |
| XC3S200A | | | -4, -5 |
| XC3S400A | | | -4, -5 |
| XC3S700A | | | -4, -5 |
| XC3S1400A | | | -4, -5 |

Table 17 provides the recent history of the Spartan-3A FPGA speed files.

*Table 17:* **Spartan-3A Speed File Version History**

| Version | ISE Release | Description |
|---|---|---|
| 1.41 | ISE 10.1.03 | Updated Automotive output delays |
| 1.40 | ISE 10.1.02 | Updated Automotive input delays. |
| 1.39 | ISE 10.1.01 | Added Automotive parts. |
| 1.38 | ISE 9.2.03i | Added Absolute Minimum values. |
| 1.37 | ISE 9.2.01i | Updated pin-to-pin setup and hold times (Table 19), TMDS output adjustment (Table 26) multiplier setup/hold times (Table 34), and block RAM clock width (Table 35). |
| 1.36 | ISE 9.2i; previously available via Answer Record AR24992 | XC3S400A, all speed grades and all temperature grades, upgraded to Production |
| 1.35 | Answer Record AR24992 | XC3S50A, XC3S200A, XC3S700A, XC3S1400A, all speed grades and all temperature grades, upgraded to Production. |
| 1.34 | ISE 9.1.03i | XC3S700A and XC3S1400A -4 speed grade upgraded to Production. Updated pin-to-pin timing numbers. |

## Input Timing Adjustments

*Table 23:* **Input Timing Adjustments by IOSTANDARD**

| Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD) | Add the Adjustment Below | | Units |
|---|---|---|---|
| | Speed Grade | | |
| | -5 | -4 | |
| **Single-Ended Standards** | | | |
| LVTTL | 0.62 | 0.62 | ns |
| LVCMOS33 | 0.54 | 0.54 | ns |
| LVCMOS25 | 0 | 0 | ns |
| LVCMOS18 | 0.83 | 0.83 | ns |
| LVCMOS15 | 0.60 | 0.60 | ns |
| LVCMOS12 | 0.31 | 0.31 | ns |
| PCI33_3 | 0.41 | 0.41 | ns |
| PCI66_3 | 0.41 | 0.41 | ns |
| HSTL_I | 0.72 | 0.72 | ns |
| HSTL_III | 0.77 | 0.77 | ns |
| HSTL_I_18 | 0.69 | 0.69 | ns |
| HSTL_II_18 | 0.69 | 0.69 | ns |
| HSTL_III_18 | 0.79 | 0.79 | ns |
| SSTL18_I | 0.71 | 0.71 | ns |
| SSTL18_II | 0.71 | 0.71 | ns |
| SSTL2_I | 0.68 | 0.68 | ns |
| SSTL2_II | 0.68 | 0.68 | ns |
| SSTL3_I | 0.78 | 0.78 | ns |
| SSTL3_II | 0.78 | 0.78 | ns |

*Table 23:* **Input Timing Adjustments by IOSTANDARD*(Continued)***

| Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD) | Add the Adjustment Below | | Units |
|---|---|---|---|
| | Speed Grade | | |
| | -5 | -4 | |
| **Differential Standards** | | | |
| LVDS_25 | 0.76 | 0.76 | ns |
| LVDS_33 | 0.79 | 0.79 | ns |
| BLVDS_25 | 0.79 | 0.79 | ns |
| MINI_LVDS_25 | 0.78 | 0.78 | ns |
| MINI_LVDS_33 | 0.79 | 0.79 | ns |
| LVPECL_25 | 0.78 | 0.78 | ns |
| LVPECL_33 | 0.79 | 0.79 | ns |
| RSDS_25 | 0.79 | 0.79 | ns |
| RSDS_33 | 0.77 | 0.77 | ns |
| TMDS_33 | 0.79 | 0.79 | ns |
| PPDS_25 | 0.79 | 0.79 | ns |
| PPDS_33 | 0.79 | 0.79 | ns |
| DIFF_HSTL_I_18 | 0.74 | 0.74 | ns |
| DIFF_HSTL_II_18 | 0.72 | 0.72 | ns |
| DIFF_HSTL_III_18 | 1.05 | 1.05 | ns |
| DIFF_HSTL_I | 0.72 | 0.72 | ns |
| DIFF_HSTL_III | 1.05 | 1.05 | ns |
| DIFF_SSTL18_I | 0.71 | 0.71 | ns |
| DIFF_SSTL18_II | 0.71 | 0.71 | ns |
| DIFF_SSTL2_I | 0.74 | 0.74 | ns |
| DIFF_SSTL2_II | 0.75 | 0.75 | ns |
| DIFF_SSTL3_I | 1.06 | 1.06 | ns |
| DIFF_SSTL3_II | 1.06 | 1.06 | ns |

**Notes:**

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8, Table 11, and Table 13.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

## Configurable Logic Block (CLB) Timing

*Table 30:* **CLB (SLICEM) Timing**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -5 | | -4 | | |
| | | Min | Max | Min | Max | |
| **Clock-to-Output Times** | | | | | | |
| $T_{CKO}$ | When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output | – | 0.60 | – | 0.68 | ns |
| **Setup Times** | | | | | | |
| $T_{AS}$ | Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB | 0.18 | – | 0.36 | – | ns |
| $T_{DICK}$ | Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB | 1.58 | – | 1.88 | – | ns |
| **Hold Times** | | | | | | |
| $T_{AH}$ | Time from the active transition at the CLK input to the point where data is last held at the F or G input | 0 | – | 0 | – | ns |
| $T_{CKDI}$ | Time from the active transition at the CLK input to the point where data is last held at the BX or BY input | 0 | – | 0 | – | ns |
| **Clock Timing** | | | | | | |
| $T_{CH}$ | The High pulse width of the CLB's CLK signal | 0.63 | – | 0.75 | – | ns |
| $T_{CL}$ | The Low pulse width of the CLK signal | 0.63 | – | 0.75 | – | ns |
| $F_{TOG}$ | Toggle frequency (for export control) | 0 | 770 | 0 | 667 | MHz |
| **Propagation Times** | | | | | | |
| $T_{ILO}$ | The time it takes for data to travel from the CLB's F (G) input to the X (Y) output | – | 0.62 | – | 0.71 | ns |
| **Set/Reset Pulse Width** | | | | | | |
| $T_{RPW\_CLB}$ | The minimum allowable pulse width, High or Low, to the CLB's SR input | 1.33 | – | 1.61 | – | ns |

**Notes:**

1. The numbers in this table are based on the operating conditions set forth in Table 8.

## Clock Buffer/Multiplexer Switching Characteristics

*Table 33:* **Clock Distribution Switching Characteristics**

| Description | Symbol | Minimum | Maximum Speed Grade | | Units |
|---|---|---|---|---|---|
| | | | -5 | -4 | |
| Global clock buffer (BUFG, BUFGMUX, BUFGCE) I input to O-output delay | $T_{GIO}$ | – | 0.22 | 0.23 | ns |
| Global clock multiplexer (BUFGMUX) select S-input setup to I0 and I1 inputs. Same as BUFGCE enable CE-input | $T_{GSI}$ | – | 0.56 | 0.63 | ns |
| Frequency of signals distributed on global buffers (all sides) | $F_{BUFG}$ | 0 | 350 | 334 | MHz |

**Notes:**

1. The numbers in this table are based on the operating conditions set forth in Table 8.

## Digital Frequency Synthesizer (DFS)

*Table 38:* **Recommended Operating Conditions for the DFS**

| Symbol | | Description | | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | -5 | | -4 | | |
| | | | | Min | Max | Min | Max | |
| **Input Frequency Ranges(2)** | | | | | | | | |
| $F_{CLKIN}$ | CLKIN_FREQ_FX | Frequency for the CLKIN input | | 0.200 | 333(4) | 0.200 | 333(4) | MHz |
| **Input Clock Jitter Tolerance(3)** | | | | | | | | |
| CLKIN_CYC_JITT_FX_LF | | Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency | $F_{CLKFX} \leq 150$ MHz | – | ±300 | – | ±300 | ps |
| CLKIN_CYC_JITT_FX_HF | | | $F_{CLKFX} > 150$ MHz | – | ±150 | – | ±150 | ps |
| CLKIN_PER_JITT_FX | | Period jitter at the CLKIN input | | – | ±1 | – | ±1 | ns |

**Notes:**

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 36.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.
4. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM.

*Table 39:* **Switching Characteristics for the DFS**

| Symbol | Description | | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | -5 | | -4 | | |
| | | | | Min | Max | Min | Max | |
| **Output Frequency Ranges** | | | | | | | | |
| CLKOUT_FREQ_FX(2) | Frequency for the CLKFX and CLKFX180 outputs | | All | 5 | 350 | 5 | 320 | MHz |
| **Output Clock Jitter(3,4)** | | | | | | | | |
| CLKOUT_PER_JITT_FX | Period jitter at the CLKFX and CLKFX180 outputs. | | All | **Typ** | **Max** | **Typ** | **Max** | |
| | | CLKIN ≤ 20 MHz | | Use the Spartan-3A Jitter Calculator: www.xilinx.com/support/documentation/data_sheets/s3a_jitter_calc.zip | | | | ps |
| | | CLKIN > 20 MHz | | ±[1% of CLKFX period + 100] | ±[1% of CLKFX period + 200] | ±[1% of CLKFX period + 100] | ±[1% of CLKFX period + 200] | ps |
| **Duty Cycle(5,6)** | | | | | | | | |
| CLKOUT_DUTY_CYCLE_FX | Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion | | All | – | ±[1% of CLKFX period + 350] | – | ±[1% of CLKFX period + 350] | ps |
| **Phase Alignment(6)** | | | | | | | | |
| CLKOUT_PHASE_FX | Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used | | All | – | ±200 | – | ±200 | ps |
| CLKOUT_PHASE_FX180 | Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used | | All | – | ±[1% of CLKFX period + 200] | – | ±[1% of CLKFX period + 200] | ps |

*Table 55:* **Configuration Timing Requirements for Attached Parallel NOR BPI Flash**

| Symbol | Description | Requirement | Units |
|---|---|---|---|
| $T_{CE}$ ($t_{ELQV}$) | Parallel NOR Flash PROM chip-select time | $T_{CE} \leq T_{INITADDR}$ | ns |
| $T_{OE}$ ($t_{GLQV}$) | Parallel NOR Flash PROM output-enable time | $T_{OE} \leq T_{INITADDR}$ | ns |
| $T_{ACC}$ ($t_{AVQV}$) | Parallel NOR Flash PROM read access time | $T_{ACC} \leq 50\% T_{CCLKn(min)} - T_{CCO} - T_{DCC} - PCB$ | ns |
| $T_{BYTE}$ ($t_{FLQV}$, $t_{FHQV}$) | For x8/x16 PROMs only: BYTE# to output valid time(3) | $T_{BYTE} \leq T_{INITADDR}$ | ns |

**Notes:**

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's PUDC_B pin is High or Low.

*Table 59:* **Maximum User I/O by Package**

| Device | Package | Maximum User I/Os and Input-Only | Maximum Input-Only | Maximum Differential Pairs | All Possible I/Os by Type | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | I/O | INPUT | DUAL | VREF | CLK | N.C. |
| XC3S50A | VQ100 | 68 | 6 | 60 | 17 | 2 | 20 | 6 | 23 | 0 |
| XC3S200A | | 68 | 6 | 60 | 17 | 2 | 20 | 6 | 23 | 0 |
| XC3S50A | TQ144 | 108 | 7 | 50 | 42 | 2 | 26 | 8 | 30 | 0 |
| XC3S50A | FT256 | 144 | 32 | 64 | 53 | 20 | 26 | 15 | 30 | 51 |
| XC3S200A | | 195 | 35 | 90 | 69 | 21 | 52 | 21 | 32 | 0 |
| XC3S400A | | 195 | 35 | 90 | 69 | 21 | 52 | 21 | 32 | 0 |
| XC3S700A | | 161 | 13 | 60 | 59 | 2 | 52 | 18 | 30 | 0 |
| XC3S1400A | | 161 | 13 | 60 | 59 | 2 | 52 | 18 | 30 | 0 |
| XC3S200A | FG320 | 248 | 56 | 112 | 101 | 40 | 52 | 23 | 32 | 3 |
| XC3S400A | | 251 | 59 | 112 | 101 | 42 | 52 | 24 | 32 | 0 |
| XC3S400A | FG400 | 311 | 63 | 142 | 155 | 46 | 52 | 26 | 32 | 0 |
| XC3S700A | | 311 | 63 | 142 | 155 | 46 | 52 | 26 | 32 | 0 |
| XC3S700A | FG484 | 372 | 84 | 165 | 194 | 61 | 52 | 33 | 32 | 3 |
| XC3S1400A | | 375 | 87 | 165 | 195 | 62 | 52 | 34 | 32 | 0 |
| XC3S1400A | FG676 | 502 | 94 | 227 | 313 | 67 | 52 | 38 | 32 | 17 |

**Notes:**

1. Some VREFs are on INPUT pins. See pinout tables for details.

Electronic versions of the package pinout tables and footprints are available for download from the Xilinx website. Using a spreadsheet program, the data can be sorted and reformatted according to any specific needs. Similarly, the ASCII-text file is easily parsed by most scripting programs.

http://www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip

# VQ100: 100-lead Very Thin Quad Flat Package

The XC3S50A and XC3S200 are available in the 100-lead very thin quad flat package, VQ100.

Table 63 lists all the package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The VQ100 does not support Suspend mode (SUSPEND and AWAKE are not connected), the address output pins for the Byte-wide Peripheral Interface (BPI) configuration mode, or daisy chain configuration (DOUT is not connected).

Table 63 also indicates that some differential I/O pairs have different assignments between the XC3S50A and the XC3S200A, highlighted in light blue. See "Footprint Migration Differences," page 72 for additional information.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

## Pinout Table

*Table 63:* **Spartan-3A VQ100 Pinout**

| Bank | Pin Name | Pin | Type |
|---|---|---|---|
| 0 | IO_0/GCLK11 | P90 | CLK |
| 0 | IO_L01N_0 | P78 | IO |
| 0 | IO_L01P_0/VREF_0 | P77 | VREF |
| 0 | IO_L02N_0/GCLK5 | P84 | CLK |
| 0 | IO_L02P_0/GCLK4 | P83 | CLK |
| 0 | IO_L03N_0/GCLK7 | P86 | CLK |
| 0 | IO_L03P_0/GCLK6 | P85 | CLK |
| 0 | IO_L04N_0/GCLK9 | P89 | CLK |
| 0 | IO_L04P_0/GCLK8 | P88 | CLK |
| 0 | IO_L05N_0 | P94 | IO |
| 0 | IO_L05P_0 | P93 | IO |
| 0 | IO_L06N_0/PUDC_B | P99 | DUAL |
| 0 | IO_L06P_0/VREF_0 | P98 | VREF |
| 0 | IP_0 | P97 | IP |
| 0 | IP_0/VREF_0 | P82 | VREF |
| 0 | VCCO_0 | P79 | VCCO |
| 0 | VCCO_0 | P96 | VCCO |
| 1 | IO_L01N_1 | P57 | IO |
| 1 | IO_L01P_1 | P56 | IO |
| 1 | IO_L02N_1/RHCLK1 | P60 | CLK |
| 1 | IO_L02P_1/RHCLK0 | P59 | CLK |
| 1 | IO_L03N_1/TRDY1/RHCLK3 | P62 | CLK |
| 1 | IO_L03P_1/RHCLK2 | P61 | CLK |
| 1 | IO_L04N_1/RHCLK7 | P65 | CLK |
| 1 | IO_L04P_1/IRDY1/RHCLK6 | P64 | CLK |
| 1 | IO_L05N_1 | P71 | IO |
| 1 | IO_L05P_1 | P70 | IO |
| 1 | IO_L06N_1 | P73 | IO |
| 1 | IO_L06P_1 | P72 | IO |
| 1 | IP_1/VREF_1 | P68 | VREF |
| 1 | VCCO_1 | P67 | VCCO |
| 2 | IO_2/MOSI/CSI_B | P46 | DUAL |
| 2 | IO_L01N_2/M0 | P25 | DUAL |
| 2 | IO_L01P_2/M1 | P23 | DUAL |
| 2 | IO_L02N_2/CSO_B | P27 | DUAL |
| 2 | IO_L02P_2/M2 | P24 | DUAL |
| 2 | IO_L03N_2/VS1 (3S50A)<br>IO_L04P_2/VS1 (3S200A) | P30 | DUAL |
| 2 | IO_L03P_2/RDWR_B | P28 | DUAL |
| 2 | IO_L04N_2/VS0 | P31 | DUAL |
| 2 | IO_L04P_2/VS2 (3S50A)<br>IO_L03N_2/VS2 (3S200A) | P29 | DUAL |
| 2 | IO_L05N_2/D7 (3S50A)<br>IO_L06P_2/D7 (3S200A) | P34 | DUAL |
| 2 | IO_L05P_2 | P32 | IO |
| 2 | IO_L06N_2/D6 | P35 | DUAL |
| 2 | IO_L06P_2 (3S50A)<br>IO_L05N_2 (3S200A) | P33 | IO |
| 2 | IO_L07N_2/D4 | P37 | DUAL |
| 2 | IO_L07P_2/D5 | P36 | DUAL |
| 2 | IO_L08N_2/GCLK15 | P41 | CLK |
| 2 | IO_L08P_2/GCLK14 | P40 | CLK |
| 2 | IO_L09N_2/GCLK1 | P44 | CLK |
| 2 | IO_L09P_2/GCLK0 | P43 | CLK |
| 2 | IO_L10N_2/D3 | P49 | DUAL |
| 2 | IO_L10P_2/INIT_B | P48 | DUAL |
| 2 | IO_L11N_2/D0/DIN/MISO (3S50A)<br>IO_L12P_2/D0/DIN/MISO (3S200A) | P51 | DUAL |
| 2 | IO_L11P_2/D2 | P50 | DUAL |
| 2 | IO_L12N_2/CCLK | P53 | DUAL |

## User I/Os by Bank

Table 64 indicates how the 68 available user-I/O pins are distributed between the four I/O banks on the VQ100 package.

*Table 64:* **User I/Os Per Bank for the XC3S50A and XC3S200A in the VQ100 Package**

| Package Edge | I/O Bank | Maximum I/O | All Possible I/O Pins by Type | | | | |
|---|---|---|---|---|---|---|---|
| | | | I/O | INPUT | DUAL | VREF | CLK |
| Top | 0 | 15 | 3 | 1 | 1 | 3 | 7 |
| Right | 1 | 13 | 6 | 0 | 0 | 1 | 6 |
| Bottom | 2 | 26 | 2 | 0 | 19 | 1 | 4 |
| Left | 3 | 14 | 6 | 1 | 0 | 1 | 6 |
| **TOTAL** | | **68** | **17** | **2** | **20** | **6** | **23** |

## Footprint Migration Differences

The XC3S50A and XC3S200 have common VQ100 pinouts except for some differences in alignment of differential I/O pairs.

### Differential I/O Alignment Differences

Some differential I/O pairs in the VQ100 on the XC3S50A FPGA are aligned differently than the corresponding pairs on the XC3S200A FPGAs, as shown in Table 65. All the mismatched pairs are in I/O Bank 2. These differences are indicated with the black diamond character (◆) in the footprint diagrams Figure 17 and Figure 18.

*Table 65:* **Differential I/O Differences in VQ100**

| VQ100 Pin | Bank | XC3S50A | XC3S200A |
|---|---|---|---|
| P29 | 2 | IIO_L04P_2/VS2 | IO_L03N_2/VS2 |
| P30 | | IO_L03N_2/VS1 | IO_L04P_2/VS1 |
| P33 | | IO_L06P_2 | IO_L05N_2 |
| P34 | | IO_L05N_2/D7 | IO_L06P_2/D7 |
| P51 | | IO_L11N_2/D0/DIN/MISO | IO_L12P_2/D0/DIN/MISO |
| P52 | | IO_L12P_2/D1 | IO_L11N_2/D1 |

## VQ100 Footprint (XC3S200A)

Note pin 1 indicator in top-left corner and logo orientation.

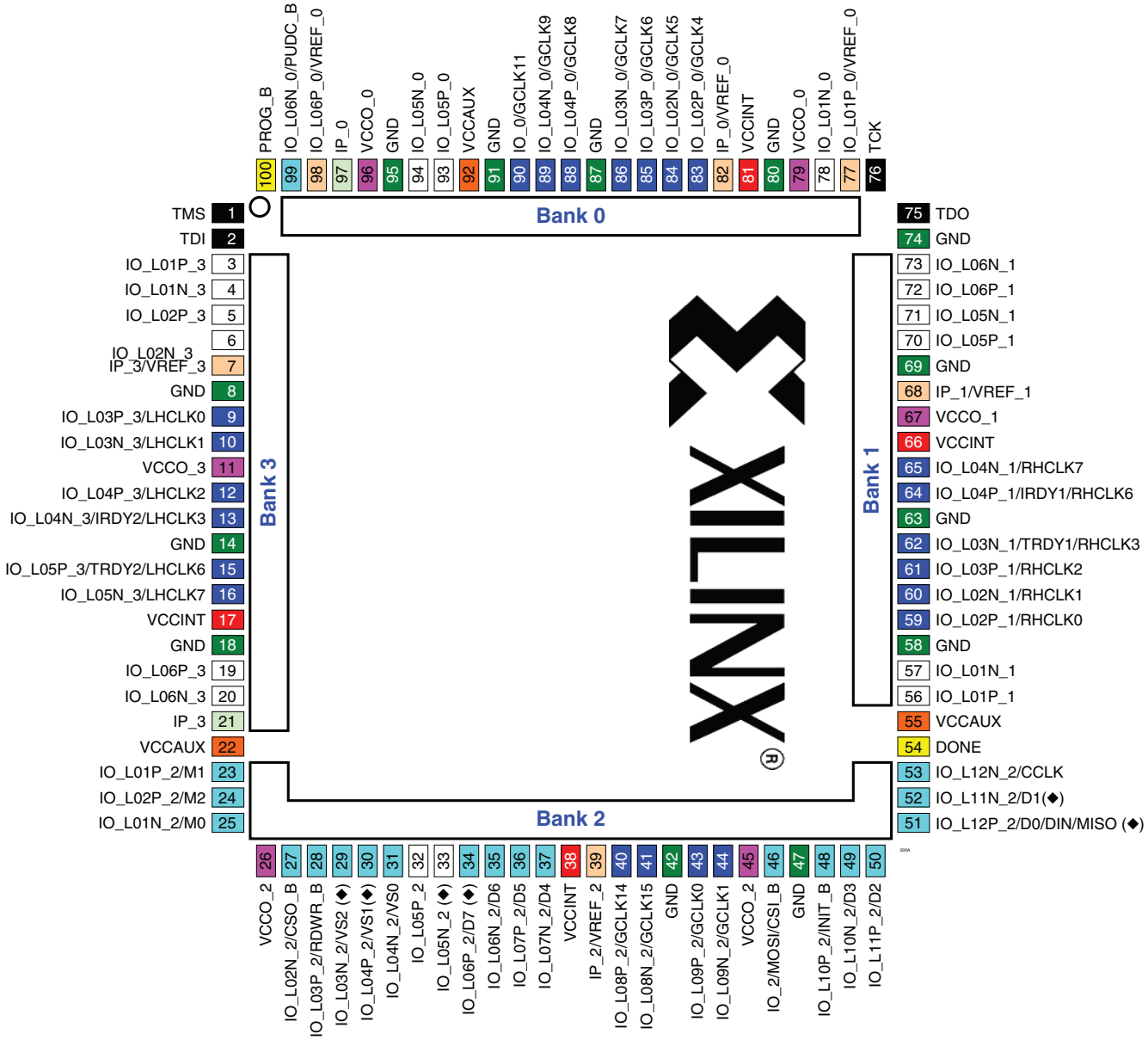


*Figure 18:* **VQ100 Package Footprint - XC3S200A (Top View)**

| | | | | | |
|---|---|---|---|---|---|
| 17 | **I/O:** Unrestricted, general-purpose user I/O | 20 | **DUAL:** Configuration pins, then possible user I/O | 6 | **VREF:** User I/O or input voltage reference for bank |
| 2 | **INPUT:** Unrestricted, general-purpose input pin | 23 | **CLK:** User I/O, input, or global buffer input | 6 | **VCCO:** Output voltage supply for bank |
| 2 | **CONFIG:** Dedicated configuration pins | 4 | **JTAG:** Dedicated JTAG port pins | 4 | **VCCINT:** Internal core supply voltage (+1.2V) |
| 0 | **N.C.:** Not connected | 13 | **GND:** Ground | 3 | **VCCAUX:** Auxiliary supply voltage |

*Table 69:* **Spartan-3A FT256 Pinout (XC3S700A,**

| Bank | XC3S700A XC3S1400A | FT256 Ball | Type |
|---|---|---|---|
| 3 | IO_L16N_3 | L2 | I/O |
| 3 | IO_L16P_3/VREF_3 | L1 | VREF |
| 3 | IO_L18N_3 | L3 | I/O |
| 3 | IO_L18P_3 | K4 | I/O |
| 3 | IO_L19N_3 | L4 | I/O |
| 3 | IO_L19P_3 | M3 | I/O |
| 3 | IO_L20N_3 | N1 | I/O |
| 3 | IO_L20P_3 | M1 | I/O |
| 3 | IO_L22N_3 | P1 | I/O |
| 3 | IO_L22P_3/VREF_3 | N2 | VREF |
| 3 | IO_L23N_3 | P2 | I/O |
| 3 | IO_L23P_3 | R1 | I/O |
| 3 | IO_L24N_3 | M4 | I/O |
| 3 | IO_L24P_3 | N3 | I/O |
| 3 | IP_3 | J4 | INPUT |
| 3 | IP_3/VREF_3 | G4 | VREF |
| 3 | IP_3/VREF_3 | J5 | VREF |
| 3 | VCCO_3 | D2 | VCCO |
| 3 | VCCO_3 | H2 | VCCO |
| 3 | VCCO_3 | M2 | VCCO |
| GND | GND | A1 | GND |
| GND | GND | A16 | GND |
| GND | GND | B11 | GND |
| GND | GND | B7 | GND |
| GND | GND | C14 | GND |
| GND | GND | C3 | GND |
| GND | GND | E10 | GND |
| GND | GND | E12 | GND |
| GND | GND | E5 | GND |
| GND | GND | F11 | GND |
| GND | GND | F2 | GND |
| GND | GND | F6 | GND |
| GND | GND | F7 | GND |
| GND | GND | F8 | GND |
| GND | GND | F9 | GND |
| GND | GND | G10 | GND |
| GND | GND | G12 | GND |
| GND | GND | G15 | GND |
| GND | GND | G5 | GND |
| GND | GND | G6 | GND |

*Table 69:* **Spartan-3A FT256 Pinout (XC3S700A,**

| Bank | XC3S700A XC3S1400A | FT256 Ball | Type |
|---|---|---|---|
| GND | GND | G8 | GND |
| GND | GND | H11 | GND |
| GND | GND | H5 | GND |
| GND | GND | H7 | GND |
| GND | GND | H9 | GND |
| GND | GND | J10 | GND |
| GND | GND | J6 | GND |
| GND | GND | J8 | GND |
| GND | GND | K11 | GND |
| GND | GND | K12 | GND |
| GND | GND | K2 | GND |
| GND | GND | K5 | GND |
| GND | GND | K7 | GND |
| GND | GND | K9 | GND |
| GND | GND | L10 | GND |
| GND | GND | L11 | GND |
| GND | GND | L15 | GND |
| GND | GND | L6 | GND |
| GND | GND | L8 | GND |
| GND | GND | M12 | GND |
| GND | GND | M5 | GND |
| GND | GND | M8 | GND |
| GND | GND | N10 | GND |
| GND | GND | N7 | GND |
| GND | GND | P14 | GND |
| GND | GND | P3 | GND |
| GND | GND | R10 | GND |
| GND | GND | R6 | GND |
| GND | GND | T1 | GND |
| GND | GND | T16 | GND |
| VCCAUX | SUSPEND | R16 | PWRMGT |
| VCCAUX | DONE | T15 | CONFIG |
| VCCAUX | PROG_B | A2 | CONFIG |
| VCCAUX | TCK | A15 | JTAG |
| VCCAUX | TDI | B1 | JTAG |
| VCCAUX | TDO | B16 | JTAG |
| VCCAUX | TMS | B2 | JTAG |
| VCCAUX | VCCAUX | D6 | VCCAUX |
| VCCAUX | VCCAUX | E11 | VCCAUX |
| VCCAUX | VCCAUX | F12 | VCCAUX |

# FT256 Footprint (XC3S200A, XC3S400A)

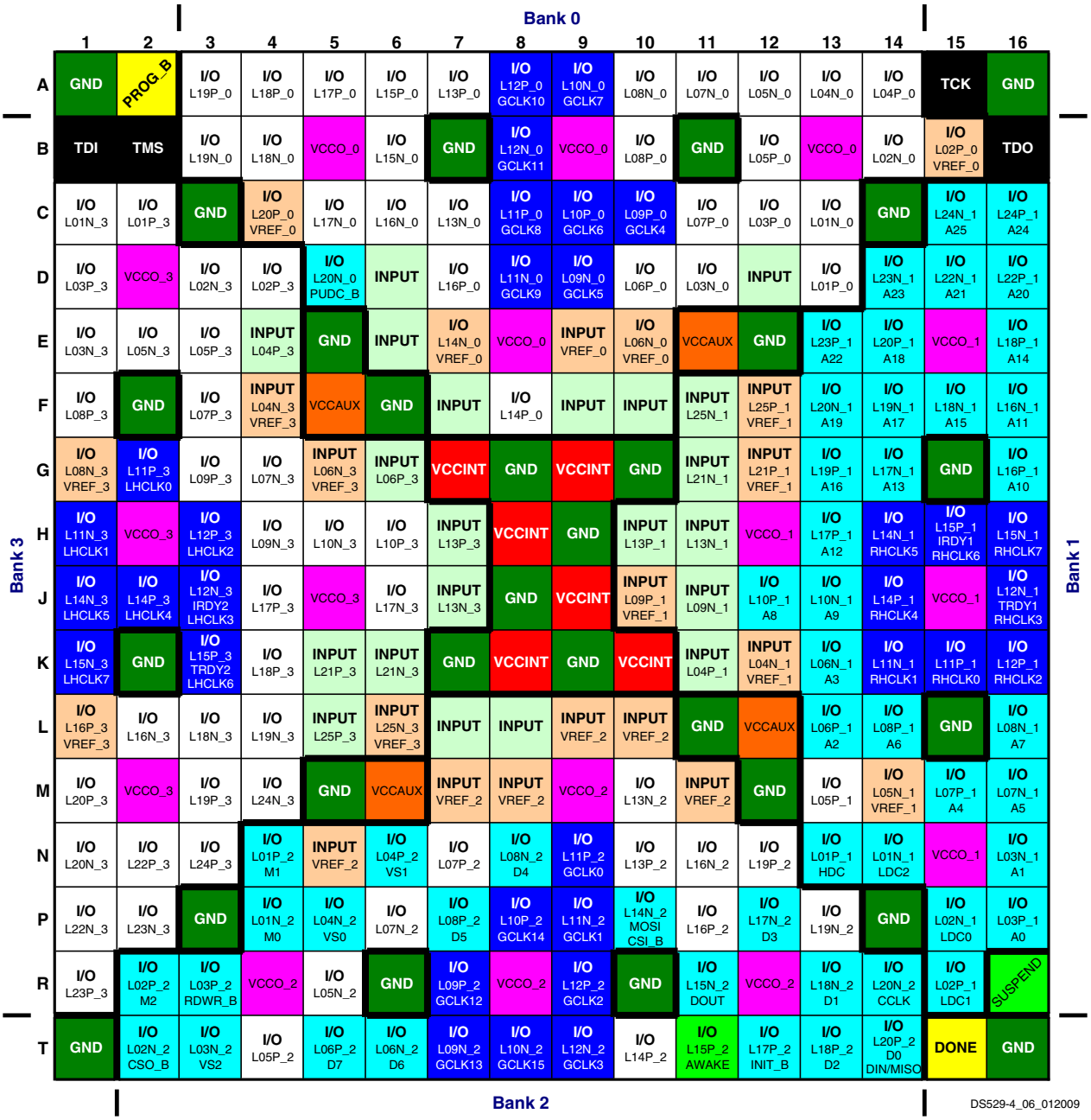


*Figure 21:* **XC3S200A and XC3S400A FT256 Package Footprint (Top View)**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 69 | **I/O:** Unrestricted, general-purpose user I/O | 51 | **DUAL:** Configuration pins, then possible user I/O | 21 | **VREF:** User I/O or input voltage reference for bank | 2 | **SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins |
| 21 | **INPUT:** Unrestricted, general-purpose input pin | 32 | **CLK:** User I/O, input, or global buffer input | 16 | **VCCO:** Output voltage supply for bank | | |
| 2 | **CONFIG:** Dedicated configuration pins | 4 | **JTAG:** Dedicated JTAG port pins | 6 | **VCCINT:** Internal core supply voltage (+1.2V) | | |
| 0 | **N.C.:** Not connected | 28 | **GND:** Ground | 4 | **VCCAUX:** Auxiliary supply voltage | | |

# FG400: 400-ball Fine-pitch Ball Grid Array

The 400-ball fine-pitch ball grid array, FG400, supports two different Spartan-3A FPGAs, the XC3S400A and the XC3S700A. Both devices share a common footprint for this package as shown in Table 81 and Figure 24.

Table 81 lists all the FG400 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

## Pinout Table

*Table 81:* **Spartan-3A FG400 Pinout**

| Bank | Pin Name | FG400 Ball | Type |
|---|---|---|---|
| 0 | IO_L01N_0 | A18 | I/O |
| 0 | IO_L01P_0 | B18 | I/O |
| 0 | IO_L02N_0 | C17 | I/O |
| 0 | IO_L02P_0/VREF_0 | D17 | VREF |
| 0 | IO_L03N_0 | E15 | I/O |
| 0 | IO_L03P_0 | D16 | I/O |
| 0 | IO_L04N_0 | A17 | I/O |
| 0 | IO_L04P_0/VREF_0 | B17 | VREF |
| 0 | IO_L05N_0 | A16 | I/O |
| 0 | IO_L05P_0 | C16 | I/O |
| 0 | IO_L06N_0 | C15 | I/O |
| 0 | IO_L06P_0 | D15 | I/O |
| 0 | IO_L07N_0 | A14 | I/O |
| 0 | IO_L07P_0 | C14 | I/O |
| 0 | IO_L08N_0 | A15 | I/O |
| 0 | IO_L08P_0 | B15 | I/O |
| 0 | IO_L09N_0 | F13 | I/O |
| 0 | IO_L09P_0 | E13 | I/O |
| 0 | IO_L10N_0/VREF_0 | C13 | VREF |
| 0 | IO_L10P_0 | D14 | I/O |
| 0 | IO_L11N_0 | C12 | I/O |
| 0 | IO_L11P_0 | B13 | I/O |
| 0 | IO_L12N_0 | F12 | I/O |
| 0 | IO_L12P_0 | D12 | I/O |
| 0 | IO_L13N_0 | A12 | I/O |

*Table 81:* **Spartan-3A FG400 Pinout *(Continued)***

| Bank | Pin Name | FG400 Ball | Type |
|---|---|---|---|
| 0 | IO_L13P_0 | B12 | I/O |
| 0 | IO_L14N_0 | C11 | I/O |
| 0 | IO_L14P_0 | B11 | I/O |
| 0 | IO_L15N_0/GCLK5 | E11 | GCLK |
| 0 | IO_L15P_0/GCLK4 | D11 | GCLK |
| 0 | IO_L16N_0/GCLK7 | C10 | GCLK |
| 0 | IO_L16P_0/GCLK6 | A10 | GCLK |
| 0 | IO_L17N_0/GCLK9 | E10 | GCLK |
| 0 | IO_L17P_0/GCLK8 | D10 | GCLK |
| 0 | IO_L18N_0/GCLK11 | A8 | GCLK |
| 0 | IO_L18P_0/GCLK10 | A9 | GCLK |
| 0 | IO_L19N_0 | C9 | I/O |
| 0 | IO_L19P_0 | B9 | I/O |
| 0 | IO_L20N_0 | C8 | I/O |
| 0 | IO_L20P_0 | B8 | I/O |
| 0 | IO_L21N_0 | D8 | I/O |
| 0 | IO_L21P_0 | C7 | I/O |
| 0 | IO_L22N_0/VREF_0 | F9 | VREF |
| 0 | IO_L22P_0 | E9 | I/O |
| 0 | IO_L23N_0 | F8 | I/O |
| 0 | IO_L23P_0 | E8 | I/O |
| 0 | IO_L24N_0 | A7 | I/O |
| 0 | IO_L24P_0 | B7 | I/O |
| 0 | IO_L25N_0 | C6 | I/O |
| 0 | IO_L25P_0 | A6 | I/O |
| 0 | IO_L26N_0 | B5 | I/O |
| 0 | IO_L26P_0 | A5 | I/O |
| 0 | IO_L27N_0 | F7 | I/O |
| 0 | IO_L27P_0 | E7 | I/O |
| 0 | IO_L28N_0 | D6 | I/O |
| 0 | IO_L28P_0 | C5 | I/O |
| 0 | IO_L29N_0 | C4 | I/O |
| 0 | IO_L29P_0 | A4 | I/O |
| 0 | IO_L30N_0 | B3 | I/O |
| 0 | IO_L30P_0 | A3 | I/O |
| 0 | IO_L31N_0 | F6 | I/O |
| 0 | IO_L31P_0 | E6 | I/O |
| 0 | IO_L32N_0/PUDC_B | B2 | DUAL |

## FG484 Footprint

### Left Half of FG484 Package (Top View)

195 **I/O:** Unrestricted, general-purpose user I/O

60-62 **INPUT:** Unrestricted, general-purpose input pin

51 **DUAL:** Configuration pins, then possible user I/O

33-34 **VREF:** User I/O or input voltage reference for bank

32 **CLK:** User I/O, input, or clock buffer input

2 **SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins

2 **CONFIG:** Dedicated configuration pins

4 **JTAG:** Dedicated JTAG port pins

53 **GND:** Ground

24 **VCCO:** Output voltage supply for bank

15 **VCCINT:** Internal core supply voltage (+1.2V)

10 **VCCAUX:** Auxiliary supply voltage

3 ◆ **N.C.:** Not connected (XC3S700A only)

**Bank 0**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | GND | I/O L36N_0 PUDC_B | I/O L33P_0 | I/O L31P_0 | I/O L28N_0 | I/O L26N_0 | I/O L26P_0 | I/O L22N_0 | I/O L22P_0 | I/O L21P_0 | I/O L18N_0 GCLK7 |
| B | I/O L02P_3 | I/O L36P_0 VREF_0 | I/O L33N_0 | I/O L31N_0 | VCCO_0 | I/O L28P_0 | GND | I/O L25P_0 | I/O L24P_0 | VCCO_0 | I/O L19P_0 GCLK8 |
| C | I/O L01P_3 | I/O L02N_3 | GND | PROG_B | I/O L32P_0 | I/O L29P_0 | I/O L27N_0 | I/O L25N_0 | I/O L24N_0 VREF_0 | I/O L21N_0 | I/O L19N_0 GCLK9 |
| D | I/O L06P_3 | I/O L01N_3 | I/O L03P_3 | TMS | I/O L32N_0 | I/O L29N_0 | I/O L27P_0 | I/O L30N_0 | GND | I/O L23P_0 | I/O L20P_0 GCLK10 |
| E | I/O L06N_3 | VCCO_3 | I/O L07N_3 | I/O L03N_3 | VCCAUX | I/O L35N_0 | I/O L34P_0 | INPUT | I/O L30P_0 | I/O L23N_0 | I/O L20N_0 GCLK11 |
| F | I/O L12N_3 | I/O L12P_3 | I/O L08P_3 | I/O L07P_3 | TDI | GND | I/O L35P_0 | I/O L34N_0 | VCCO_0 | INPUT | GND |
| G | I/O L13N_3 | GND | I/O L13P_3 | I/O L08N_3 | I/O L05N_3 | I/O L05P_3 | INPUT | INPUT VREF_0 | INPUT | INPUT | INPUT |
| H | I/O L16N_3 | I/O L16P_3 | I/O L14N_3 | I/O L14P_3 | I/O L09P_3 | I/O L09N_3 | INPUT L04N_3 VREF_3 | INPUT L04P_3 | INPUT VREF_0 | INPUT | VCCAUX |
| J | I/O L17N_3 VREF_3 | VCCO_3 | I/O L17P_3 | GND | I/O L10N_3 | VCCO_3 | INPUT L11P_3 | INPUT VREF_3 | GND | VCCINT | GND |
| K | I/O L22P_3 LHCLK2 | I/O L20N_3 | I/O L20P_3 | I/O L18N_3 | I/O L18P_3 | I/O L10P_3 | INPUT L15P_3 | INPUT L11N_3 | VCCINT | GND | VCCINT |
| L | I/O L22N_3 IRDY2 LHCLK3 | GND | I/O L21N_3 LHCLK1 | VCCAUX | I/O L21P_3 LHCLK0 | GND | INPUT L19P_3 | INPUT L15N_3 VREF_3 | GND | VCCINT | GND |
| M | I/O L24P_3 LHCLK4 | I/O L24N_3 LHCLK5 | I/O L25P_3 TRDY2 LHCLK6 | I/O L25N_3 LHCLK7 | I/O L30P_3 | INPUT L23N_3 | INPUT L23P_3 | INPUT L19N_3 | VCCINT | GND | VCCINT |
| N | I/O L26P_3 VREF_3 | VCCO_3 | I/O L26N_3 | I/O L30N_3 | INPUT L31N_3 | INPUT L31P_3 | INPUT L35P_3 | INPUT L27P_3 | INPUT L27N_3 | VCCINT | GND |
| P | I/O L28P_3 | I/O L28N_3 | I/O L29P_3 | GND | I/O L29N_3 | VCCO_3 | INPUT L39P_3 | INPUT L35N_3 | GND | GND | VCCAUX |
| R | I/O L32P_3 | I/O L32N_3 | I/O L33P_3 | I/O L33N_3 | I/O L34P_3 | INPUT VREF_3 | INPUT L46P_3 | INPUT L39N_3 | INPUT | INPUT | INPUT |
| T | I/O L36P_3 VREF_3 | GND | I/O L36N_3 | I/O L34N_3 | I/O L40P_3 | INPUT L46N_3 VREF_3 | INPUT VREF_2 | INPUT VREF_2 ◆ | INPUT | INPUT VREF_2 | INPUT VREF_2 |
| U | I/O L37P_3 | I/O L37N_3 | I/O L41P_3 | I/O L41N_3 | I/O L40N_3 | GND | INPUT ◆ | INPUT | VCCO_2 | INPUT | I/O L17P_2 GCLK12 |
| V | I/O L38P_3 | VCCO_3 | I/O L38N_3 | I/O L43P_3 | VCCAUX | I/O L01P_2 M1 | INPUT | INPUT VREF_2 | I/O L09P_2 RDWR_B | I/O L13P_2 | I/O L17N_2 GCLK13 |
| W | I/O L42P_3 | I/O L42N_3 | I/O L43N_3 | I/O L02P_2 M2 | I/O L01N_2 M0 | I/O L05P_2 | I/O L07P_2 | I/O L11P_2 VS1 | I/O L09N_2 VS2 | GND | VCCAUX |
| Y | I/O L44P_3 | I/O L44N_3 | GND | I/O L02N_2 CSO_B | I/O L05N_2 | I/O L07N_2 | I/O L10P_2 | I/O L11N_2 VS0 | I/O L14P_2 D7 | I/O L13N_2 | I/O L16P_2 D5 |
| AA | I/O L45P_3 | I/O L45N_3 | I/O L03N_2 | I/O L04N_2 | VCCO_2 | I/O L08P_2 | GND | I/O L12P_2 | VCCO_2 | I/O L15P_2 | GND |
| AB | GND | I/O L03P_2 | I/O L04P_2 | I/O L06P_2 | I/O L06N_2 | I/O L08N_2 | I/O L10N_2 | I/O L12N_2 | I/O L14N_2 D6 | I/O L15N_2 | I/O L16N_2 D4 |

**Bank 3** (rows A–AB)

**Bank 2**

DS529-4_01_101106

*Figure 25:* **FG484 Package Footprint (Top View)**

**Right Half of FG484 Package (Top View)**


**Figure 26:**

*Table 87:* **Spartan-3A FG676 Pinout*(Continued)***

| Bank | Pin Name | FG676 Ball | Type |
|---|---|---|---|
| 1 | IO_L53P_1 | L20 | I/O |
| 1 | IO_L54N_1 | F24 | I/O |
| 1 | IO_L54P_1 | F25 | I/O |
| 1 | IO_L55N_1 | L17 | I/O |
| 1 | IO_L55P_1 | L18 | I/O |
| 1 | IO_L56N_1 | F23 | I/O |
| 1 | IO_L56P_1 | E24 | I/O |
| 1 | IO_L57N_1 | K18 | I/O |
| 1 | IO_L57P_1 | K19 | I/O |
| 1 | IO_L58N_1 | G22 | I/O |
| 1 | IO_L58P_1/VREF_1 | F22 | VREF |
| 1 | IO_L59N_1 | J20 | I/O |
| 1 | IO_L59P_1 | J19 | I/O |
| 1 | IO_L60N_1 | D26 | I/O |
| 1 | IO_L60P_1 | E26 | I/O |
| 1 | IO_L61N_1 | D24 | I/O |
| 1 | IO_L61P_1 | D25 | I/O |
| 1 | IO_L62N_1/A21 | H21 | DUAL |
| 1 | IO_L62P_1/A20 | J21 | DUAL |
| 1 | IO_L63N_1/A23 | C25 | DUAL |
| 1 | IO_L63P_1/A22 | C26 | DUAL |
| 1 | IO_L64N_1/A25 | G21 | DUAL |
| 1 | IO_L64P_1/A24 | H20 | DUAL |
| 1 | IP_L16N_1 | Y26 | INPUT |
| 1 | IP_L16P_1 | W25 | INPUT |
| 1 | IP_L20N_1/VREF_1 | V26 | VREF |
| 1 | IP_L20P_1 | W26 | INPUT |
| 1 | IP_L24N_1/VREF_1 | U26 | VREF |
| 1 | IP_L24P_1 | U25 | INPUT |
| 1 | IP_L28N_1 | R24 | INPUT |
| 1 | IP_L28P_1/VREF_1 | R23 | VREF |
| 1 | IP_L32N_1 | N25 | INPUT |
| 1 | IP_L32P_1 | N26 | INPUT |
| 1 | IP_L36N_1 | N23 | INPUT |
| 1 | IP_L36P_1/VREF_1 | M24 | VREF |
| 1 | IP_L40N_1 | L23 | INPUT |
| 1 | IP_L40P_1 | K24 | INPUT |
| 1 | IP_L44N_1 | H25 | INPUT |
| 1 | IP_L44P_1/VREF_1 | H26 | VREF |
| 1 | IP_L48N_1 | H24 | INPUT |
| 1 | IP_L48P_1 | H23 | INPUT |
| 1 | IP_L52N_1/VREF_1 | G25 | VREF |
| 1 | IP_L52P_1 | G26 | INPUT |
| 1 | IP_L65N_1 | B25 | INPUT |
| 1 | IP_L65P_1/VREF_1 | B26 | VREF |
| 1 | VCCO_1 | AB25 | VCCO |
| 1 | VCCO_1 | E25 | VCCO |
| 1 | VCCO_1 | H22 | VCCO |
| 1 | VCCO_1 | L19 | VCCO |
| 1 | VCCO_1 | L25 | VCCO |
| 1 | VCCO_1 | N22 | VCCO |
| 1 | VCCO_1 | T19 | VCCO |
| 1 | VCCO_1 | T25 | VCCO |
| 1 | VCCO_1 | W22 | VCCO |
| 2 | IO_L01N_2/M0 | AD4 | DUAL |
| 2 | IO_L01P_2/M1 | AC4 | DUAL |
| 2 | IO_L02N_2/CSO_B | AA7 | DUAL |
| 2 | IO_L02P_2/M2 | Y7 | DUAL |
| 2 | IO_L05N_2 | Y9 | I/O |
| 2 | IO_L05P_2 | W9 | I/O |
| 2 | IO_L06N_2 | AF3 | I/O |
| 2 | IO_L06P_2 | AE3 | I/O |
| 2 | IO_L07N_2 | AF4 | I/O |
| 2 | IO_L07P_2 | AE4 | I/O |
| 2 | IO_L08N_2 | AD6 | I/O |
| 2 | IO_L08P_2 | AC6 | I/O |
| 2 | IO_L09N_2 | W10 | I/O |
| 2 | IO_L09P_2 | V10 | I/O |
| 2 | IO_L10N_2 | AE6 | I/O |
| 2 | IO_L10P_2 | AF5 | I/O |
| 2 | IO_L11N_2 | AE7 | I/O |
| 2 | IO_L11P_2 | AD7 | I/O |
| 2 | IO_L12N_2 | AA10 | I/O |
| 2 | IO_L12P_2 | Y10 | I/O |
| 2 | IO_L13N_2 | U11 | I/O |
| 2 | IO_L13P_2 | V11 | I/O |
| 2 | IO_L14N_2 | AB7 | I/O |
| 2 | IO_L14P_2 | AC8 | I/O |
| 2 | IO_L15N_2 | AC9 | I/O |
| 2 | IO_L15P_2 | AB9 | I/O |