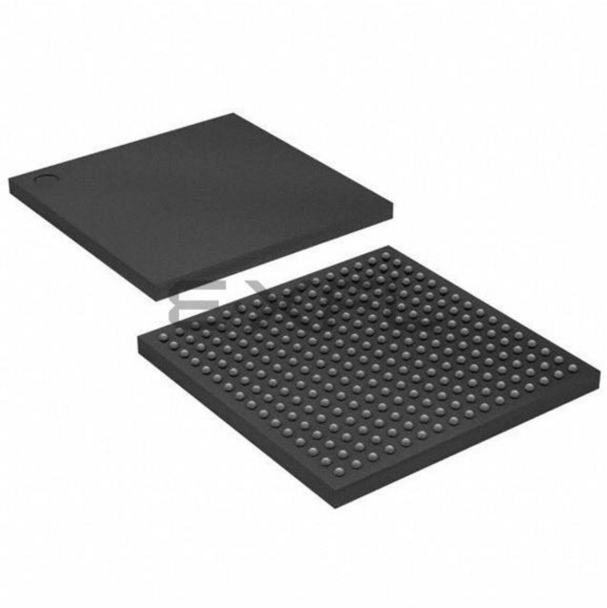

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Details	
Product Status	Active
Number of LABs/CLBs	176
Number of Logic Elements/Cells	1584
Total RAM Bits	55296
Number of I/O	144
Number of Gates	50000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s50a-4ftg256i

General Recommended Operating Conditions

Table 8: **General Recommended Operating Conditions**

Symbol	Description			Min	Nominal	Max	Units
T_J	Junction temperature	Commercial		0	–	85	°C
		Industrial		–40	–	100	°C
V_{CCINT}	Internal supply voltage			1.14	1.20	1.26	V
V_{CCO} (1)	Output driver supply voltage			1.10	–	3.60	V
V_{CCAUX}	Auxiliary supply voltage(2)	V_{CCAUX} = 2.5		2.25	2.50	2.75	V
		V_{CCAUX} = 3.3		3.00	3.30	3.60	V
V_{IN}	Input voltage(3)	PCI IOSTANDARD		–0.5	–	V_{CCO}+0.5	V
		All other IOSTANDARDs	IP or IO_#	–0.5	–	4.10	V
			IO_Lxxy_#(4)	–0.5	–	4.10	V
T_{IN}	Input signal transition time(5)			–	–	500	ns

Notes:

1. This V_{CCO} range spans the lowest and highest operating voltages for all supported I/O standards. Table 11 lists the recommended V_{CCO} range specific to each of the single-ended I/O standards, and Table 13 lists that specific to the differential standards.
2. Define V_{CCAUX} selection using CONFIG VCCAUX constraint.
3. See XAPP459, "Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins."
4. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in UG331, *Spartan-3 Generation FPGA User Guide*.
5. Measured between 10% and 90% V_{CCO}. Follow Signal Integrity recommendations.

General DC Characteristics for I/O Pins

Table 9: **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins**[1]

Symbol	Description	Test Conditions		Min	Typ	Max	Units
I_L[2]	Leakage current at User I/O, input-only, dual-purpose, and dedicated pins, FPGA powered	Driver is in a high-impedance state, V_{IN} = 0V or V_{CCO} max, sample-tested		–10	–	+10	µA
I_{HS}	Leakage current on pins during hot socketing, FPGA unpowered	All pins except INIT_B, PROG_B, DONE, and JTAG pins when PUDC_B = 1.		–10	–	+10	µA
		INIT_B, PROG_B, DONE, and JTAG pins or other pins when PUDC_B = 0.		Add I_{HS} + I_{RPU}			µA
I_{RPU}[3]	Current through pull-up resistor at User I/O, dual-purpose, input-only, and dedicated pins. Dedicated pins are powered by V_{CCAUX}.	V_{IN} = GND	V_{CCO} or V_{CCAUX} = 3.0V to 3.6V	–151	–315	–710	µA
			V_{CCO} or V_{CCAUX} = 2.3V to 2.7V	–82	–182	–437	µA
			V_{CCO} = 1.7V to 1.9V	–36	–88	–226	µA
			V_{CCO} = 1.4V to 1.6V	–22	–56	–148	µA
			V_{CCO} = 1.14V to 1.26V	–11	–31	–83	µA
R_{PU}[3]	Equivalent pull-up resistor value at User I/O, dual-purpose, input-only, and dedicated pins (based on I_{RPU} per Note 3)	V_{IN} = GND	V_{CCO} = 3.0V to 3.6V	5.1	11.4	23.9	kΩ
			V_{CCO} = 2.3V to 2.7V	6.2	14.8	33.1	kΩ
			V_{CCO} = 1.7V to 1.9V	8.4	21.6	52.6	kΩ
			V_{CCO} = 1.4V to 1.6V	10.8	28.4	74.0	kΩ
			V_{CCO} = 1.14V to 1.26V	15.3	41.1	119.4	kΩ
I_{RPD}[3]	Current through pull-down resistor at User I/O, dual-purpose, input-only, and dedicated pins. Dedicated pins are powered by V_{CCAUX}.	V_{IN} = V_{CCO}	V_{CCAUX} = 3.0V to 3.6V	167	346	659	µA
			V_{CCAUX} = 2.25V to 2.75V	100	225	457	µA
R_{PD}[3]	Equivalent pull-down resistor value at User I/O, dual-purpose, input-only, and dedicated pins (based on I_{RPD} per Note 3)	V_{CCAUX} = 3.0V to 3.6V	V_{IN} = 3.0V to 3.6V	5.5	10.4	20.8	kΩ
			V_{IN} = 2.3V to 2.7V	4.1	7.8	15.7	kΩ
			V_{IN} = 1.7V to 1.9V	3.0	5.7	11.1	kΩ
			V_{IN} = 1.4V to 1.6V	2.7	5.1	9.6	kΩ
			V_{IN} = 1.14V to 1.26V	2.4	4.5	8.1	kΩ
		V_{CCAUX} = 2.25V to 2.75V	V_{IN} = 3.0V to 3.6V	7.9	16.0	35.0	kΩ
			V_{IN} = 2.3V to 2.7V	5.9	12.0	26.3	kΩ
			V_{IN} = 1.7V to 1.9V	4.2	8.5	18.6	kΩ
			V_{IN} = 1.4V to 1.6V	3.6	7.2	15.7	kΩ
			V_{IN} = 1.14V to 1.26V	3.0	6.0	12.5	kΩ
I_{REF}	V_{REF} current per pin	All V_{CCO} levels		–10	–	+10	µA
C_{IN}	Input capacitance	–		–	–	10	pF
R_{DT}	Resistance of optional differential termination circuit within a differential I/O pair. Not available on Input-only pairs.	V_{CCO} = 3.3V ± 10%	LVDS_33, MINI_LVDS_33, RSDS_33	90	100	115	Ω
		V_{CCO} = 2.5V ± 10%	LVDS_25, MINI_LVDS_25, RSDS_25	90	110	–	Ω

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8.
2. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See "Parasitic Leakage" in UG331, *Spartan-3 Generation FPGA User Guide*.
3. This parameter is based on characterization. The pull-up resistance $R_{PU} = V_{CCO} / I_{RPU}$. The pull-down resistance $R_{PD} = V_{IN} / I_{RPD}$.

Pin-to-Pin Setup and Hold Times

Table 19: **Pin-to-Pin Setup and Hold Times for the IOB Input Path (System Synchronous)**

Symbol	Description	Conditions	Device	Speed Grade -5 Min	Speed Grade -4 Min	Units
Setup Times						
T_{PSDCM}	When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0, with DCM(4)	XC3S50A	2.45	2.68	ns
			XC3S200A	2.59	2.84	ns
			XC3S400A	2.38	2.68	ns
			XC3S700A	2.38	2.57	ns
			XC3S1400A	1.91	2.17	ns
T_{PSFD}	When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 5, without DCM	XC3S50A	2.55	2.76	ns
			XC3S200A	2.32	2.76	ns
			XC3S400A	2.21	2.60	ns
			XC3S700A	2.28	2.63	ns
			XC3S1400A	2.33	2.41	ns
Hold Times						
T_{PHDCM}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 0, with DCM(4)	XC3S50A	-0.36	-0.36	ns
			XC3S200A	-0.52	-0.52	ns
			XC3S400A	-0.33	-0.29	ns
			XC3S700A	-0.17	-0.12	ns
			XC3S1400A	-0.07	0.00	ns
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 5, without DCM	XC3S50A	-0.63	-0.58	ns
			XC3S200A	-0.56	-0.56	ns
			XC3S400A	-0.42	-0.42	ns
			XC3S700A	-0.80	-0.75	ns
			XC3S1400A	-0.69	-0.69	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, subtract the appropriate adjustment from Table 23. If this is true of the data Input, add the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, add the appropriate Input adjustment from Table 23. If this is true of the data Input, subtract the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Table 22: **Propagation Times for the IOB Input Path*(Continued)***

Symbol	Description	Conditions	DELAY_VALUE	Device	Speed Grade -5 Max	Speed Grade -4 Max	Units
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25(2)	5	XC3S400A	3.55	4.18	ns
			6		4.34	5.03	ns
			7		5.09	5.88	ns
			8		5.58	6.42	ns
			1	XC3S700A	1.96	2.18	ns
			2		2.76	3.06	ns
			3		3.45	3.95	ns
			4		3.97	4.54	ns
			5		3.83	4.37	ns
			6		4.74	5.42	ns
			7		5.53	6.33	ns
			8		6.06	6.96	ns
			1	XC3S1400A	1.93	2.40	ns
			2		2.69	3.15	ns
			3		3.52	3.99	ns
			4		3.89	4.55	ns
			5		3.95	4.42	ns
			6		4.53	5.32	ns
			7		5.30	6.21	ns
			8		5.83	6.80	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 23.

Output Propagation Times

Table 24: **Timing for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade -5 Max	Speed Grade -4 Max	Units
Clock-to-Output Times						
T_{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OCLK input to data appearing at the Output pin	LVCMOS25[(2)], 12 mA output drive, Fast slew rate	All	2.87	3.13	ns
Propagation Times						
T_{IOOP}	The time it takes for data to travel from the IOB's O input to the Output pin	LVCMOS25[(2)], 12 mA output drive, Fast slew rate	All	2.78	2.91	ns
Set/Reset Times						
T_{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the Output pin	LVCMOS25[(2)], 12 mA output drive, Fast slew rate	All	3.63	3.89	ns
T_{IOGSRQ}	Time from asserting the Global Set Reset (GSR) input on the STARTUP_SPARTAN3A primitive to setting/resetting data at the Output pin			8.62	9.65	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 26.

Three-State Output Propagation Times

Table 25: **Timing for the IOB Three-State Path**

Symbol	Description	Conditions	Device	Speed Grade -5 Max	Speed Grade -4 Max	Units
Synchronous Output Enable/Disable Times						
T_{IOCKHZ}	Time from the active transition at the OTCLK input of the Three-state Flip-Flop (TFF) to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	0.63	0.76	ns
T_{IOCKON}[(2)]	Time from the active transition at TFF's OTCLK input to when the Output pin drives valid data		All	2.80	3.06	ns
Asynchronous Output Enable/Disable Times						
T_{GTS}	Time from asserting the Global Three State (GTS) input on the STARTUP_SPARTAN3A primitive to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	9.47	10.36	ns
Set/Reset Times						
T_{IOSRHZ}	Time from asserting TFF's SR input to when the Output pin enters a high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.61	1.86	ns
T_{IOSRON}[(2)]	Time from asserting TFF's SR input at TFF to when the Output pin drives valid data		All	3.57	3.82	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 26.

Table 29: **Recommended Number of Simultaneously Switching Outputs per VCCO-GND Pair (V_{CCAUX}=3.3V)*(Continued)***

Signal Standard (IOSTANDARD)			VQ100, TQ144 Top, Bottom (Banks 0,2)	VQ100, TQ144 Left, Right (Banks 1,3)	FT256, FG320, FG400, FG484, FG676 Top, Bottom (Banks 0,2)	FT256, FG320, FG400, FG484, FG676 Left, Right (Banks 1,3)
LVCMOS25	Slow	2	16	16	76	76
		4	10	10	46	46
		6	8	8	33	33
		8	7	7	24	24
		12	6	6	18	18
		16	–	6	–	11
		24	–	5	–	7
	Fast	2	12	12	18	18
		4	10	10	14	14
		6	8	8	6	6
		8	6	6	6	6
		12	3	3	3	3
		16	–	3	–	3
		24	–	2	–	2
	QuietIO	2	36	36	76	76
		4	30	30	60	60
		6	24	24	48	48
		8	20	20	36	36
		12	12	12	36	36
		16	–	12	–	36
		24	–	8	–	8
LVCMOS18	Slow	2	13	13	64	64
		4	8	8	34	34
		6	8	8	22	22
		8	7	7	18	18
		12	–	5	–	13
		16	–	5	–	10
	Fast	2	13	13	18	18
		4	8	8	9	9
		6	7	7	7	7
		8	4	4	4	4
		12	–	4	–	4
		16	–	3	–	3
	QuietIO	2	30	30	64	64
		4	24	24	64	64
		6	20	20	48	48
		8	16	16	36	36
		12	–	12	–	36
		16	–	12	–	24

Table 29: **Recommended Number of Simultaneously Switching Outputs per VCCO-GND Pair (V_{CCAUX}=3.3V)*(Continued)***

Signal Standard (IOSTANDARD)			VQ100, TQ144 Top, Bottom (Banks 0,2)	VQ100, TQ144 Left, Right (Banks 1,3)	FT256, FG320, FG400, FG484, FG676 Top, Bottom (Banks 0,2)	FT256, FG320, FG400, FG484, FG676 Left, Right (Banks 1,3)
LVCMOS15	Slow	2	12	12	55	55
		4	7	7	31	31
		6	7	7	18	18
		8	–	6	–	15
		12	–	5	–	10
	Fast	2	10	10	25	25
		4	7	7	10	10
		6	6	6	6	6
		8	–	4	–	4
		12	–	3	–	3
	QuietIO	2	30	30	70	70
		4	21	21	40	40
		6	18	18	31	31
		8	–	12	–	31
		12	–	12	–	20
LVCMOS12	Slow	2	17	17	40	40
		4	–	13	–	25
		6	–	10	–	18
	Fast	2	12	9	31	31
		4	–	9	–	13
		6	–	9	–	9
	QuietIO	2	36	36	55	55
		4	–	33	–	36
		6	–	27	–	36
PCI33_3			9	9	16	16
PCI66_3			–	9	–	13
HSTL_I			–	11	–	20
HSTL_III			–	7	–	8
HSTL_I_18			13	13	17	17
HSTL_II_18			–	5	–	5
HSTL_III_18			8	8	10	8
SSTL18_I			7	13	7	15
SSTL18_II			–	9	–	9
SSTL2_I			10	10	18	18
SSTL2_II			–	6	–	9
SSTL3_I			7	8	8	10
SSTL3_II			5	6	6	7

Digital Frequency Synthesizer (DFS)

Table 38: **Recommended Operating Conditions for the DFS**

Symbol		Description		Speed Grade -5 Min	-5 Max	-4 Min	-4 Max	Units
Input Frequency Ranges(2)								
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input		0.200	333(4)	0.200	333(4)	MHz
Input Clock Jitter Tolerance(3)								
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency	$F_{CLKFX} \leq 150$ MHz	–	±300	–	±300	ps
CLKIN_CYC_JITT_FX_HF			$F_{CLKFX} > 150$ MHz	–	±150	–	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input		–	±1	–	±1	ns

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 36.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.
4. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM.

Table 39: **Switching Characteristics for the DFS**

Symbol	Description		Device	Speed Grade -5 Min	-5 Max	-4 Min	-4 Max	Units
Output Frequency Ranges								
CLKOUT_FREQ_FX(2)	Frequency for the CLKFX and CLKFX180 outputs		All	5	350	5	320	MHz
Output Clock Jitter(3,4)								
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.		All	**Typ**	**Max**	**Typ**	**Max**	
		CLKIN ≤ 20 MHz		Use the Spartan-3A Jitter Calculator: www.xilinx.com/support/documentation/data_sheets/s3a_jitter_calc.zip				ps
		CLKIN > 20 MHz		±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	ps
Duty Cycle(5,6)								
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	–	±[1% of CLKFX period + 350]	–	±[1% of CLKFX period + 350]	ps
Phase Alignment(6)								
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used		All	–	±200	–	±200	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used		All	–	±[1% of CLKFX period + 200]	–	±[1% of CLKFX period + 200]	ps

Configuration Clock (CCLK) Characteristics

Table 46: **Master Mode CCLK Output Period by *ConfigRate* Opti0on Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
T_{CCLK1}	CCLK clock period by ***ConfigRate*** setting	1 *(power-on value)*	Commercial	1,254	2,500	ns
			Industrial	1,180		ns
T_{CCLK3}		3	Commercial	413	833	ns
			Industrial	390		ns
T_{CCLK6}		6 (default)	Commercial	207	417	ns
			Industrial	195		ns
T_{CCLK7}		7	Commercial	178	357	ns
			Industrial	168		ns
T_{CCLK8}		8	Commercial	156	313	ns
			Industrial	147		ns
T_{CCLK10}		10	Commercial	123	250	ns
			Industrial	116		ns
T_{CCLK12}		12	Commercial	103	208	ns
			Industrial	97		ns
T_{CCLK13}		13	Commercial	93	192	ns
			Industrial	88		ns
T_{CCLK17}		17	Commercial	72	147	ns
			Industrial	68		ns
T_{CCLK22}		22	Commercial	54	114	ns
			Industrial	51		ns
T_{CCLK25}		25	Commercial	47	100	ns
			Industrial	45		ns
T_{CCLK27}		27	Commercial	44	93	ns
			Industrial	42		ns
T_{CCLK33}		33	Commercial	36	76	ns
			Industrial	34		ns
T_{CCLK44}		44	Commercial	26	57	ns
			Industrial	25		ns
T_{CCLK50}		50	Commercial	22	50	ns
			Industrial	21		ns
$T_{CCLK100}$		100	Commercial	11.2	25	ns
			Industrial	10.6		ns

Notes:

1. Set the ***ConfigRate*** option value when generating a configuration bitstream.

Table 55: **Configuration Timing Requirements for Attached Parallel NOR BPI Flash**

Symbol	Description	Requirement	Units
T_{CE} (t_{ELQV})	Parallel NOR Flash PROM chip-select time	$T_{CE} \leq T_{INITADDR}$	ns
T_{OE} (t_{GLQV})	Parallel NOR Flash PROM output-enable time	$T_{OE} \leq T_{INITADDR}$	ns
T_{ACC} (t_{AVQV})	Parallel NOR Flash PROM read access time	$T_{ACC} \leq 50\% T_{CCLKn(min)} - T_{CCO} - T_{DCC} - PCB$	ns
T_{BYTE} (t_{FLQV}, t_{FHQV})	For x8/x16 PROMs only: BYTE# to output valid time(3)	$T_{BYTE} \leq T_{INITADDR}$	ns

Notes:

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's PUDC_B pin is High or Low.

Package Overview

Table 60 shows the six low-cost, space-saving production package styles for the Spartan-3A family.

Table 60: **Spartan-3A Family Package Options**

Package	Leads	Type	Maximum I/O	Lead Pitch (mm)	Body Area (mm)	Height (mm)	Mass[1] (g)
VQ100 / VQG100	100	Very Thin Quad Flat Pack (VQFP)	68	0.5	14 x 14	1.20	0.6
TQ144 / TQG144	144	Thin Quad Flat Pack (TQFP)	108	0.5	20 x 20	1.60	1.4
FT256 / FTG256	256	Fine-pitch Thin Ball Grid Array (FBGA)	195	1.0	17 x 17	1.55	0.9
FG320 / FGG320	320	Fine-pitch Ball Grid Array (FBGA)	251	1.0	19 x 19	2.00	1.4
FG400 / FGG400	400	Fine-pitch Ball Grid Array (FBGA)	311	1.0	21 x 21	2.43	2.2
FG484 / FGG484	484	Fine-pitch Ball Grid Array (FBGA)	375	1.0	23 x 23	2.60	2.2
FG676 / FGG676	676	Fine-pitch Ball Grid Array (FBGA)	502	1.0	27 x 27	2.60	3.4

Notes:

1. Package mass is ±10%.

Each package style is available in an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra 'G' in the package style name. For example, the standard "CS484" package becomes "CSG484" when ordered as the Pb-free option. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 61.

For additional package information, see UG112: *Device Package User Guide*.

Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx web site at the specified location in Table 61.

Material Declaration Data Sheets (MDDS) are also available on the **Xilinx web site** for each package.

Table 61: **Xilinx Package Documentation**

Package	Drawing	MDDS
VQ100	Package Drawing	PK173_VQ100
VQG100		PK130_VQG100
TQ144	Package Drawing	PK169_TQ144
TQG144		PK126_TQG144
FT256	Package Drawing	PK158_FT256
FTG256		PK115_FTG256
FG320	Package Drawing	PK152_FG320
FGG320		PK106_FGG320
FG400	Package Drawing	PK182_FG400
FGG400		PK108_FGG400
FG484	Package Drawing	PK183_FG484
FGG484		PK110_FGG484
FG676	Package Drawing	PK155_FG676
FGG676		PK111_FGG676

Table 68: **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400)** ***(Continued)***

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
2	IO_L01N_2/M0	IO_L01N_2/M0	P4	DUAL
2	IO_L01P_2/M1	IO_L01P_2/M1	N4	DUAL
2	IO_L02N_2/ CSO_B	IO_L02N_2/ CSO_B	T2	DUAL
2	IO_L02P_2/M2	IO_L02P_2/M2	R2	DUAL
2	IO_L04P_2/VS2	IO_L03N_2/VS2	T3	DUAL
2	IO_L03P_2/ RDWR_B	IO_L03P_2/ RDWR_B	R3	DUAL
2	IO_L04N_2/VS0	IO_L04N_2/VS0	P5	DUAL
2	IO_L03N_2/VS1	IO_L04P_2/VS1	N6	DUAL
2	IO_L06P_2	IO_L05N_2	R5	I/O
2	IO_L05P_2	IO_L05P_2	T4	I/O
2	IO_L06N_2/D6	IO_L06N_2/D6	T6	DUAL
2	IO_L05N_2/D7	IO_L06P_2/D7	T5	DUAL
2	N.C. (◆)	IO_L07N_2	P6	I/O
2	N.C. (◆)	IO_L07P_2	N7	I/O
2	IO_L08N_2/D4	IO_L08N_2/D4	N8	DUAL
2	IO_L08P_2/D5	IO_L08P_2/D5	P7	DUAL
2	N.C. (◆)	IO_L09N_2/ GCLK13	T7	GCLK
2	N.C. (◆)	IO_L09P_2/ GCLK12	R7	GCLK
2	IO_L10N_2/ GCLK15	IO_L10N_2/ GCLK15	T8	GCLK
2	IO_L10P_2/ GCLK14	IO_L10P_2/ GCLK14	P8	GCLK
2	IO_L11N_2/ GCLK1	IO_L11N_2/ GCLK1	P9	GCLK
2	IO_L11P_2/ GCLK0	IO_L11P_2/ GCLK0	N9	GCLK
2	IO_L12N_2/ GCLK3	IO_L12N_2/ GCLK3	T9	GCLK
2	IO_L12P_2/ GCLK2	IO_L12P_2/ GCLK2	R9	GCLK
2	N.C. (◆)	IO_L13N_2	M10	I/O
2	N.C. (◆)	IO_L13P_2	N10	I/O
2	IO_L14P_2/ MOSI/CSI_B	IO_L14N_2/ MOSI/CSI_B	P10	DUAL
2	IO_L14N_2	IO_L14P_2	T10	I/O
2	IO_L15N_2/ DOUT	IO_L15N_2/ DOUT	R11	DUAL
2	IO_L15P_2/ AWAKE	IO_L15P_2/ AWAKE	T11	PWR MGMT
2	IO_L16N_2	IO_L16N_2	N11	I/O
2	IO_L16P_2	IO_L16P_2	P11	I/O
2	IO_L17N_2/D3	IO_L17N_2/D3	P12	DUAL
2	IO_L17P_2/ INIT_B	IO_L17P_2/ INIT_B	T12	DUAL

Table 68: **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400)** ***(Continued)***

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
2	IO_L20P_2/D1	IO_L18N_2/D1	R13	DUAL
2	IO_L18P_2/D2	IO_L18P_2/D2	T13	DUAL
2	N.C. (◆)	IO_L19N_2	P13	I/O
2	N.C. (◆)	IO_L19P_2	N12	I/O
2	IO_L20N_2/ CCLK	IO_L20N_2/ CCLK	R14	DUAL
2	IO_L18N_2/D0/ DIN/MISO	IO_L20P_2/D0/ DIN/MISO	T14	DUAL
2	IP_2	IP_2	L7	INPUT
2	IP_2	IP_2	L8	INPUT
2	IP_2/VREF_2	IP_2/VREF_2	L9	VREF
2	IP_2/VREF_2	IP_2/VREF_2	L10	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M7	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M8	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M11	VREF
2	IP_2/VREF_2	IP_2/VREF_2	N5	VREF
2	VCCO_2	VCCO_2	M9	VCCO
2	VCCO_2	VCCO_2	R4	VCCO
2	VCCO_2	VCCO_2	R8	VCCO
2	VCCO_2	VCCO_2	R12	VCCO
3	IO_L01N_3	IO_L01N_3	C1	I/O
3	IO_L01P_3	IO_L01P_3	C2	I/O
3	IO_L02N_3	IO_L02N_3	D3	I/O
3	IO_L02P_3	IO_L02P_3	D4	I/O
3	IO_L03N_3	IO_L03N_3	E1	I/O
3	IO_L03P_3	IO_L03P_3	D1	I/O
3	N.C. (◆)	IO_L05N_3	E2	I/O
3	N.C. (◆)	IO_L05P_3	E3	I/O
3	N.C. (◆)	IO_L07N_3	G4	I/O
3	N.C. (◆)	IO_L07P_3	F3	I/O
3	IO_L08N_3/ VREF_3	IO_L08N_3/ VREF_3	G1	VREF
3	IO_L08P_3	IO_L08P_3	F1	I/O
3	N.C. (◆)	IO_L09N_3	H4	I/O
3	N.C. (◆)	IO_L09P_3	G3	I/O
3	N.C. (◆)	IO_L10N_3	H5	I/O
3	N.C. (◆)	IO_L10P_3	H6	I/O
3	IO_L11N_3/ LHCLK1	IO_L11N_3/ LHCLK1	H1	LHCLK
3	IO_L11P_3/ LHCLK0	IO_L11P_3/ LHCLK0	G2	LHCLK
3	IO_L12N_3/ IRDY2/LHCLK3	IO_L12N_3/ IRDY2/LHCLK3	J3	LHCLK
3	IO_L12P_3/ LHCLK2	IO_L12P_3/ LHCLK2	H3	LHCLK

Table 68: **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400)** ***(Continued)***

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
3	IO_L14N_3/ LHCLK5	IO_L14N_3/ LHCLK5	J1	LHCLK
3	IO_L14P_3/ LHCLK4	IO_L14P_3/ LHCLK4	J2	LHCLK
3	IO_L15N_3/ LHCLK7	IO_L15N_3/ LHCLK7	K1	LHCLK
3	IO_L15P_3/ TRDY2/LHCLK6	IO_L15P_3/ TRDY2/LHCLK6	K3	LHCLK
3	N.C. (◆)	IO_L16N_3	L2	I/O
3	N.C. (◆)	IO_L16P_3/ VREF_3	L1	VREF
3	N.C. (◆)	IO_L17N_3	J6	I/O
3	N.C. (◆)	IO_L17P_3	J4	I/O
3	N.C. (◆)	IO_L18N_3	L3	I/O
3	N.C. (◆)	IO_L18P_3	K4	I/O
3	N.C. (◆)	IO_L19N_3	L4	I/O
3	N.C. (◆)	IO_L19P_3	M3	I/O
3	IO_L20N_3	IO_L20N_3	N1	I/O
3	IO_L20P_3	IO_L20P_3	M1	I/O
3	IO_L22N_3	IO_L22N_3	P1	I/O
3	IO_L22P_3	IO_L22P_3	N2	I/O
3	IO_L23N_3	IO_L23N_3	P2	I/O
3	IO_L23P_3	IO_L23P_3	R1	I/O
3	IO_L24N_3	IO_L24N_3	M4	I/O
3	IO_L24P_3	IO_L24P_3	N3	I/O
3	IP_L04N_3/ VREF_3	IP_L04N_3/ VREF_3	F4	VREF
3	IP_L04P_3	IP_L04P_3	E4	INPUT
3	N.C. (◆)	IP_L06N_3/ VREF_3	G5	VREF
3	N.C. (◆)	IP_L06P_3	G6	INPUT
3	IP_L13N_3	IP_L13N_3	J7	INPUT
3	IP_L13P_3	IP_L13P_3	H7	INPUT
3	IP_L21N_3	IP_L21N_3	K6	INPUT
3	IP_L21P_3	IP_L21P_3	K5	INPUT
3	IP_L25N_3/ VREF_3	IP_L25N_3/ VREF_3	L6	VREF
3	IP_L25P_3	IP_L25P_3	L5	INPUT
3	VCCO_3	VCCO_3	D2	VCCO
3	VCCO_3	VCCO_3	H2	VCCO
3	VCCO_3	VCCO_3	J5	VCCO
3	VCCO_3	VCCO_3	M2	VCCO
GND	GND	GND	A1	GND
GND	GND	GND	A16	GND
GND	GND	GND	B7	GND

Table 68: **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400)** ***(Continued)***

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
GND	GND	GND	B11	GND
GND	GND	GND	C3	GND
GND	GND	GND	C14	GND
GND	GND	GND	E5	GND
GND	GND	GND	E12	GND
GND	GND	GND	F2	GND
GND	GND	GND	F6	GND
GND	GND	GND	G8	GND
GND	GND	GND	G10	GND
GND	GND	GND	G15	GND
GND	GND	GND	H9	GND
GND	GND	GND	J8	GND
GND	GND	GND	K2	GND
GND	GND	GND	K7	GND
GND	GND	GND	K9	GND
GND	GND	GND	L11	GND
GND	GND	GND	L15	GND
GND	GND	GND	M5	GND
GND	GND	GND	M12	GND
GND	GND	GND	P3	GND
GND	GND	GND	P14	GND
GND	GND	GND	R6	GND
GND	GND	GND	R10	GND
GND	GND	GND	T1	GND
GND	GND	GND	T16	GND
VCCAUX	SUSPEND	SUSPEND	R16	PWR MGMT
VCCAUX	DONE	DONE	T15	CONFIG
VCCAUX	PROG_B	PROG_B	A2	CONFIG
VCCAUX	TCK	TCK	A15	JTAG
VCCAUX	TDI	TDI	B1	JTAG
VCCAUX	TDO	TDO	B16	JTAG
VCCAUX	TMS	TMS	B2	JTAG
VCCAUX	VCCAUX	VCCAUX	E11	VCCAUX
VCCAUX	VCCAUX	VCCAUX	F5	VCCAUX
VCCAUX	VCCAUX	VCCAUX	L12	VCCAUX
VCCAUX	VCCAUX	VCCAUX	M6	VCCAUX
VCCINT	VCCINT	VCCINT	G7	VCCINT
VCCINT	VCCINT	VCCINT	G9	VCCINT
VCCINT	VCCINT	VCCINT	H8	VCCINT
VCCINT	VCCINT	VCCINT	J9	VCCINT

Table 69: **Spartan-3A FT256 Pinout (XC3S700A,**

Bank	XC3S700A XC3S1400A	FT256 Ball	Type
3	IO_L16N_3	L2	I/O
3	IO_L16P_3/VREF_3	L1	VREF
3	IO_L18N_3	L3	I/O
3	IO_L18P_3	K4	I/O
3	IO_L19N_3	L4	I/O
3	IO_L19P_3	M3	I/O
3	IO_L20N_3	N1	I/O
3	IO_L20P_3	M1	I/O
3	IO_L22N_3	P1	I/O
3	IO_L22P_3/VREF_3	N2	VREF
3	IO_L23N_3	P2	I/O
3	IO_L23P_3	R1	I/O
3	IO_L24N_3	M4	I/O
3	IO_L24P_3	N3	I/O
3	IP_3	J4	INPUT
3	IP_3/VREF_3	G4	VREF
3	IP_3/VREF_3	J5	VREF
3	VCCO_3	D2	VCCO
3	VCCO_3	H2	VCCO
3	VCCO_3	M2	VCCO
GND	GND	A1	GND
GND	GND	A16	GND
GND	GND	B11	GND
GND	GND	B7	GND
GND	GND	C14	GND
GND	GND	C3	GND
GND	GND	E10	GND
GND	GND	E12	GND
GND	GND	E5	GND
GND	GND	F11	GND
GND	GND	F2	GND
GND	GND	F6	GND
GND	GND	F7	GND
GND	GND	F8	GND
GND	GND	F9	GND
GND	GND	G10	GND
GND	GND	G12	GND
GND	GND	G15	GND
GND	GND	G5	GND
GND	GND	G6	GND

Table 69: **Spartan-3A FT256 Pinout (XC3S700A,**

Bank	XC3S700A XC3S1400A	FT256 Ball	Type
GND	GND	G8	GND
GND	GND	H11	GND
GND	GND	H5	GND
GND	GND	H7	GND
GND	GND	H9	GND
GND	GND	J10	GND
GND	GND	J6	GND
GND	GND	J8	GND
GND	GND	K11	GND
GND	GND	K12	GND
GND	GND	K2	GND
GND	GND	K5	GND
GND	GND	K7	GND
GND	GND	K9	GND
GND	GND	L10	GND
GND	GND	L11	GND
GND	GND	L15	GND
GND	GND	L6	GND
GND	GND	L8	GND
GND	GND	M12	GND
GND	GND	M5	GND
GND	GND	M8	GND
GND	GND	N10	GND
GND	GND	N7	GND
GND	GND	P14	GND
GND	GND	P3	GND
GND	GND	R10	GND
GND	GND	R6	GND
GND	GND	T1	GND
GND	GND	T16	GND
VCCAUX	SUSPEND	R16	PWRMGT
VCCAUX	DONE	T15	CONFIG
VCCAUX	PROG_B	A2	CONFIG
VCCAUX	TCK	A15	JTAG
VCCAUX	TDI	B1	JTAG
VCCAUX	TDO	B16	JTAG
VCCAUX	TMS	B2	JTAG
VCCAUX	VCCAUX	D6	VCCAUX
VCCAUX	VCCAUX	E11	VCCAUX
VCCAUX	VCCAUX	F12	VCCAUX

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
0	IP_0	F12	INPUT
0	IP_0	G7	INPUT
0	IP_0	G8	INPUT
0	IP_0	G9	INPUT
0	IP_0	G11	INPUT
0	IP_0/VREF_0	E10	VREF
0	VCCO_0	B5	VCCO
0	VCCO_0	B14	VCCO
0	VCCO_0	D11	VCCO
0	VCCO_0	E8	VCCO
1	IO_L01N_1/LDC2	T17	DUAL
1	IO_L01P_1/HDC	R16	DUAL
1	IO_L02N_1/LDC0	U18	DUAL
1	IO_L02P_1/LDC1	U17	DUAL
1	IO_L03N_1/A1	R17	DUAL
1	IO_L03P_1/A0	T18	DUAL
1	IO_L05N_1	N16	I/O
1	IO_L05P_1	P16	I/O
1	IO_L06N_1	M14	I/O
1	IO_L06P_1	N15	I/O
1	IO_L07N_1/VREF_1	P18	VREF
1	IO_L07P_1	R18	I/O
1	IO_L09N_1/A3	M17	DUAL
1	IO_L09P_1/A2	M16	DUAL
1	IO_L10N_1/A5	N18	DUAL
1	IO_L10P_1/A4	N17	DUAL
1	IO_L11N_1/A7	L12	DUAL
1	IO_L11P_1/A6	L13	DUAL
1	IO_L13N_1/A9	K16	DUAL
1	IO_L13P_1/A8	L17	DUAL
1	IO_L14N_1/RHCLK1	K17	RHCLK
1	IO_L14P_1/RHCLK0	L18	RHCLK
1	IO_L15N_1/TRDY1/RHCLK3	J17	RHCLK
1	IO_L15P_1/RHCLK2	K18	RHCLK
1	IO_L17N_1/RHCLK5	K15	RHCLK
1	IO_L17P_1/RHCLK4	J16	RHCLK
1	IO_L18N_1/RHCLK7	H17	RHCLK
1	IO_L18P_1/IRDY1/RHCLK6	H18	RHCLK
1	IO_L19N_1/A11	G16	DUAL
1	IO_L19P_1/A10	H16	DUAL

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
1	IO_L21N_1	F17	I/O
1	IO_L21P_1	G17	I/O
1	IO_L22N_1/A13	E18	DUAL
1	IO_L22P_1/A12	F18	DUAL
1	IO_L23N_1/A15	H15	DUAL
1	IO_L23P_1/A14	J14	DUAL
1	IO_L25N_1	D17	I/O
1	IO_L25P_1	D18	I/O
1	IO_L26N_1/A17	E16	DUAL
1	IO_L26P_1/A16	F16	DUAL
1	IO_L27N_1/A19	F15	DUAL
1	IO_L27P_1/A18	G15	DUAL
1	IO_L29N_1/A21	E15	DUAL
1	IO_L29P_1/A20	D16	DUAL
1	IO_L30N_1/A23	B18	DUAL
1	IO_L30P_1/A22	C18	DUAL
1	IO_L31N_1/A25	B17	DUAL
1	IO_L31P_1/A24	C17	DUAL
1	IP_L04N_1/VREF_1	N14	VREF
1	IP_L04P_1	P15	INPUT
1	IP_L08N_1/VREF_1	L14	VREF
1	IP_L08P_1	M13	INPUT
1	IP_L12N_1	L16	INPUT
1	IP_L12P_1/VREF_1	M15	VREF
1	IP_L16N_1	K14	INPUT
1	IP_L16P_1	K13	INPUT
1	IP_L20N_1	J13	INPUT
1	IP_L20P_1/VREF_1	K12	VREF
1	IP_L24N_1	G14	INPUT
1	IP_L24P_1	H13	INPUT
1	IP_L28N_1	G13	INPUT
1	IP_L28P_1/VREF_1	H12	VREF
1	IP_L32N_1	F13	INPUT
1	IP_L32P_1/VREF_1	F14	VREF
1	VCCO_1	E17	VCCO
1	VCCO_1	H14	VCCO
1	VCCO_1	L15	VCCO
1	VCCO_1	P17	VCCO
2	IO_L01N_2/M0	U3	DUAL
2	IO_L01P_2/M1	T3	DUAL

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
3	IO_L10N_3/VREF_3	F1	VREF
3	IO_L10P_3	F2	I/O
3	IO_L11N_3	J6	I/O
3	IO_L11P_3	J7	I/O
3	IO_L13N_3	H1	I/O
3	IO_L13P_3	H2	I/O
3	IO_L14N_3/LHCLK1	J3	LHCLK
3	IO_L14P_3/LHCLK0	H3	LHCLK
3	IO_L15N_3/IRDY2/LHCLK3	J1	LHCLK
3	IO_L15P_3/LHCLK2	J2	LHCLK
3	IO_L17N_3/LHCLK5	K5	LHCLK
3	IO_L17P_3/LHCLK4	J4	LHCLK
3	IO_L18N_3/LHCLK7	K3	LHCLK
3	IO_L18P_3/TRDY2/LHCLK6	K2	LHCLK
3	IO_L19N_3	L2	I/O
3	IO_L19P_3/VREF_3	L1	VREF
3	IO_L21N_3	M2	I/O
3	IO_L21P_3	N1	I/O
3	IO_L22N_3	N2	I/O
3	IO_L22P_3	P1	I/O
3	IO_L23N_3	L4	I/O
3	IO_L23P_3	L3	I/O
3	IO_L25N_3	R2	I/O
3	IO_L25P_3	R1	I/O
3	IO_L26N_3	N4	I/O
3	IO_L26P_3	N3	I/O
3	IO_L27N_3	T2	I/O
3	IO_L27P_3	T1	I/O
3	IO_L29N_3	N6	I/O
3	IO_L29P_3	N5	I/O
3	IO_L30N_3	R3	I/O
3	IO_L30P_3	P3	I/O
3	IO_L31N_3	U2	I/O
3	IO_L31P_3	U1	I/O
3	IP_L04N_3/VREF_3	H7	VREF
3	IP_L04P_3	G6	INPUT
3	IP_L08N_3/VREF_3	H5	VREF
3	IP_L08P_3	H6	INPUT
3	IP_L12N_3	G2	INPUT
3	IP_L12P_3	G3	INPUT

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
3	IP_L16N_3	K6	INPUT
3	IP_L16P_3	J5	INPUT
3	IP_L20N_3	L6	INPUT
3	IP_L20P_3	L7	INPUT
3	IP_L24N_3	M4	INPUT
3	IP_L24P_3	M3	INPUT
3	IP_L28N_3	M5	INPUT
3	IP_L28P_3	M6	INPUT
3	IP_L32N_3/VREF_3	P4	VREF
3	IP_L32P_3	P5	INPUT
3	VCCO_3	E2	VCCO
3	VCCO_3	H4	VCCO
3	VCCO_3	L5	VCCO
3	VCCO_3	P2	VCCO
GND	GND	A1	GND
GND	GND	A7	GND
GND	GND	A12	GND
GND	GND	A18	GND
GND	GND	C10	GND
GND	GND	D4	GND
GND	GND	D7	GND
GND	GND	D15	GND
GND	GND	F6	GND
GND	GND	G1	GND
GND	GND	G12	GND
GND	GND	G18	GND
GND	GND	H8	GND
GND	GND	H10	GND
GND	GND	J11	GND
GND	GND	J15	GND
GND	GND	K4	GND
GND	GND	K8	GND
GND	GND	L9	GND
GND	GND	L11	GND
GND	GND	M1	GND
GND	GND	M7	GND
GND	GND	M18	GND
GND	GND	N13	GND
GND	GND	R4	GND
GND	GND	R12	GND

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
GND	GND	R15	GND
GND	GND	T9	GND
GND	GND	V1	GND
GND	GND	V7	GND
GND	GND	V12	GND
GND	GND	V18	GND
VCCAUX	SUSPEND	T16	PWR MGMT
VCCAUX	DONE	V17	CONFIG
VCCAUX	PROG_B	C4	CONFIG
VCCAUX	TCK	A17	JTAG
VCCAUX	TDI	E4	JTAG
VCCAUX	TDO	E14	JTAG
VCCAUX	TMS	C3	JTAG
VCCAUX	VCCAUX	A9	VCCAUX
VCCAUX	VCCAUX	G10	VCCAUX
VCCAUX	VCCAUX	J12	VCCAUX
VCCAUX	VCCAUX	J18	VCCAUX
VCCAUX	VCCAUX	K1	VCCAUX
VCCAUX	VCCAUX	K7	VCCAUX
VCCAUX	VCCAUX	M10	VCCAUX
VCCAUX	VCCAUX	V10	VCCAUX
VCCINT	VCCINT	H9	VCCINT
VCCINT	VCCINT	H11	VCCINT
VCCINT	VCCINT	J8	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	L8	VCCINT
VCCINT	VCCINT	L10	VCCINT

Table 81: **Spartan-3A FG400 Pinout*(Continued)***

Bank	Pin Name	FG400 Ball	Type
VCCAUX	TDO	E17	JTAG
VCCAUX	TMS	E4	JTAG
VCCAUX	VCCAUX	A13	VCCAUX
VCCAUX	VCCAUX	E16	VCCAUX
VCCAUX	VCCAUX	H1	VCCAUX
VCCAUX	VCCAUX	K13	VCCAUX
VCCAUX	VCCAUX	L8	VCCAUX
VCCAUX	VCCAUX	N20	VCCAUX
VCCAUX	VCCAUX	T5	VCCAUX
VCCAUX	VCCAUX	Y8	VCCAUX
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	J12	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	N10	VCCINT

User I/Os by Bank

Table 82 indicates how the 311 available user-I/O pins are distributed between the four I/O banks on the FG400 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 82: **User I/Os Per Bank for the XC3S400A and XC3S700A in the FG400 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	77	50	12	1	6	8
Right	1	79	21	12	30	8	8
Bottom	2	76	35	6	21	6	8
Left	3	79	49	16	0	6	8
TOTAL		**311**	**155**	**46**	**52**	**26**	**32**

Footprint Migration Differences

The XC3S400A and XC3S700A FPGAs have identical footprints in the FG400 package. Designs can migrate between the XC3S400A and XC3S700A FPGAs without further consideration.

Table 83: **Spartan-3A FG484 Pinout*(Continued)***

Bank	Pin Name	FG484 Ball	Type
2	VCCO_2	AA18	VCCO
2	VCCO_2	AA5	VCCO
2	VCCO_2	AA9	VCCO
2	VCCO_2	U14	VCCO
2	VCCO_2	U9	VCCO
3	IO_L01N_3	D2	I/O
3	IO_L01P_3	C1	I/O
3	IO_L02N_3	C2	I/O
3	IO_L02P_3	B1	I/O
3	IO_L03N_3	E4	I/O
3	IO_L03P_3	D3	I/O
3	IO_L05N_3	G5	I/O
3	IO_L05P_3	G6	I/O
3	IO_L06N_3	E1	I/O
3	IO_L06P_3	D1	I/O
3	IO_L07N_3	E3	I/O
3	IO_L07P_3	F4	I/O
3	IO_L08N_3	G4	I/O
3	IO_L08P_3	F3	I/O
3	IO_L09N_3	H6	I/O
3	IO_L09P_3	H5	I/O
3	IO_L10N_3	J5	I/O
3	IO_L10P_3	K6	I/O
3	IO_L12N_3	F1	I/O
3	IO_L12P_3	F2	I/O
3	IO_L13N_3	G1	I/O
3	IO_L13P_3	G3	I/O
3	IO_L14N_3	H3	I/O
3	IO_L14P_3	H4	I/O
3	IO_L16N_3	H1	I/O
3	IO_L16P_3	H2	I/O
3	IO_L17N_3/VREF_3	J1	VREF
3	IO_L17P_3	J3	I/O
3	IO_L18N_3	K4	I/O
3	IO_L18P_3	K5	I/O
3	IO_L20N_3	K2	I/O
3	IO_L20P_3	K3	I/O
3	IO_L21N_3/LHCLK1	L3	LHCLK
3	IO_L21P_3/LHCLK0	L5	LHCLK
3	IO_L22N_3/IRDY2/LHCLK3	L1	LHCLK

Table 83: **Spartan-3A FG484 Pinout*(Continued)***

Bank	Pin Name	FG484 Ball	Type
3	IO_L22P_3/LHCLK2	K1	LHCLK
3	IO_L24N_3/LHCLK5	M2	LHCLK
3	IO_L24P_3/LHCLK4	M1	LHCLK
3	IO_L25N_3/LHCLK7	M4	LHCLK
3	IO_L25P_3/TRDY2/LHCLK6	M3	LHCLK
3	IO_L26N_3	N3	I/O
3	IO_L26P_3/VREF_3	N1	VREF
3	IO_L28N_3	P2	I/O
3	IO_L28P_3	P1	I/O
3	IO_L29N_3	P5	I/O
3	IO_L29P_3	P3	I/O
3	IO_L30N_3	N4	I/O
3	IO_L30P_3	M5	I/O
3	IO_L32N_3	R2	I/O
3	IO_L32P_3	R1	I/O
3	IO_L33N_3	R4	I/O
3	IO_L33P_3	R3	I/O
3	IO_L34N_3	T4	I/O
3	IO_L34P_3	R5	I/O
3	IO_L36N_3	T3	I/O
3	IO_L36P_3/VREF_3	T1	VREF
3	IO_L37N_3	U2	I/O
3	IO_L37P_3	U1	I/O
3	IO_L38N_3	V3	I/O
3	IO_L38P_3	V1	I/O
3	IO_L40N_3	U5	I/O
3	IO_L40P_3	T5	I/O
3	IO_L41N_3	U4	I/O
3	IO_L41P_3	U3	I/O
3	IO_L42N_3	W2	I/O
3	IO_L42P_3	W1	I/O
3	IO_L43N_3	W3	I/O
3	IO_L43P_3	V4	I/O
3	IO_L44N_3	Y2	I/O
3	IO_L44P_3	Y1	I/O
3	IO_L45N_3	AA2	I/O
3	IO_L45P_3	AA1	I/O
3	IP_3/VREF_3	J8	VREF
3	IP_3/VREF_3	R6	VREF
3	IP_L04N_3/VREF_3	H7	VREF

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
3	IP_L58P_3	AA4	INPUT
3	IP_L62N_3	AB4	INPUT
3	IP_L62P_3	AB3	INPUT
3	IP_L66N_3/VREF_3	AE2	VREF
3	IP_L66P_3	AE1	INPUT
3	VCCO_3	AB2	VCCO
3	VCCO_3	E2	VCCO
3	VCCO_3	H5	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	L8	VCCO
3	VCCO_3	P5	VCCO
3	VCCO_3	T2	VCCO
3	VCCO_3	T8	VCCO
3	VCCO_3	W5	VCCO
GND	GND	A1	GND
GND	GND	A6	GND
GND	GND	A11	GND
GND	GND	A16	GND
GND	GND	A21	GND
GND	GND	A26	GND
GND	GND	AA1	GND
GND	GND	AA6	GND
GND	GND	AA11	GND
GND	GND	AA16	GND
GND	GND	AA21	GND
GND	GND	AA26	GND
GND	GND	AD3	GND
GND	GND	AD8	GND
GND	GND	AD13	GND
GND	GND	AD18	GND
GND	GND	AD24	GND
GND	GND	AF1	GND
GND	GND	AF6	GND
GND	GND	AF11	GND
GND	GND	AF16	GND
GND	GND	AF21	GND
GND	GND	AF26	GND
GND	GND	C3	GND
GND	GND	C9	GND
GND	GND	C14	GND

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
GND	GND	C19	GND
GND	GND	C24	GND
GND	GND	F1	GND
GND	GND	F6	GND
GND	GND	F11	GND
GND	GND	F16	GND
GND	GND	F21	GND
GND	GND	F26	GND
GND	GND	H3	GND
GND	GND	H8	GND
GND	GND	H14	GND
GND	GND	H19	GND
GND	GND	J24	GND
GND	GND	K10	GND
GND	GND	K17	GND
GND	GND	L1	GND
GND	GND	L6	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L15	GND
GND	GND	L21	GND
GND	GND	L26	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M16	GND
GND	GND	N3	GND
GND	GND	N8	GND
GND	GND	N11	GND
GND	GND	N15	GND
GND	GND	P12	GND
GND	GND	P16	GND
GND	GND	P19	GND
GND	GND	P24	GND
GND	GND	R11	GND
GND	GND	R13	GND
GND	GND	R15	GND
GND	GND	T1	GND
GND	GND	T6	GND
GND	GND	T12	GND
GND	GND	T14	GND

User I/Os by Bank

Table 88 indicates how the 502 available user-I/O pins are distributed between the four I/O banks on the FG676 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 88: **User I/Os Per Bank for the XC3S1400A in the FG676 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	120	82	20	1	9	8
Right	1	130	67	15	30	10	8
Bottom	2	120	67	14	21	10	8
Left	3	132	97	18	0	9	8
TOTAL		**502**	**313**	**67**	**52**	**38**	**32**

Footprint Migration Differences

The XC3S1400A FPGA is the only Spartan-3A device offered in the FG676 package. However, Table 89 summarizes footprint and functionality differences between the XC3S1400A and the XC3SD1800A in the Spartan-3A DSP family. There are 17 unconnected balls in the XC3S1400A that become 16 input-only pins and one I/O pin in the XC3SD1800A. All other pins not listed in Table 89 unconditionally migrate between the Spartan-3A devices and the Spartan-3A DSP devices available in the FG676 package. The arrows indicate the direction for easy migration. For more details on the Spartan-3A DSP family and pinouts, and additional differences in the FG676 pinout for the XC3SD3400A device, see DS610.

Table 89: **FG676 Footprint Differences**

Pin	Bank	XC3S1400A	Migration	XC3SD1800A
A24	0	N.C.	→	INPUT
B24	0	N.C.	→	INPUT
D5	0	N.C.	→	INPUT
E6	0	N.C.	→	VREF (INPUT)
E9	0	N.C.	→	INPUT
F9	0	N.C.	→	VREF (INPUT)
F18	0	N.C.	→	INPUT
G18	0	N.C.	→	VREF (INPUT)
W18	2	N.C.	→	VREF (INPUT)
Y8	2	N.C.	→	VREF (INPUT)
Y18	2	N.C.	→	INPUT
Y19	2	N.C.	→	INPUT
AA8	2	N.C.	→	INPUT
AC5	2	N.C.	→	INPUT
AC22	2	N.C.	→	I/O
AD5	2	N.C.	→	INPUT
AD23	2	N.C.	→	VREF(INPUT)
DIFFERENCES			**17**	

Legend:

→ This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction is possible depending on how the pin is configured for the device on the right.