AMD Xilinx - XC3S50A-4VQ100I Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	176
Number of Logic Elements/Cells	1584
Total RAM Bits	55296
Number of I/O	68
Number of Gates	50000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s50a-4vq100i

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

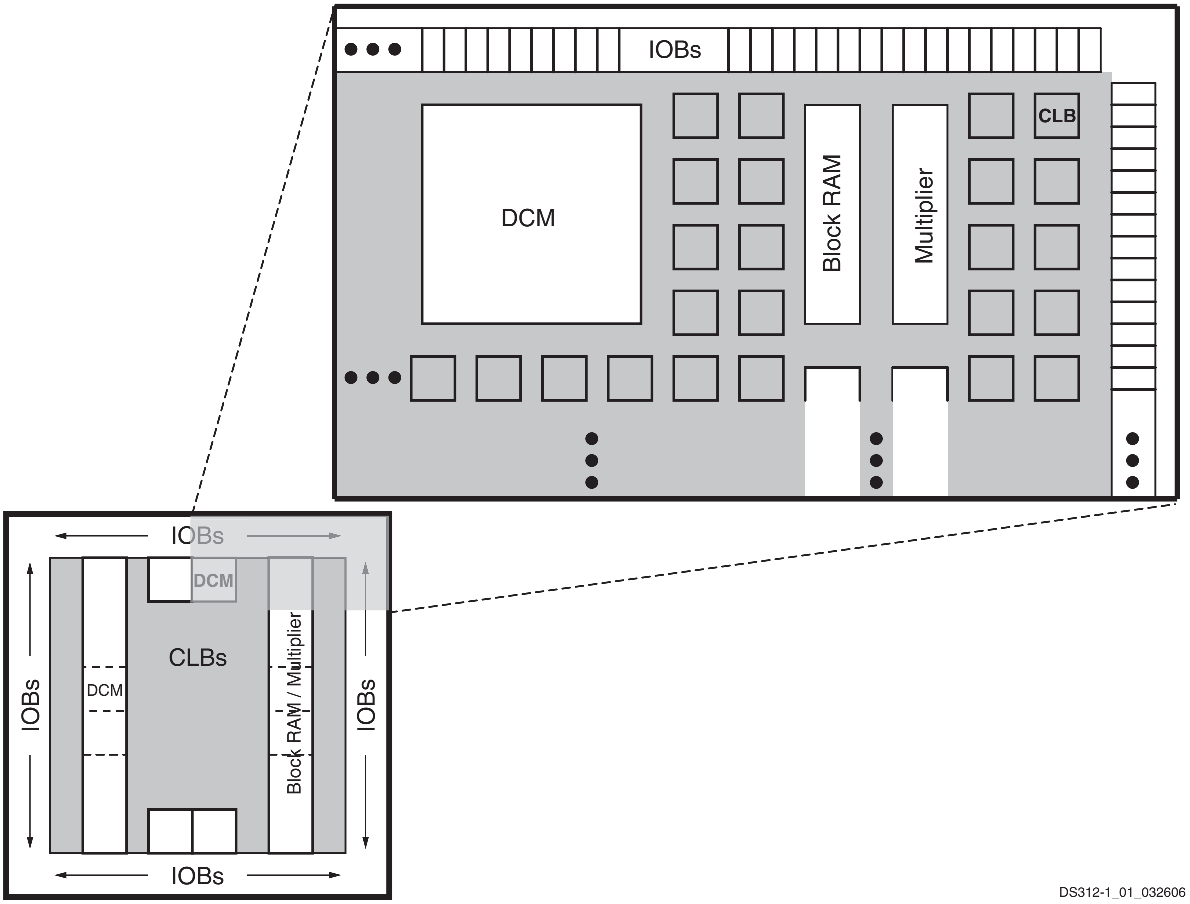
Architectural Overview

The Spartan-3A family architecture consists of five fundamental programmable functional elements:

- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. IOBs support bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including several high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A dual ring of staggered IOBs surrounds a regular array of CLBs. Each device has two columns of block RAM except for the XC3S50A, which has one column. Each RAM column consists of several 18-Kbit RAM blocks. Each block RAM is associated with a dedicated multiplier. The DCMs are positioned in the center with two at the top and two at the bottom of the device. The XC3S50A has DCMs only at the top, while the XC3S700A and XC3S1400A add two DCMs in the middle of the two columns of block RAM and multipliers.

The Spartan-3A family features a rich network of routing that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



Notes:

1. The XC3S700A and XC3S1400A have two additional DCMs on both the left and right sides as indicated by the dashed lines. The XC3S50A has only two DCMs at the top and only one Block RAM/Multiplier column.

Figure 1: **Spartan-3A FPGA Architecture**

Production Status

Table 3 indicates the production status of each Spartan-3A FPGA by temperature range and speed grade. The table also lists the earliest speed file version required for creating a production configuration bitstream. Later versions are also supported.

Table 3: **Spartan-3A FPGA Production Status (Production Speed File)**

Temperature Range		**Commercial (C)**		**Industrial**
Speed Grade		**Standard (–4)**	**High-Performance (–5)**	**Standard (–4)**
Part Number	**XC3S50A**	**Production** (v1.35)	**Production** (v1.35)	**Production** (v1.35)
	XC3S200A	**Production** (v1.35)	**Production** (v1.35)	**Production** (v1.35)
	XC3S400A	**Production** (v1.36)	**Production** (v1.36)	**Production** (v1.36)
	XC3S700A	**Production** (v1.34)	**Production** (v1.35)	**Production** (v1.34)
	XC3S1400A	**Production** (v1.34)	**Production** (v1.35)	**Production** (v1.34)

Package Marking

Figure 2 provides a top marking example for Spartan-3A FPGAs in the quad-flat packages. Figure 3 shows the top marking for Spartan-3A FPGAs in BGA packages. The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator.

The "`5C`" and "`4I`" Speed Grade/Temperature Range part combinations may be dual marked as "`5C/4I`". Devices with a single mark are only guaranteed for the marked speed grade and temperature range.

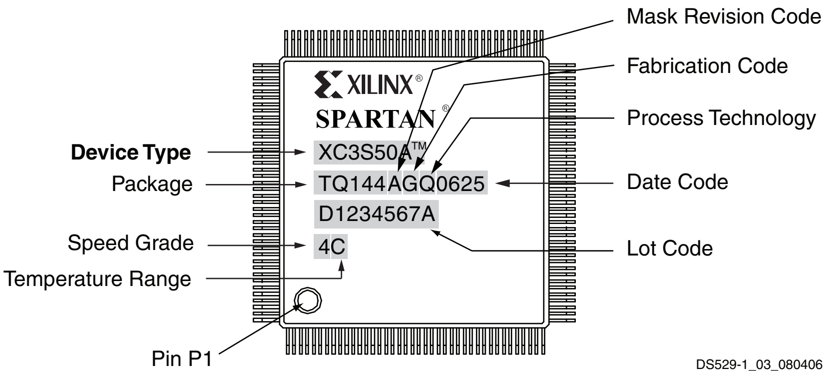


Figure 2: **Spartan-3A QFP Package Marking Example**

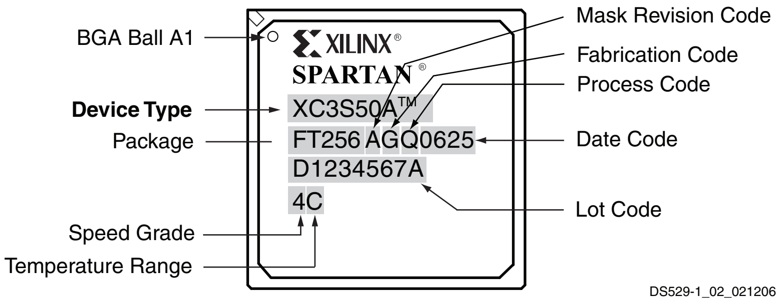
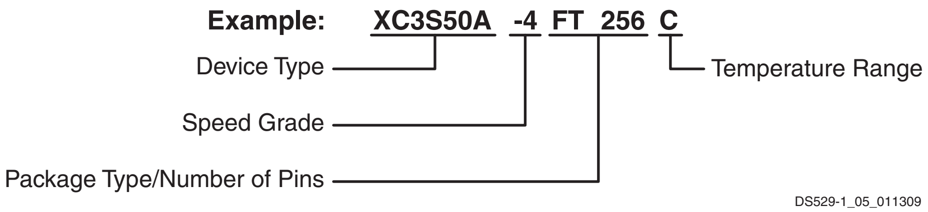


Figure 3: **Spartan-3A BGA Package Marking Example**

Ordering Information

Spartan-3A FPGAs are available in both standard and Pb-free packaging options for all device/package combinations. The Pb-free packages include a ‘G’ character in the ordering code.



Device
XC3S50A
XC3S200A
XC3S400A
XC3S700A
XC3S1400A

Speed Grade	
–4	Standard Performance
–5	High Performance (Commercial only)

Package Type / Number of Pins[1]	
VQ100/ VQG100	100-pin Very Thin Quad Flat Pack (VQFP)
TQ144/ TQG144	144-pin Thin Quad Flat Pack (TQFP)
FT256/ FTG256	256-ball Fine-Pitch Thin Ball Grid Array (FTBGA)
FG320/ FGG320	320-ball Fine-Pitch Ball Grid Array (FBGA)
FG400/ FGG400	400-ball Fine-Pitch Ball Grid Array (FBGA)
FG484/ FGG484	484-ball Fine-Pitch Ball Grid Array (FBGA)
FG676 FGG676	676-ball Fine-Pitch Ball Grid Array (FBGA)

Temperature Range (T_J)	
C	Commercial (0°C to 85°C)
I	Industrial (–40°C to 100°C)

Notes:

1. See Table 2 for specific device/package combinations.
2. See DS681 for the XA Automotive Spartan-3A FPGAs.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/05/06	1.0	Initial release.
02/02/07	1.1	Promoted to Preliminary status. Updated maximum differential I/O count for XC3S50A in Table 1. Updated differential input-only pin counts in Table 2.
03/16/07	1.2	Minor formatting updates.
04/23/07	1.3	Added "Production Status" section.
05/08/07	1.4	Updated XC3S400A to Production.
07/10/07	1.4.1	Minor updates.
04/15/08	1.6	Added VQ100 for XC3S50A and XC3S200A and extended FT256 to XC3S700A and XC3S1400A Added reference to SCD 4103 for 750 Mbps performance.
05/28/08	1.7	Added reference to XA Automotive version.
03/06/09	1.8	Simplified Ordering Information. Added references to Extended Spartan-3A Family. Removed reference to SCD 4103.
08/19/10	2.0	Updated Table 2 to clarify TQ/VQ size.

Table 20: **Setup and Hold Times for the IOB Input Path*(Continued)***

Symbol	Description	Conditions	IFD_ DELAY_ VALUE	Device	Speed Grade		Units
					-5	-4	
					Min	Min	
$T_{IOICKPD}$	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25[3]	1	XC3S400A	–1.12	–1.12	ns
			2		–1.70	–1.70	ns
			3		–2.08	–2.08	ns
			4		–2.38	–2.38	ns
			5		–2.23	–2.23	ns
			6		–2.69	–2.69	ns
			7		–3.08	–3.08	ns
			8		–3.35	–3.35	ns
			1	XC3S700A	–1.67	–1.67	ns
			2		–2.27	–2.27	ns
			3		–2.59	–2.59	ns
			4		–2.92	–2.92	ns
			5		–2.89	–2.89	ns
			6		–3.22	–3.22	ns
			7		–3.52	–3.52	ns
			8		–3.81	–3.81	ns
			1	XC3S1400A	–1.60	–1.60	ns
			2		–2.06	–2.06	ns
			3		–2.46	–2.46	ns
			4		–2.86	–2.86	ns
			5		–2.88	–2.88	ns
			6		–3.24	–3.24	ns
			7		–3.55	–3.55	ns
			8		–3.89	–3.89	ns
Set/Reset Pulse Width							
T_{RPW_IOB}	Minimum pulse width to SR control input on IOB	-	-	All	1.33	1.61	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 23.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 23. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 21: **Sample Window (Source Synchronous)**

Symbol	Description	Max	Units
T_{SAMP}	Setup and hold capture window of an IOB flip-flop.	The input capture sample window value is highly specific to a particular application, device, package, I/O standard, I/O placement, DCM usage, and clock buffer. Please consult the appropriate Xilinx Answer Record for application-specific values. • Answer Record 30879	ps

Output Propagation Times

Table 24: **Timing for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade -5 Max	Speed Grade -4 Max	Units
Clock-to-Output Times						
T_{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OCLK input to data appearing at the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	All	2.87	3.13	ns
Propagation Times						
T_{IOOP}	The time it takes for data to travel from the IOB's O input to the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	All	2.78	2.91	ns
Set/Reset Times						
T_{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	All	3.63	3.89	ns
T_{IOGSRQ}	Time from asserting the Global Set Reset (GSR) input on the STARTUP_SPARTAN3A primitive to setting/resetting data at the Output pin			8.62	9.65	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 26.

Three-State Output Propagation Times

Table 25: **Timing for the IOB Three-State Path**

Symbol	Description	Conditions	Device	Speed Grade -5 Max	Speed Grade -4 Max	Units
Synchronous Output Enable/Disable Times						
T_{IOCKHZ}	Time from the active transition at the OTCLK input of the Three-state Flip-Flop (TFF) to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	0.63	0.76	ns
T_{IOCKON}(2)	Time from the active transition at TFF's OTCLK input to when the Output pin drives valid data		All	2.80	3.06	ns
Asynchronous Output Enable/Disable Times						
T_{GTS}	Time from asserting the Global Three State (GTS) input on the STARTUP_SPARTAN3A primitive to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	9.47	10.36	ns
Set/Reset Times						
T_{IOSRHZ}	Time from asserting TFF's SR input to when the Output pin enters a high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.61	1.86	ns
T_{IOSRON}(2)	Time from asserting TFF's SR input at TFF to when the Output pin drives valid data		All	3.57	3.82	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 26.

Table 29: **Recommended Number of Simultaneously Switching Outputs per VCCO-GND Pair (V_{CCAUX}=3.3V)*(Continued)***

Signal Standard (IOSTANDARD)	Package Type			
	VQ100, TQ144		FT256, FG320, FG400, FG484, FG676	
	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)
Differential Standards (Number of I/O *Pairs* or Channels)				
LVDS_25	8	–	22	–
LVDS_33	8	–	27	–
BLVDS_25	1	1	4	4
MINI_LVDS_25	8	–	22	–
MINI_LVDS_33	8	–	27	–
LVPECL_25	Input Only			
LVPECL_33	Input Only			
RSDS_25	8	–	22	–
RSDS_33	8	–	27	–
TMDS_33	8	–	27	–
PPDS_25	8	–	22	–
PPDS_33	8	–	27	–
DIFF_HSTL_I	–	5	–	10
DIFF_HSTL_III	–	3	–	4
DIFF_HSTL_I_18	6	6	8	8
DIFF_HSTL_II_18	–	2	–	2
DIFF_HSTL_III_18	4	4	5	4
DIFF_SSTL18_I	3	6	3	7
DIFF_SSTL18_II	–	4	–	4
DIFF_SSTL2_I	5	5	9	9
DIFF_SSTL2_II	–	3	–	4
DIFF_SSTL3_I	3	4	4	5
DIFF_SSTL3_II	2	3	3	3

Notes:

1. Not all I/O standards are supported on all I/O banks. The left and right banks (I/O banks 1 and 3) support higher output drive current than the top and bottom banks (I/O banks 0 and 2). Similarly, true differential output standards, such as LVDS, RSDS, PPDS, miniLVDS, and TMDS, are only supported in top or bottom banks (I/O banks 0 and 2). Refer to UG331: *Spartan-3 Generation FPGA User Guide* for additional information.
2. The numbers in this table are recommendations that assume sound board lay out practice. Test limits are the V_{IL}/V_{IH} voltage limits for the respective I/O standard.
3. If more than one signal standard is assigned to the I/Os of a given bank, refer to XAPP689: *Managing Ground Bounce in Large FPGAs* for information on how to perform weighted average SSO calculations.

Configurable Logic Block (CLB) Timing

Table 30: **CLB (SLICEM) Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{CKO}	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	–	0.60	–	0.68	ns
Setup Times						
T_{AS}	Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB	0.18	–	0.36	–	ns
T_{DICK}	Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB	1.58	–	1.88	–	ns
Hold Times						
T_{AH}	Time from the active transition at the CLK input to the point where data is last held at the F or G input	0	–	0	–	ns
T_{CKDI}	Time from the active transition at the CLK input to the point where data is last held at the BX or BY input	0	–	0	–	ns
Clock Timing						
T_{CH}	The High pulse width of the CLB's CLK signal	0.63	–	0.75	–	ns
T_{CL}	The Low pulse width of the CLK signal	0.63	–	0.75	–	ns
F_{TOG}	Toggle frequency (for export control)	0	770	0	667	MHz
Propagation Times						
T_{ILO}	The time it takes for data to travel from the CLB's F (G) input to the X (Y) output	–	0.62	–	0.71	ns
Set/Reset Pulse Width						
T_{RPW_CLB}	The minimum allowable pulse width, High or Low, to the CLB's SR input	1.33	–	1.61	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.

Table 31: CLB Distributed RAM Switching Characteristics

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output	–	1.69	–	2.01	ns
Setup Times						
T_{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	–0.07	–	–0.02	–	ns
T_{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.18	–	0.36	–	ns
T_{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.30	–	0.59	–	ns
Hold Times						
T_{DH}	Hold time of the BX and BY data inputs after the active transition at the CLK input of the distributed RAM	0.13	–	0.13	–	ns
T_{AH}, T_{WH}	Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM	0.01	–	0.01	–	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.88	–	1.01	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.

Table 32: CLB Shift Register Switching Characteristics

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{REG}	Time from the active edge at the CLK input to data appearing on the shift register output	–	4.11	–	4.82	ns
Setup Times						
T_{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.13	–	0.18	–	ns
Hold Times						
T_{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0.16	–	0.16	–	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.90	–	1.01	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.

Byte Peripheral Interface (BPI) Configuration Timing

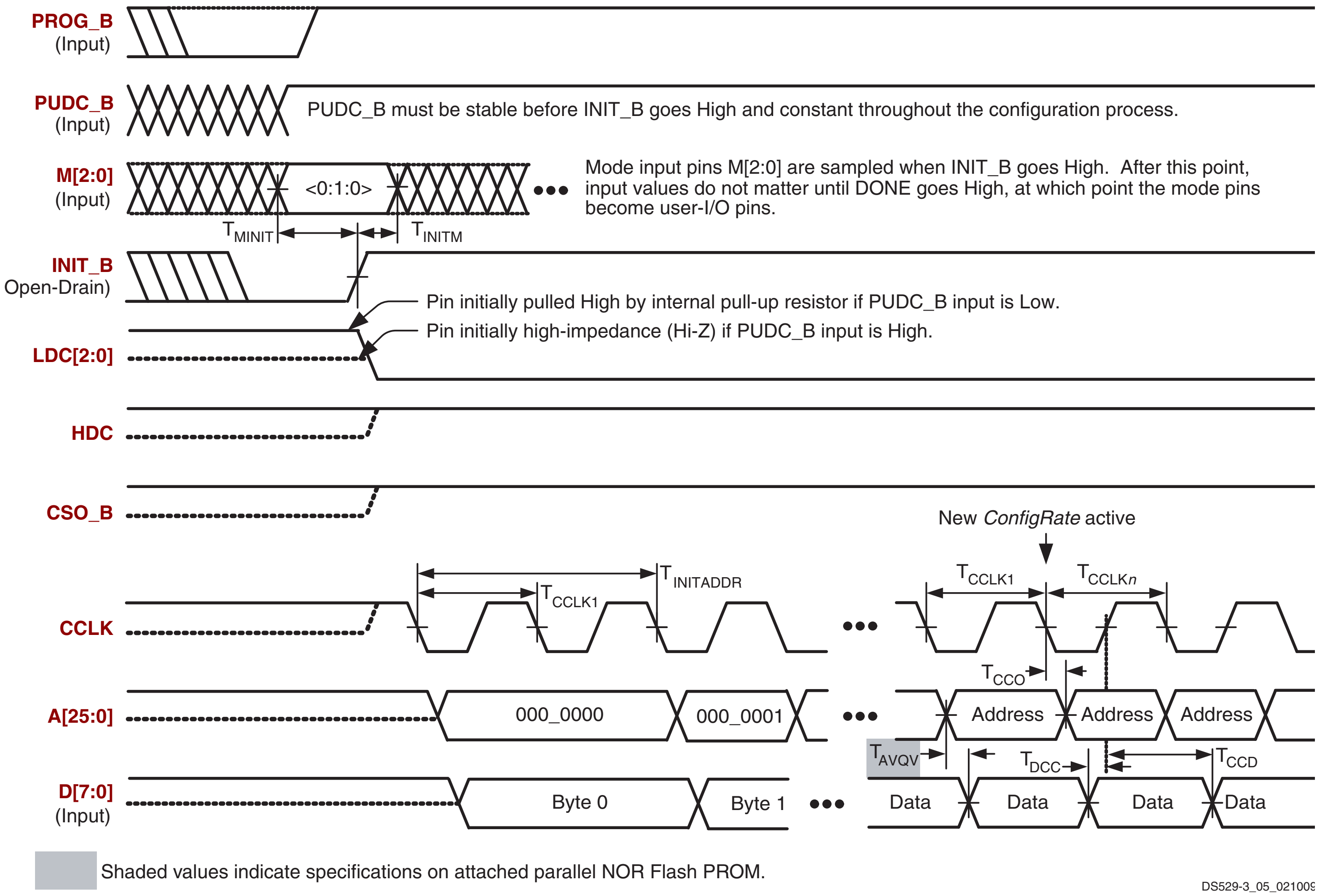


Figure 15: **Waveforms for Byte-wide Peripheral Interface (BPI) Configuration**

Table 54: **Timing for Byte-wide Peripheral Interface (BPI) Configuration Mode**

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	See Table 46		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting	See Table 46		
T_{MINIT}	Setup time on M[2:0] mode pins before the rising edge of INIT_B	50	–	ns
T_{INITM}	Hold time on M[2:0] mode pins after the rising edge of INIT_B	0	–	ns
$T_{INITADDR}$	Minimum period of initial A[25:0] address cycle; LDC[2:0] and HDC are asserted and valid	5	5	T_{CCLK1} cycles
T_{CCO}	Address A[25:0] outputs valid after CCLK falling edge	See Table 50		
T_{DCC}	Setup time on D[7:0] data inputs before CCLK rising edge	See T_{SMDCC} in Table 51		
T_{CCD}	Hold time on D[7:0] data inputs after CCLK rising edge	0	–	ns

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/05/06	1.0	Initial release.
02/02/07	1.1	Promoted to Preliminary status. Moved Table 15 to under "DC Electrical Characteristics" section. Updated all timing specifications for the v1.32 speed files. Added recommended Simultaneous Switching Output (SSO) limits in Table 29. Set a 10 µs maximum pulse width for the DNA_PORT READ signal and the JTAG clock input during the ISC_DNA command, affecting both Table 43 and Table 56. Described "External Termination Requirements for Differential I/O." Added separate DIN hold time for Slave mode in Table 50. Corrected wording in Table 52 and Table 54; no specifications affected.
03/16/07	1.2	Updated all AC timing specifications to the v1.34 speeds file. Promoted the XC3S700A and XC3S1400A FPGAs offered in the -4 speed grade to Production status, as shown in Table 16. Added Note 2 to Table 39 regarding the extra logic (one LUT) automatically added by ISE 9.1i and later software revisions for any DCM application that leverages the Digital Frequency Synthesizer (DFS). Separated some JTAG specifications by array size or function, as shown in Table 56. Updated quiescent current limits in Table 10.
04/23/07	1.3	Updated all AC timing specifications to the v1.35 speeds file. Promoted all devices except the XC3S400A to Production status, as shown in Table 16.
05/08/07	1.4	Updated XC3S400A to Production and v1.36 speeds file. Added banking rules and other explanatory footnotes to Table 12 and Table 13. Corrected DIFF_SSTL3_II V_{OL} Max in Table 14. Improved XC3S400A Pin-to-Pin Clock-to-Output times in Table 18. Updated XC3S400A Pin-to-Pin Setup Times in Table 19. Updated TIOICKPD for -5 in Table 20. Added SSO numbers to Table 28 and Table 29. Removed invalid Embedded Multiplier Hold Times in Table 34. Improved CLKOUT_FREQ_CLK90 in Table 37. Improved T_{TDITCK} and F_{TCK} performance for XC3S400A in Table 56.
07/10/07	1.5	Added DIFF_HSTL_I and DIFF_HSTL_III to Table 13, Table 14, Table 27, and Table 29. Updated TMDS DC characteristics in Table 14. Updated for speed file v1.37 in ISE 9.2.01i as shown in Table 17. Updated pin-to-pin setup and hold times in Table 19. Updated TMDS output adjustment in Table 26. Updated I/O Test Method values in Table 27. Added BLVDS SSO numbers inTable 29. For Multiplier block, updated setup times and added hold times to Table 34. Updated block RAM clock width in Table 35. Updated CLKOUT_PER_JITT_2X and CLKOUT_PER_JITT_DV2 in Table 37. Added CCLK specifications for Commercial in Table 46 through Table 48.
04/15/08	1.6	Added V_{IN} to Recommended Operating Conditions in Table 8 and added reference to XAPP459, “Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins.” Reduced typical I_{CCINTQ} and I_{CCAUXQ} quiescent current values by 12%-58% in Table 10. Increased V_{IL} max to 0.4V for LVCMOS12/15/18 and improved V_{IH} min to 0.7V for LVCMOS12 in Table 11. Changed V_{OL} max to 0.4V and V_{OH} min to V_{CCO}-0.4V for LVCMOS15/18 in Table 12. Noted latest speed file v1.39 in ISE 10.1 software in Table 16. Added new packages to SSO limits in Table 28 and Table 29. Improved SSTL18_II SSO limit for FG packages in Table 29. Improved F_{BUFG} for -4 to 334 MHz in Table 33. Added references to 375 MHz performance via SCD 4103 in Table 33,Table 38, Table 39, and Table 40. Restored Units column to Table 44. Updated CCLK output maximum period in Table 46 to match minimum frequency in Table 47. Corrected BPI active clock edge in Figure 15 and Table 54.
05/28/08	1.7	Improved V_{CCAUXT} and V_{CCO2T} POR minimum in Table 5 and updated V_{CCO} POR levels in Figure 11. Clarified recommended V_{IN} in Table 8. Added reference to V_{CCAUX} in "Simultaneously Switching Output Guidelines". Added reference to Sample Window in Table 21. Removed DNA_RETENTION limit of 10 years in Table 15 since number of Read cycles is the only unique limit. Added references to UG332.
03/06/09	1.8	Changed typical quiescent current temperature from ambient to junction. Updated BPI configuration waveforms in Figure 15 and updated Table 55. Updated selected I/O standard DC characteristics. Added TIOPI and TIOPID in Table 22. Removed references to SCD 4103.
08/19/10	2.0	Added I_{IK} to Table 4. Updated V_{IN} in Table 8 and footnoted I_L in Table 9 to note potential leakage between pins of a differential pair. Clarified LVPECL notes to Table 13. Corrected symbols for TSUSPEND_GTS and TSUSPEND_GWE in Table 44.

Spartan-3A FPGA Family: Pinout Descriptions

DS529-4 (v2.0) August 19, 2010 **Product Specification**

Introduction

This section describes how the various pins on a Spartan®-3A FPGA connect within the supported component packages, and provides device-specific thermal characteristics. For general information on the pin functions and the package characteristics, see the Packaging section of UG331: *Spartan-3 Generation FPGA User Guide*.

- **UG331: Spartan-3 Generation FPGA User Guide** www.xilinx.com/support/documentation/user_guides/ug331.pdf

Spartan-3A FPGAs are available in both standard and Pb-free, RoHS versions of each package, with the Pb-free version adding a "G" to the middle of the package code.

Except for the thermal characteristics, all information for the standard package applies equally to the Pb-free package.

Pin Types

Most pins on a Spartan-3A FPGA are general-purpose, user-defined I/O pins. There are, however, up to 12 different functional types of pins on Spartan-3A FPGA packages, as outlined in Table 57. In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Table 57: **Types of Pins on Spartan-3A FPGAs**

Type / Color Code	Description	Pin Name(s) in Type
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO_# IO_Lxxy_#
INPUT	Unrestricted, general-purpose input-only pin. This pin does not have an output structure, differential termination resistor, or PCI clamp diode.	IP_# IP_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. See UG332: *Spartan-3 Generation Configuration User Guide* for additional information on these signals.	M[2:0] PUDC_B CCLK MOSI/CSI_B D[7:1] D0/DIN DOUT CSO_B RDWR_B INIT_B A[25:0] VS[2:0] LDC[2:0] HDC
VREF	Dual-purpose pin that is either a user-I/O pin or Input-only pin, or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected.	IP/VREF_# IP_Lxxy_#/VREF_# IO/VREF_# IO_Lxxy_#/VREF_#
CLK	Either a user-I/O pin or an input to a specific clock buffer driver. Most packages have 16 global clock inputs that optionally clock the entire device. The exceptions are the TQ144 and the XC3S50A in the FT256 package). The RHCLK inputs optionally clock the right half of the device. The LHCLK inputs optionally clock the left half of the device. See the Using Global Clock Resources chapter in UG331: *Spartan-3 Generation FPGA User Guide* for additional information on these signals.	IO_Lxxy_#/GCLK[15:0], IO_Lxxy_#/LHCLK[7:0], IO_Lxxy_#/RHCLK[7:0]
CONFIG	Dedicated configuration pin, two per device. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See the UG332: *Spartan-3 Generation Configuration User Guide* for additional information on the DONE and PROG_B signals.	DONE, PROG_B

VQ100 Footprint (XC3S50A)

Note pin 1 indicator in top-left corner and logo orientation.

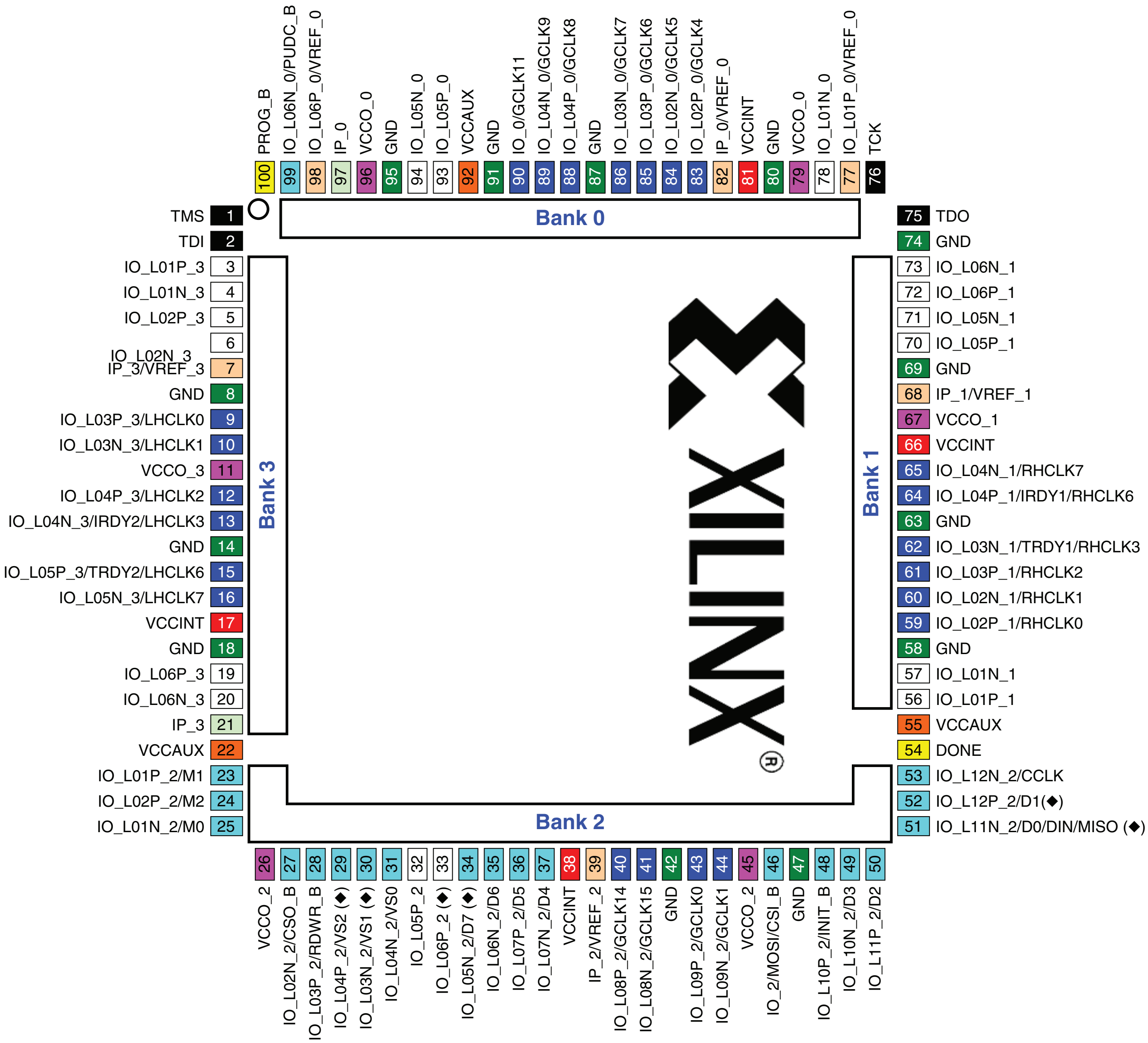


Figure 17: **VQ100 Package Footprint - XC3S50A (Top View)**

17	**I/O:** Unrestricted, general-purpose user I/O	20	**DUAL:** Configuration pins, then possible user I/O	6	**VREF:** User I/O or input voltage reference for bank
2	**INPUT:** Unrestricted, general-purpose input pin	23	**CLK:** User I/O, input, or global buffer input	6	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core supply voltage (+1.2V)
0	**N.C.:** Not connected	13	**GND:** Ground	3	**VCCAUX:** Auxiliary supply voltage

TQ144: 144-lead Thin Quad Flat Package

The XC3S50A is available in the 144-lead thin quad flat package, TQ144.

Table 66 lists all the package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The XC3S50A does not support the address output pins for the Byte-wide Peripheral Interface (BPI) configuration mode.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

> www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 66: **Spartan-3A TQ144 Pinout**

Bank	Pin Name	Pin	Type
0	IO_0	P142	I/O
0	IO_L01N_0	P111	I/O
0	IO_L01P_0	P110	I/O
0	IO_L02N_0	P113	I/O
0	IO_L02P_0/VREF_0	P112	VREF
0	IO_L03N_0	P117	I/O
0	IO_L03P_0	P115	I/O
0	IO_L04N_0	P116	I/O
0	IO_L04P_0	P114	I/O
0	IO_L05N_0	P121	I/O
0	IO_L05P_0	P120	I/O
0	IO_L06N_0/GCLK5	P126	GCLK
0	IO_L06P_0/GCLK4	P124	GCLK
0	IO_L07N_0/GCLK7	P127	GCLK
0	IO_L07P_0/GCLK6	P125	GCLK
0	IO_L08N_0/GCLK9	P131	GCLK
0	IO_L08P_0/GCLK8	P129	GCLK
0	IO_L09N_0/GCLK11	P132	GCLK
0	IO_L09P_0/GCLK10	P130	GCLK
0	IO_L10N_0	P135	I/O
0	IO_L10P_0	P134	I/O
0	IO_L11N_0	P139	I/O
0	IO_L11P_0	P138	I/O
0	IO_L12N_0/PUDC_B	P143	DUAL
0	IO_L12P_0/VREF_0	P141	VREF
0	IP_0	P140	INPUT
0	IP_0/VREF_0	P123	VREF
0	VCCO_0	P119	VCCO
0	VCCO_0	P136	VCCO
1	IO_1	P79	I/O
1	IO_L01N_1/LDC2	P78	DUAL
1	IO_L01P_1/HDC	P76	DUAL
1	IO_L02N_1/LDC0	P77	DUAL
1	IO_L02P_1/LDC1	P75	DUAL
1	IO_L03N_1	P84	I/O
1	IO_L03P_1	P82	I/O
1	IO_L04N_1/RHCLK1	P85	RHCLK
1	IO_L04P_1/RHCLK0	P83	RHCLK
1	IO_L05N_1/TRDY1/RHCLK3	P88	RHCLK
1	IO_L05P_1/RHCLK2	P87	RHCLK
1	IO_L06N_1/RHCLK5	P92	RHCLK
1	IO_L06P_1/RHCLK4	P90	RHCLK
1	IO_L07N_1/RHCLK7	P93	RHCLK
1	IO_L07P_1/IRDY1/RHCLK6	P91	RHCLK
1	IO_L08N_1	P98	I/O
1	IO_L08P_1	P96	I/O
1	IO_L09N_1	P101	I/O
1	IO_L09P_1	P99	I/O
1	IO_L10N_1	P104	I/O
1	IO_L10P_1	P102	I/O
1	IO_L11N_1	P105	I/O
1	IO_L11P_1	P103	I/O
1	IP_1/VREF_1	P80	VREF
1	IP_1/VREF_1	P97	VREF
1	VCCO_1	P86	VCCO
1	VCCO_1	P95	VCCO
2	IO_2/MOSI/CSI_B	P62	DUAL
2	IO_L01N_2/M0	P38	DUAL
2	IO_L01P_2/M1	P37	DUAL
2	IO_L02N_2/CSO_B	P41	DUAL
2	IO_L02P_2/M2	P39	DUAL
2	IO_L03N_2/VS1	P44	DUAL
2	IO_L03P_2/RDWR_B	P42	DUAL
2	IO_L04N_2/VS0	P45	DUAL
2	IO_L04P_2/VS2	P43	DUAL
2	IO_L05N_2/D7	P48	DUAL

Footprint Migration Differences

Unconnected Balls on XC3S50A

Table 73 summarizes any footprint and functionality differences between the XC3S50A and the XC3S200A or XC3S400A FPGAs that might affect easy migration between these devices in the FT256 package. The XC3S200A and XC3S400A have identical pinouts. The XC3S50A pinout is compatible, but there are 52 balls that are different. Generally, designs easily migrate upward from the XC3S50A to either the XC3S200A or XC3S400A. If using differential I/O, see Table 74. If using the BPI configuration mode (parallel Flash), see Table 75.

Table 73: **FT256 XC3S50A Footprint Migration Difference**

FT256 Ball	Bank	XC3S50A Type	Migration	XC3S200A/ XC3S400A Type
A7	0	N.C.	→	I/O
A12	0	N.C.	→	I/O
B12	0	INPUT	→	I/O
C7	0	N.C.	→	I/O
D10	0	N.C.	→	I/O
E2	3	N.C.	→	I/O
E3	3	N.C.	→	I/O
E7	0	N.C.	→	I/O
E10	0	N.C.	→	I/O
E16	1	N.C.	→	I/O
F3	3	N.C.	→	I/O
F8	0	N.C.	→	I/O
F14	1	N.C.	→	I/O
F15	1	N.C.	→	I/O
F16	1	N.C.	→	I/O
G3	3	N.C.	→	I/O
G4	3	N.C.	→	I/O
G5	3	N.C.	→	INPUT
G6	3	N.C.	→	INPUT
G13	1	N.C.	→	I/O
G14	1	N.C.	→	I/O
G16	1	N.C.	→	I/O
H4	3	N.C.	→	I/O
H5	3	N.C.	→	I/O
H6	3	N.C.	→	I/O
H13	1	N.C.	→	I/O
J4	3	N.C.	→	I/O
J6	3	N.C.	→	I/O
J10	1	N.C.	→	INPUT
J11	1	N.C.	→	INPUT
K4	3	N.C.	→	I/O
K13	1	N.C.	→	I/O
L1	3	N.C.	→	I/O
L2	3	N.C.	→	I/O
L3	3	N.C.	→	I/O
L4	3	N.C.	→	I/O
L13	1	N.C.	→	I/O
L14	1	N.C.	→	I/O
L16	1	N.C.	→	I/O
M3	3	N.C.	→	I/O
M10	2	N.C.	→	I/O
M13	1	N.C.	→	I/O
M14	1	N.C.	→	I/O
M15	1	N.C.	→	I/O
M16	1	N.C.	→	I/O
N7	2	N.C.	→	I/O
N10	2	N.C.	→	I/O
N12	2	N.C.	→	I/O
P6	2	N.C.	→	I/O
P13	2	N.C.	→	I/O
R7	2	N.C.	→	I/O
T7	2	N.C.	→	I/O
DIFFERENCES			**52**	

Legend:

→	This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction is possible depending on how the pin is configured for the device on the right.

XC3S50A Differential I/O Alignment Differences

Also, some differential I/O pairs on the XC3S50A FPGA are aligned differently than the corresponding pairs on the XC3S200A or XC3S400A FPGAs, as shown in Table 74. All the mismatched pairs are in I/O Bank 2. The shading highlights the N side of each pair.

Table 74: **Differential I/O Differences in FT256**

FT256 Ball	Bank	XC3S50A	XC3S200A XC3S400A
T3	2	IO_L04P_2/VS2	IO_L03N_2/VS2
N6		IO_L03N_2/VS1	IO_L04P_2/VS1
R5		IO_L06P_2	IO_L05N_2
T5		IO_L05N_2/D7	IO_L06P_2/D7
P10		IO_L14P_2/MOSI /CSI_B	IO_L14N_2/MOSI /CSI_B
T10		IO_L14N_2	IO_L14P_2
R13		IO_L20P_2	IO_L18N_2
T14		IO_L18N_2	IO_L20P_2

XC3S50A Does Not Have BPI Mode Address Outputs

The XC3S50A FPGA does not generate the BPI-mode address pins during configuration. Table 75 summarizes these differences.

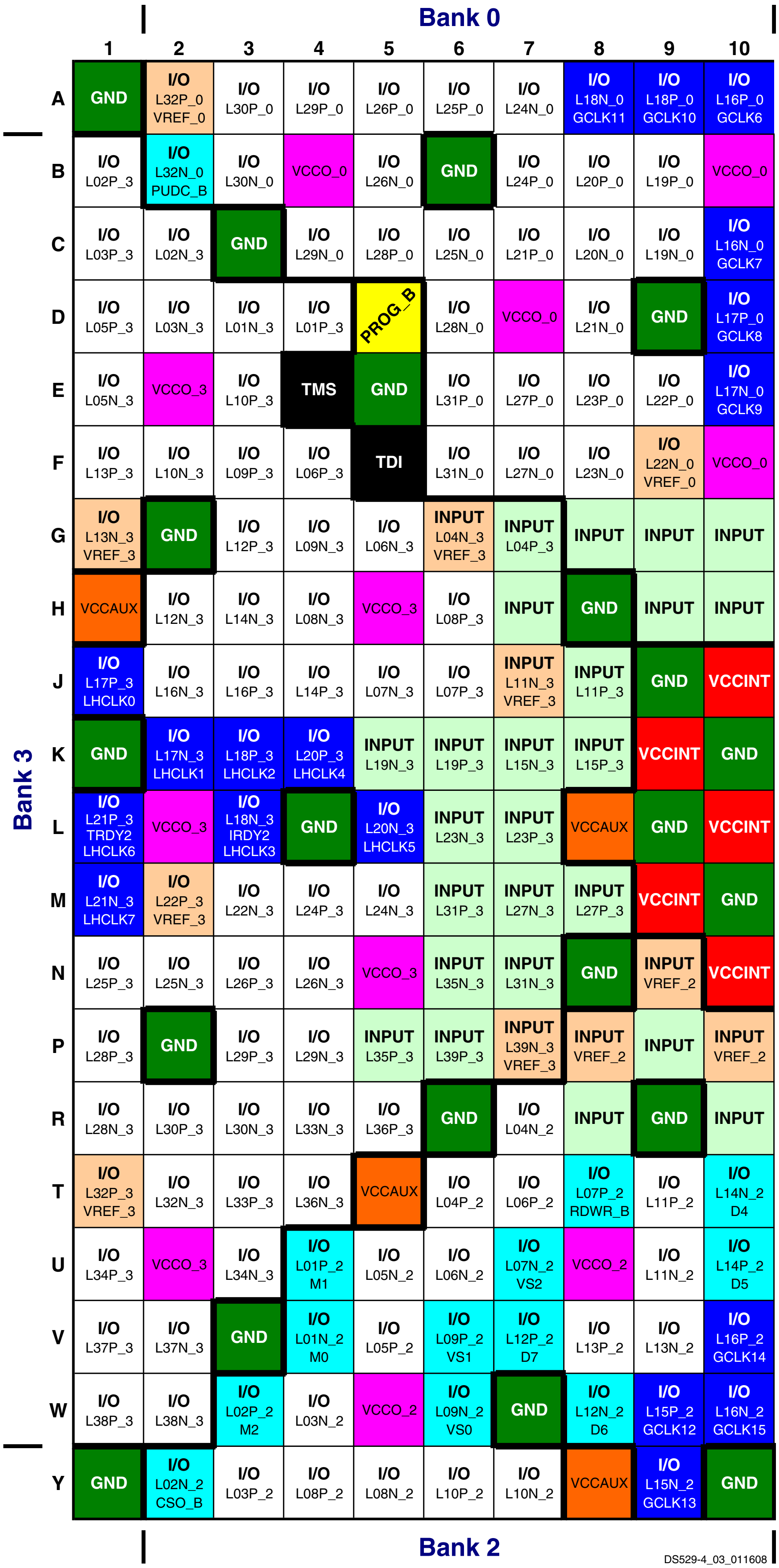
Table 75: **XC3S50A BPI Functional Differences**

FT256 Ball	Bank	XC3S50A	XC3S200A XC3S400A
N16	1	IO_L03N_1	IO_L03N_1/A1
P16		IO_L03P_1	IO_L03P_1/A0
J13		IO_L10N_1	IO_L10N_1/A9
J12		IO_L10P_1	IO_L10P_1/A8
F13		IO_L20N_1	IO_L20N_1/A19
E14		IO_L20P_1	IO_L20P_1/A18
D15		IO_L22N_1	IO_L22N_1/A21
D16		IO_L22P_1	IO_L22P_1/A20
D14		IO_L23N_1	IO_L23N_1/A23
E13		IO_L23P_1	IO_L23P_1/A22
C15		IO_L24N_1	IO_L24N_1/A25
C16		IO_L24P_1	IO_L24P_1/A24

FG400 Footprint

Left Half of FG400 Package (Top View)

155	**I/O:** Unrestricted, general-purpose user I/O
46	**INPUT:** Unrestricted, general-purpose input pin
51	**DUAL:** Configuration pins, then possible user I/O
26	**VREF:** User I/O or input voltage reference for bank
32	**CLK:** User I/O, input, or clock buffer input
2	**CONFIG:** Dedicated configuration pins
4	**JTAG:** Dedicated JTAG port pins
2	**SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins
43	**GND:** Ground
22	**VCCO:** Output voltage supply for bank
9	**VCCINT:** Internal core supply voltage (+1.2V)
8	**VCCAUX:** Auxiliary supply voltage



	1	2	3	4	5	6	7	8	9	10
A	GND	I/O L32P_0 VREF_0	I/O L30P_0	I/O L29P_0	I/O L26P_0	I/O L25P_0	I/O L24N_0	I/O L18N_0 GCLK11	I/O L18P_0 GCLK10	I/O L16P_0 GCLK6
B	I/O L02P_3	I/O L32N_0 PUDC_B	I/O L30N_0	VCCO_0	I/O L26N_0	GND	I/O L24P_0	I/O L20P_0	I/O L19P_0	VCCO_0
C	I/O L03P_3	I/O L02N_3	GND	I/O L29N_0	I/O L28P_0	I/O L25N_0	I/O L21P_0	I/O L20N_0	I/O L19N_0	I/O L16N_0 GCLK7
D	I/O L05P_3	I/O L03N_3	I/O L01N_3	I/O L01P_3	PROG_B	I/O L28N_0	VCCO_0	I/O L21N_0	GND	I/O L17P_0 GCLK8
E	I/O L05N_3	VCCO_3	I/O L10P_3	TMS	GND	I/O L31P_0	I/O L27P_0	I/O L23P_0	I/O L22P_0	I/O L17N_0 GCLK9
F	I/O L13P_3	I/O L10N_3	I/O L09P_3	I/O L06P_3	TDI	I/O L31N_0	I/O L27N_0	I/O L23N_0	I/O L22N_0 VREF_0	VCCO_0
G	I/O L13N_3 VREF_3	GND	I/O L12P_3	I/O L09N_3	I/O L06N_3	INPUT L04N_3 VREF_3	INPUT L04P_3	INPUT	INPUT	INPUT
H	VCCAUX	I/O L12N_3	I/O L14N_3	I/O L08N_3	VCCO_3	I/O L08P_3	INPUT	GND	INPUT	INPUT
J	I/O L17P_3 LHCLK0	I/O L16N_3	I/O L16P_3	I/O L14P_3	I/O L07N_3	I/O L07P_3	INPUT L11N_3 VREF_3	INPUT L11P_3	GND	VCCINT
K	GND	I/O L17N_3 LHCLK1	I/O L18P_3 LHCLK2	I/O L20P_3 LHCLK4	INPUT L19N_3	INPUT L19P_3	INPUT L15N_3	INPUT L15P_3	VCCINT	GND
L	I/O L21P_3 TRDY2 LHCLK6	VCCO_3	I/O L18N_3 IRDY2 LHCLK3	GND	I/O L20N_3 LHCLK5	INPUT L23N_3	INPUT L23P_3	VCCAUX	GND	VCCINT
M	I/O L21N_3 LHCLK7	I/O L22P_3 VREF_3	I/O L22N_3	I/O L24P_3	I/O L24N_3	INPUT L31P_3	INPUT L27N_3	INPUT L27P_3	VCCINT	GND
N	I/O L25P_3	I/O L25N_3	I/O L26P_3	I/O L26N_3	VCCO_3	INPUT L35N_3	INPUT L31N_3	GND	INPUT VREF_2	VCCINT
P	I/O L28P_3	GND	I/O L29P_3	I/O L29N_3	INPUT L35P_3	INPUT L39P_3	INPUT L39N_3 VREF_3	INPUT VREF_2	INPUT	INPUT VREF_2
R	I/O L28N_3	I/O L30P_3	I/O L30N_3	I/O L33N_3	I/O L36P_3	GND	I/O L04N_2	INPUT	GND	INPUT
T	I/O L32P_3 VREF_3	I/O L32N_3	I/O L33P_3	I/O L36N_3	VCCAUX	I/O L04P_2	I/O L06P_2	I/O L07P_2 RDWR_B	I/O L11P_2	I/O L14N_2 D4
U	I/O L34P_3	VCCO_3	I/O L34N_3	I/O L01P_2 M1	I/O L05N_2	I/O L06N_2	I/O L07N_2 VS2	VCCO_2	I/O L11N_2	I/O L14P_2 D5
V	I/O L37P_3	I/O L37N_3	GND	I/O L01N_2 M0	I/O L05P_2	I/O L09P_2 VS1	I/O L12P_2 D7	I/O L13P_2	I/O L13N_2	I/O L16P_2 GCLK14
W	I/O L38P_3	I/O L38N_3	I/O L02P_2 M2	I/O L03N_2	VCCO_2	I/O L09N_2 VS0	GND	I/O L12N_2 D6	I/O L15P_2 GCLK12	I/O L16N_2 GCLK15
Y	GND	I/O L02N_2 CSO_B	I/O L03P_2	I/O L08P_2	I/O L08N_2	I/O L10P_2	I/O L10N_2	VCCAUX	I/O L15N_2 GCLK13	GND

Figure 24: **FG400 Package Footprint (Top View)**

Table 83: **Spartan-3A FG484 Pinout*(Continued)***

Bank	Pin Name	FG484 Ball	Type
1	IO_L26P_1/A10	K22	DUAL
1	IO_L28N_1	L19	I/O
1	IO_L28P_1	L18	I/O
1	IO_L29N_1/A13	J20	DUAL
1	IO_L29P_1/A12	J21	DUAL
1	IO_L30N_1/A15	G22	DUAL
1	IO_L30P_1/A14	H22	DUAL
1	IO_L32N_1	K18	I/O
1	IO_L32P_1	K17	I/O
1	IO_L33N_1/A17	H20	DUAL
1	IO_L33P_1/A16	H21	DUAL
1	IO_L34N_1/A19	F21	DUAL
1	IO_L34P_1/A18	F22	DUAL
1	IO_L36N_1	G20	I/O
1	IO_L36P_1	G19	I/O
1	IO_L37N_1	H19	I/O
1	IO_L37P_1	J18	I/O
1	IO_L38N_1	F20	I/O
1	IO_L38P_1	E20	I/O
1	IO_L40N_1	F18	I/O
1	IO_L40P_1	F19	I/O
1	IO_L41N_1	D22	I/O
1	IO_L41P_1	E22	I/O
1	IO_L42N_1	D20	I/O
1	IO_L42P_1	D21	I/O
1	IO_L44N_1/A21	C21	DUAL
1	IO_L44P_1/A20	C22	DUAL
1	IO_L45N_1/A23	B21	DUAL
1	IO_L45P_1/A22	B22	DUAL
1	IO_L46N_1/A25	G17	DUAL
1	IO_L46P_1/A24	G18	DUAL
1	IP_L04N_1/VREF_1	R16	VREF
1	IP_L04P_1	R15	INPUT
1	IP_L08N_1	P16	INPUT
1	IP_L08P_1	P15	INPUT
1	IP_L12N_1/VREF_1	R18	VREF
1	IP_L12P_1	R17	INPUT
1	IP_L16N_1/VREF_1	N16	VREF
1	IP_L16P_1	N15	INPUT
1	IP_L23N_1	M16	INPUT

Table 83: **Spartan-3A FG484 Pinout*(Continued)***

Bank	Pin Name	FG484 Ball	Type
1	IP_L23P_1	M17	INPUT
1	IP_L27N_1	L16	INPUT
1	IP_L27P_1/VREF_1	M15	VREF
1	IP_L31N_1	K16	INPUT
1	IP_L31P_1	L15	INPUT
1	IP_L35N_1	K15	INPUT
1	IP_L35P_1/VREF_1	K14	VREF
1	IP_L39N_1	H18	INPUT
1	IP_L39P_1	H17	INPUT
1	IP_L43N_1/VREF_1	J15	VREF
1	IP_L43P_1	J16	INPUT
1	IP_L47N_1	H15	INPUT
1	IP_L47P_1/VREF_1	H16	VREF
VCCAUX	SUSPEND	U18	PWR MGMT
1	VCCO_1	E21	VCCO
1	VCCO_1	J17	VCCO
1	VCCO_1	K21	VCCO
1	VCCO_1	P17	VCCO
1	VCCO_1	P21	VCCO
1	VCCO_1	V21	VCCO
2	IO_L01N_2/M0	W5	DUAL
2	IO_L01P_2/M1	V6	DUAL
2	IO_L02N_2/CSO_B	Y4	DUAL
2	IO_L02P_2/M2	W4	DUAL
2	IO_L03N_2	AA3	I/O
2	IO_L03P_2	AB2	I/O
2	IO_L04N_2	AA4	I/O
2	IO_L04P_2	AB3	I/O
2	IO_L05N_2	Y5	I/O
2	IO_L05P_2	W6	I/O
2	IO_L06N_2	AB5	I/O
2	IO_L06P_2	AB4	I/O
2	IO_L07N_2	Y6	I/O
2	IO_L07P_2	W7	I/O
2	IO_L08N_2	AB6	I/O
2	IO_L08P_2	AA6	I/O
2	IO_L09N_2/VS2	W9	DUAL
2	IO_L09P_2/RDWR_B	V9	DUAL
2	IO_L10N_2	AB7	I/O

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
2	IP_2	AD10	INPUT
2	IP_2	AD16	INPUT
2	IP_2	AF2	INPUT
2	IP_2	AF7	INPUT
2	IP_2	Y11	INPUT
2	IP_2/VREF_2	AA9	VREF
2	IP_2/VREF_2	AA20	VREF
2	IP_2/VREF_2	AB6	VREF
2	IP_2/VREF_2	AB10	VREF
2	IP_2/VREF_2	AC10	VREF
2	IP_2/VREF_2	AD12	VREF
2	IP_2/VREF_2	AF15	VREF
2	IP_2/VREF_2	AF17	VREF
2	IP_2/VREF_2	AF22	VREF
2	IP_2/VREF_2	Y16	VREF
2	N.C. (◆)	AA8	N.C.
2	N.C. (◆)	AC5	N.C.
2	N.C. (◆)	AC22	N.C.
2	N.C. (◆)	AD5	N.C.
2	N.C. (◆)	Y18	N.C.
2	N.C. (◆)	Y19	N.C.
2	N.C. (◆)	AD23	N.C.
2	N.C. (◆)	W18	N.C.
2	N.C. (◆)	Y8	N.C.
2	VCCO_2	AB8	VCCO
2	VCCO_2	AB14	VCCO
2	VCCO_2	AB19	VCCO
2	VCCO_2	AE5	VCCO
2	VCCO_2	AE11	VCCO
2	VCCO_2	AE16	VCCO
2	VCCO_2	AE22	VCCO
2	VCCO_2	W11	VCCO
2	VCCO_2	W16	VCCO
3	IO_L01N_3	J9	I/O
3	IO_L01P_3	J8	I/O
3	IO_L02N_3	B1	I/O
3	IO_L02P_3	B2	I/O
3	IO_L03N_3	H7	I/O
3	IO_L03P_3	G6	I/O
3	IO_L05N_3	K8	I/O

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
3	IO_L05P_3	K9	I/O
3	IO_L06N_3	E4	I/O
3	IO_L06P_3	D3	I/O
3	IO_L07N_3	F4	I/O
3	IO_L07P_3	E3	I/O
3	IO_L09N_3	G4	I/O
3	IO_L09P_3	F5	I/O
3	IO_L10N_3	H6	I/O
3	IO_L10P_3	J7	I/O
3	IO_L11N_3	F2	I/O
3	IO_L11P_3	E1	I/O
3	IO_L13N_3	J6	I/O
3	IO_L13P_3	K7	I/O
3	IO_L14N_3	F3	I/O
3	IO_L14P_3	G3	I/O
3	IO_L15N_3	L9	I/O
3	IO_L15P_3	L10	I/O
3	IO_L17N_3	H1	I/O
3	IO_L17P_3	H2	I/O
3	IO_L18N_3	L7	I/O
3	IO_L18P_3	K6	I/O
3	IO_L19N_3	J4	I/O
3	IO_L19P_3	J5	I/O
3	IO_L21N_3	M9	I/O
3	IO_L21P_3	M10	I/O
3	IO_L22N_3	K4	I/O
3	IO_L22P_3	K5	I/O
3	IO_L23N_3	K2	I/O
3	IO_L23P_3	K3	I/O
3	IO_L25N_3	L3	I/O
3	IO_L25P_3	L4	I/O
3	IO_L26N_3	M7	I/O
3	IO_L26P_3	M8	I/O
3	IO_L27N_3	M3	I/O
3	IO_L27P_3	M4	I/O
3	IO_L28N_3	M6	I/O
3	IO_L28P_3	M5	I/O
3	IO_L29N_3/VREF_3	M1	VREF
3	IO_L29P_3	M2	I/O
3	IO_L30N_3	N4	I/O

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
3	IO_L30P_3	N5	I/O
3	IO_L31N_3	N2	I/O
3	IO_L31P_3	N1	I/O
3	IO_L32N_3/LHCLK1	N7	LHCLK
3	IO_L32P_3/LHCLK0	N6	LHCLK
3	IO_L33N_3/IRDY2/LHCLK3	P2	LHCLK
3	IO_L33P_3/LHCLK2	P1	LHCLK
3	IO_L34N_3/LHCLK5	P3	LHCLK
3	IO_L34P_3/LHCLK4	P4	LHCLK
3	IO_L35N_3/LHCLK7	P10	LHCLK
3	IO_L35P_3/TRDY2/LHCLK6	N9	LHCLK
3	IO_L36N_3	R2	I/O
3	IO_L36P_3/VREF_3	R1	VREF
3	IO_L37N_3	R4	I/O
3	IO_L37P_3	R3	I/O
3	IO_L38N_3	T4	I/O
3	IO_L38P_3	T3	I/O
3	IO_L39N_3	P6	I/O
3	IO_L39P_3	P7	I/O
3	IO_L40N_3	R6	I/O
3	IO_L40P_3	R5	I/O
3	IO_L41N_3	P9	I/O
3	IO_L41P_3	P8	I/O
3	IO_L42N_3	U4	I/O
3	IO_L42P_3	T5	I/O
3	IO_L43N_3	R9	I/O
3	IO_L43P_3/VREF_3	R10	VREF
3	IO_L44N_3	U2	I/O
3	IO_L44P_3	U1	I/O
3	IO_L45N_3	R7	I/O
3	IO_L45P_3	R8	I/O
3	IO_L47N_3	V2	I/O
3	IO_L47P_3	V1	I/O
3	IO_L48N_3	T9	I/O
3	IO_L48P_3	T10	I/O
3	IO_L49N_3	V5	I/O
3	IO_L49P_3	U5	I/O
3	IO_L51N_3	U6	I/O
3	IO_L51P_3	T7	I/O
3	IO_L52N_3	W4	I/O

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
3	IO_L52P_3	W3	I/O
3	IO_L53N_3	Y2	I/O
3	IO_L53P_3	Y1	I/O
3	IO_L55N_3	AA3	I/O
3	IO_L55P_3	AA2	I/O
3	IO_L56N_3	U8	I/O
3	IO_L56P_3	U7	I/O
3	IO_L57N_3	Y6	I/O
3	IO_L57P_3	Y5	I/O
3	IO_L59N_3	V6	I/O
3	IO_L59P_3	V7	I/O
3	IO_L60N_3	AC1	I/O
3	IO_L60P_3	AB1	I/O
3	IO_L61N_3	V8	I/O
3	IO_L61P_3	U9	I/O
3	IO_L63N_3	W6	I/O
3	IO_L63P_3	W7	I/O
3	IO_L64N_3	AC3	I/O
3	IO_L64P_3	AC2	I/O
3	IO_L65N_3	AD2	I/O
3	IO_L65P_3	AD1	I/O
3	IP_L04N_3/VREF_3	C1	VREF
3	IP_L04P_3	C2	INPUT
3	IP_L08N_3	D1	INPUT
3	IP_L08P_3	D2	INPUT
3	IP_L12N_3/VREF_3	H4	VREF
3	IP_L12P_3	G5	INPUT
3	IP_L16N_3	G1	INPUT
3	IP_L16P_3	G2	INPUT
3	IP_L20N_3/VREF_3	J2	VREF
3	IP_L20P_3	J3	INPUT
3	IP_L24N_3	K1	INPUT
3	IP_L24P_3	J1	INPUT
3	IP_L46N_3	V4	INPUT
3	IP_L46P_3	U3	INPUT
3	IP_L50N_3/VREF_3	W2	VREF
3	IP_L50P_3	W1	INPUT
3	IP_L54N_3	Y4	INPUT
3	IP_L54P_3	Y3	INPUT
3	IP_L58N_3/VREF_3	AA5	VREF