

Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	176
Number of Logic Elements/Cells	1584
Total RAM Bits	55296
Number of I/O	68
Number of Gates	50000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s50a-4vqg100c

Production Status

Table 3 indicates the production status of each Spartan-3A FPGA by temperature range and speed grade. The table also lists the earliest speed file version required for creating

a production configuration bitstream. Later versions are also supported.

Table 3: Spartan-3A FPGA Production Status (Production Speed File)

Temperature Range		Commercial (C)		Industrial
Speed Grade		Standard (-4)	High-Performance (-5)	Standard (-4)
Part Number	XC3S50A	Production (v1.35)	Production (v1.35)	Production (v1.35)
	XC3S200A	Production (v1.35)	Production (v1.35)	Production (v1.35)
	XC3S400A	Production (v1.36)	Production (v1.36)	Production (v1.36)
	XC3S700A	Production (v1.34)	Production (v1.35)	Production (v1.34)
	XC3S1400A	Production (v1.34)	Production (v1.35)	Production (v1.34)

Package Marking

Figure 2 provides a top marking example for Spartan-3A FPGAs in the quad-flat packages. Figure 3 shows the top marking for Spartan-3A FPGAs in BGA packages. The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator.

The “5C” and “4I” Speed Grade/Temperature Range part combinations may be dual marked as “5C/4I”. Devices with a single mark are only guaranteed for the marked speed grade and temperature range.

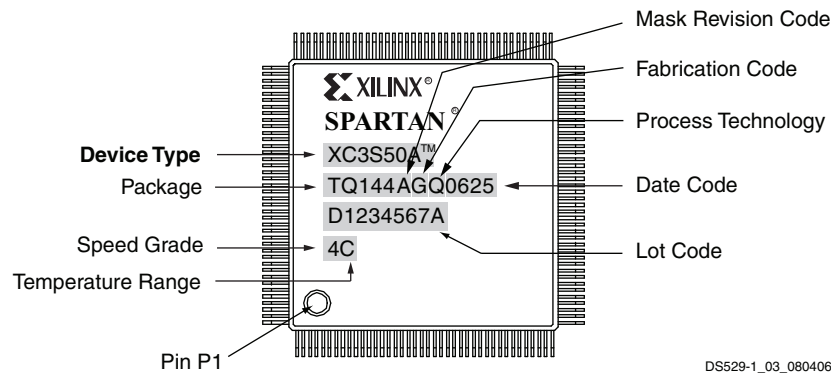


Figure 2: Spartan-3A QFP Package Marking Example

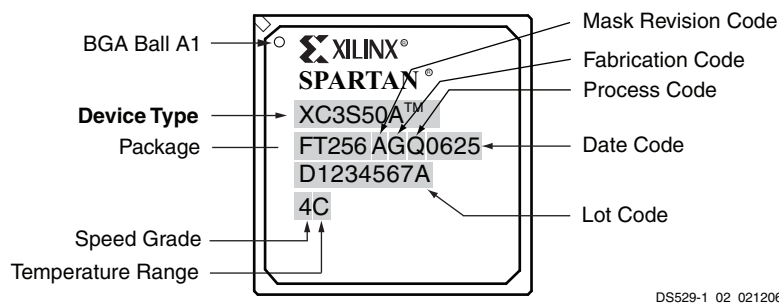


Figure 3: Spartan-3A BGA Package Marking Example

General Recommended Operating Conditions

Table 8: General Recommended Operating Conditions

Symbol	Description		Min	Nominal	Max	Units	
T_J	Junction temperature	Commercial	0	–	85	°C	
		Industrial	–40	–	100	°C	
V_{CCINT}	Internal supply voltage		1.14	1.20	1.26	V	
$V_{CCO}^{(1)}$	Output driver supply voltage		1.10	–	3.60	V	
V_{CCAUX}	Auxiliary supply voltage ⁽²⁾	$V_{CCAUX} = 2.5$	2.25	2.50	2.75	V	
		$V_{CCAUX} = 3.3$	3.00	3.30	3.60	V	
V_{IN}	Input voltage ⁽³⁾	PCI IOSTANDARD	–0.5	–	$V_{CCO}+0.5$	V	
		All other IOSTANDARDS	IP or IO_#	–0.5	–	4.10	V
			IO_Lxxy_# ⁽⁴⁾	–0.5	–	4.10	V
T_{IN}	Input signal transition time ⁽⁵⁾		–	–	500	ns	

Notes:

1. This V_{CCO} range spans the lowest and highest operating voltages for all supported I/O standards. [Table 11](#) lists the recommended V_{CCO} range specific to each of the single-ended I/O standards, and [Table 13](#) lists that specific to the differential standards.
2. Define V_{CCAUX} selection using CONFIG VCCAUX constraint.
3. See [XAPP459](#), “Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins.”
4. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in [UG331](#), *Spartan-3 Generation FPGA User Guide*.
5. Measured between 10% and 90% V_{CCO} . Follow [Signal Integrity](#) recommendations.

Quiescent Current Requirements

Table 10: Quiescent Supply Current Characteristics

Symbol	Description	Device	Typical ⁽²⁾	Commercial Maximum ⁽²⁾	Industrial Maximum ⁽²⁾	Units
I _{CCINTQ}	Quiescent V _{CCINT} supply current	XC3S50A	2	20	30	mA
		XC3S200A	7	50	70	mA
		XC3S400A	10	85	125	mA
		XC3S700A	13	120	185	mA
		XC3S1400A	24	220	310	mA
I _{CCOQ}	Quiescent V _{CCO} supply current	XC3S50A	0.2	2	3	mA
		XC3S200A	0.2	2	3	mA
		XC3S400A	0.3	3	4	mA
		XC3S700A	0.3	3	4	mA
		XC3S1400A	0.3	3	4	mA
I _{CCAUXQ}	Quiescent V _{CCAUX} supply current	XC3S50A	3	8	10	mA
		XC3S200A	5	12	15	mA
		XC3S400A	5	18	24	mA
		XC3S700A	6	28	34	mA
		XC3S1400A	10	50	58	mA

Notes:

- The numbers in this table are based on the conditions set forth in [Table 8](#).
- Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using typical devices at room temperature (T_J of 25°C at V_{CCINT} = 1.2V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.6V, and V_{CCAUX} = 3.6V. The FPGA is programmed with a “blank” configuration data file (that is, a design with no functional elements instantiated). For conditions other than those described above (for example, a design including functional elements), measured quiescent current levels will be different than the values in the table.
- For more accurate estimates for a specific design, use the Xilinx XPower tools. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The [Spartan-3A FPGA XPower Estimator](#) provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer uses a netlist as input to provide maximum estimates as well as more accurate typical estimates.
- The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.
- For information on the power-saving Suspend mode, see [XAPP480: Using Suspend Mode in Spartan-3 Generation FPGAs](#). Suspend mode typically saves 40% total power consumption compared to quiescent current.

Single-Ended I/O Standards

Table 11: Recommended Operating Conditions for User I/Os Using Single-Ended Standards

IOSTANDARD Attribute	V_{CCO} for Drivers ⁽²⁾			V_{REF}			V_{IL}	V_{IH}
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
LVTTTL	3.0	3.3	3.6	V_{REF} is not used for these I/O standards			0.8	2.0
LVC MOS33 ⁽⁴⁾	3.0	3.3	3.6				0.8	2.0
LVC MOS25 ^(4,5)	2.3	2.5	2.7				0.7	1.7
LVC MOS18	1.65	1.8	1.95				0.4	0.8
LVC MOS15	1.4	1.5	1.6				0.4	0.8
LVC MOS12	1.1	1.2	1.3				0.4	0.7
PCI33_3 ⁽⁶⁾	3.0	3.3	3.6				$0.3 \cdot V_{CCO}$	$0.5 \cdot V_{CCO}$
PCI66_3 ⁽⁶⁾	3.0	3.3	3.6				$0.3 \cdot V_{CCO}$	$0.5 \cdot V_{CCO}$
HSTL_I	1.4	1.5	1.6	0.68	0.75	0.9	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_III	1.4	1.5	1.6	–	0.9	–	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_II_18	1.7	1.8	1.9	–	0.9	–	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_III_18	1.7	1.8	1.9	–	1.1	–	$V_{REF} - 0.1$	$V_{REF} + 0.1$
SSTL18_I	1.7	1.8	1.9	0.833	0.900	0.969	$V_{REF} - 0.125$	$V_{REF} + 0.125$
SSTL18_II	1.7	1.8	1.9	0.833	0.900	0.969	$V_{REF} - 0.125$	$V_{REF} + 0.125$
SSTL2_I	2.3	2.5	2.7	1.13	1.25	1.38	$V_{REF} - 0.150$	$V_{REF} + 0.150$
SSTL2_II	2.3	2.5	2.7	1.13	1.25	1.38	$V_{REF} - 0.150$	$V_{REF} + 0.150$
SSTL3_I	3.0	3.3	3.6	1.3	1.5	1.7	$V_{REF} - 0.2$	$V_{REF} + 0.2$
SSTL3_II	3.0	3.3	3.6	1.3	1.5	1.7	$V_{REF} - 0.2$	$V_{REF} + 0.2$

Notes:

- Descriptions of the symbols used in this table are as follows:
 V_{CCO} – the supply voltage for output drivers
 V_{REF} – the reference voltage for setting the input switching threshold
 V_{IL} – the input voltage that indicates a Low logic level
 V_{IH} – the input voltage that indicates a High logic level
- In general, the V_{CCO} rails supply only output drivers, not input circuits. The exceptions are for LVC MOS25 inputs when $V_{CCAUX} = 3.3V$ range and for PCI I/O standards.
- For device operation, the maximum signal voltage (V_{IH} max) can be as high as V_{IN} max. See [Table 8](#).
- There is approximately 100 mV of hysteresis on inputs using LVC MOS33 and LVC MOS25 I/O standards.
- All Dedicated pins (PROG_B, DONE, SUSPEND, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail and use the LVC MOS25 or LVC MOS33 standard depending on V_{CCAUX} . The dual-purpose configuration pins use the LVC MOS standard before the User mode. When using these pins as part of a standard 2.5V configuration interface, apply 2.5V to the V_{CCO} lines of Banks 0, 1, and 2 at power-on as well as throughout configuration.
- For information on PCI IP solutions, see www.xilinx.com/pci. The PCI IOSTANDARD is not supported on input-only pins. The PCIX IOSTANDARD is available and has equivalent characteristics but no PCI-X IP is supported.

Table 22: Propagation Times for the IOB Input Path(Continued)

Symbol	Description	Conditions	DELAY_VALUE	Device	Speed Grade		Units
					-5	-4	
					Max	Max	
T _{IOPID}	The time it takes for data to travel from the Input pin to the I output with the input delay programmed	LVCMOS25 ⁽²⁾	5	XC3S1400A	3.17	3.52	ns
			6		3.52	3.92	ns
			7		3.82	4.18	ns
			8		4.10	4.57	ns
			9		3.84	4.31	ns
			10		4.20	4.79	ns
			11		4.46	5.06	ns
			12		4.87	5.51	ns
			13		5.07	5.73	ns
			14		5.43	6.08	ns
			15		5.73	6.33	ns
			16		6.01	6.77	ns
T _{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25 ⁽²⁾	IFD_DELAY_VALUE=0	XC3S50A	1.70	1.81	ns
				XC3S200A	1.85	2.04	ns
				XC3S400A	1.44	1.74	ns
				XC3S700A	1.48	1.74	ns
				XC3S1400A	1.50	1.97	ns
T _{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25 ⁽²⁾	1	XC3S50A	2.30	2.41	ns
			2		3.24	3.35	ns
			3		3.65	3.98	ns
			4		4.18	4.55	ns
			5		4.02	4.47	ns
			6		4.86	5.32	ns
			7		5.61	6.17	ns
			8		6.11	6.75	ns
			1	XC3S200A	2.19	2.43	ns
			2		2.86	3.16	ns
			3		3.52	4.01	ns
			4		4.02	4.60	ns
			5		3.83	4.43	ns
			6		4.70	5.46	ns
			7		5.48	6.33	ns
			8		5.99	6.94	ns
			1	XC3S400A	1.93	2.25	ns
			2		2.57	2.90	ns
			3		3.16	3.66	ns
			4		3.63	4.19	ns

Using IBIS Models to Simulate Load Conditions in Application

IBIS models permit the most accurate prediction of timing delays for a given application. The parameters found in the IBIS model (V_{REF} , R_{REF} , and V_{MEAS}) correspond directly with the parameters used in [Table 27](#) (V_T , R_T , and V_M). Do not confuse V_{REF} (the termination voltage) from the IBIS model with V_{REF} (the input-switching threshold) from the table. A fourth parameter, C_{REF} is always zero. The four parameters describe all relevant output test conditions. IBIS models are found in the Xilinx development software as well as at the following link:

www.xilinx.com/support/download/index.htm

Delays for a given application are simulated according to its specific load conditions as follows:

1. Simulate the desired signal standard with the output driver connected to the test setup shown in [Figure 9](#). Use parameter values V_T , R_T , and V_M from [Table 27](#). C_{REF} is zero.
2. Record the time to V_M .
3. Simulate the same signal standard with the output driver connected to the PCB trace with load. Use the appropriate IBIS model (including V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} values) or capacitive value to represent the load.
4. Record the time to V_{MEAS} .
5. Compare the results of steps 2 and 4. Add (or subtract) the increase (or decrease) in delay to (or from) the appropriate Output standard adjustment ([Table 26](#)) to yield the worst-case delay of the PCB trace.

Simultaneously Switching Output Guidelines

This section provides guidelines for the recommended maximum allowable number of Simultaneous Switching Outputs (SSOs). These guidelines describe the maximum number of user I/O pins of a given output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of ground and power bounce.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common voltage rail. Low-to-High transitions conduct to the V_{CCO} rail; High-to-Low transitions conduct to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the die pad and the power supply or ground return. The inductance is associated with bonding wires, the package lead frame, and any other signal routing inside the package. Other variables contribute to SSO noise levels, including stray inductance on the PCB as well as capacitive loading at receivers. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

[Table 28](#) and [Table 29](#) provide the essential SSO guidelines. For each device/package combination, [Table 28](#) provides the number of equivalent V_{CCO}/GND pairs. The equivalent number of pairs is based on characterization and may not match the physical number of pairs. For each output signal standard and drive strength, [Table 29](#) recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The guidelines in [Table 29](#) are categorized by package style, slew rate, and output drive current. Furthermore, the number of SSOs is specified by I/O bank. Generally, the left and right I/O banks (Banks 1 and 3) support higher output drive current.

Multiply the appropriate numbers from [Table 28](#) and [Table 29](#) to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines might result in increased power or ground bounce, degraded signal integrity, or increased system jitter.

$$SSO_{MAX}/IO \text{ Bank} = \text{Table 28} \times \text{Table 29}$$

The recommended maximum SSO values assume that the FPGA is soldered on the printed circuit board and that the board uses sound design practices. The SSO values do not apply for FPGAs mounted in sockets, due to the lead inductance introduced by the socket.

The SSO values assume that the V_{CCAUX} is powered at 3.3V. Setting V_{CCAUX} to 2.5V provides better SSO characteristics.

The number of SSOs allowed for quad-flat packages (VQ/TQ) is lower than for ball grid array packages (FG) due to the larger lead inductance of the quad-flat packages. Ball grid array packages are recommended for applications with a large number of simultaneously switching outputs.

Table 47: Master Mode CCLK Output Frequency by ConfigRate Option Setting

Symbol	Description	ConfigRate Setting	Temperature Range	Minimum	Maximum	Units
F _{CCLK1}	Equivalent CCLK clock frequency by ConfigRate setting	1 (power-on value)	Commercial	0.400	0.797	MHz
			Industrial		0.847	MHz
F _{CCLK3}		3	Commercial	1.20	2.42	MHz
			Industrial		2.57	MHz
F _{CCLK6}		6 (default)	Commercial	2.40	4.83	MHz
			Industrial		5.13	MHz
F _{CCLK7}		7	Commercial	2.80	5.61	MHz
			Industrial		5.96	MHz
F _{CCLK8}		8	Commercial	3.20	6.41	MHz
			Industrial		6.81	MHz
F _{CCLK10}		10	Commercial	4.00	8.12	MHz
			Industrial		8.63	MHz
F _{CCLK12}		12	Commercial	4.80	9.70	MHz
			Industrial		10.31	MHz
F _{CCLK13}		13	Commercial	5.20	10.69	MHz
			Industrial		11.37	MHz
F _{CCLK17}		17	Commercial	6.80	13.74	MHz
			Industrial		14.61	MHz
F _{CCLK22}		22	Commercial	8.80	18.44	MHz
			Industrial		19.61	MHz
F _{CCLK25}	25	Commercial	10.00	20.90	MHz	
		Industrial		22.23	MHz	
F _{CCLK27}	27	Commercial	10.80	22.39	MHz	
		Industrial		23.81	MHz	
F _{CCLK33}	33	Commercial	13.20	27.48	MHz	
		Industrial		29.23	MHz	
F _{CCLK44}	44	Commercial	17.60	37.60	MHz	
		Industrial		40.00	MHz	
F _{CCLK50}	50	Commercial	20.00	44.80	MHz	
		Industrial		47.66	MHz	
F _{CCLK100}	100	Commercial	40.00	88.68	MHz	
		Industrial		94.34	MHz	

Table 48: Master Mode CCLK Output Minimum Low and High Time

Symbol	Description	ConfigRate Setting																Units	
		1	3	6	7	8	10	12	13	17	22	25	27	33	44	50	100		
T _{MCCL} , T _{MCCH}	Master Mode CCLK Minimum Low and High Time	Commercial	595	196	98.3	84.5	74.1	58.4	48.9	44.1	34.2	25.6	22.3	20.9	17.1	12.3	10.4	5.3	ns
		Industrial	560	185	92.6	79.8	69.8	55.0	46.0	41.8	32.3	24.2	21.4	20.0	16.2	11.9	10.0	5.0	ns

Table 49: Slave Mode CCLK Input Low and High Time

Symbol	Description	Min	Max	Units
T _{SCCL} , T _{SCCH}	CCLK Low and High time	5	∞	ns

Table 53: Configuration Timing Requirements for Attached SPI Serial Flash

Symbol	Description	Requirement	Units
T_{CCS}	SPI serial Flash PROM chip-select time	$T_{CCS} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DSU}	SPI serial Flash PROM data input setup time	$T_{DSU} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DH}	SPI serial Flash PROM data input hold time	$T_{DH} \leq T_{MCCH1}$	ns
T_V	SPI serial Flash PROM data clock-to-output time	$T_V \leq T_{MCCLn} - T_{DCC}$	ns
f_C or f_R	Maximum SPI serial Flash PROM clock frequency (also depends on specific read command used)	$f_C \geq \frac{1}{T_{CCLKn(min)}}$	MHz

Notes:

1. These requirements are for successful FPGA configuration in SPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.

IEEE 1149.1/1532 JTAG Test Access Port Timing

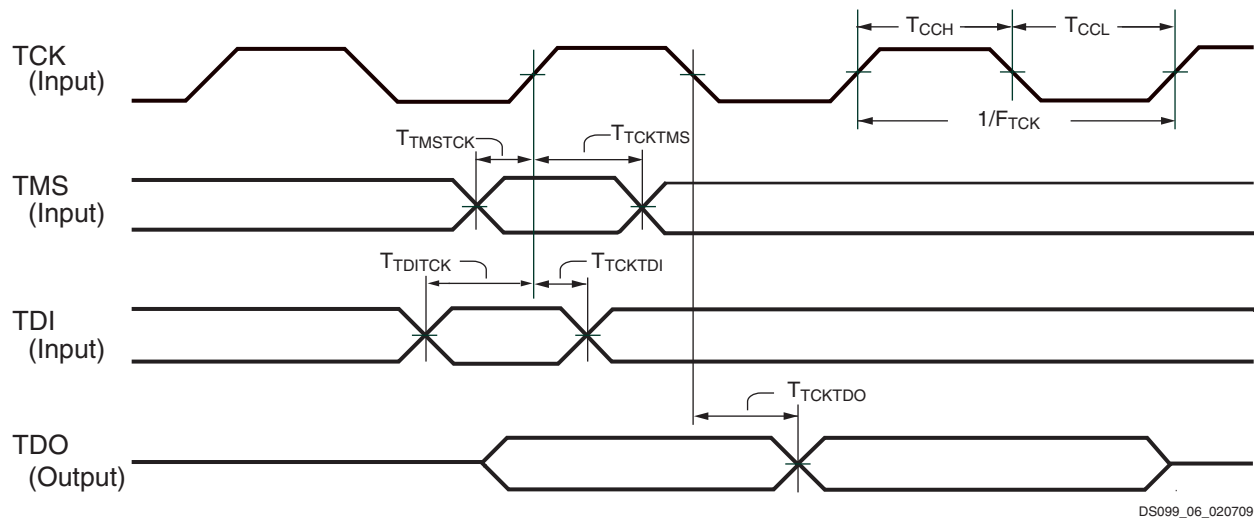


Figure 16: JTAG Waveforms

Table 56: Timing for the JTAG Test Access Port

Symbol	Description	All Speed Grades		Units	
		Min	Max		
Clock-to-Output Times					
T _{TCKTDO}	The time from the falling transition on the TCK pin to data appearing at the TDO pin	1.0	11.0	ns	
Setup Times					
T _{TDITCK}	The time from the setup of data at the TDI pin to the rising transition at the TCK pin	All devices and functions except those shown below	7.0	–	ns
		Boundary scan commands (INTEST, EXTEST, SAMPLE) on XC3S700A and XC3S1400A FPGAs	11.0		
T _{TMSTCK}	The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin	7.0	–	ns	
Hold Times					
T _{TCKTDI}	The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin	All functions except those shown below	0	–	ns
		Configuration commands (CFG_IN, ISC_PROGRAM)	2.0		
T _{TCKTMS}	The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin	0	–	ns	
Clock Timing					
T _{CCH}	The High pulse width at the TCK pin	All functions except ISC_DNA command	5	–	ns
T _{CCL}	The Low pulse width at the TCK pin		5	–	ns
T _{CCHDNA}	The High pulse width at the TCK pin	During ISC_DNA command	10	10,000	ns
T _{CCLDNA}	The Low pulse width at the TCK pin		10	10,000	ns
F _{TCK}	Frequency of the TCK signal	All operations on XC3S50A, XC3S200A, and XC3S400A FPGAs and for BYPASS or HIGHZ instructions on all FPGAs	0	33	MHz
		All operations on XC3S700A and XC3S1400A FPGAs, except for BYPASS or HIGHZ instructions		20	

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.
2. For details on JTAG see Chapter 9 “JTAG Configuration Mode and Boundary-Scan” in UG332 Spartan-3 Generation Configuration User Guide.

Introduction

This section describes how the various pins on a Spartan®-3A FPGA connect within the supported component packages, and provides device-specific thermal characteristics. For general information on the pin functions and the package characteristics, see the Packaging section of UG331: *Spartan-3 Generation FPGA User Guide*.

- UG331: Spartan-3 Generation FPGA User Guide**
www.xilinx.com/support/documentation/user_guides/ug331.pdf

Spartan-3A FPGAs are available in both standard and Pb-free, RoHS versions of each package, with the Pb-free version adding a “G” to the middle of the package code.

Table 57: Types of Pins on Spartan-3A FPGAs

Type / Color Code	Description	Pin Name(s) in Type
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO_# IO_Lxxy_#
INPUT	Unrestricted, general-purpose input-only pin. This pin does not have an output structure, differential termination resistor, or PCI clamp diode.	IP_# IP_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. See UG332: Spartan-3 Generation Configuration User Guide for additional information on these signals.	M[2:0] PUDC_B CCLK MOSI/CSI_B D[7:1] D0/DIN DOUT CSO_B RDWR_B INIT_B A[25:0] VS[2:0] LDC[2:0] HDC
VREF	Dual-purpose pin that is either a user-I/O pin or Input-only pin, or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected.	IP/VREF_# IP_Lxxy_#/VREF_# IO/VREF_# IO_Lxxy_#/VREF_#
CLK	Either a user-I/O pin or an input to a specific clock buffer driver. Most packages have 16 global clock inputs that optionally clock the entire device. The exceptions are the TQ144 and the XC3S50A in the FT256 package). The RHCLK inputs optionally clock the right half of the device. The LHCLK inputs optionally clock the left half of the device. See the Using Global Clock Resources chapter in UG331: Spartan-3 Generation FPGA User Guide for additional information on these signals.	IO_Lxxy_#/GCLK[15:0], IO_Lxxy_#/LHCLK[7:0], IO_Lxxy_#/RHCLK[7:0]
CONFIG	Dedicated configuration pin, two per device. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See the UG332: Spartan-3 Generation Configuration User Guide for additional information on the DONE and PROG_B signals.	DONE, PROG_B

Except for the thermal characteristics, all information for the standard package applies equally to the Pb-free package.

Pin Types

Most pins on a Spartan-3A FPGA are general-purpose, user-defined I/O pins. There are, however, up to 12 different functional types of pins on Spartan-3A FPGA packages, as outlined in [Table 57](#). In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

VQ100 Footprint (XC3S50A)

Note pin 1 indicator in top-left corner and logo orientation.

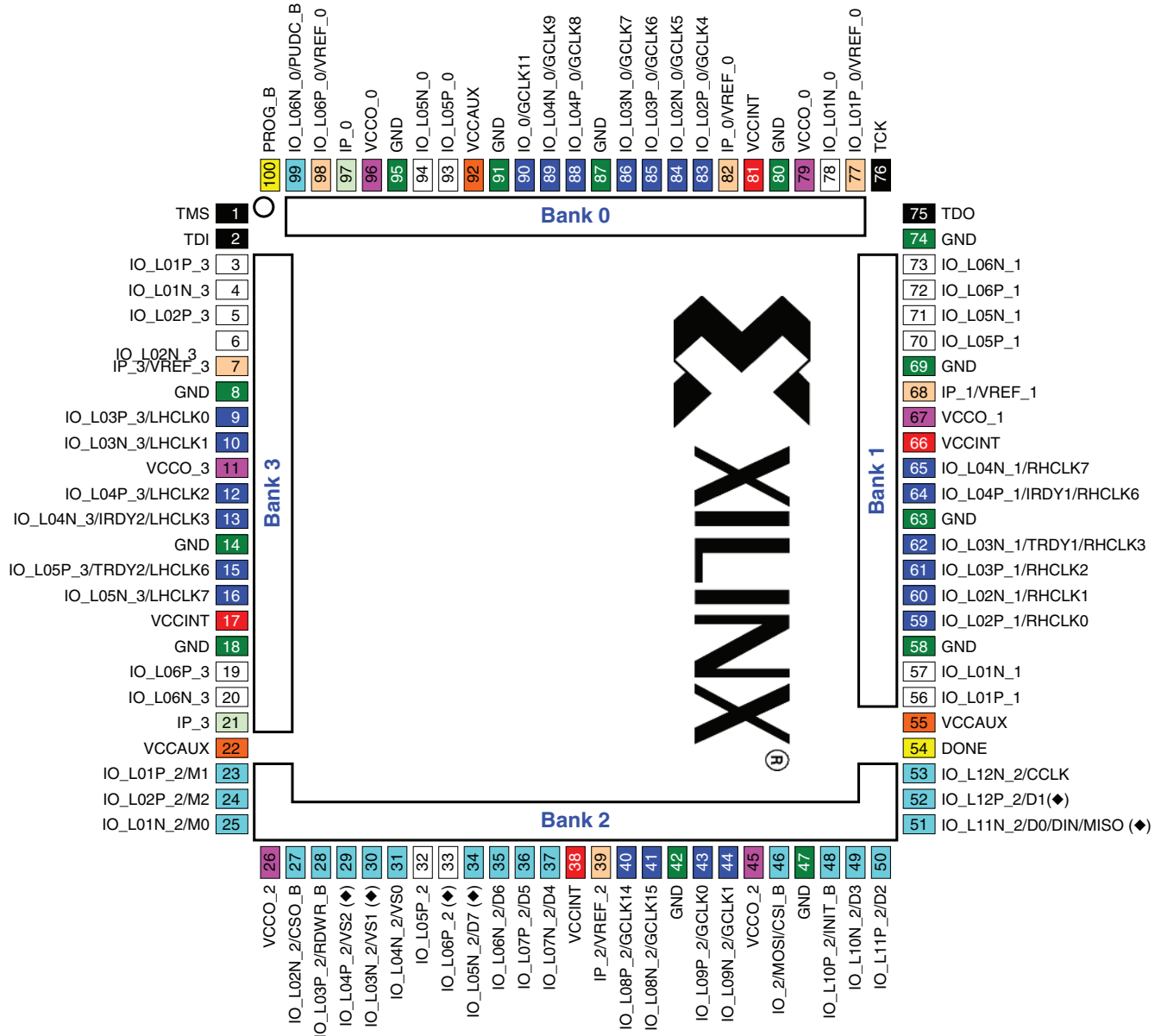


Figure 17: VQ100 Package Footprint - XC3S50A (Top View)

17	IO: Unrestricted, general-purpose user I/O	20	DUAL: Configuration pins, then possible user I/O	6	VREF: User I/O or input voltage reference for bank
2	INPUT: Unrestricted, general-purpose input pin	23	CLK: User I/O, input, or global buffer input	6	VCCO: Output voltage supply for bank
2	CONFIG: Dedicated configuration pins	4	JTAG: Dedicated JTAG port pins	4	VCCINT: Internal core supply voltage (+1.2V)
0	N.C.: Not connected	13	GND: Ground	3	VCCAUX: Auxiliary supply voltage

VQ100 Footprint (XC3S200A)

Note pin 1 indicator in top-left corner and logo orientation.

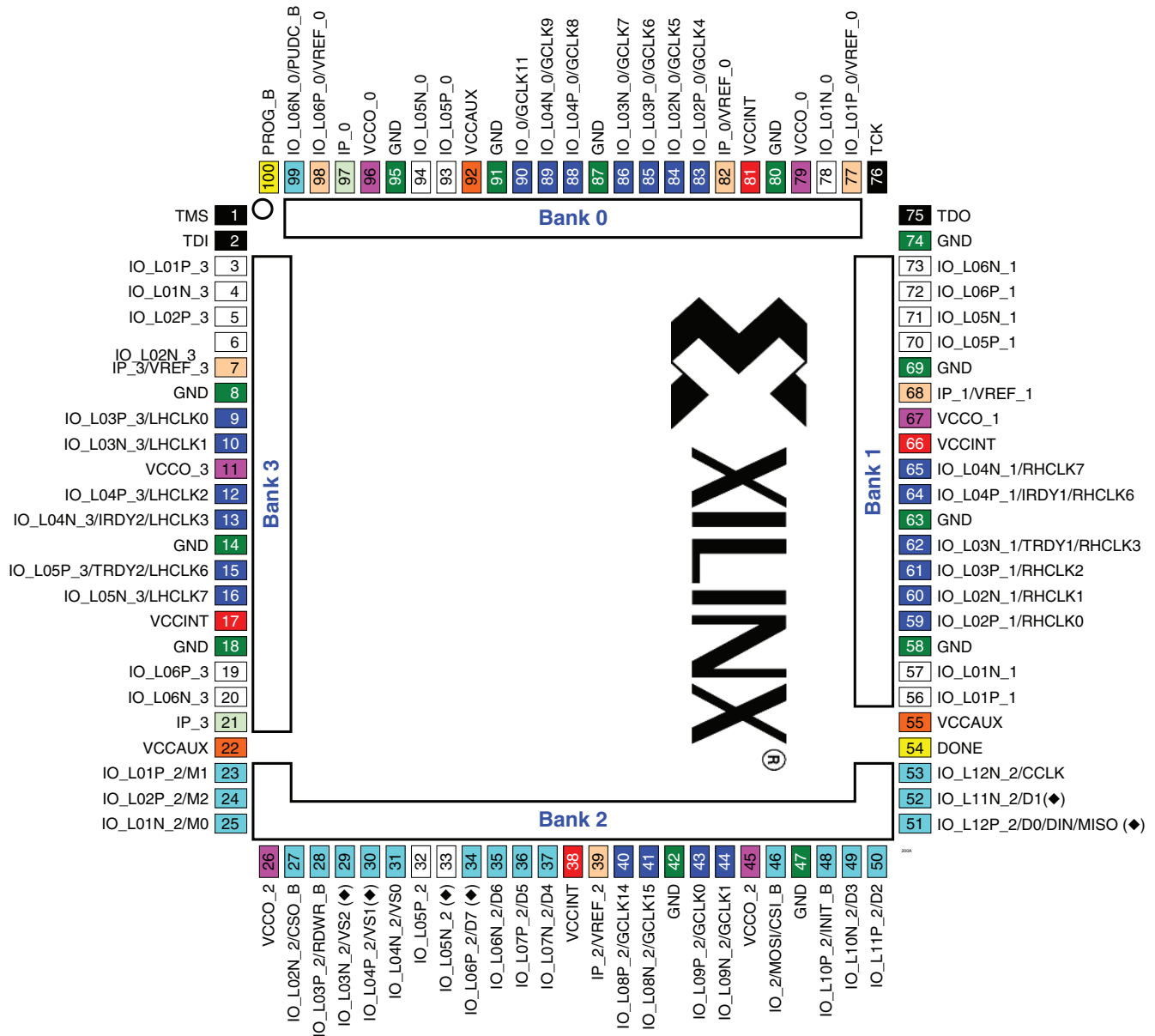


Figure 18: VQ100 Package Footprint - XC3S200A (Top View)

17	I/O: Unrestricted, general-purpose user I/O	20	DUAL: Configuration pins, then possible user I/O	6	VREF: User I/O or input voltage reference for bank
2	INPUT: Unrestricted, general-purpose input pin	23	CLK: User I/O, input, or global buffer input	6	VCCO: Output voltage supply for bank
2	CONFIG: Dedicated configuration pins	4	JTAG: Dedicated JTAG port pins	4	VCCINT: Internal core supply voltage (+1.2V)
0	N.C.: Not connected	13	GND: Ground	3	VCCAUX: Auxiliary supply voltage

Table 68: Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400) (Continued)

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
2	IO_L01N_2/M0	IO_L01N_2/M0	P4	DUAL
2	IO_L01P_2/M1	IO_L01P_2/M1	N4	DUAL
2	IO_L02N_2/ CSO_B	IO_L02N_2/ CSO_B	T2	DUAL
2	IO_L02P_2/M2	IO_L02P_2/M2	R2	DUAL
2	IO_L04P_2/VS2	IO_L03N_2/VS2	T3	DUAL
2	IO_L03P_2/ RDWR_B	IO_L03P_2/ RDWR_B	R3	DUAL
2	IO_L04N_2/VS0	IO_L04N_2/VS0	P5	DUAL
2	IO_L03N_2/VS1	IO_L04P_2/VS1	N6	DUAL
2	IO_L06P_2	IO_L05N_2	R5	I/O
2	IO_L05P_2	IO_L05P_2	T4	I/O
2	IO_L06N_2/D6	IO_L06N_2/D6	T6	DUAL
2	IO_L05N_2/D7	IO_L06P_2/D7	T5	DUAL
2	N.C. (◆)	IO_L07N_2	P6	I/O
2	N.C. (◆)	IO_L07P_2	N7	I/O
2	IO_L08N_2/D4	IO_L08N_2/D4	N8	DUAL
2	IO_L08P_2/D5	IO_L08P_2/D5	P7	DUAL
2	N.C. (◆)	IO_L09N_2/ GCLK13	T7	GCLK
2	N.C. (◆)	IO_L09P_2/ GCLK12	R7	GCLK
2	IO_L10N_2/ GCLK15	IO_L10N_2/ GCLK15	T8	GCLK
2	IO_L10P_2/ GCLK14	IO_L10P_2/ GCLK14	P8	GCLK
2	IO_L11N_2/ GCLK1	IO_L11N_2/ GCLK1	P9	GCLK
2	IO_L11P_2/ GCLK0	IO_L11P_2/ GCLK0	N9	GCLK
2	IO_L12N_2/ GCLK3	IO_L12N_2/ GCLK3	T9	GCLK
2	IO_L12P_2/ GCLK2	IO_L12P_2/ GCLK2	R9	GCLK
2	N.C. (◆)	IO_L13N_2	M10	I/O
2	N.C. (◆)	IO_L13P_2	N10	I/O
2	IO_L14P_2/ MOSI/CSI_B	IO_L14N_2/ MOSI/CSI_B	P10	DUAL
2	IO_L14N_2	IO_L14P_2	T10	I/O
2	IO_L15N_2/ DOUT	IO_L15N_2/ DOUT	R11	DUAL
2	IO_L15P_2/ AWAKE	IO_L15P_2/ AWAKE	T11	PWR MGMT
2	IO_L16N_2	IO_L16N_2	N11	I/O
2	IO_L16P_2	IO_L16P_2	P11	I/O
2	IO_L17N_2/D3	IO_L17N_2/D3	P12	DUAL
2	IO_L17P_2/ INIT_B	IO_L17P_2/ INIT_B	T12	DUAL

Table 68: Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400) (Continued)

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
2	IO_L20P_2/D1	IO_L18N_2/D1	R13	DUAL
2	IO_L18P_2/D2	IO_L18P_2/D2	T13	DUAL
2	N.C. (◆)	IO_L19N_2	P13	I/O
2	N.C. (◆)	IO_L19P_2	N12	I/O
2	IO_L20N_2/ CCLK	IO_L20N_2/ CCLK	R14	DUAL
2	IO_L18N_2/D0/ DIN/MISO	IO_L20P_2/D0/ DIN/MISO	T14	DUAL
2	IP_2	IP_2	L7	INPUT
2	IP_2	IP_2	L8	INPUT
2	IP_2/VREF_2	IP_2/VREF_2	L9	VREF
2	IP_2/VREF_2	IP_2/VREF_2	L10	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M7	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M8	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M11	VREF
2	IP_2/VREF_2	IP_2/VREF_2	N5	VREF
2	VCCO_2	VCCO_2	M9	VCCO
2	VCCO_2	VCCO_2	R4	VCCO
2	VCCO_2	VCCO_2	R8	VCCO
2	VCCO_2	VCCO_2	R12	VCCO
3	IO_L01N_3	IO_L01N_3	C1	I/O
3	IO_L01P_3	IO_L01P_3	C2	I/O
3	IO_L02N_3	IO_L02N_3	D3	I/O
3	IO_L02P_3	IO_L02P_3	D4	I/O
3	IO_L03N_3	IO_L03N_3	E1	I/O
3	IO_L03P_3	IO_L03P_3	D1	I/O
3	N.C. (◆)	IO_L05N_3	E2	I/O
3	N.C. (◆)	IO_L05P_3	E3	I/O
3	N.C. (◆)	IO_L07N_3	G4	I/O
3	N.C. (◆)	IO_L07P_3	F3	I/O
3	IO_L08N_3/ VREF_3	IO_L08N_3/ VREF_3	G1	VREF
3	IO_L08P_3	IO_L08P_3	F1	I/O
3	N.C. (◆)	IO_L09N_3	H4	I/O
3	N.C. (◆)	IO_L09P_3	G3	I/O
3	N.C. (◆)	IO_L10N_3	H5	I/O
3	N.C. (◆)	IO_L10P_3	H6	I/O
3	IO_L11N_3/ LHCLK1	IO_L11N_3/ LHCLK1	H1	LHCLK
3	IO_L11P_3/ LHCLK0	IO_L11P_3/ LHCLK0	G2	LHCLK
3	IO_L12N_3/ IRDY2/LHCLK3	IO_L12N_3/ IRDY2/LHCLK3	J3	LHCLK
3	IO_L12P_3/ LHCLK2	IO_L12P_3/ LHCLK2	H3	LHCLK

Table 69: Spartan-3A FT256 Pinout (XC3S700A,

Bank	XC3S700A XC3S1400A	FT256 Ball	Type
1	IO_L20P_1/A18	E14	DUAL
1	IO_L22N_1/A21	D15	DUAL
1	IO_L22P_1/A20	D16	DUAL
1	IO_L23N_1/A23	D14	DUAL
1	IO_L23P_1/A22	E13	DUAL
1	IO_L24N_1/A25	C15	DUAL
1	IO_L24P_1/A24	C16	DUAL
1	IP_1/VREF_1	H12	VREF
1	IP_1/VREF_1	J14	VREF
1	IP_1/VREF_1	M13	VREF
1	IP_1/VREF_1	M14	VREF
1	VCCO_1	E15	VCCO
1	VCCO_1	J15	VCCO
1	VCCO_1	N15	VCCO
2	IO_L01N_2/M0	P4	DUAL
2	IO_L01P_2/M1	N4	DUAL
2	IO_L02N_2/CSO_B	T2	DUAL
2	IO_L02P_2/M2	R2	DUAL
2	IO_L03N_2/VS2	T3	DUAL
2	IO_L03P_2/RDWR_B	R3	DUAL
2	IO_L04N_2/VS0	P5	DUAL
2	IO_L04P_2/VS1	N6	DUAL
2	IO_L05N_2	R5	I/O
2	IO_L05P_2	T4	I/O
2	IO_L06N_2/D6	T6	DUAL
2	IO_L06P_2/D7	T5	DUAL
2	IO_L08N_2/D4	N8	DUAL
2	IO_L08P_2/D5	P7	DUAL
2	IO_L09N_2/GCLK13	T7	GCLK
2	IO_L09P_2/GCLK12	R7	GCLK
2	IO_L10N_2/GCLK15	T8	GCLK
2	IO_L10P_2/GCLK14	P8	GCLK
2	IO_L11N_2/GCLK1	P9	GCLK
2	IO_L11P_2/GCLK0	N9	GCLK
2	IO_L12N_2/GCLK3	T9	GCLK
2	IO_L12P_2/GCLK2	R9	GCLK
2	IO_L14N_2/MOSI/CSI_B	P10	DUAL
2	IO_L14P_2	T10	I/O
2	IO_L15N_2/DOUT	R11	DUAL
2	IO_L15P_2/AWAKE	T11	PWRMGT

Table 69: Spartan-3A FT256 Pinout (XC3S700A,

Bank	XC3S700A XC3S1400A	FT256 Ball	Type
2	IO_L16N_2	N11	I/O
2	IO_L16P_2	P11	I/O
2	IO_L17N_2/D3	P12	DUAL
2	IO_L17P_2/INIT_B	T12	DUAL
2	IO_L18N_2/D1	R13	DUAL
2	IO_L18P_2/D2	T13	DUAL
2	IO_L19N_2	P13	I/O
2	IO_L19P_2	N12	I/O
2	IO_L20N_2/CCLK	R14	DUAL
2	IO_L20P_2/D0/DIN/MISO	T14	DUAL
2	IP_2/VREF_2	M11	VREF
2	IP_2/VREF_2	M7	VREF
2	IP_2/VREF_2	M9	VREF
2	IP_2/VREF_2	N5	VREF
2	IP_2/VREF_2	P6	VREF
2	VCCO_2	R12	VCCO
2	VCCO_2	R4	VCCO
2	VCCO_2	R8	VCCO
3	IO_L01N_3	C1	I/O
3	IO_L01P_3	C2	I/O
3	IO_L02N_3	D3	I/O
3	IO_L02P_3	D4	I/O
3	IO_L03N_3	E1	I/O
3	IO_L03P_3	D1	I/O
3	IO_L04N_3	F4	I/O
3	IO_L04P_3	E4	I/O
3	IO_L05N_3	E2	I/O
3	IO_L05P_3	E3	I/O
3	IO_L07N_3	G3	I/O
3	IO_L07P_3	F3	I/O
3	IO_L08N_3/VREF_3	G1	VREF
3	IO_L08P_3	F1	I/O
3	IO_L11N_3/LHCLK1	H1	LHCLK
3	IO_L11P_3/LHCLK0	G2	LHCLK
3	IO_L12N_3/IRDY2/LHCLK3	J3	LHCLK
3	IO_L12P_3/LHCLK2	H3	LHCLK
3	IO_L14N_3/LHCLK5	J1	LHCLK
3	IO_L14P_3/LHCLK4	J2	LHCLK
3	IO_L15N_3/LHCLK7	K1	LHCLK
3	IO_L15P_3/TRDY2/LHCLK6	K3	LHCLK

FT256 Footprint (XC3S700A, XC3S1400A)

		Bank 0																
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
Bank 3	A	GND	PROG_B	I/O L19P_0	I/O L18P_0	I/O L17P_0	I/O L15P_0	I/O L13P_0	I/O L12P_0 GCLK10	I/O L10N_0 GCLK7	I/O L08N_0	I/O L07N_0	I/O L05N_0	I/O L04N_0	I/O L04P_0	TCK	GND	
	B	TDI	TMS	I/O L19N_0	I/O L18N_0	VCCO_0	I/O L15N_0	GND	I/O L12N_0 GCLK11	VCCO_0	I/O L08P_0	GND	I/O L05P_0	VCCO_0	I/O L02N_0	I/O L02P_0 VREF_0	TDO	
	C	I/O L01N_3	I/O L01P_3	GND	I/O L20P_0 VREF_0	I/O L17N_0	I/O L16N_0	I/O L13N_0	I/O L11P_0 GCLK8	I/O L10P_0 GCLK6	I/O L09P_0 GCLK4	I/O L07P_0	I/O L03P_0	I/O L01N_0	GND	I/O L24N_1 A25	I/O L24P_1 A24	
	D	I/O L03P_3	VCCO_3	I/O L02N_3	I/O L02P_3	I/O L20N_0 PUDC_B	VCCAUX	I/O L16P_0	I/O L11N_0 GCLK9	I/O L09N_0 GCLK5	I/O L06N_0 VREF_0	I/O L06P_0	I/O L03N_0	I/O L01P_0	I/O L23N_1 A23	I/O L22N_1 A21	I/O L22P_1 A20	
	E	I/O L03N_3	I/O L05N_3	I/O L05P_3	I/O L04P_3	GND	INPUT	I/O L14N_0 VREF_0	VCCO_0	I/O L14P_0	GND	VCCAUX	GND	I/O L23P_1 A22	I/O L20P_1 A18	VCCO_1	I/O L18P_1 A14	
	F	I/O L08P_3	GND	I/O L07P_3	I/O L04N_3	VCCAUX	GND	GND	GND	GND	VCCINT	GND	VCCAUX	GND	I/O L20N_1 A19	I/O L19N_1 A17	I/O L18N_1 A15	I/O L16N_1 A11
	G	I/O L08N_3 VREF_3	I/O L11P_3 LHCLK0	I/O L07N_3	INPUT VREF_3	GND	GND	VCCINT	GND	VCCINT	GND	VCCINT	GND	I/O L19P_1 A16	I/O L17N_1 A13	GND	I/O L16P_1 A10	
	H	I/O L11N_3 LHCLK1	VCCO_3	I/O L12P_3 LHCLK2	VCCAUX	GND	VCCINT	GND	VCCINT	GND	VCCINT	GND	INPUT VREF_1	I/O L17P_1 A12	VCCAUX	I/O L15P_1 IRDY1 RHCLK6	I/O L15N_1 RHCLK7	
	J	I/O L14N_3 LHCLK5	I/O L14P_3 LHCLK4	I/O L12N_3 IRDY2 LHCLK3	INPUT	INPUT VREF_3	GND	VCCINT	GND	VCCINT	GND	VCCINT	I/O L10P_1 A8	I/O L10N_1 A9	INPUT VREF_1	VCCO_1	I/O L12N_1 TRDY1 RHCLK3	
	K	I/O L15N_3 LHCLK7	GND	I/O L15P_3 TRDY2 LHCLK6	I/O L18P_3	GND	VCCINT	GND	VCCINT	GND	VCCINT	GND	GND	I/O L06N_1 A3	I/O L11N_1 RHCLK1	I/O L11P_1 RHCLK0	I/O L12P_1 RHCLK2	
	L	I/O L16P_3 VREF_3	I/O L16N_3	I/O L18N_3	I/O L19N_3	VCCAUX	GND	VCCINT	GND	VCCINT	GND	GND	VCCAUX	I/O L06P_1 A2	I/O L08P_1 A6	GND	I/O L08N_1 A7	
	M	I/O L20P_3	VCCO_3	I/O L19P_3	I/O L24N_3	GND	VCCAUX	INPUT VREF_2	GND	INPUT VREF_2	VCCAUX	INPUT VREF_2	GND	INPUT VREF_1	INPUT VREF_1	I/O L07P_1 A4	I/O L07N_1 A5	
	N	I/O L20N_3	I/O L22P_3 VREF_3	I/O L24P_3	I/O L01P_2 M1	INPUT VREF_2	I/O L04P_2 VS1	GND	I/O L08N_2 D4	I/O L11P_2 GCLK0	GND	I/O L16N_2	I/O L19P_2	I/O L01P_1 HDC	I/O L01N_1 LDC2	VCCO_1	I/O L03N_1 A1	
	P	I/O L22N_3	I/O L23N_3	GND	I/O L01N_2 M0	I/O L04N_2 VS0	INPUT VREF_2	I/O L08P_2 D5	I/O L10P_2 GCLK14	I/O L11N_2 GCLK1	I/O L14N_2 MOSI CSI_B	I/O L16P_2	I/O L17N_2 D3	I/O L19N_2	GND	I/O L02N_1 LDC0	I/O L03P_1 A0	
	R	I/O L23P_3	I/O L02P_2 M2	I/O L03P_2 RDWR_B	VCCO_2	I/O L05N_2	GND	I/O L09P_2 GCLK12	VCCO_2	I/O L12P_2 GCLK2	GND	I/O L15N_2 DOUT	VCCO_2	I/O L18N_2 D1	I/O L20N_2 CCLK	I/O L02P_1 LDC1	SUSPEND	
	T	GND	I/O L02N_2 CSO_B	I/O L03N_2 VS2	I/O L05P_2	I/O L06P_2 D7	I/O L06N_2 D6	I/O L09N_2 GCLK13	I/O L10N_2 GCLK15	I/O L12N_2 GCLK3	I/O L14P_2	I/O L15P_2 AWAKE	I/O L17P_2 INIT_B	I/O L18P_2 D2	I/O L20P_2 DO/DIN MISO	DONE	GND	
		Bank 2																

Figure 22: XC3S700A and XC3S1400A FT256 Package Footprint (Top View)

DS529-4_012009

- 59** I/O: Unrestricted, general-purpose user I/O
- 2** INPUT: Unrestricted, general-purpose input pin
- 2** CONFIG: Dedicated configuration pins
- 0** N.C.: Not connected
- 51** DUAL: Configuration, then possible user I/O
- 30** CLK: User I/O, input, or global buffer input
- 4** JTAG: Dedicated JTAG port pins
- 50** GND: Ground
- 18** VREF: User I/O or input voltage reference for bank
- 13** VCCO: Output voltage supply for bank
- 15** VCCINT: Internal core supply voltage (+1.2V)
- 10** VCCAUX: Auxiliary supply voltage
- 2** SUSPEND: Dedicated SUSPEND and dual-purpose AWAKE Power Management pins

Table 81: Spartan-3A FG400 Pinout(Continued)

Bank	Pin Name	FG400 Ball	Type
2	IO_L28P_2	Y16	I/O
2	IO_L29N_2	U16	I/O
2	IO_L29P_2	V16	I/O
2	IO_L30N_2	Y18	I/O
2	IO_L30P_2	Y17	I/O
2	IO_L31N_2	U17	I/O
2	IO_L31P_2	V17	I/O
2	IO_L32N_2/CCCLK	Y19	DUAL
2	IO_L32P_2/D0/DIN/MISO	W18	DUAL
2	IP_2	P9	INPUT
2	IP_2	P12	INPUT
2	IP_2	P13	INPUT
2	IP_2	R8	INPUT
2	IP_2	R10	INPUT
2	IP_2	T11	INPUT
2	IP_2/VREF_2	N9	VREF
2	IP_2/VREF_2	N12	VREF
2	IP_2/VREF_2	P8	VREF
2	IP_2/VREF_2	P10	VREF
2	IP_2/VREF_2	P11	VREF
2	IP_2/VREF_2	R14	VREF
2	VCCO_2	R11	VCCO
2	VCCO_2	U8	VCCO
2	VCCO_2	U14	VCCO
2	VCCO_2	W5	VCCO
2	VCCO_2	W11	VCCO
2	VCCO_2	W17	VCCO
3	IO_L01N_3	D3	I/O
3	IO_L01P_3	D4	I/O
3	IO_L02N_3	C2	I/O
3	IO_L02P_3	B1	I/O
3	IO_L03N_3	D2	I/O
3	IO_L03P_3	C1	I/O
3	IO_L05N_3	E1	I/O
3	IO_L05P_3	D1	I/O
3	IO_L06N_3	G5	I/O
3	IO_L06P_3	F4	I/O
3	IO_L07N_3	J5	I/O
3	IO_L07P_3	J6	I/O
3	IO_L08N_3	H4	I/O

Table 81: Spartan-3A FG400 Pinout(Continued)

Bank	Pin Name	FG400 Ball	Type
3	IO_L08P_3	H6	I/O
3	IO_L09N_3	G4	I/O
3	IO_L09P_3	F3	I/O
3	IO_L10N_3	F2	I/O
3	IO_L10P_3	E3	I/O
3	IO_L12N_3	H2	I/O
3	IO_L12P_3	G3	I/O
3	IO_L13N_3/VREF_3	G1	VREF
3	IO_L13P_3	F1	I/O
3	IO_L14N_3	H3	I/O
3	IO_L14P_3	J4	I/O
3	IO_L16N_3	J2	I/O
3	IO_L16P_3	J3	I/O
3	IO_L17N_3/LHCLK1	K2	LHCLK
3	IO_L17P_3/LHCLK0	J1	LHCLK
3	IO_L18N_3/IRDY2/LHCLK3	L3	LHCLK
3	IO_L18P_3/LHCLK2	K3	LHCLK
3	IO_L20N_3/LHCLK5	L5	LHCLK
3	IO_L20P_3/LHCLK4	K4	LHCLK
3	IO_L21N_3/LHCLK7	M1	LHCLK
3	IO_L21P_3/TRDY2/LHCLK6	L1	LHCLK
3	IO_L22N_3	M3	I/O
3	IO_L22P_3/VREF_3	M2	VREF
3	IO_L24N_3	M5	I/O
3	IO_L24P_3	M4	I/O
3	IO_L25N_3	N2	I/O
3	IO_L25P_3	N1	I/O
3	IO_L26N_3	N4	I/O
3	IO_L26P_3	N3	I/O
3	IO_L28N_3	R1	I/O
3	IO_L28P_3	P1	I/O
3	IO_L29N_3	P4	I/O
3	IO_L29P_3	P3	I/O
3	IO_L30N_3	R3	I/O
3	IO_L30P_3	R2	I/O
3	IO_L32N_3	T2	I/O
3	IO_L32P_3/VREF_3	T1	VREF
3	IO_L33N_3	R4	I/O
3	IO_L33P_3	T3	I/O
3	IO_L34N_3	U3	I/O

Bank 0											A
12	13	14	15	16	17	18	19	20	21	22	
I/O L18P_0 GCLK6	I/O L16N_0	I/O L13N_0	I/O L12N_0 VREF_0	I/O L12P_0	I/O L10N_0	I/O L05N_0	I/O L06N_0	I/O L03N_0	TCK	GND	B
GND	I/O L16P_0	VCCO_0	I/O L13P_0	GND	I/O L10P_0	VCCO_0	I/O L06P_0 VREF_0	I/O L03P_0	I/O L45N_1 A23	I/O L45P_1 A22	C
I/O L17P_0 GCLK4	I/O L15N_0	I/O L09P_0	I/O L11N_0	I/O L08N_0	I/O L07N_0	I/O L05P_0	I/O L02N_0	GND	I/O L44N_1 A21	I/O L44P_1 A20	D
VCCAUX	I/O L15P_0	GND	I/O L11P_0	I/O L08P_0	I/O L07P_0	I/O L01N_0	I/O L02P_0 VREF_0	I/O L42N_1	I/O L42P_1	I/O L41N_1	E
I/O L17N_0 GCLK5	I/O L14N_0	I/O L09N_0	I/O L04P_0	INPUT	I/O L01P_0	VCCAUX	TDO	I/O L38P_1	VCCO_1	I/O L41P_1	F
INPUT	I/O L14P_0	VCCO_0	I/O L04N_0	INPUT	GND	I/O L40N_1	I/O L40P_1	I/O L38N_1	I/O L34N_1 A19	I/O L34P_1 A18	G
INPUT	INPUT	INPUT	INPUT	INPUT	I/O L46N_1 A25	I/O L46P_1 A24	I/O L36P_1	I/O L36N_1	GND	I/O L30N_1 A15	H
INPUT VREF_0	INPUT	INPUT	INPUT L47N_1	INPUT L47P_1 VREF_1	INPUT L39P_1	INPUT L39N_1	I/O L37N_1	I/O L33N_1 A17	I/O L33P_1 A16	I/O L30P_1 A14	J
VCCINT	GND	GND	INPUT L43N_1 VREF_1	INPUT L43P_1	VCCO_1	I/O L37P_1	GND	I/O L29N_1 A13	I/O L29P_1 A12	I/O L26N_1 A11	K
GND	VCCINT	INPUT L35P_1 VREF_1	INPUT L35N_1	INPUT L31N_1	I/O L32P_1	I/O L32N_1	I/O L25N_1 RHCLK7	I/O L25P_1 IRDY1 RHCLK6	VCCO_1	I/O L26P_1 A10	L
VCCINT	GND	VCCINT	INPUT L31P_1	INPUT L27N_1	GND	I/O L28P_1	I/O L28N_1	I/O L22N_1 TRDY1 RHCLK3	I/O L22P_1 RHCLK2	I/O L21N_1 RHCLK1	M
GND	VCCINT	GND	INPUT L27P_1 VREF_1	INPUT L23N_1	INPUT L23P_1	I/O L24P_1 RHCLK4	VCCAUX	I/O L24N_1 RHCLK5	GND	I/O L21P_1 RHCLK0	N
VCCINT	GND	VCCINT	INPUT L16P_1	INPUT L16N_1 VREF_1	I/O L20N_1 A9	I/O L20P_1 A8	I/O L19N_1 A7	I/O L19P_1 A6	I/O L18N_1 A5	I/O L18P_1 A4	P
INPUT	VCCINT	GND	INPUT L08P_1	INPUT L08N_1	VCCO_1	I/O L17N_1 A3	GND	I/O L15P_1	VCCO_1	I/O L15N_1 VREF_1	R
INPUT VREF_2	INPUT VREF_2	INPUT VREF_2	INPUT L04P_1	INPUT L04N_1 VREF_1	INPUT L12P_1	INPUT L12N_1 VREF_1	I/O L17P_1 A2	I/O L13P_1	I/O L14P_1	I/O L14N_1	T
GND	INPUT	INPUT	INPUT VREF_2	INPUT VREF_2	I/O L03P_1 A0	I/O L03N_1 A1	I/O L13N_1	I/O L11P_1	GND	I/O L11N_1	U
I/O L20N_2 GCLK3	I/O L26N_2 D3	VCCO_2	INPUT	INPUT	GND	SUSPEND	I/O L10N_1	I/O L10P_1	I/O L09N_1	I/O L09P_1	V
I/O L20P_2 GCLK2	I/O L26P_2 INIT_B	I/O L30P_2	I/O L30N_2	I/O L31N_2	I/O L33N_2	VCCAUX	I/O L06P_1	I/O L06N_1	VCCO_1	I/O L07N_1	W
I/O L18P_2 GCLK14	I/O L23P_2	GND	I/O L25P_2	I/O L31P_2	I/O L34N_2	I/O L33P_2	I/O L02P_1 LDC1	I/O L02N_1 LDC0	I/O L05N_1	I/O L07P_1	Y
I/O L18N_2 GCLK15	I/O L21N_2	I/O L23N_2	I/O L25N_2	I/O L27N_2	I/O L28N_2 D1	I/O L34P_2	DONE	GND	I/O L01N_1 LDC2	I/O L05P_1	A
I/O L19P_2 GCLK0	VCCO_2	I/O L22P_2	I/O L24N_2 DOUT	GND	I/O L28P_2 D2	VCCO_2	I/O L32N_2	I/O L36N_2 CCLK	I/O L35N_2	I/O L01P_1 HDC	A
I/O L19N_2 GCLK1	I/O L21P_2	I/O L22N_2 MOSI CSI_B	I/O L24P_2 AWAKE	I/O L27P_2	I/O L29P_2	I/O L29N_2	I/O L32P_2	I/O L36P_2 D0 DIN/MISO	I/O L35P_2	GND	B

Right Half of FG484 Package (Top View)

DS529-4_02_012009

Figure 26:

Table 87: Spartan-3A FG676 Pinout(Continued)

Bank	Pin Name	FG676 Ball	Type
1	IO_L03P_1/A0	AC23	DUAL
1	IO_L04N_1	W21	I/O
1	IO_L04P_1	W20	I/O
1	IO_L05N_1	AC25	I/O
1	IO_L05P_1	AD26	I/O
1	IO_L06N_1	AB26	I/O
1	IO_L06P_1	AC26	I/O
1	IO_L07N_1/VREF_1	AB24	VREF
1	IO_L07P_1	AB23	I/O
1	IO_L08N_1	V19	I/O
1	IO_L08P_1	V18	I/O
1	IO_L09N_1	AA23	I/O
1	IO_L09P_1	AA22	I/O
1	IO_L10N_1	U20	I/O
1	IO_L10P_1	V21	I/O
1	IO_L11N_1	AA25	I/O
1	IO_L11P_1	AA24	I/O
1	IO_L12N_1	U18	I/O
1	IO_L12P_1	U19	I/O
1	IO_L13N_1	Y23	I/O
1	IO_L13P_1	Y22	I/O
1	IO_L14N_1	T20	I/O
1	IO_L14P_1	U21	I/O
1	IO_L15N_1	Y25	I/O
1	IO_L15P_1	Y24	I/O
1	IO_L17N_1	T17	I/O
1	IO_L17P_1	T18	I/O
1	IO_L18N_1	V22	I/O
1	IO_L18P_1	W23	I/O
1	IO_L19N_1	V25	I/O
1	IO_L19P_1	V24	I/O
1	IO_L21N_1	U22	I/O
1	IO_L21P_1	V23	I/O
1	IO_L22N_1	R20	I/O
1	IO_L22P_1	R19	I/O
1	IO_L23N_1/VREF_1	U24	VREF
1	IO_L23P_1	U23	I/O
1	IO_L25N_1/A3	R22	DUAL
1	IO_L25P_1/A2	R21	DUAL
1	IO_L26N_1/A5	T24	DUAL

Table 87: Spartan-3A FG676 Pinout(Continued)

Bank	Pin Name	FG676 Ball	Type
1	IO_L26P_1/A4	T23	DUAL
1	IO_L27N_1/A7	R17	DUAL
1	IO_L27P_1/A6	R18	DUAL
1	IO_L29N_1/A9	R26	DUAL
1	IO_L29P_1/A8	R25	DUAL
1	IO_L30N_1/RHCLK1	P20	RHCLK
1	IO_L30P_1/RHCLK0	P21	RHCLK
1	IO_L31N_1/TRDY1/RHCLK3	P25	RHCLK
1	IO_L31P_1/RHCLK2	P26	RHCLK
1	IO_L33N_1/RHCLK5	N24	RHCLK
1	IO_L33P_1/RHCLK4	P23	RHCLK
1	IO_L34N_1/RHCLK7	N19	RHCLK
1	IO_L34P_1/IRDY1/RHCLK6	P18	RHCLK
1	IO_L35N_1/A11	M25	DUAL
1	IO_L35P_1/A10	M26	DUAL
1	IO_L37N_1	N21	I/O
1	IO_L37P_1	P22	I/O
1	IO_L38N_1/A13	M23	DUAL
1	IO_L38P_1/A12	L24	DUAL
1	IO_L39N_1/A15	N17	DUAL
1	IO_L39P_1/A14	N18	DUAL
1	IO_L41N_1	K26	I/O
1	IO_L41P_1	K25	I/O
1	IO_L42N_1/A17	M20	DUAL
1	IO_L42P_1/A16	N20	DUAL
1	IO_L43N_1/A19	J25	DUAL
1	IO_L43P_1/A18	J26	DUAL
1	IO_L45N_1	M22	I/O
1	IO_L45P_1	M21	I/O
1	IO_L46N_1	K22	I/O
1	IO_L46P_1	K23	I/O
1	IO_L47N_1	M18	I/O
1	IO_L47P_1	M19	I/O
1	IO_L49N_1	J22	I/O
1	IO_L49P_1	J23	I/O
1	IO_L50N_1	K21	I/O
1	IO_L50P_1	L22	I/O
1	IO_L51N_1	G24	I/O
1	IO_L51P_1	G23	I/O
1	IO_L53N_1	K20	I/O

FG676 Footprint

Left Half of FG676 Package (Top View)

- 313 I/O: Unrestricted, general-purpose user I/O
- 67 INPUT: Unrestricted, general-purpose input pin
- 51 DUAL: Configuration pins, then possible user I/O
- 2 SUSPEND: Dedicated SUSPEND and dual-purpose AWAKE Power Management pins
- 38 VREF: User I/O or input voltage reference for bank
- 32 CLK: User I/O, input, or clock buffer input
- 2 CONFIG: Dedicated configuration pins
- 4 JTAG: Dedicated JTAG port pins
- 77 GND: Ground
- 36 VCCO: Output voltage supply for bank
- 23 VCCINT: Internal core supply voltage (+1.2V)
- 14 VCCAUX: Auxiliary supply voltage
- 17 N.C.: Not connected

		Bank 0												
		1	2	3	4	5	6	7	8	9	10	11	12	13
Bank 3	A	GND	PROG_B	I/O L51P_0	I/O L45P_0	INPUT	GND	INPUT	I/O L38P_0	I/O L36P_0	I/O L33P_0	GND	I/O L29P_0	INPUT
	B	I/O L02N_3	I/O L02P_3	I/O L51N_0	I/O L45N_0	VCCO_0	I/O L41P_0	I/O L42P_0	I/O L38N_0	I/O L36N_0	I/O L33N_0	VCCO_0	I/O L29N_0	I/O L28P_0 GCLK10
	C	INPUT L04N_3 VREF_3	INPUT L04P_3	GND	INPUT	I/O L44P_0	I/O L41N_0	I/O L42N_0	I/O L40P_0	GND	I/O L34P_0	I/O L32P_0	I/O L30N_0	I/O L28N_0 GCLK11
	D	INPUT L08N_3	INPUT L08P_3	I/O L06P_3	TMS	N.C.	I/O L44N_0	INPUT VREF_0	I/O L40N_0	I/O L37N_0	I/O L34N_0	I/O L32N_0 VREF_0	INPUT	I/O L30P_0
	E	I/O L11P_3	VCCO_3	I/O L07P_3	I/O L06N_3	VCCAUX	N.C.	I/O L48N_0	VCCO_0	N.C.	I/O L37P_0	INPUT	I/O L31P_0	VCCO_0
	F	GND	I/O L11N_3	I/O L14N_3	I/O L07N_3	I/O L09P_3	GND	I/O L48P_0	I/O L52P_0 VREF_0	N.C.	INPUT	GND	I/O L31N_0	I/O L27P_0 GCLK8
	G	INPUT L16N_3	INPUT L16P_3	I/O L14P_3	I/O L09N_3	INPUT L12P_3	I/O L03P_3	TDI	I/O L52N_0 PUDC_B	I/O L47P_0	I/O L46P_0	INPUT VREF_0	I/O L35P_0	I/O L27N_0 GCLK9
	H	I/O L17N_3	I/O L17P_3	GND	INPUT L12N_3 VREF_3	VCCO_3	I/O L10N_3	I/O L03N_3	GND	I/O L47N_0	I/O L46N_0	VCCO_0	I/O L35N_0	INPUT
	J	INPUT L24P_3	INPUT L20N_3 VREF_3	INPUT L20P_3	I/O L19N_3	I/O L19P_3	I/O L13N_3	I/O L10P_3	I/O L01P_3	I/O L01N_3	INPUT	I/O L43P_0	I/O L39P_0	INPUT
	K	INPUT L24N_3	I/O L23N_3	I/O L23P_3	I/O L22N_3	I/O L22P_3	I/O L18P_3	I/O L13P_3	I/O L05N_3	I/O L05P_3	GND	I/O L43N_0	I/O L39N_0	VCCAUX
	L	GND	VCCO_3	I/O L25N_3	I/O L25P_3	VCCAUX	GND	I/O L18N_3	VCCO_3	I/O L15N_3	I/O L15P_3	GND	VCCINT	GND
	M	I/O L29N_3 VREF_3	I/O L29P_3	I/O L27N_3	I/O L27P_3	I/O L28P_3	I/O L28N_3	I/O L26N_3	I/O L26P_3	I/O L21N_3	I/O L21P_3	VCCINT	GND	VCCINT
	N	I/O L31P_3	I/O L31N_3	GND	I/O L30N_3	I/O L30P_3	I/O L32P_3 LHCLK0	I/O L32N_3 LHCLK1	GND	I/O L35P_3 TRDY2 LHCLK6	VCCAUX	GND	VCCINT	VCCINT
	P	I/O L33P_3 LHCLK2	I/O L33N_3 IRDY2 LHCLK3	I/O L34N_3 LHCLK5	I/O L34P_3 LHCLK4	VCCO_3	I/O L39N_3	I/O L39P_3	I/O L41P_3	I/O L41N_3	I/O L43P_3 LHCLK7	VCCINT	GND	VCCINT
	R	I/O L36P_3 VREF_3	I/O L36N_3	I/O L37P_3	I/O L37N_3	I/O L40P_3	I/O L40N_3	I/O L45N_3	I/O L45P_3	I/O L43N_3	I/O L43P_3 VREF_3	GND	VCCINT	GND
	T	GND	VCCO_3	I/O L38P_3	I/O L38N_3	I/O L42P_3	GND	I/O L51P_3	VCCO_3	I/O L48N_3	I/O L48P_3	VCCINT	GND	VCCINT
	U	I/O L44P_3	I/O L44N_3	INPUT L46P_3	I/O L42N_3	I/O L49P_3	I/O L51N_3	I/O L56P_3	I/O L56N_3	I/O L61P_3	GND	I/O L13N_2	VCCINT	GND
	V	I/O L47P_3	I/O L47N_3	GND	INPUT L46N_3	I/O L49N_3	I/O L59N_3	I/O L59P_3	I/O L61N_3	VCCAUX	I/O L09P_2	I/O L13P_2	I/O L16P_2	I/O L20P_2
	W	INPUT L50P_3	INPUT L50N_3 VREF_3	I/O L52P_3	I/O L52N_3	VCCO_3	I/O L63N_3	I/O L63P_3	GND	I/O L05P_2	I/O L09N_2	VCCO_2	I/O L16N_2	I/O L20N_2
Y	I/O L53P_3	I/O L53N_3	INPUT L54P_3	INPUT L54N_3	I/O L57P_3	I/O L57N_3	I/O L02P_2 M2	N.C.	I/O L05N_2	I/O L12P_2	INPUT	I/O L17P_2 RDWR_B	I/O L25N_2 GCLK13	
A	GND	I/O L55P_3	I/O L55N_3	INPUT L58P_3	INPUT L58N_3 VREF_3	GND	I/O L02N_2 CSO_B	N.C.	INPUT VREF_2	I/O L12N_2	GND	I/O L17N_2 VS2	I/O L25P_2 GCLK12	
A	I/O L60P_3	VCCO_3	INPUT L62P_3	INPUT L62N_3	VCCAUX	INPUT VREF_2	I/O L14N_2	VCCO_2	I/O L15P_2	INPUT VREF_2	VCCAUX	I/O L21P_2	INPUT	
A	I/O L60N_3	I/O L64P_3	I/O L64N_3	I/O L01P_2 M1	N.C.	I/O L08P_2	INPUT	I/O L14P_2	I/O L15N_2	INPUT VREF_2	I/O L23N_2	I/O L21N_2	INPUT	
A	I/O L65P_3	I/O L65N_3	GND	I/O L01N_2 M0	N.C.	I/O L08N_2	I/O L11P_2	GND	INPUT	INPUT	I/O L23P_2	INPUT VREF_2	GND	
A	INPUT L66P_3	INPUT L66N_3 VREF_3	I/O L06P_2	I/O L07P_2	VCCO_2	I/O L10N_2	I/O L11N_2	I/O L18P_2	I/O L19P_2 VS1	I/O L22P_2 D7	VCCO_2	I/O L24N_2 D4	I/O L28N_2 GCLK15	
A	GND	INPUT	I/O L06N_2	I/O L07N_2	I/O L10P_2	GND	INPUT	I/O L18N_2	I/O L19N_2 VS0	I/O L22N_2 D6	GND	I/O L24P_2 D5	I/O L28P_2 GCLK14	

Figure 27: FG676 Package Footprint (Top View)

DS529-4_07_102506