AMD Xilinx - XC3S50A-5TQG144C Datasheet

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Details	
Product Status	Active
Number of LABs/CLBs	176
Number of Logic Elements/Cells	1584
Total RAM Bits	55296
Number of I/O	108
Number of Gates	50000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s50a-5tqg144c

DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

Advance: Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

Production: These specifications are approved once the silicon has been characterized over numerous production lots. Parameter values are considered stable with no future changes expected.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan®-3A devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Absolute Maximum Ratings

Stresses beyond those listed under Table 4: Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 4: **Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Max	Units
V_{CCINT}	Internal supply voltage		–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage		–0.5	3.75	V
V_{CCO}	Output driver supply voltage		–0.5	3.75	V
V_{REF}	Input reference voltage		–0.5	V_{CCO} + 0.5	V
V_{IN}	Voltage applied to all User I/O pins and dual-purpose pins	Driver in a high-impedance state	–0.95	4.6	V
	Voltage applied to all Dedicated pins		–0.5	4.6	V
I_{IK}	Input clamp current per I/O pin	$-0.5V < V_{IN} < (V_{CCO} + 0.5V)$ (1)	–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model	–	±2000	V
		Charged device model	–	±500	V
		Machine model	–	±200	V
T_J	Junction temperature		–	125	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Upper clamp applies only when using PCI IOSTANDARDs.
2. For soldering guidelines, see UG112: *Device Packaging and Thermal Characteristics* and XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

Quiescent Current Requirements

Table 10: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Typical(2)	Commercial Maximum(2)	Industrial Maximum(2)	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC3S50A	2	20	30	mA
		XC3S200A	7	50	70	mA
		XC3S400A	10	85	125	mA
		XC3S700A	13	120	185	mA
		XC3S1400A	24	220	310	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC3S50A	0.2	2	3	mA
		XC3S200A	0.2	2	3	mA
		XC3S400A	0.3	3	4	mA
		XC3S700A	0.3	3	4	mA
		XC3S1400A	0.3	3	4	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC3S50A	3	8	10	mA
		XC3S200A	5	12	15	mA
		XC3S400A	5	18	24	mA
		XC3S700A	6	28	34	mA
		XC3S1400A	10	50	58	mA

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8.
2. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using typical devices at room temperature (T_J of 25°C at V_{CCINT} = 1.2V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.6V, and V_{CCAUX} = 3.6V. The FPGA is programmed with a "blank" configuration data file (that is, a design with no functional elements instantiated). For conditions other than those described above (for example, a design including functional elements), measured quiescent current levels will be different than the values in the table.
3. For more accurate estimates for a specific design, use the Xilinx XPower tools. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3A FPGA XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer uses a netlist as input to provide maximum estimates as well as more accurate typical estimates.
4. The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.
5. For information on the power-saving Suspend mode, see XAPP480: *Using Suspend Mode in Spartan-3 Generation FPGAs*. Suspend mode typically saves 40% total power consumption compared to quiescent current.

Table 20: **Setup and Hold Times for the IOB Input Path *(Continued)***

Symbol	Description	Conditions	IFD_DELAY_VALUE	Device	Speed Grade -5 Min	Speed Grade -4 Min	Units
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). The Input Delay is programmed.	LVCMOS25(2)	1	XC3S700A	1.82	1.95	ns
			2		2.62	2.83	ns
			3		3.32	3.72	ns
			4		3.83	4.31	ns
			5		3.69	4.14	ns
			6		4.60	5.19	ns
			7		5.39	6.10	ns
			8		5.92	6.73	ns
			1	XC3S1400A	1.79	2.17	ns
			2		2.55	2.92	ns
			3		3.38	3.76	ns
			4		3.75	4.32	ns
			5		3.81	4.19	ns
			6		4.39	5.09	ns
			7		5.16	5.98	ns
			8		5.69	6.57	ns
Hold Times							
T_{IOICKP}	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. No Input Delay is programmed.	LVCMOS25(3)	0	XC3S50A	–0.66	–0.64	ns
				XC3S200A	–0.85	–0.65	ns
				XC3S400A	–0.42	–0.42	ns
				XC3S700A	–0.81	–0.67	ns
				XC3S1400A	–0.71	–0.71	ns
$T_{IOICKPD}$	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25(3)	1	XC3S50A	–0.88	–0.88	ns
			2		–1.33	–1.33	ns
			3		–2.05	–2.05	ns
			4		–2.43	–2.43	ns
			5		–2.34	–2.34	ns
			6		–2.81	–2.81	ns
			7		–3.03	–3.03	ns
			8		–3.83	–3.57	ns
			1	XC3S200A	–1.51	–1.51	ns
			2		–2.09	–2.09	ns
			3		–2.40	–2.40	ns
			4		–2.68	–2.68	ns
			5		–2.56	–2.56	ns
			6		–2.99	–2.99	ns
			7		–3.29	–3.29	ns
			8		–3.61	–3.61	ns

Table 22: **Propagation Times for the IOB Input Path *(Continued)***

Symbol	Description	Conditions	DELAY_VALUE	Device	Speed Grade		Units
					-5	-4	
					Max	Max	
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25(2)	5	XC3S400A	3.55	4.18	ns
			6		4.34	5.03	ns
			7		5.09	5.88	ns
			8		5.58	6.42	ns
			1	XC3S700A	1.96	2.18	ns
			2		2.76	3.06	ns
			3		3.45	3.95	ns
			4		3.97	4.54	ns
			5		3.83	4.37	ns
			6		4.74	5.42	ns
			7		5.53	6.33	ns
			8		6.06	6.96	ns
			1	XC3S1400A	1.93	2.40	ns
			2		2.69	3.15	ns
			3		3.52	3.99	ns
			4		3.89	4.55	ns
			5		3.95	4.42	ns
			6		4.53	5.32	ns
			7		5.30	6.21	ns
			8		5.83	6.80	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 23.

Output Timing Adjustments

Table 26: **Output Timing Adjustments for IOB**

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
Single-Ended Standards					
LVTTL	Slow	2 mA	5.58	5.58	ns
		4 mA	3.16	3.16	ns
		6 mA	3.17	3.17	ns
		8 mA	2.09	2.09	ns
		12 mA	1.62	1.62	ns
		16 mA	1.24	1.24	ns
		24 mA	2.74(3)	2.74(3)	ns
	Fast	2 mA	3.03	3.03	ns
		4 mA	1.71	1.71	ns
		6 mA	1.71	1.71	ns
		8 mA	0.53	0.53	ns
		12 mA	0.53	0.53	ns
		16 mA	0.59	0.59	ns
		24 mA	0.60	0.60	ns
	QuietIO	2 mA	27.67	27.67	ns
		4 mA	27.67	27.67	ns
		6 mA	27.67	27.67	ns
		8 mA	16.71	16.71	ns
		12 mA	16.67	16.67	ns
		16 mA	16.22	16.22	ns
		24 mA	12.11	12.11	ns

Table 26: **Output Timing Adjustments for IOB*(Continued)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS33	Slow	2 mA	5.58	5.58	ns
		4 mA	3.17	3.17	ns
		6 mA	3.17	3.17	ns
		8 mA	2.09	2.09	ns
		12 mA	1.24	1.24	ns
		16 mA	1.15	1.15	ns
		24 mA	2.55(3)	2.55(3)	ns
	Fast	2 mA	3.02	3.02	ns
		4 mA	1.71	1.71	ns
		6 mA	1.72	1.72	ns
		8 mA	0.53	0.53	ns
		12 mA	0.59	0.59	ns
		16 mA	0.59	0.59	ns
		24 mA	0.51	0.51	ns
	QuietIO	2 mA	27.67	27.67	ns
		4 mA	27.67	27.67	ns
		6 mA	27.67	27.67	ns
		8 mA	16.71	16.71	ns
		12 mA	16.29	16.29	ns
		16 mA	16.18	16.18	ns
		24 mA	12.11	12.11	ns

Table 31: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output	–	1.69	–	2.01	ns
Setup Times						
T_{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	–0.07	–	–0.02	–	ns
T_{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.18	–	0.36	–	ns
T_{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.30	–	0.59	–	ns
Hold Times						
T_{DH}	Hold time of the BX and BY data inputs after the active transition at the CLK input of the distributed RAM	0.13	–	0.13	–	ns
T_{AH}, T_{WH}	Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM	0.01	–	0.01	–	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.88	–	1.01	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.

Table 32: **CLB Shift Register Switching Characteristics**

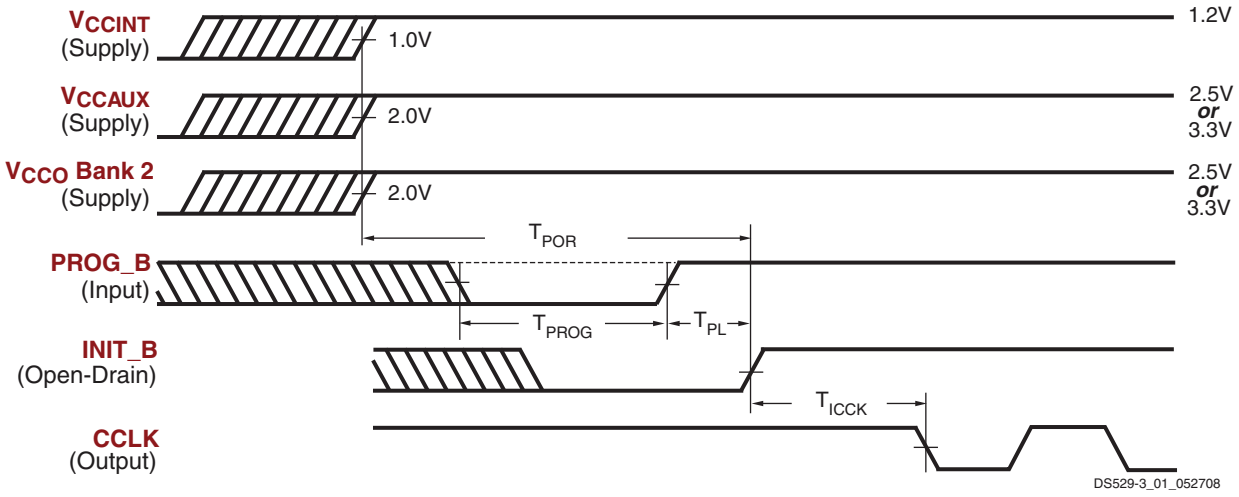
Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{REG}	Time from the active edge at the CLK input to data appearing on the shift register output	–	4.11	–	4.82	ns
Setup Times						
T_{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.13	–	0.18	–	ns
Hold Times						
T_{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0.16	–	0.16	–	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.90	–	1.01	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.

Configuration and JTAG Timing

General Configuration Power-On/Reconfigure Timing



Notes:

1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies can be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 11: **Waveforms for Power-On and the Beginning of Configuration**

Table 45: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	All	–	18	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	-	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XC3S50A	–	0.5	ms
		XC3S200A	–	0.5	ms
		XC3S400A	–	1	ms
		XC3S700A	–	2	ms
		XC3S1400A	–	2	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	250	–	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, and BPI modes.
4. For details on configuration, see UG332 *Spartan-3 Generation Configuration User Guide*.

Table 66: **Spartan-3A TQ144 Pinout*(Continued)***

Bank	Pin Name	Pin	Type
2	IO_L05P_2	P46	I/O
2	IO_L06N_2/D6	P49	DUAL
2	IO_L06P_2	P47	I/O
2	IO_L07N_2/D4	P51	DUAL
2	IO_L07P_2/D5	P50	DUAL
2	IO_L08N_2/GCLK15	P55	GCLK
2	IO_L08P_2/GCLK14	P54	GCLK
2	IO_L09N_2/GCLK1	P59	GCLK
2	IO_L09P_2/GCLK0	P57	GCLK
2	IO_L10N_2/GCLK3	P60	GCLK
2	IO_L10P_2/GCLK2	P58	GCLK
2	IO_L11N_2/DOUT	P64	DUAL
2	IO_L11P_2/AWAKE	P63	PWR MGMT
2	IO_L12N_2/D3	P68	DUAL
2	IO_L12P_2/INIT_B	P67	DUAL
2	IO_L13N_2/D0/DIN/MISO	P71	DUAL
2	IO_L13P_2/D2	P69	DUAL
2	IO_L14N_2/CCLK	P72	DUAL
2	IO_L14P_2/D1	P70	DUAL
2	IP_2/VREF_2	P53	VREF
2	VCCO_2	P40	VCCO
2	VCCO_2	P61	VCCO
3	IO_L01N_3	P6	I/O
3	IO_L01P_3	P4	I/O
3	IO_L02N_3	P5	I/O
3	IO_L02P_3	P3	I/O
3	IO_L03N_3	P8	I/O
3	IO_L03P_3	P7	I/O
3	IO_L04N_3/VREF_3	P11	VREF
3	IO_L04P_3	P10	I/O
3	IO_L05N_3/LHCLK1	P13	LHCLK
3	IO_L05P_3/LHCLK0	P12	LHCLK
3	IO_L06N_3/IRDY2/LHCLK3	P16	LHCLK
3	IO_L06P_3/LHCLK2	P15	LHCLK
3	IO_L07N_3/LHCLK5	P20	LHCLK
3	IO_L07P_3/LHCLK4	P18	LHCLK
3	IO_L08N_3/LHCLK7	P21	LHCLK
3	IO_L08P_3/TRDY2/LHCLK6	P19	LHCLK
3	IO_L09N_3	P25	I/O
3	IO_L09P_3	P24	I/O
3	IO_L10N_3	P29	I/O

Table 66: **Spartan-3A TQ144 Pinout*(Continued)***

Bank	Pin Name	Pin	Type
3	IO_L10P_3	P27	I/O
3	IO_L11N_3	P30	I/O
3	IO_L11P_3	P28	I/O
3	IO_L12N_3	P32	I/O
3	IO_L12P_3	P31	I/O
3	IP_L13N_3/VREF_3	P35	VREF
3	IP_L13P_3	P33	INPUT
3	VCCO_3	P14	VCCO
3	VCCO_3	P23	VCCO
GND	GND	P9	GND
GND	GND	P17	GND
GND	GND	P26	GND
GND	GND	P34	GND
GND	GND	P56	GND
GND	GND	P65	GND
GND	GND	P81	GND
GND	GND	P89	GND
GND	GND	P100	GND
GND	GND	P106	GND
GND	GND	P118	GND
GND	GND	P128	GND
GND	GND	P137	GND
VCCAUX	SUSPEND	P74	PWR MGMT
VCCAUX	DONE	P73	CONFIG
VCCAUX	PROG_B	P144	CONFIG
VCCAUX	TCK	P109	JTAG
VCCAUX	TDI	P2	JTAG
VCCAUX	TDO	P107	JTAG
VCCAUX	TMS	P1	JTAG
VCCAUX	VCCAUX	P36	VCCAUX
VCCAUX	VCCAUX	P66	VCCAUX
VCCAUX	VCCAUX	P108	VCCAUX
VCCAUX	VCCAUX	P133	VCCAUX
VCCINT	VCCINT	P22	VCCINT
VCCINT	VCCINT	P52	VCCINT
VCCINT	VCCINT	P94	VCCINT
VCCINT	VCCINT	P122	VCCINT

User I/Os by Bank

Table 67 indicates how the 108 available user-I/O pins are distributed between the four I/O banks on the TQ144 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 67: **User I/Os Per Bank for the XC3S50A in the TQ144 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	27	14	1	1	3	8
Right	1	25	11	0	4	2	8
Bottom	2	30	2	0	21	1	6
Left	3	26	15	1	0	2	8
TOTAL		**108**	**42**	**2**	**26**	**8**	**30**

Footprint Migration Differences

The XC3S50A FPGA is the only Spartan-3A device offered in the TQ144 package.

Footprint Migration Differences

Unconnected Balls on XC3S50A

Table 73 summarizes any footprint and functionality differences between the XC3S50A and the XC3S200A or XC3S400A FPGAs that might affect easy migration between these devices in the FT256 package. The XC3S200A and XC3S400A have identical pinouts. The XC3S50A pinout is compatible, but there are 52 balls that are different. Generally, designs easily migrate upward from the XC3S50A to either the XC3S200A or XC3S400A. If using differential I/O, see Table 74. If using the BPI configuration mode (parallel Flash), see Table 75.

Table 73: **FT256 XC3S50A Footprint Migration Difference**

FT256 Ball	Bank	XC3S50A Type	Migration	XC3S200A/ XC3S400A Type
A7	0	N.C.	→	I/O
A12	0	N.C.	→	I/O
B12	0	INPUT	→	I/O
C7	0	N.C.	→	I/O
D10	0	N.C.	→	I/O
E2	3	N.C.	→	I/O
E3	3	N.C.	→	I/O
E7	0	N.C.	→	I/O
E10	0	N.C.	→	I/O
E16	1	N.C.	→	I/O
F3	3	N.C.	→	I/O
F8	0	N.C.	→	I/O
F14	1	N.C.	→	I/O
F15	1	N.C.	→	I/O
F16	1	N.C.	→	I/O
G3	3	N.C.	→	I/O
G4	3	N.C.	→	I/O
G5	3	N.C.	→	INPUT
G6	3	N.C.	→	INPUT
G13	1	N.C.	→	I/O
G14	1	N.C.	→	I/O
G16	1	N.C.	→	I/O
H4	3	N.C.	→	I/O
H5	3	N.C.	→	I/O
H6	3	N.C.	→	I/O
H13	1	N.C.	→	I/O
J4	3	N.C.	→	I/O
J6	3	N.C.	→	I/O
J10	1	N.C.	→	INPUT
J11	1	N.C.	→	INPUT
K4	3	N.C.	→	I/O
K13	1	N.C.	→	I/O
L1	3	N.C.	→	I/O
L2	3	N.C.	→	I/O
L3	3	N.C.	→	I/O
L4	3	N.C.	→	I/O
L13	1	N.C.	→	I/O
L14	1	N.C.	→	I/O
L16	1	N.C.	→	I/O
M3	3	N.C.	→	I/O
M10	2	N.C.	→	I/O
M13	1	N.C.	→	I/O
M14	1	N.C.	→	I/O
M15	1	N.C.	→	I/O
M16	1	N.C.	→	I/O
N7	2	N.C.	→	I/O
N10	2	N.C.	→	I/O
N12	2	N.C.	→	I/O
P6	2	N.C.	→	I/O
P13	2	N.C.	→	I/O
R7	2	N.C.	→	I/O
T7	2	N.C.	→	I/O
DIFFERENCES			**52**	

Legend:

→ This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction is possible depending on how the pin is configured for the device on the right.

Differences Between XC3S200A/XC3S400A and XC3S700A/XC3S1400A

The XC3S700A and XC3S1400A FPGAs have several additional power and ground pins as compared to the XC3S200A and XC3S400A. Table 76 summarizes all the differences. All dedicated and dual-purpose configuration pins are in the same location.

Table 76: **Differences Between XC3S200A/XC3S400A and XC3S700A/XC3S1400A**

FT256 Ball	Bank	XC3S200A XC3S400A		XC3S700A XC3S1400A	
		Pin Name	Type	Pin Name	Type
F8	0	IO_L14P_0	I/O	GND	GND
D11	0	IO_L03N_0	I/O	IO_L06P_0	I/O
D10	0	IO_L06P_0	I/O	IO_L06N_0/ VREF_0	VREF
F7	0	IP_0	INPUT	GND	GND
F9	0	IP_0	INPUT	GND	GND
D12	0	IP_0	INPUT	IO_L03N_0	I/O
E9	0	IP_0/ VREF_0	INPUT	IO_L14P_0	I/O
D6	0	IP_0	INPUT	VCCAUX	VCCAUX
F10	0	IP_0	INPUT	VCCINT	VCCINT
E10	0	IO_L06N_0/ VREF_0	VREF	GND	GND
M13	1	IO_L05P_1	I/O	IP_1/ VREF_1	VREF
F11	1	IP_L25N_1	INPUT	GND	GND
H11	1	IP_L13N_1	INPUT	GND	GND
K11	1	IP_L04P_1	INPUT	GND	GND
G11	1	IP_L21N_1	INPUT	VCCINT	VCCINT
H10	1	IP_L13P_1	INPUT	VCCINT	VCCINT
J11	1	IP_L09N_1	INPUT	VCCINT	VCCINT
H14	1	IO_L14N_1/ RHCLK5	RHCLK	VCCAUX	VCCAUX
J14	1	IO_L14P_1/ RHCLK4	RHCLK	IP_1/ VREF_1	VREF
H12	1	VCCO_1	VCCO	IP_1/ VREF_1	VREF
G12	1	IP_L21P_1/ VREF_1	VREF	GND	GND
J10	1	IP_L09P_1/ VREF_1	VREF	GND	GND
K12	1	IP_L04N_1/ VREF_1	VREF	GND	GND
F12	1	IP_L25P_1/ VREF_1	VREF	VCCAUX	VCCAUX
M14	1	IO_L05N_1/ VREF_1	VREF	IP_1/ VREF_1	VREF
N7	2	IO_L07P_2	I/O	GND	GND
N10	2	IO_L13P_2	I/O	GND	GND
M10	2	IO_L13N_2	I/O	VCCAUX	VCCAUX
P6	2	IO_L07N_2	I/O	IP_2/ VREF_2	VREF
L8	2	IP_2	INPUT	GND	GND
L7	2	IP_2	INPUT	VCCINT	VCCINT
M9	2	VCCO_2	VCCO	IP_2/ VREF_2	VREF
L10	2	IP_2/ VREF_2	VREF	GND	GND
M8	2	IP_2/ VREF_2	VREF	GND	GND
L9	2	IP_2/ VREF_2	VREF	VCCINT	VCCINT
H5	3	IO_L10N_3	I/O	GND	GND
J6	3	IO_L17N_3	I/O	GND	GND
G3	3	IO_L09P_3	I/O	IO_L07N_3	I/O
J4	3	IO_L17P_3	I/O	IP_3	IP
H4	3	IO_L09N_3	I/O	VCCAUX	VCCAUX
H6	3	IO_L10P_3	I/O	VCCINT	VCCINT
N2	3	IO_L22P_3	I/O	IO_L22P_3/ VREF_3	VREF
G4	3	IO_L07N_3	I/O	IP_3/ VREF_3	VREF
G6	3	IP_L06P_3	INPUT	GND	GND
H7	3	IP_L13P_3	INPUT	GND	GND
K5	3	IP_L21P_3	INPUT	GND	GND
E4	3	IP_L04P_3	INPUT	IO_L04P_3	I/O
L5	3	IP_L25P_3	INPUT	VCCAUX	VCCAUX
J7	3	IP_L13N_3	INPUT	VCCINT	VCCINT
K6	3	IP_L21N_3	INPUT	VCCINT	VCCINT
J5	3	VCCO_3	VCCO	IP_3/ VREF_3	VREF
G5	3	IP_L06N_3/ VREF_3	VREF	GND	GND
L6	3	IP_L25N_3/ VREF_3	VREF	GND	GND
F4	3	IP_L04N_3/ VREF_3	VREF	IO_L04N_3	I/O

FG320: 320-ball Fine-pitch Ball Grid Array

The 320-ball fine-pitch ball grid array package, FG320, supports two Spartan-3A FPGAs, the XC3S200A and the XC3S400A, as shown in Table 77 and Figure 23.

The FG320 package is an 18 x 18 array of solder balls minus the four center balls.

Table 77 lists all the package pins. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The shaded rows indicate pinout differences between the XC3S200A and the XC3S400A FPGAs. The XC3S200A has three unconnected balls, indicated as N.C. (No Connection) in Table 77 and with the black diamond character (◆) in Table 77 and Figure 23.

All other balls have nearly identical functionality on all three devices. Table 80 summarizes the Spartan-3A FPGA footprint migration differences for the FG320 package.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 77: **Spartan-3A FG320 Pinout**

Bank	Pin Name	FG320 Ball	Type
0	IO_L01N_0	C15	I/O
0	IO_L01P_0	C16	I/O
0	IO_L02N_0	A16	I/O
0	IO_L02P_0/VREF_0	B16	VREF
0	IO_L03N_0	A14	I/O
0	IO_L03P_0	A15	I/O
0	IO_L04N_0	C14	I/O
0	IO_L04P_0	B15	I/O
0	IO_L05N_0	D12	I/O
0	IO_L05P_0	C13	I/O
0	IO_L06N_0/VREF_0	A13	VREF
0	IO_L06P_0	B13	I/O
0	IO_L07N_0	B12	I/O
0	IO_L07P_0	C12	I/O
0	IO_L08N_0	F11	I/O
0	IO_L08P_0	E11	I/O
0	IO_L09N_0	A11	I/O
0	IO_L09P_0	B11	I/O
0	IO_L10N_0	D10	I/O
0	IO_L10P_0	C11	I/O
0	IO_L11N_0/GCLK5	C9	GCLK
0	IO_L11P_0/GCLK4	B10	GCLK
0	IO_L12N_0/GCLK7	B9	GCLK
0	IO_L12P_0/GCLK6	A10	GCLK
0	IO_L13N_0/GCLK9	B7	GCLK
0	IO_L13P_0/GCLK8	A8	GCLK
0	IO_L14N_0/GCLK11	C8	GCLK
0	IO_L14P_0/GCLK10	B8	GCLK
0	IO_L15N_0	C7	I/O
0	IO_L15P_0	D8	I/O
0	IO_L16N_0	E9	I/O
0	IO_L16P_0	D9	I/O
0	IO_L17N_0	B6	I/O
0	IO_L17P_0	A6	I/O
0	IO_L18N_0/VREF_0	A4	VREF
0	IO_L18P_0	A5	I/O
0	IO_L19N_0	E7	I/O
0	IO_L19P_0	F8	I/O
0	IO_L20N_0	D6	I/O
0	IO_L20P_0	C6	I/O
0	IO_L21N_0	A3	I/O
0	IO_L21P_0	B4	I/O
0	IO_L22N_0	D5	I/O
0	IO_L22P_0	C5	I/O
0	IO_L23N_0	A2	I/O
0	IO_L23P_0	B3	I/O
0	IO_L24N_0/PUDC_B	E5	DUAL
0	IO_L24P_0/VREF_0	E6	VREF
0	IP_0	D13	INPUT
0	IP_0	D14	INPUT
0	IP_0	E12	INPUT
0	***XC3S400A:*** IP_0 ***XC3S200A:*** N.C. (◆)	E13	INPUT
0	IP_0	F7	INPUT
0	IP_0	F9	INPUT
0	IP_0	F10	INPUT

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
0	IP_0	F12	INPUT
0	IP_0	G7	INPUT
0	IP_0	G8	INPUT
0	IP_0	G9	INPUT
0	IP_0	G11	INPUT
0	IP_0/VREF_0	E10	VREF
0	VCCO_0	B5	VCCO
0	VCCO_0	B14	VCCO
0	VCCO_0	D11	VCCO
0	VCCO_0	E8	VCCO
1	IO_L01N_1/LDC2	T17	DUAL
1	IO_L01P_1/HDC	R16	DUAL
1	IO_L02N_1/LDC0	U18	DUAL
1	IO_L02P_1/LDC1	U17	DUAL
1	IO_L03N_1/A1	R17	DUAL
1	IO_L03P_1/A0	T18	DUAL
1	IO_L05N_1	N16	I/O
1	IO_L05P_1	P16	I/O
1	IO_L06N_1	M14	I/O
1	IO_L06P_1	N15	I/O
1	IO_L07N_1/VREF_1	P18	VREF
1	IO_L07P_1	R18	I/O
1	IO_L09N_1/A3	M17	DUAL
1	IO_L09P_1/A2	M16	DUAL
1	IO_L10N_1/A5	N18	DUAL
1	IO_L10P_1/A4	N17	DUAL
1	IO_L11N_1/A7	L12	DUAL
1	IO_L11P_1/A6	L13	DUAL
1	IO_L13N_1/A9	K16	DUAL
1	IO_L13P_1/A8	L17	DUAL
1	IO_L14N_1/RHCLK1	K17	RHCLK
1	IO_L14P_1/RHCLK0	L18	RHCLK
1	IO_L15N_1/TRDY1/RHCLK3	J17	RHCLK
1	IO_L15P_1/RHCLK2	K18	RHCLK
1	IO_L17N_1/RHCLK5	K15	RHCLK
1	IO_L17P_1/RHCLK4	J16	RHCLK
1	IO_L18N_1/RHCLK7	H17	RHCLK
1	IO_L18P_1/IRDY1/RHCLK6	H18	RHCLK
1	IO_L19N_1/A11	G16	DUAL
1	IO_L19P_1/A10	H16	DUAL

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
1	IO_L21N_1	F17	I/O
1	IO_L21P_1	G17	I/O
1	IO_L22N_1/A13	E18	DUAL
1	IO_L22P_1/A12	F18	DUAL
1	IO_L23N_1/A15	H15	DUAL
1	IO_L23P_1/A14	J14	DUAL
1	IO_L25N_1	D17	I/O
1	IO_L25P_1	D18	I/O
1	IO_L26N_1/A17	E16	DUAL
1	IO_L26P_1/A16	F16	DUAL
1	IO_L27N_1/A19	F15	DUAL
1	IO_L27P_1/A18	G15	DUAL
1	IO_L29N_1/A21	E15	DUAL
1	IO_L29P_1/A20	D16	DUAL
1	IO_L30N_1/A23	B18	DUAL
1	IO_L30P_1/A22	C18	DUAL
1	IO_L31N_1/A25	B17	DUAL
1	IO_L31P_1/A24	C17	DUAL
1	IP_L04N_1/VREF_1	N14	VREF
1	IP_L04P_1	P15	INPUT
1	IP_L08N_1/VREF_1	L14	VREF
1	IP_L08P_1	M13	INPUT
1	IP_L12N_1	L16	INPUT
1	IP_L12P_1/VREF_1	M15	VREF
1	IP_L16N_1	K14	INPUT
1	IP_L16P_1	K13	INPUT
1	IP_L20N_1	J13	INPUT
1	IP_L20P_1/VREF_1	K12	VREF
1	IP_L24N_1	G14	INPUT
1	IP_L24P_1	H13	INPUT
1	IP_L28N_1	G13	INPUT
1	IP_L28P_1/VREF_1	H12	VREF
1	IP_L32N_1	F13	INPUT
1	IP_L32P_1/VREF_1	F14	VREF
1	VCCO_1	E17	VCCO
1	VCCO_1	H14	VCCO
1	VCCO_1	L15	VCCO
1	VCCO_1	P17	VCCO
2	IO_L01N_2/M0	U3	DUAL
2	IO_L01P_2/M1	T3	DUAL

User I/Os by Bank

Table 78 and Table 79 indicate how the available user-I/O pins are distributed between the four I/O banks on the FG320 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 78: **User I/Os Per Bank for XC3S200A in the FG320 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	60	35	11	1	5	8
Right	1	64	9	10	30	7	8
Bottom	2	60	19	6	21	6	8
Left	3	64	38	13	0	5	8
TOTAL		**248**	**101**	**40**	**52**	**23**	**32**

Table 79: **User I/Os Per Bank for XC3S400A in the FG320 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	61	35	12	1	5	8
Right	1	64	9	10	30	7	8
Bottom	2	62	19	7	21	7	8
Left	3	64	38	13	0	5	8
TOTAL		**251**	**101**	**42**	**52**	**24**	**32**

Footprint Migration Differences

Table 80 summarizes any footprint and functionality differences between the XC3S200A and the XC3S400A FPGAs that might affect easy migration between devices available in the FG320 package. There are three such balls. All other pins not listed in Table 80 unconditionally migrate between Spartan-3A devices available in the FG320 package.

The arrows indicate the direction for easy migration.

Table 80: **FG320 Footprint Migration Differences**

Pin	Bank	XC3S200A	Migration	XC3S400A
E13	0	N.C.	→	INPUT
N7	2	N.C.	→	INPUT
P14	2	N.C.	→	INPUT/VREF
DIFFERENCES			**3**	

Legend:

→ This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction is possible depending on how the pin is configured for the device on the right.

FG400: 400-ball Fine-pitch Ball Grid Array

The 400-ball fine-pitch ball grid array, FG400, supports two different Spartan-3A FPGAs, the XC3S400A and the XC3S700A. Both devices share a common footprint for this package as shown in Table 81 and Figure 24.

Table 81 lists all the FG400 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 81: **Spartan-3A FG400 Pinout**

Bank	Pin Name	FG400 Ball	Type
0	IO_L01N_0	A18	I/O
0	IO_L01P_0	B18	I/O
0	IO_L02N_0	C17	I/O
0	IO_L02P_0/VREF_0	D17	VREF
0	IO_L03N_0	E15	I/O
0	IO_L03P_0	D16	I/O
0	IO_L04N_0	A17	I/O
0	IO_L04P_0/VREF_0	B17	VREF
0	IO_L05N_0	A16	I/O
0	IO_L05P_0	C16	I/O
0	IO_L06N_0	C15	I/O
0	IO_L06P_0	D15	I/O
0	IO_L07N_0	A14	I/O
0	IO_L07P_0	C14	I/O
0	IO_L08N_0	A15	I/O
0	IO_L08P_0	B15	I/O
0	IO_L09N_0	F13	I/O
0	IO_L09P_0	E13	I/O
0	IO_L10N_0/VREF_0	C13	VREF
0	IO_L10P_0	D14	I/O
0	IO_L11N_0	C12	I/O
0	IO_L11P_0	B13	I/O
0	IO_L12N_0	F12	I/O
0	IO_L12P_0	D12	I/O
0	IO_L13N_0	A12	I/O

Table 81: **Spartan-3A FG400 Pinout *(Continued)***

Bank	Pin Name	FG400 Ball	Type
0	IO_L13P_0	B12	I/O
0	IO_L14N_0	C11	I/O
0	IO_L14P_0	B11	I/O
0	IO_L15N_0/GCLK5	E11	GCLK
0	IO_L15P_0/GCLK4	D11	GCLK
0	IO_L16N_0/GCLK7	C10	GCLK
0	IO_L16P_0/GCLK6	A10	GCLK
0	IO_L17N_0/GCLK9	E10	GCLK
0	IO_L17P_0/GCLK8	D10	GCLK
0	IO_L18N_0/GCLK11	A8	GCLK
0	IO_L18P_0/GCLK10	A9	GCLK
0	IO_L19N_0	C9	I/O
0	IO_L19P_0	B9	I/O
0	IO_L20N_0	C8	I/O
0	IO_L20P_0	B8	I/O
0	IO_L21N_0	D8	I/O
0	IO_L21P_0	C7	I/O
0	IO_L22N_0/VREF_0	F9	VREF
0	IO_L22P_0	E9	I/O
0	IO_L23N_0	F8	I/O
0	IO_L23P_0	E8	I/O
0	IO_L24N_0	A7	I/O
0	IO_L24P_0	B7	I/O
0	IO_L25N_0	C6	I/O
0	IO_L25P_0	A6	I/O
0	IO_L26N_0	B5	I/O
0	IO_L26P_0	A5	I/O
0	IO_L27N_0	F7	I/O
0	IO_L27P_0	E7	I/O
0	IO_L28N_0	D6	I/O
0	IO_L28P_0	C5	I/O
0	IO_L29N_0	C4	I/O
0	IO_L29P_0	A4	I/O
0	IO_L30N_0	B3	I/O
0	IO_L30P_0	A3	I/O
0	IO_L31N_0	F6	I/O
0	IO_L31P_0	E6	I/O
0	IO_L32N_0/PUDC_B	B2	DUAL

Table 81: **Spartan-3A FG400 Pinout *(Continued)***

Bank	Pin Name	FG400 Ball	Type
VCCAUX	TDO	E17	JTAG
VCCAUX	TMS	E4	JTAG
VCCAUX	VCCAUX	A13	VCCAUX
VCCAUX	VCCAUX	E16	VCCAUX
VCCAUX	VCCAUX	H1	VCCAUX
VCCAUX	VCCAUX	K13	VCCAUX
VCCAUX	VCCAUX	L8	VCCAUX
VCCAUX	VCCAUX	N20	VCCAUX
VCCAUX	VCCAUX	T5	VCCAUX
VCCAUX	VCCAUX	Y8	VCCAUX
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	J12	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	N10	VCCINT

User I/Os by Bank

Table 82 indicates how the 311 available user-I/O pins are distributed between the four I/O banks on the FG400 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 82: **User I/Os Per Bank for the XC3S400A and XC3S700A in the FG400 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	77	50	12	1	6	8
Right	1	79	21	12	30	8	8
Bottom	2	76	35	6	21	6	8
Left	3	79	49	16	0	6	8
TOTAL		**311**	**155**	**46**	**52**	**26**	**32**

Footprint Migration Differences

The XC3S400A and XC3S700A FPGAs have identical footprints in the FG400 package. Designs can migrate between the XC3S400A and XC3S700A FPGAs without further consideration.

FG400 Footprint

Left Half of FG400 Package (Top View)

155 **I/O:** Unrestricted, general-purpose user I/O

46 **INPUT:** Unrestricted, general-purpose input pin

51 **DUAL:** Configuration pins, then possible user I/O

26 **VREF:** User I/O or input voltage reference for bank

32 **CLK:** User I/O, input, or clock buffer input

2 **CONFIG:** Dedicated configuration pins

4 **JTAG:** Dedicated JTAG port pins

2 **SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins

43 **GND:** Ground

22 **VCCO:** Output voltage supply for bank

9 **VCCINT:** Internal core supply voltage (+1.2V)

8 **VCCAUX:** Auxiliary supply voltage

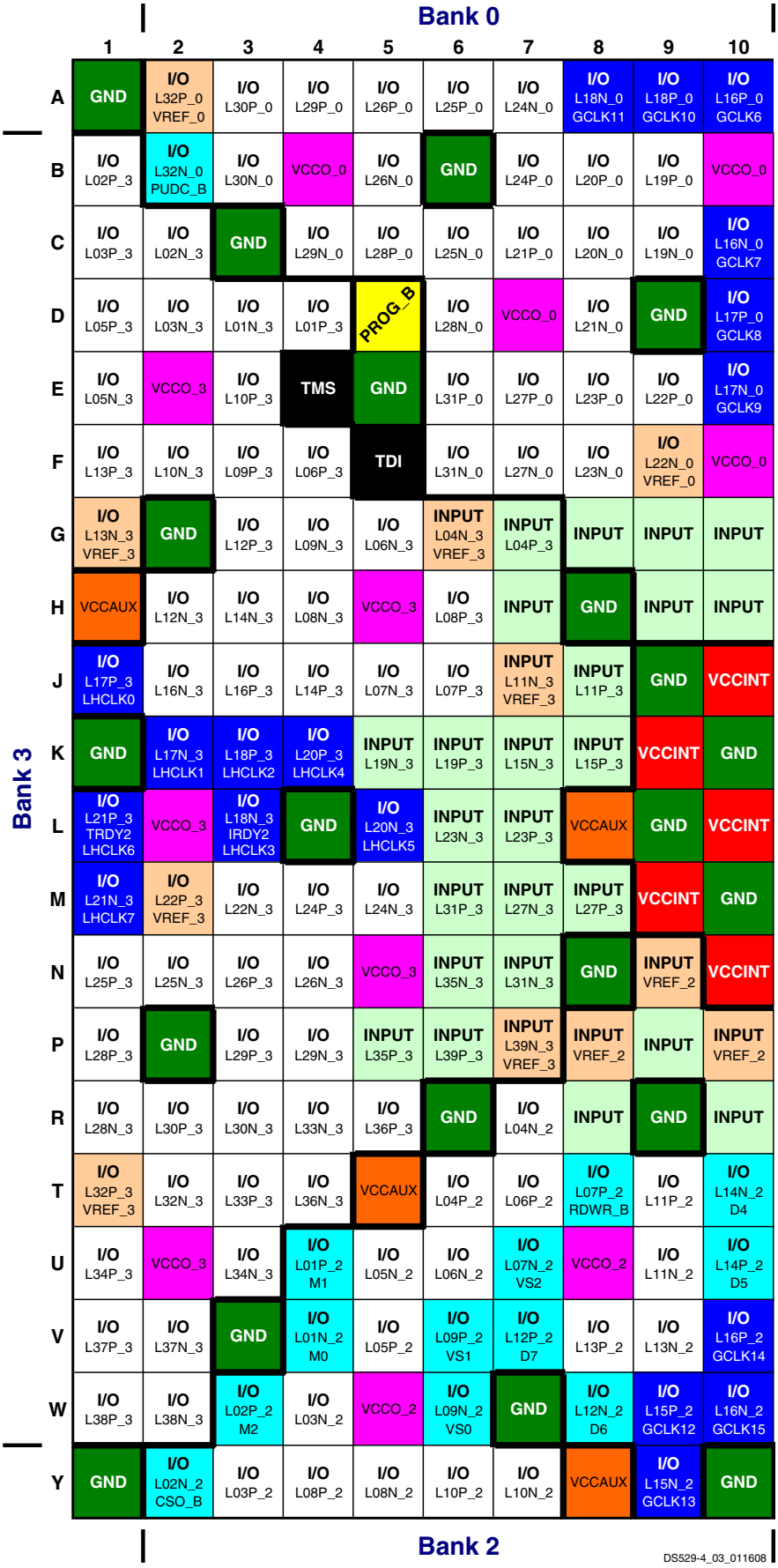


Figure 24: **FG400 Package Footprint (Top View)**

Table 83: **Spartan-3A FG484 Pinout*(Continued)***

Bank	Pin Name	FG484 Ball	Type
2	IO_L10P_2	Y7	I/O
2	IO_L11N_2/VS0	Y8	DUAL
2	IO_L11P_2/VS1	W8	DUAL
2	IO_L12N_2	AB8	I/O
2	IO_L12P_2	AA8	I/O
2	IO_L13N_2	Y10	I/O
2	IO_L13P_2	V10	I/O
2	IO_L14N_2/D6	AB9	DUAL
2	IO_L14P_2/D7	Y9	DUAL
2	IO_L15N_2	AB10	I/O
2	IO_L15P_2	AA10	I/O
2	IO_L16N_2/D4	AB11	DUAL
2	IO_L16P_2/D5	Y11	DUAL
2	IO_L17N_2/GCLK13	V11	GCLK
2	IO_L17P_2/GCLK12	U11	GCLK
2	IO_L18N_2/GCLK15	Y12	GCLK
2	IO_L18P_2/GCLK14	W12	GCLK
2	IO_L19N_2/GCLK1	AB12	GCLK
2	IO_L19P_2/GCLK0	AA12	GCLK
2	IO_L20N_2/GCLK3	U12	GCLK
2	IO_L20P_2/GCLK2	V12	GCLK
2	IO_L21N_2	Y13	I/O
2	IO_L21P_2	AB13	I/O
2	IO_L22N_2/MOSI/CSI_B	AB14	DUAL
2	IO_L22P_2	AA14	I/O
2	IO_L23N_2	Y14	I/O
2	IO_L23P_2	W13	I/O
2	IO_L24N_2/ DOUT	AA15	DUAL
2	IO_L24P_2/AWAKE	AB15	PWR MGMT
2	IO_L25N_2	Y15	I/O
2	IO_L25P_2	W15	I/O
2	IO_L26N_2/D3	U13	DUAL
2	IO_L26P_2/INIT_B	V13	DUAL
2	IO_L27N_2	Y16	I/O
2	IO_L27P_2	AB16	I/O
2	IO_L28N_2/D1	Y17	DUAL
2	IO_L28P_2/D2	AA17	DUAL
2	IO_L29N_2	AB18	I/O
2	IO_L29P_2	AB17	I/O

Table 83: **Spartan-3A FG484 Pinout*(Continued)***

Bank	Pin Name	FG484 Ball	Type
2	IO_L30N_2	V15	I/O
2	IO_L30P_2	V14	I/O
2	IO_L31N_2	V16	I/O
2	IO_L31P_2	W16	I/O
2	IO_L32N_2	AA19	I/O
2	IO_L32P_2	AB19	I/O
2	IO_L33N_2	V17	I/O
2	IO_L33P_2	W18	I/O
2	IO_L34N_2	W17	I/O
2	IO_L34P_2	Y18	I/O
2	IO_L35N_2	AA21	I/O
2	IO_L35P_2	AB21	I/O
2	IO_L36N_2/CCLK	AA20	DUAL
2	IO_L36P_2/D0/DIN/MISO	AB20	DUAL
2	IP_2	P12	INPUT
2	IP_2	R10	INPUT
2	IP_2	R11	INPUT
2	IP_2	R9	INPUT
2	IP_2	T13	INPUT
2	IP_2	T14	INPUT
2	IP_2	T9	INPUT
2	IP_2	U10	INPUT
2	IP_2	U15	INPUT
2	***XC3S1400A:*** IP_2 ***XC3S700A:*** N.C. (◆)	U16	INPUT
2	***XC3S1400A:*** IP_2 ***XC3S700A:*** N.C. (◆)	U7	INPUT
2	IP_2	U8	INPUT
2	IP_2	V7	INPUT
2	IP_2/VREF_2	R12	VREF
2	IP_2/VREF_2	R13	VREF
2	IP_2/VREF_2	R14	VREF
2	IP_2/VREF_2	T10	VREF
2	IP_2/VREF_2	T11	VREF
2	IP_2/VREF_2	T15	VREF
2	IP_2/VREF_2	T16	VREF
2	IP_2/VREF_2	T7	VREF
2	***XC3S1400A:*** IP_2/VREF_2 ***XC3S700A:*** N.C. (◆)	T8	VREF
2	IP_2/VREF_2	V8	VREF
2	VCCO_2	AA13	VCCO

Table 83: **Spartan-3A FG484 Pinout*(Continued)***

Bank	Pin Name	FG484 Ball	Type
VCCAUX	DONE	Y19	CONFIG
VCCAUX	PROG_B	C4	CONFIG
VCCAUX	TCK	A21	JTAG
VCCAUX	TDI	F5	JTAG
VCCAUX	TDO	E19	JTAG
VCCAUX	TMS	D4	JTAG
VCCAUX	VCCAUX	D12	VCCAUX
VCCAUX	VCCAUX	E18	VCCAUX
VCCAUX	VCCAUX	E5	VCCAUX
VCCAUX	VCCAUX	H11	VCCAUX
VCCAUX	VCCAUX	L4	VCCAUX
VCCAUX	VCCAUX	M19	VCCAUX
VCCAUX	VCCAUX	P11	VCCAUX
VCCAUX	VCCAUX	V18	VCCAUX
VCCAUX	VCCAUX	V5	VCCAUX
VCCAUX	VCCAUX	W11	VCCAUX
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	J12	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	K13	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	L14	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	M13	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	N10	VCCINT
VCCINT	VCCINT	N12	VCCINT
VCCINT	VCCINT	N14	VCCINT
VCCINT	VCCINT	P13	VCCINT

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
0	IO_L34N_0	D10	I/O
0	IO_L34P_0	C10	I/O
0	IO_L35N_0	H12	I/O
0	IO_L35P_0	G12	I/O
0	IO_L36N_0	B9	I/O
0	IO_L36P_0	A9	I/O
0	IO_L37N_0	D9	I/O
0	IO_L37P_0	E10	I/O
0	IO_L38N_0	B8	I/O
0	IO_L38P_0	A8	I/O
0	IO_L39N_0	K12	I/O
0	IO_L39P_0	J12	I/O
0	IO_L40N_0	D8	I/O
0	IO_L40P_0	C8	I/O
0	IO_L41N_0	C6	I/O
0	IO_L41P_0	B6	I/O
0	IO_L42N_0	C7	I/O
0	IO_L42P_0	B7	I/O
0	IO_L43N_0	K11	I/O
0	IO_L43P_0	J11	I/O
0	IO_L44N_0	D6	I/O
0	IO_L44P_0	C5	I/O
0	IO_L45N_0	B4	I/O
0	IO_L45P_0	A4	I/O
0	IO_L46N_0	H10	I/O
0	IO_L46P_0	G10	I/O
0	IO_L47N_0	H9	I/O
0	IO_L47P_0	G9	I/O
0	IO_L48N_0	E7	I/O
0	IO_L48P_0	F7	I/O
0	IO_L51N_0	B3	I/O
0	IO_L51P_0	A3	I/O
0	IO_L52N_0/PUDC_B	G8	DUAL
0	IO_L52P_0/VREF_0	F8	VREF
0	IP_0	A5	INPUT
0	IP_0	A7	INPUT
0	IP_0	A13	INPUT
0	IP_0	A17	INPUT
0	IP_0	A23	INPUT
0	IP_0	C4	INPUT

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
0	IP_0	D12	INPUT
0	IP_0	D15	INPUT
0	IP_0	D19	INPUT
0	IP_0	E11	INPUT
0	IP_0	E18	INPUT
0	IP_0	E20	INPUT
0	IP_0	F10	INPUT
0	IP_0	G14	INPUT
0	IP_0	G16	INPUT
0	IP_0	H13	INPUT
0	IP_0	H18	INPUT
0	IP_0	J10	INPUT
0	IP_0	J13	INPUT
0	IP_0	J15	INPUT
0	IP_0/VREF_0	D7	VREF
0	IP_0/VREF_0	D14	VREF
0	IP_0/VREF_0	G11	VREF
0	IP_0/VREF_0	J17	VREF
0	N.C. (◆)	A24	N.C.
0	N.C. (◆)	B24	N.C.
0	N.C. (◆)	D5	N.C.
0	N.C. (◆)	E9	N.C.
0	N.C. (◆)	F18	N.C.
0	N.C. (◆)	E6	N.C.
0	N.C. (◆)	F9	N.C.
0	N.C. (◆)	G18	N.C.
0	VCCO_0	B5	VCCO
0	VCCO_0	B11	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	B22	VCCO
0	VCCO_0	E8	VCCO
0	VCCO_0	E13	VCCO
0	VCCO_0	E19	VCCO
0	VCCO_0	H11	VCCO
0	VCCO_0	H16	VCCO
1	IO_L01N_1/LDC2	Y21	DUAL
1	IO_L01P_1/HDC	Y20	DUAL
1	IO_L02N_1/LDC0	AD25	DUAL
1	IO_L02P_1/LDC1	AE26	DUAL
1	IO_L03N_1/A1	AC24	DUAL