AMD Xilinx - XC3S50A-5VQG100C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	176
Number of Logic Elements/Cells	1584
Total RAM Bits	55296
Number of I/O	68
Number of Gates	50000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s50a-5vqg100c

Spartan-3A FPGA Family: Introduction and Ordering Information

DS529-1 (v2.0) August 19, 2010 **Product Specification**

Introduction

The Spartan®-3A family of Field-Programmable Gate Arrays (FPGAs) solves the design challenges in most high-volume, cost-sensitive, I/O-intensive electronic applications. The five-member family offers densities ranging from 50,000 to 1.4 million system gates, as shown in Table 1.

The Spartan-3A FPGAs are part of the Extended Spartan-3A family, which also include the non-volatile Spartan-3AN and the higher density Spartan-3A DSP FPGAs. The Spartan-3A family builds on the success of the earlier Spartan-3E and Spartan-3 FPGA families. New features improve system performance and reduce the cost of configuration. These Spartan-3A family enhancements, combined with proven 90 nm process technology, deliver more functionality and bandwidth per dollar than ever before, setting the new standard in the programmable logic industry.

Because of their exceptionally low cost, Spartan-3A FPGAs are ideally suited to a wide range of consumer electronics applications, including broadband access, home networking, display/projection, and digital television equipment.

The Spartan-3A family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, lengthy development cycles, and the inherent inflexibility of conventional ASICs, and permit field design upgrades.

Features

- Very low cost, high-performance logic solution for high-volume, cost-conscious applications
- Dual-range V_{CCAUX} supply simplifies 3.3V-only design
- Suspend, Hibernate modes reduce system power
- Multi-voltage, multi-standard SelectIO™ interface pins
    - Up to 502 I/O pins or 227 differential signal pairs
    - LVCMOS, LVTTL, HSTL, and SSTL single-ended I/O
    - 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V signaling
    - Selectable output drive, up to 24 mA per pin
    - QUIETIO standard reduces I/O switching noise
    - Full 3.3V ± 10% compatibility and hot swap compliance
    - 640+ Mb/s data transfer rate per differential I/O
    - LVDS, RSDS, mini-LVDS, HSTL/SSTL differential I/O with integrated differential termination resistors
    - Enhanced Double Data Rate (DDR) support
    - DDR/DDR2 SDRAM support up to 400 Mb/s
    - Fully compliant 32-/64-bit, 33/66 MHz PCI® technology support
- Abundant, flexible logic resources
    - Densities up to 25,344 logic cells, including optional shift register or distributed RAM support
    - Efficient wide multiplexers, wide logic
    - Fast look-ahead carry logic
    - Enhanced 18 x 18 multipliers with optional pipeline
    - IEEE 1149.1/1532 JTAG programming/debug port
- Hierarchical SelectRAM™ memory architecture
    - Up to 576 Kbits of fast block RAM with byte write enables for processor applications
    - Up to 176 Kbits of efficient distributed RAM
- Up to eight Digital Clock Managers (DCMs)
    - Clock skew elimination (delay locked loop)
    - Frequency synthesis, multiplication, division
    - High-resolution phase shifting
    - Wide frequency range (5 MHz to over 320 MHz)
- Eight low-skew global clock networks, eight additional clocks per half device, plus abundant low-skew routing
- Configuration interface to industry-standard PROMs
    - Low-cost, space-saving SPI serial Flash PROM
    - x8 or x8/x16 BPI parallel NOR Flash PROM
    - Low-cost Xilinx® Platform Flash with JTAG
    - Unique Device DNA identifier for design authentication
    - Load multiple bitstreams under FPGA control
    - Post-configuration CRC checking
- Complete Xilinx ISE® and WebPACK™ development system software support plus Spartan-3A Starter Kit
- MicroBlaze™ and PicoBlaze™ embedded processors
- Low-cost QFP and BGA packaging, Pb-free options
    - Common footprints support easy density migration
    - Compatible with select Spartan-3AN nonvolatile FPGAs
    - Compatible with higher density Spartan-3A DSP FPGAs
- XA Automotive version available

Table 1: **Summary of Spartan-3A FPGA Attributes**

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM bits[1]	Block RAM bits[1]	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	CLBs	Slices						
XC3S50A	50K	1,584	16	12	176	704	11K	54K	3	2	144	64
XC3S200A	200K	4,032	32	16	448	1,792	28K	288K	16	4	248	112
XC3S400A	400K	8,064	40	24	896	3,584	56K	360K	20	4	311	142
XC3S700A	700K	13,248	48	32	1,472	5,888	92K	360K	20	8	372	165
XC3S1400A	1400K	25,344	72	40	2,816	11,264	176K	576K	32	8	502	227

Notes:

1. By convention, one Kb is equivalent to 1,024 bits.

Spartan-3A FPGA Family: DC and Switching Characteristics

DS529-3 (v2.0) August 19, 2010

Product Specification

DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

Advance: Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

Production: These specifications are approved once the silicon has been characterized over numerous production lots. Parameter values are considered stable with no future changes expected.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan®-3A devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Absolute Maximum Ratings

Stresses beyond those listed under Table 4: Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 4: **Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Max	Units
V_{CCINT}	Internal supply voltage		–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage		–0.5	3.75	V
V_{CCO}	Output driver supply voltage		–0.5	3.75	V
V_{REF}	Input reference voltage		–0.5	$V_{CCO} + 0.5$	V
V_{IN}	Voltage applied to all User I/O pins and dual-purpose pins	Driver in a high-impedance state	–0.95	4.6	V
	Voltage applied to all Dedicated pins		–0.5	4.6	V
I_{IK}	Input clamp current per I/O pin	$-0.5V < V_{IN} < (V_{CCO} + 0.5V)$(1)	–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model	–	±2000	V
		Charged device model	–	±500	V
		Machine model	–	±200	V
T_J	Junction temperature		–	125	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Upper clamp applies only when using PCI IOSTANDARDs.
2. For soldering guidelines, see UG112: *Device Packaging and Thermal Characteristics* and XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

Differential I/O Standards

Differential Input Pairs

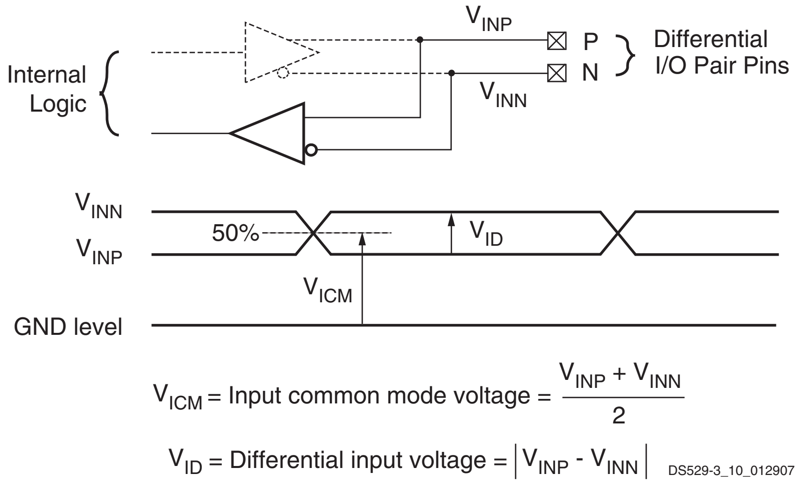


Figure 4: **Differential Input Voltages**

Table 13: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers[1]			V_{ID}			V_{ICM}[2]		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LVDS_25[3]	2.25	2.5	2.75	100	350	600	0.3	1.25	2.35
LVDS_33[3]	3.0	3.3	3.6	100	350	600	0.3	1.25	2.35
BLVDS_25[4]	2.25	2.5	2.75	100	300	–	0.3	1.3	2.35
MINI_LVDS_25[3]	2.25	2.5	2.75	200	–	600	0.3	1.2	1.95
MINI_LVDS_33[3]	3.0	3.3	3.6	200	–	600	0.3	1.2	1.95
LVPECL_25[5]	Inputs Only			100	800	1000	0.3	1.2	1.95
LVPECL_33[5]	Inputs Only			100	800	1000	0.3	1.2	2.8[6]
RSDS_25[3]	2.25	2.5	2.75	100	200	–	0.3	1.2	1.5
RSDS_33[3]	3.0	3.3	3.6	100	200	–	0.3	1.2	1.5
TMDS_33[3, 4, 7]	3.14	3.3	3.47	150	–	1200	2.7	–	3.23
PPDS_25[3]	2.25	2.5	2.75	100	–	400	0.2	–	2.3
PPDS_33[3]	3.0	3.3	3.6	100	–	400	0.2	–	2.3
DIFF_HSTL_I_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_II_18[8]	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_III_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_I	1.4	1.5	1.6	100	–	–	0.68		0.9
DIFF_HSTL_III	1.4	1.5	1.6	100	–	–	–	0.9	–
DIFF_SSTL18_I	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL18_II[8]	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL2_I	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL2_II[8]	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL3_I	3.0	3.3	3.6	100	–	–	1.1	–	1.9
DIFF_SSTL3_II	3.0	3.3	3.6	100	–	–	1.1	–	1.9

Notes:

1. The V_{CCO} rails supply only differential output drivers, not input circuits.
2. V_{ICM} must be less than V_{CCAUX}.
3. These true differential output standards are supported only on FPGA banks 0 and 2. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
4. See "External Termination Requirements for Differential I/O," page 20.
5. LVPECL is supported on inputs only, not outputs. LVPECL_33 requires V_{CCAUX}=3.3V ± 10%.
6. LVPECL_33 maximum V_{ICM} = the lower of 2.8V or $V_{CCAUX} – (V_{ID} / 2)$
7. Requires V_{CCAUX} = 3.3V ± 10% for inputs. $(V_{CCAUX} – 300 \text{ mV}) \leq V_{ICM} \leq (V_{CCAUX} – 37 \text{ mV})$
8. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
9. All standards except for LVPECL and TMDS can have V_{CCAUX} at either 2.5V or 3.3V. Define your V_{CCAUX} level using the CONFIG VCCAUX constraint.

Table 22: **Propagation Times for the IOB Input Path*(Continued)***

Symbol	Description	Conditions	DELAY_VALUE	Device	Speed Grade -5 Max	Speed Grade -4 Max	Units
T_{IOPID}	The time it takes for data to travel from the Input pin to the I output with the input delay programmed	LVCMOS25[(2)]	15	XC3S200A	5.43	6.24	ns
			16		5.75	6.59	ns
			1	XC3S400A	1.32	1.43	ns
			2		1.67	1.83	ns
			3		1.90	2.07	ns
			4		2.33	2.52	ns
			5		2.60	2.91	ns
			6		2.94	3.20	ns
			7		3.23	3.51	ns
			8		3.50	3.85	ns
			9		3.18	3.55	ns
			10		3.53	3.95	ns
			11		3.76	4.20	ns
			12		4.26	4.67	ns
			13		4.51	4.97	ns
			14		4.85	5.32	ns
			15		5.14	5.64	ns
			16		5.40	5.95	ns
			1	XC3S700A	1.84	1.87	ns
			2		2.20	2.27	ns
			3		2.46	2.60	ns
			4		2.93	3.15	ns
			5		3.21	3.45	ns
			6		3.54	3.80	ns
			7		3.86	4.16	ns
			8		4.13	4.48	ns
			9		3.82	4.19	ns
			10		4.17	4.58	ns
			11		4.43	4.89	ns
			12		4.95	5.49	ns
			13		5.22	5.83	ns
			14		5.57	6.21	ns
			15		5.89	6.55	ns
			16		6.16	6.89	ns
			1	XC3S1400A	1.95	2.18	ns
			2		2.29	2.59	ns
			3		2.54	2.84	ns
			4		2.96	3.30	ns

Input Timing Adjustments

Table 23: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Single-Ended Standards			
LVTTL	0.62	0.62	ns
LVCMOS33	0.54	0.54	ns
LVCMOS25	0	0	ns
LVCMOS18	0.83	0.83	ns
LVCMOS15	0.60	0.60	ns
LVCMOS12	0.31	0.31	ns
PCI33_3	0.41	0.41	ns
PCI66_3	0.41	0.41	ns
HSTL_I	0.72	0.72	ns
HSTL_III	0.77	0.77	ns
HSTL_I_18	0.69	0.69	ns
HSTL_II_18	0.69	0.69	ns
HSTL_III_18	0.79	0.79	ns
SSTL18_I	0.71	0.71	ns
SSTL18_II	0.71	0.71	ns
SSTL2_I	0.68	0.68	ns
SSTL2_II	0.68	0.68	ns
SSTL3_I	0.78	0.78	ns
SSTL3_II	0.78	0.78	ns
Differential Standards			
LVDS_25	0.76	0.76	ns
LVDS_33	0.79	0.79	ns
BLVDS_25	0.79	0.79	ns
MINI_LVDS_25	0.78	0.78	ns
MINI_LVDS_33	0.79	0.79	ns
LVPECL_25	0.78	0.78	ns
LVPECL_33	0.79	0.79	ns
RSDS_25	0.79	0.79	ns
RSDS_33	0.77	0.77	ns
TMDS_33	0.79	0.79	ns
PPDS_25	0.79	0.79	ns
PPDS_33	0.79	0.79	ns
DIFF_HSTL_I_18	0.74	0.74	ns
DIFF_HSTL_II_18	0.72	0.72	ns
DIFF_HSTL_III_18	1.05	1.05	ns
DIFF_HSTL_I	0.72	0.72	ns
DIFF_HSTL_III	1.05	1.05	ns
DIFF_SSTL18_I	0.71	0.71	ns
DIFF_SSTL18_II	0.71	0.71	ns
DIFF_SSTL2_I	0.74	0.74	ns
DIFF_SSTL2_II	0.75	0.75	ns
DIFF_SSTL3_I	1.06	1.06	ns
DIFF_SSTL3_II	1.06	1.06	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8, Table 11, and Table 13.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Table 26: **Output Timing Adjustments for IOB*(Continued)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS25	Slow	2 mA	5.33	5.33	ns
		4 mA	2.81	2.81	ns
		6 mA	2.82	2.82	ns
		8 mA	1.14	1.14	ns
		12 mA	1.10	1.10	ns
		16 mA	0.83	0.83	ns
		24 mA	2.26(3)	2.26(3)	ns
	Fast	2 mA	4.36	4.36	ns
		4 mA	1.76	1.76	ns
		6 mA	1.25	1.25	ns
		8 mA	0.38	0.38	ns
		12 mA	0	0	ns
		16 mA	0.01	0.01	ns
		24 mA	0.01	0.01	ns
	QuietIO	2 mA	25.92	25.92	ns
		4 mA	25.92	25.92	ns
		6 mA	25.92	25.92	ns
		8 mA	15.57	15.57	ns
		12 mA	15.59	15.59	ns
		16 mA	14.27	14.27	ns
		24 mA	11.37	11.37	ns
LVCMOS18	Slow	2 mA	4.48	4.48	ns
		4 mA	3.69	3.69	ns
		6 mA	2.91	2.91	ns
		8 mA	1.99	1.99	ns
		12 mA	1.57	1.57	ns
		16 mA	1.19	1.19	ns
	Fast	2 mA	3.96	3.96	ns
		4 mA	2.57	2.57	ns
		6 mA	1.90	1.90	ns
		8 mA	1.06	1.06	ns
		12 mA	0.83	0.83	ns
		16 mA	0.63	0.63	ns
	QuietIO	2 mA	24.97	24.97	ns
		4 mA	24.97	24.97	ns
		6 mA	24.08	24.08	ns
		8 mA	16.43	16.43	ns
		12 mA	14.52	14.52	ns
		16 mA	13.41	13.41	ns

Table 26: **Output Timing Adjustments for IOB*(Continued)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS15	Slow	2 mA	5.82	5.82	ns
		4 mA	3.97	3.97	ns
		6 mA	3.21	3.21	ns
		8 mA	2.53	2.53	ns
		12 mA	2.06	2.06	ns
	Fast	2 mA	5.23	5.23	ns
		4 mA	3.05	3.05	ns
		6 mA	1.95	1.95	ns
		8 mA	1.60	1.60	ns
		12 mA	1.30	1.30	ns
	QuietIO	2 mA	34.11	34.11	ns
		4 mA	25.66	25.66	ns
		6 mA	24.64	24.64	ns
		8 mA	22.06	22.06	ns
		12 mA	20.64	20.64	ns
LVCMOS12	Slow	2 mA	7.14	7.14	ns
		4 mA	4.87	4.87	ns
		6 mA	5.67	5.67	ns
	Fast	2 mA	6.77	6.77	ns
		4 mA	5.02	5.02	ns
		6 mA	4.09	4.09	ns
	QuietIO	2 mA	50.76	50.76	ns
		4 mA	43.17	43.17	ns
		6 mA	37.31	37.31	ns
PCI33_3			0.34	0.34	ns
PCI66_3			0.34	0.34	ns
HSTL_I			0.78	0.78	ns
HSTL_III			1.16	1.16	ns
HSTL_I_18			0.35	0.35	ns
HSTL_II_18			0.30	0.30	ns
HSTL_III_18			0.47	0.47	ns
SSTL18_I			0.40	0.40	ns
SSTL18_II			0.30	0.30	ns
SSTL2_I			0	0	ns
SSTL2_II			–0.05	–0.05	ns
SSTL3_I			0	0	ns
SSTL3_II			0.17	0.17	ns

Table 29: **Recommended Number of Simultaneously Switching Outputs per VCCO-GND Pair (V_{CCAUX}=3.3V)*(Continued)***

Signal Standard (IOSTANDARD)	Package Type			
	VQ100, TQ144		FT256, FG320, FG400, FG484, FG676	
	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)
Differential Standards (Number of I/O *Pairs* or Channels)				
LVDS_25	8	–	22	–
LVDS_33	8	–	27	–
BLVDS_25	1	1	4	4
MINI_LVDS_25	8	–	22	–
MINI_LVDS_33	8	–	27	–
LVPECL_25	Input Only			
LVPECL_33	Input Only			
RSDS_25	8	–	22	–
RSDS_33	8	–	27	–
TMDS_33	8	–	27	–
PPDS_25	8	–	22	–
PPDS_33	8	–	27	–
DIFF_HSTL_I	–	5	–	10
DIFF_HSTL_III	–	3	–	4
DIFF_HSTL_I_18	6	6	8	8
DIFF_HSTL_II_18	–	2	–	2
DIFF_HSTL_III_18	4	4	5	4
DIFF_SSTL18_I	3	6	3	7
DIFF_SSTL18_II	–	4	–	4
DIFF_SSTL2_I	5	5	9	9
DIFF_SSTL2_II	–	3	–	4
DIFF_SSTL3_I	3	4	4	5
DIFF_SSTL3_II	2	3	3	3

Notes:

1. Not all I/O standards are supported on all I/O banks. The left and right banks (I/O banks 1 and 3) support higher output drive current than the top and bottom banks (I/O banks 0 and 2). Similarly, true differential output standards, such as LVDS, RSDS, PPDS, miniLVDS, and TMDS, are only supported in top or bottom banks (I/O banks 0 and 2). Refer to UG331: *Spartan-3 Generation FPGA User Guide* for additional information.
2. The numbers in this table are recommendations that assume sound board lay out practice. Test limits are the V_{IL}/V_{IH} voltage limits for the respective I/O standard.
3. If more than one signal standard is assigned to the I/Os of a given bank, refer to XAPP689: *Managing Ground Bounce in Large FPGAs* for information on how to perform weighted average SSO calculations.

18 x 18 Embedded Multiplier Timing

Table 34: **18 x 18 Embedded Multiplier Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Combinatorial Delay						
T_{MULT}	Combinational multiplier propagation delay from the A and B inputs to the P outputs, assuming 18-bit inputs and a 36-bit product (AREG, BREG, and PREG registers unused)	–	4.36	–	4.88	ns
Clock-to-Output Times						
T_{MSCKP_P}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using the PREG register(2,3)	–	0.84	–	1.30	ns
T_{MSCKP_A} T_{MSCKP_B}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using either the AREG or BREG register(2,4)	–	4.44	–	4.97	ns
Setup Times						
T_{MSDCK_P}	Data setup time at the A or B input before the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused)(3)	3.56	–	3.98	–	ns
T_{MSDCK_A}	Data setup time at the A input before the active transition at the CLK when using the AREG input register(4)	0.00	–	0.00	–	ns
T_{MSDCK_B}	Data setup time at the B input before the active transition at the CLK when using the BREG input register(4)	0.00	–	0.00	–	ns
Hold Times						
T_{MSCKD_P}	Data hold time at the A or B input after the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused)(3)	0.00	–	0.00	–	ns
T_{MSCKD_A}	Data hold time at the A input after the active transition at the CLK when using the AREG input register(4)	0.35	–	0.45	–	ns
T_{MSCKD_B}	Data hold time at the B input after the active transition at the CLK when using the BREG input register(4)	0.35	–	0.45	–	ns
Clock Frequency						
F_{MULT}	Internal operating frequency for a two-stage 18x18 multiplier using the AREG and BREG input registers and the PREG output register(1)	0	280	0	250	MHz

Notes:

1. Combinational delay is less and pipelined performance is higher when multiplying input data with less than 18 bits.
2. The PREG register is typically used in both single-stage and two-stage pipelined multiplier implementations.
3. The PREG register is typically used when inferring a single-stage multiplier.
4. Input registers AREG or BREG are typically used when inferring a two-stage multiplier.
5. The numbers in this table are based on the operating conditions set forth in Table 8.

Table 37: **Switching Characteristics for the DLL**

Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs		All	5	280	5	250	MHz
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs			5	200	5	200	MHz
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs			10	334	10	334	MHz
CLKOUT_FREQ_DV	Frequency for the CLKDV output			0.3125	186	0.3125	166	MHz
Output Clock Jitter[2,3,4]								
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output		All	–	±100	–	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs			–	±[0.5% of CLKIN period + 100]	–	±[0.5% of CLKIN period + 100]	ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division			–	±150	–	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division			–	±[0.5% of CLKIN period + 100]	–	±[0.5% of CLKIN period + 100]	ps
Duty Cycle[4]								
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	–	±[1% of CLKIN period + 350]	–	±[1% of CLKIN period + 350]	ps
Phase Alignment[4]								
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs		All	–	±150	–	±150	ps
CLKOUT_PHASE_DLL	Phase offset between DLL outputs	CLK0 to CLK2X (not CLK2X180)		–	±[1% of CLKIN period + 100]	–	±[1% of CLKIN period + 100]	ps
		All others		–	±[1% of CLKIN period + 150]	–	±[1% of CLKIN period + 150]	ps
Lock Time								
LOCK_DLL[3]	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	$5\text{ MHz} \le F_{CLKIN} \le 15\text{ MHz}$	All	–	5	–	5	ms
		$F_{CLKIN} > 15\text{ MHz}$		–	600	–	600	µs
Delay Lines								
DCM_DELAY_STEP[5]	Finest delay resolution, averaged over all steps		All	15	35	15	35	ps

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8 and Table 36.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, the data sheet specifies a maximum jitter of "±[1% of CLKIN period + 150]". Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250ps.
5. The typical delay step size is 23 ps.

VQ100: 100-lead Very Thin Quad Flat Package

The XC3S50A and XC3S200 are available in the 100-lead very thin quad flat package, VQ100.

Table 63 lists all the package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The VQ100 does not support Suspend mode (SUSPEND and AWAKE are not connected), the address output pins for the Byte-wide Peripheral Interface (BPI) configuration mode, or daisy chain configuration (DOUT is not connected).

Table 63 also indicates that some differential I/O pairs have different assignments between the XC3S50A and the XC3S200A, highlighted in light blue. See "Footprint Migration Differences," page 72 for additional information.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

> www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 63: **Spartan-3A VQ100 Pinout**

Bank	Pin Name	Pin	Type
0	IO_0/GCLK11	P90	CLK
0	IO_L01N_0	P78	IO
0	IO_L01P_0/VREF_0	P77	VREF
0	IO_L02N_0/GCLK5	P84	CLK
0	IO_L02P_0/GCLK4	P83	CLK
0	IO_L03N_0/GCLK7	P86	CLK
0	IO_L03P_0/GCLK6	P85	CLK
0	IO_L04N_0/GCLK9	P89	CLK
0	IO_L04P_0/GCLK8	P88	CLK
0	IO_L05N_0	P94	IO
0	IO_L05P_0	P93	IO
0	IO_L06N_0/PUDC_B	P99	DUAL
0	IO_L06P_0/VREF_0	P98	VREF
0	IP_0	P97	IP
0	IP_0/VREF_0	P82	VREF
0	VCCO_0	P79	VCCO
0	VCCO_0	P96	VCCO
1	IO_L01N_1	P57	IO
1	IO_L01P_1	P56	IO
1	IO_L02N_1/RHCLK1	P60	CLK
1	IO_L02P_1/RHCLK0	P59	CLK
1	IO_L03N_1/TRDY1/RHCLK3	P62	CLK
1	IO_L03P_1/RHCLK2	P61	CLK
1	IO_L04N_1/RHCLK7	P65	CLK
1	IO_L04P_1/IRDY1/RHCLK6	P64	CLK
1	IO_L05N_1	P71	IO
1	IO_L05P_1	P70	IO
1	IO_L06N_1	P73	IO
1	IO_L06P_1	P72	IO
1	IP_1/VREF_1	P68	VREF
1	VCCO_1	P67	VCCO
2	IO_2/MOSI/CSI_B	P46	DUAL
2	IO_L01N_2/M0	P25	DUAL
2	IO_L01P_2/M1	P23	DUAL
2	IO_L02N_2/CSO_B	P27	DUAL
2	IO_L02P_2/M2	P24	DUAL
2	IO_L03N_2/VS1 (3S50A) IO_L04P_2/VS1 (3S200A)	P30	DUAL
2	IO_L03P_2/RDWR_B	P28	DUAL
2	IO_L04N_2/VS0	P31	DUAL
2	IO_L04P_2/VS2 (3S50A) IO_L03N_2/VS2 (3S200A)	P29	DUAL
2	IO_L05N_2/D7 (3S50A) IO_L06P_2/D7 (3S200A)	P34	DUAL
2	IO_L05P_2	P32	IO
2	IO_L06N_2/D6	P35	DUAL
2	IO_L06P_2 (3S50A) IO_L05N_2 (3S200A)	P33	IO
2	IO_L07N_2/D4	P37	DUAL
2	IO_L07P_2/D5	P36	DUAL
2	IO_L08N_2/GCLK15	P41	CLK
2	IO_L08P_2/GCLK14	P40	CLK
2	IO_L09N_2/GCLK1	P44	CLK
2	IO_L09P_2/GCLK0	P43	CLK
2	IO_L10N_2/D3	P49	DUAL
2	IO_L10P_2/INIT_B	P48	DUAL
2	IO_L11N_2/D0/DIN/MISO (3S50A) IO_L12P_2/D0/DIN/MISO (3S200A)	P51	DUAL
2	IO_L11P_2/D2	P50	DUAL
2	IO_L12N_2/CCLK	P53	DUAL

User I/Os by Bank

Table 64 indicates how the 68 available user-I/O pins are distributed between the four I/O banks on the VQ100 package.

Table 64: **User I/Os Per Bank for the XC3S50A and XC3S200A in the VQ100 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	**INPUT**	**DUAL**	**VREF**	**CLK**
Top	0	15	3	1	1	3	7
Right	1	13	6	0	0	1	6
Bottom	2	26	2	0	19	1	4
Left	3	14	6	1	0	1	6
TOTAL		**68**	**17**	**2**	**20**	**6**	**23**

Footprint Migration Differences

The XC3S50A and XC3S200 have common VQ100 pinouts except for some differences in alignment of differential I/O pairs.

Differential I/O Alignment Differences

Some differential I/O pairs in the VQ100 on the XC3S50A FPGA are aligned differently than the corresponding pairs on the XC3S200A FPGAs, as shown in Table 65. All the mismatched pairs are in I/O Bank 2. These differences are indicated with the black diamond character (◆) in the footprint diagrams Figure 17 and Figure 18.

Table 65: **Differential I/O Differences in VQ100**

VQ100 Pin	Bank	XC3S50A	XC3S200A
P29	2	IIO_L04P_2/VS2	IO_L03N_2/VS2
P30		IO_L03N_2/VS1	IO_L04P_2/VS1
P33		IO_L06P_2	IO_L05N_2
P34		IO_L05N_2/D7	IO_L06P_2/D7
P51		IO_L11N_2/D0/DIN/MISO	IO_L12P_2/D0/DIN/MISO
P52		IO_L12P_2/D1	IO_L11N_2/D1

VQ100 Footprint (XC3S50A)

Note pin 1 indicator in top-left corner and logo orientation.

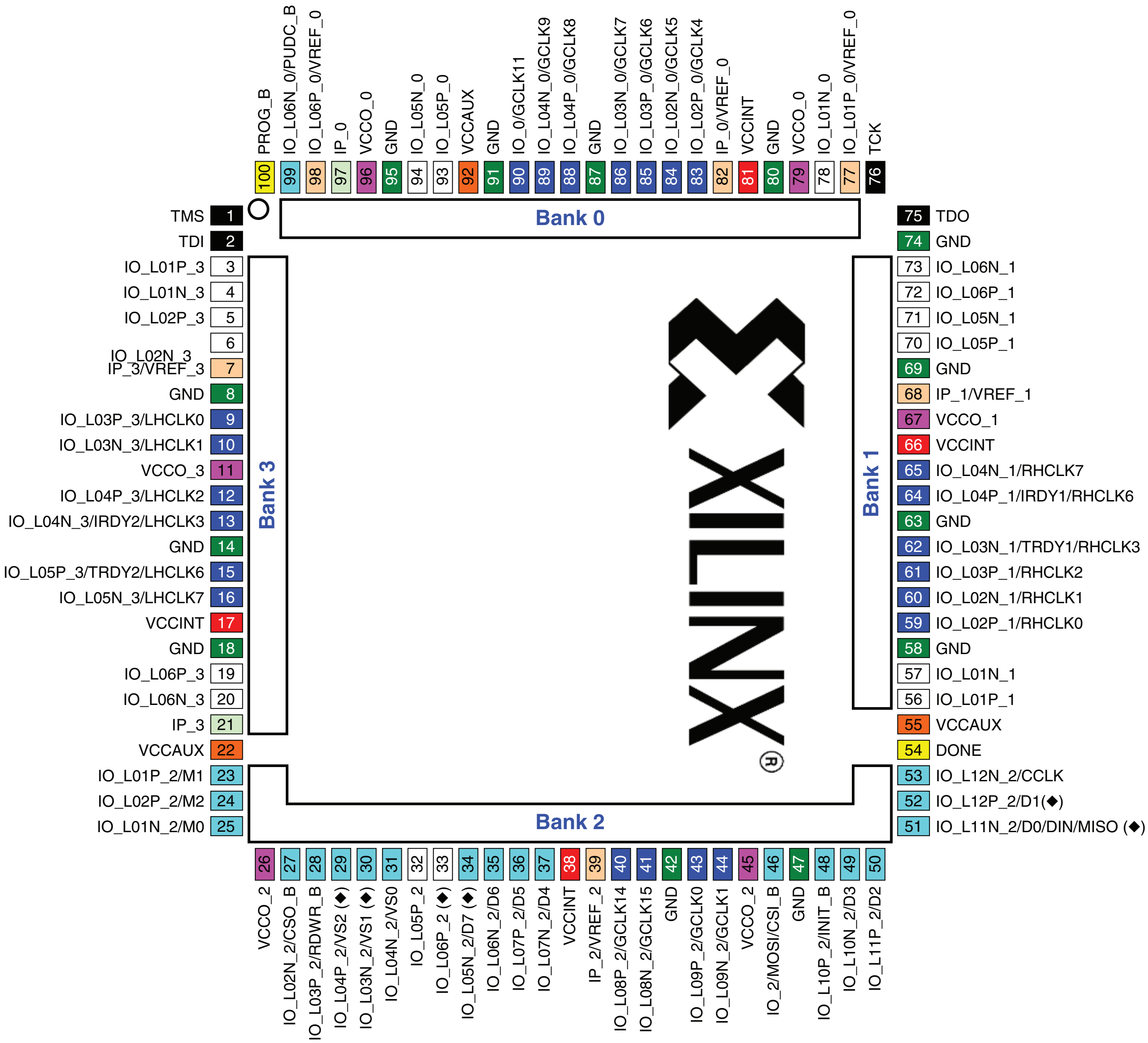


Figure 17: **VQ100 Package Footprint - XC3S50A (Top View)**

17	**I/O:** Unrestricted, general-purpose user I/O	20	**DUAL:** Configuration pins, then possible user I/O	6	**VREF:** User I/O or input voltage reference for bank
2	**INPUT:** Unrestricted, general-purpose input pin	23	**CLK:** User I/O, input, or global buffer input	6	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core supply voltage (+1.2V)
0	**N.C.:** Not connected	13	**GND:** Ground	3	**VCCAUX:** Auxiliary supply voltage

Table 68: **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400)** ***(Continued)***

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
2	IO_L01N_2/M0	IO_L01N_2/M0	P4	DUAL
2	IO_L01P_2/M1	IO_L01P_2/M1	N4	DUAL
2	IO_L02N_2/ CSO_B	IO_L02N_2/ CSO_B	T2	DUAL
2	IO_L02P_2/M2	IO_L02P_2/M2	R2	DUAL
2	IO_L04P_2/VS2	IO_L03N_2/VS2	T3	DUAL
2	IO_L03P_2/ RDWR_B	IO_L03P_2/ RDWR_B	R3	DUAL
2	IO_L04N_2/VS0	IO_L04N_2/VS0	P5	DUAL
2	IO_L03N_2/VS1	IO_L04P_2/VS1	N6	DUAL
2	IO_L06P_2	IO_L05N_2	R5	I/O
2	IO_L05P_2	IO_L05P_2	T4	I/O
2	IO_L06N_2/D6	IO_L06N_2/D6	T6	DUAL
2	IO_L05N_2/D7	IO_L06P_2/D7	T5	DUAL
2	N.C. (◆)	IO_L07N_2	P6	I/O
2	N.C. (◆)	IO_L07P_2	N7	I/O
2	IO_L08N_2/D4	IO_L08N_2/D4	N8	DUAL
2	IO_L08P_2/D5	IO_L08P_2/D5	P7	DUAL
2	N.C. (◆)	IO_L09N_2/ GCLK13	T7	GCLK
2	N.C. (◆)	IO_L09P_2/ GCLK12	R7	GCLK
2	IO_L10N_2/ GCLK15	IO_L10N_2/ GCLK15	T8	GCLK
2	IO_L10P_2/ GCLK14	IO_L10P_2/ GCLK14	P8	GCLK
2	IO_L11N_2/ GCLK1	IO_L11N_2/ GCLK1	P9	GCLK
2	IO_L11P_2/ GCLK0	IO_L11P_2/ GCLK0	N9	GCLK
2	IO_L12N_2/ GCLK3	IO_L12N_2/ GCLK3	T9	GCLK
2	IO_L12P_2/ GCLK2	IO_L12P_2/ GCLK2	R9	GCLK
2	N.C. (◆)	IO_L13N_2	M10	I/O
2	N.C. (◆)	IO_L13P_2	N10	I/O
2	IO_L14P_2/ MOSI/CSI_B	IO_L14N_2/ MOSI/CSI_B	P10	DUAL
2	IO_L14N_2	IO_L14P_2	T10	I/O
2	IO_L15N_2/ DOUT	IO_L15N_2/ DOUT	R11	DUAL
2	IO_L15P_2/ AWAKE	IO_L15P_2/ AWAKE	T11	PWR MGMT
2	IO_L16N_2	IO_L16N_2	N11	I/O
2	IO_L16P_2	IO_L16P_2	P11	I/O
2	IO_L17N_2/D3	IO_L17N_2/D3	P12	DUAL
2	IO_L17P_2/ INIT_B	IO_L17P_2/ INIT_B	T12	DUAL

Table 68: **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400)** ***(Continued)***

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
2	IO_L20P_2/D1	IO_L18N_2/D1	R13	DUAL
2	IO_L18P_2/D2	IO_L18P_2/D2	T13	DUAL
2	N.C. (◆)	IO_L19N_2	P13	I/O
2	N.C. (◆)	IO_L19P_2	N12	I/O
2	IO_L20N_2/ CCLK	IO_L20N_2/ CCLK	R14	DUAL
2	IO_L18N_2/D0/ DIN/MISO	IO_L20P_2/D0/ DIN/MISO	T14	DUAL
2	IP_2	IP_2	L7	INPUT
2	IP_2	IP_2	L8	INPUT
2	IP_2/VREF_2	IP_2/VREF_2	L9	VREF
2	IP_2/VREF_2	IP_2/VREF_2	L10	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M7	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M8	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M11	VREF
2	IP_2/VREF_2	IP_2/VREF_2	N5	VREF
2	VCCO_2	VCCO_2	M9	VCCO
2	VCCO_2	VCCO_2	R4	VCCO
2	VCCO_2	VCCO_2	R8	VCCO
2	VCCO_2	VCCO_2	R12	VCCO
3	IO_L01N_3	IO_L01N_3	C1	I/O
3	IO_L01P_3	IO_L01P_3	C2	I/O
3	IO_L02N_3	IO_L02N_3	D3	I/O
3	IO_L02P_3	IO_L02P_3	D4	I/O
3	IO_L03N_3	IO_L03N_3	E1	I/O
3	IO_L03P_3	IO_L03P_3	D1	I/O
3	N.C. (◆)	IO_L05N_3	E2	I/O
3	N.C. (◆)	IO_L05P_3	E3	I/O
3	N.C. (◆)	IO_L07N_3	G4	I/O
3	N.C. (◆)	IO_L07P_3	F3	I/O
3	IO_L08N_3/ VREF_3	IO_L08N_3/ VREF_3	G1	VREF
3	IO_L08P_3	IO_L08P_3	F1	I/O
3	N.C. (◆)	IO_L09N_3	H4	I/O
3	N.C. (◆)	IO_L09P_3	G3	I/O
3	N.C. (◆)	IO_L10N_3	H5	I/O
3	N.C. (◆)	IO_L10P_3	H6	I/O
3	IO_L11N_3/ LHCLK1	IO_L11N_3/ LHCLK1	H1	LHCLK
3	IO_L11P_3/ LHCLK0	IO_L11P_3/ LHCLK0	G2	LHCLK
3	IO_L12N_3/ IRDY2/LHCLK3	IO_L12N_3/ IRDY2/LHCLK3	J3	LHCLK
3	IO_L12P_3/ LHCLK2	IO_L12P_3/ LHCLK2	H3	LHCLK

Table 69: **Spartan-3A FT256 Pinout (XC3S700A,**

Bank	XC3S700A XC3S1400A	FT256 Ball	Type
3	IO_L16N_3	L2	I/O
3	IO_L16P_3/VREF_3	L1	VREF
3	IO_L18N_3	L3	I/O
3	IO_L18P_3	K4	I/O
3	IO_L19N_3	L4	I/O
3	IO_L19P_3	M3	I/O
3	IO_L20N_3	N1	I/O
3	IO_L20P_3	M1	I/O
3	IO_L22N_3	P1	I/O
3	IO_L22P_3/VREF_3	N2	VREF
3	IO_L23N_3	P2	I/O
3	IO_L23P_3	R1	I/O
3	IO_L24N_3	M4	I/O
3	IO_L24P_3	N3	I/O
3	IP_3	J4	INPUT
3	IP_3/VREF_3	G4	VREF
3	IP_3/VREF_3	J5	VREF
3	VCCO_3	D2	VCCO
3	VCCO_3	H2	VCCO
3	VCCO_3	M2	VCCO
GND	GND	A1	GND
GND	GND	A16	GND
GND	GND	B11	GND
GND	GND	B7	GND
GND	GND	C14	GND
GND	GND	C3	GND
GND	GND	E10	GND
GND	GND	E12	GND
GND	GND	E5	GND
GND	GND	F11	GND
GND	GND	F2	GND
GND	GND	F6	GND
GND	GND	F7	GND
GND	GND	F8	GND
GND	GND	F9	GND
GND	GND	G10	GND
GND	GND	G12	GND
GND	GND	G15	GND
GND	GND	G5	GND
GND	GND	G6	GND

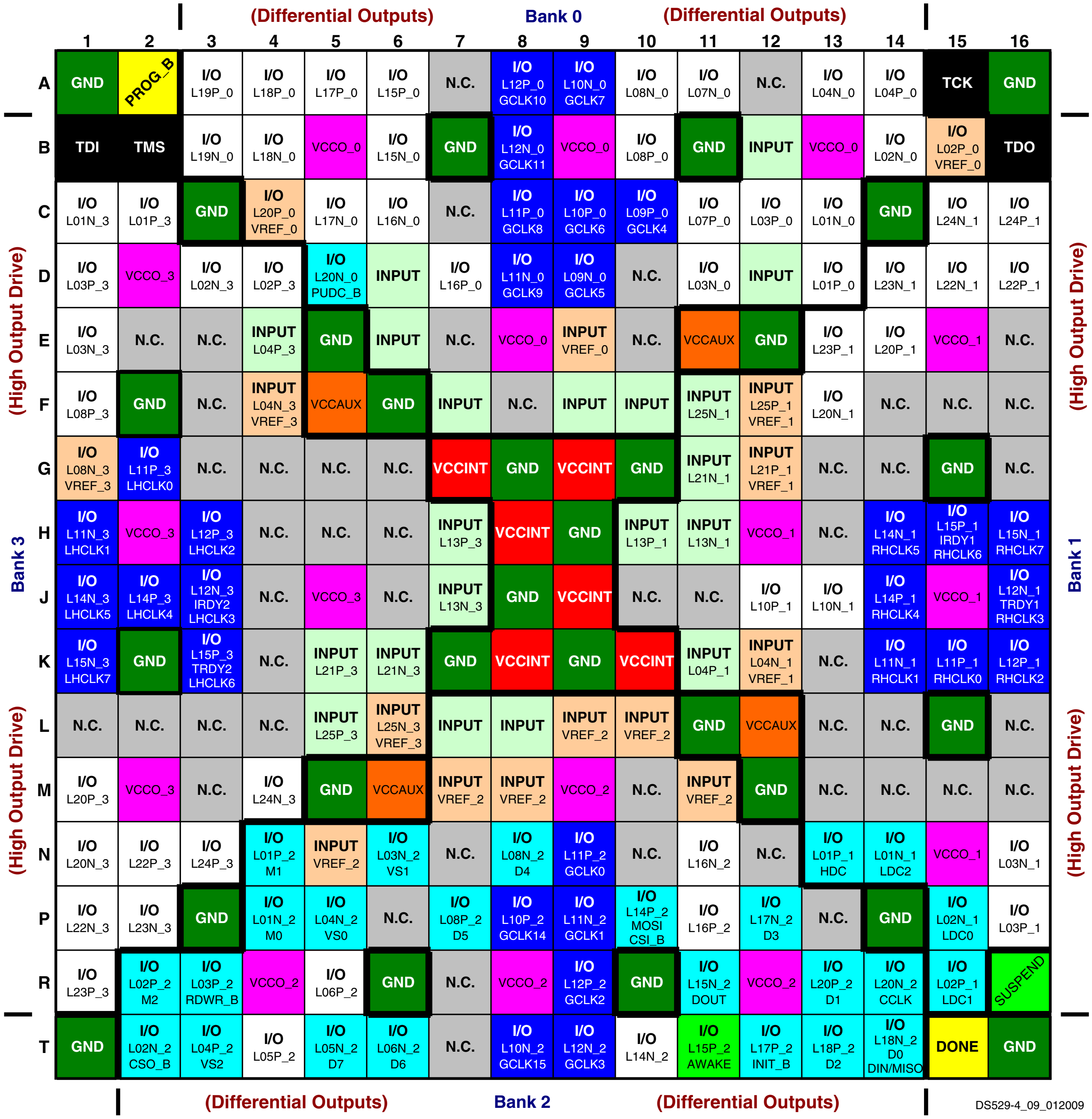
Table 69: **Spartan-3A FT256 Pinout (XC3S700A,**

Bank	XC3S700A XC3S1400A	FT256 Ball	Type
GND	GND	G8	GND
GND	GND	H11	GND
GND	GND	H5	GND
GND	GND	H7	GND
GND	GND	H9	GND
GND	GND	J10	GND
GND	GND	J6	GND
GND	GND	J8	GND
GND	GND	K11	GND
GND	GND	K12	GND
GND	GND	K2	GND
GND	GND	K5	GND
GND	GND	K7	GND
GND	GND	K9	GND
GND	GND	L10	GND
GND	GND	L11	GND
GND	GND	L15	GND
GND	GND	L6	GND
GND	GND	L8	GND
GND	GND	M12	GND
GND	GND	M5	GND
GND	GND	M8	GND
GND	GND	N10	GND
GND	GND	N7	GND
GND	GND	P14	GND
GND	GND	P3	GND
GND	GND	R10	GND
GND	GND	R6	GND
GND	GND	T1	GND
GND	GND	T16	GND
VCCAUX	SUSPEND	R16	PWRMGT
VCCAUX	DONE	T15	CONFIG
VCCAUX	PROG_B	A2	CONFIG
VCCAUX	TCK	A15	JTAG
VCCAUX	TDI	B1	JTAG
VCCAUX	TDO	B16	JTAG
VCCAUX	TMS	B2	JTAG
VCCAUX	VCCAUX	D6	VCCAUX
VCCAUX	VCCAUX	E11	VCCAUX
VCCAUX	VCCAUX	F12	VCCAUX

Table 69: **Spartan-3A FT256 Pinout (XC3S700A,**

Bank	XC3S700A XC3S1400A	FT256 Ball	Type
VCCAUX	VCCAUX	F5	VCCAUX
VCCAUX	VCCAUX	H14	VCCAUX
VCCAUX	VCCAUX	H4	VCCAUX
VCCAUX	VCCAUX	L12	VCCAUX
VCCAUX	VCCAUX	L5	VCCAUX
VCCAUX	VCCAUX	M10	VCCAUX
VCCAUX	VCCAUX	M6	VCCAUX
VCCINT	VCCINT	F10	VCCINT
VCCINT	VCCINT	G11	VCCINT
VCCINT	VCCINT	G7	VCCINT
VCCINT	VCCINT	G9	VCCINT
VCCINT	VCCINT	H10	VCCINT
VCCINT	VCCINT	H6	VCCINT
VCCINT	VCCINT	H8	VCCINT
VCCINT	VCCINT	J11	VCCINT
VCCINT	VCCINT	J7	VCCINT
VCCINT	VCCINT	J9	VCCINT
VCCINT	VCCINT	K10	VCCINT
VCCINT	VCCINT	K6	VCCINT
VCCINT	VCCINT	K8	VCCINT
VCCINT	VCCINT	L7	VCCINT
VCCINT	VCCINT	L9	VCCINT

FT256 Footprint (XC3S50A)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	GND	PROG_B	I/O L19P_0	I/O L18P_0	I/O L17P_0	I/O L15P_0	N.C.	I/O L12P_0 GCLK10	I/O L10N_0 GCLK7	I/O L08N_0	I/O L07N_0	N.C.	I/O L04N_0	I/O L04P_0	TCK	GND
B	TDI	TMS	I/O L19N_0	I/O L18N_0	VCCO_0	I/O L15N_0	GND	I/O L12N_0 GCLK11	VCCO_0	I/O L08P_0	GND	INPUT	VCCO_0	I/O L02N_0	I/O L02P_0 VREF_0	TDO
C	I/O L01N_3	I/O L01P_3	GND	I/O L20P_0 VREF_0	I/O L17N_0	I/O L16N_0	N.C.	I/O L11P_0 GCLK8	I/O L10P_0 GCLK6	I/O L09P_0 GCLK4	I/O L07P_0	I/O L03P_0	I/O L01N_0	GND	I/O L24N_1	I/O L24P_1
D	I/O L03P_3	VCCO_3	I/O L02N_3	I/O L02P_3	I/O L20N_0 PUDC_B	INPUT	I/O L16P_0	I/O L11N_0 GCLK9	I/O L09N_0 GCLK5	N.C.	I/O L03N_0	INPUT	I/O L01P_0	I/O L23N_1	I/O L22N_1	I/O L22P_1
E	I/O L03N_3	N.C.	N.C.	INPUT L04P_3	GND	INPUT	N.C.	VCCO_0	INPUT VREF_0	N.C.	VCCAUX	GND	I/O L23P_1	I/O L20P_1	VCCO_1	N.C.
F	I/O L08P_3	GND	N.C.	INPUT L04N_3 VREF_3	VCCAUX	GND	INPUT	N.C.	INPUT	INPUT	INPUT L25N_1	INPUT L25P_1 VREF_1	I/O L20N_1	N.C.	N.C.	N.C.
G	I/O L08N_3 VREF_3	I/O L11P_3 LHCLK0	N.C.	N.C.	N.C.	N.C.	VCCINT	GND	VCCINT	GND	INPUT L21N_1	INPUT L21P_1 VREF_1	N.C.	N.C.	GND	N.C.
H	I/O L11N_3 LHCLK1	VCCO_3	I/O L12P_3 LHCLK2	N.C.	N.C.	N.C.	INPUT L13P_3	VCCINT	GND	INPUT L13P_1	INPUT L13N_1	VCCO_1	N.C.	I/O L14N_1 RHCLK5	I/O L15P_1 IRDY1 RHCLK6	I/O L15N_1 RHCLK7
J	I/O L14N_3 LHCLK5	I/O L14P_3 LHCLK4	I/O L12N_3 IRDY2 LHCLK3	N.C.	VCCO_3	N.C.	INPUT L13N_3	GND	VCCINT	N.C.	N.C.	I/O L10P_1	I/O L10N_1	I/O L14P_1 RHCLK4	VCCO_1	I/O L12N_1 TRDY1 RHCLK3
K	I/O L15N_3 LHCLK7	GND	I/O L15P_3 TRDY2 LHCLK6	N.C.	INPUT L21P_3	INPUT L21N_3	GND	VCCINT	GND	VCCINT	INPUT L04P_1	INPUT L04N_1 VREF_1	N.C.	I/O L11N_1 RHCLK1	I/O L11P_1 RHCLK0	I/O L12P_1 RHCLK2
L	N.C.	N.C.	N.C.	N.C.	INPUT L25P_3	INPUT L25N_3 VREF_3	INPUT	INPUT	INPUT VREF_2	INPUT VREF_2	GND	VCCAUX	N.C.	N.C.	GND	N.C.
M	I/O L20P_3	VCCO_3	N.C.	I/O L24N_3	GND	VCCAUX	INPUT VREF_2	INPUT VREF_2	VCCO_2	N.C.	INPUT VREF_2	GND	N.C.	N.C.	N.C.	N.C.
N	I/O L20N_3	I/O L22P_3	I/O L24P_3	I/O L01P_2 M1	INPUT VREF_2	I/O L03N_2 VS1	N.C.	I/O L08N_2 D4	I/O L11P_2 GCLK0	N.C.	I/O L16N_2	N.C.	I/O L01P_1 HDC	I/O L01N_1 LDC2	VCCO_1	I/O L03N_1
P	I/O L22N_3	I/O L23N_3	GND	I/O L01N_2 M0	I/O L04N_2 VS0	N.C.	I/O L08P_2 D5	I/O L10P_2 GCLK14	I/O L11N_2 GCLK1	I/O L14P_2 MOSI CSI_B	I/O L16P_2	I/O L17N_2 D3	N.C.	GND	I/O L02N_1 LDC0	I/O L03P_1
R	I/O L23P_3	I/O L02P_2 M2	I/O L03P_2 RDWR_B	VCCO_2	I/O L06P_2	GND	N.C.	VCCO_2	I/O L12P_2 GCLK2	GND	I/O L15N_2 DOUT	VCCO_2	I/O L20P_2 D1	I/O L20N_2 CCLK	I/O L02P_1 LDC1	SUSPEND
T	GND	I/O L02N_2 CSO_B	I/O L04P_2 VS2	I/O L05P_2	I/O L05N_2 D7	I/O L06N_2 D6	N.C.	I/O L10N_2 GCLK15	I/O L12N_2 GCLK3	I/O L14N_2	I/O L15P_2 AWAKE	I/O L17P_2 INIT_B	I/O L18P_2 D2	I/O L18N_2 D0 DIN/MISO	DONE	GND

Figure 20: **XC3S50A FT256 Package Footprint (Top View)**

53	**I/O:** Unrestricted, general-purpose user I/O
20	**INPUT:** Unrestricted, general-purpose input pin
2	**CONFIG:** Dedicated configuration pins
51	**N.C.:** Not connected (XC3S50A only)
25	**DUAL:** Configuration pins, then possible user I/O
30	**CLK:** User I/O, input, or global buffer input
4	**JTAG:** Dedicated JTAG port pins
28	**GND:** Ground
15	**VREF:** User I/O or input voltage reference for bank
16	**VCCO:** Output voltage supply for bank
6	**VCCINT:** Internal core supply voltage (+1.2V)
4	**VCCAUX:** Auxiliary supply voltage
2	**SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins

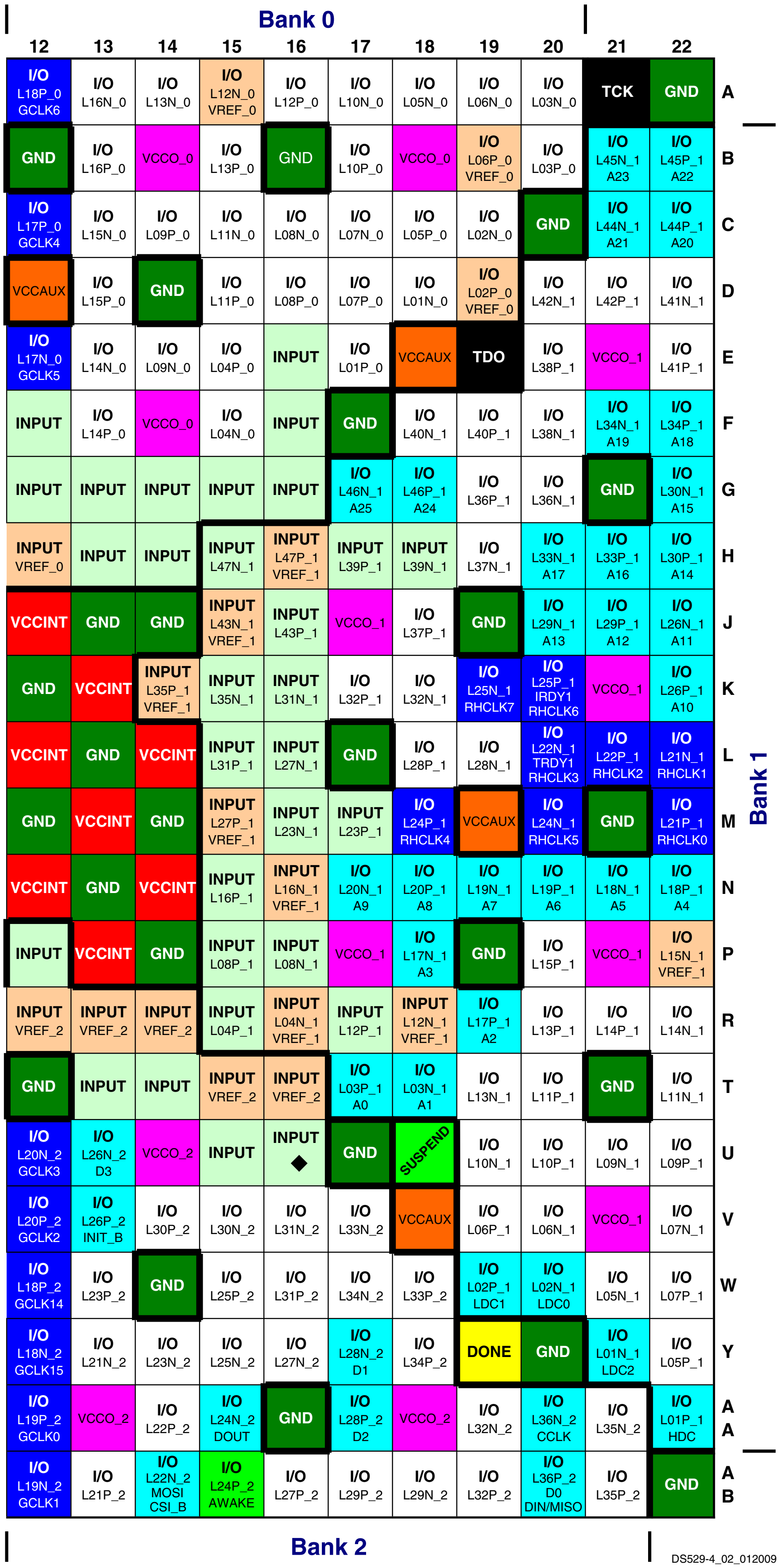
Table 83: **Spartan-3A FG484 Pinout*(Continued)***

Bank	Pin Name	FG484 Ball	Type
0	IO_L30P_0	E9	I/O
0	IO_L31N_0	B4	I/O
0	IO_L31P_0	A4	I/O
0	IO_L32N_0	D5	I/O
0	IO_L32P_0	C5	I/O
0	IO_L33N_0	B3	I/O
0	IO_L33P_0	A3	I/O
0	IO_L34N_0	F8	I/O
0	IO_L34P_0	E7	I/O
0	IO_L35N_0	E6	I/O
0	IO_L35P_0	F7	I/O
0	IO_L36N_0/PUDC_B	A2	DUAL
0	IO_L36P_0/VREF_0	B2	VREF
0	IP_0	E16	INPUT
0	IP_0	E8	INPUT
0	IP_0	F10	INPUT
0	IP_0	F12	INPUT
0	IP_0	F16	INPUT
0	IP_0	G10	INPUT
0	IP_0	G11	INPUT
0	IP_0	G12	INPUT
0	IP_0	G13	INPUT
0	IP_0	G14	INPUT
0	IP_0	G15	INPUT
0	IP_0	G16	INPUT
0	IP_0	G7	INPUT
0	IP_0	G9	INPUT
0	IP_0	H10	INPUT
0	IP_0	H13	INPUT
0	IP_0	H14	INPUT
0	IP_0/VREF_0	G8	VREF
0	IP_0/VREF_0	H12	VREF
0	IP_0/VREF_0	H9	VREF
0	VCCO_0	B10	VCCO
0	VCCO_0	B14	VCCO
0	VCCO_0	B18	VCCO
0	VCCO_0	B5	VCCO
0	VCCO_0	F14	VCCO
0	VCCO_0	F9	VCCO
1	IO_L01N_1/LDC2	Y21	DUAL

Table 83: **Spartan-3A FG484 Pinout*(Continued)***

Bank	Pin Name	FG484 Ball	Type
1	IO_L01P_1/HDC	AA22	DUAL
1	IO_L02N_1/LDC0	W20	DUAL
1	IO_L02P_1/LDC1	W19	DUAL
1	IO_L03N_1/A1	T18	DUAL
1	IO_L03P_1/A0	T17	DUAL
1	IO_L05N_1	W21	I/O
1	IO_L05P_1	Y22	I/O
1	IO_L06N_1	V20	I/O
1	IO_L06P_1	V19	I/O
1	IO_L07N_1	V22	I/O
1	IO_L07P_1	W22	I/O
1	IO_L09N_1	U21	I/O
1	IO_L09P_1	U22	I/O
1	IO_L10N_1	U19	I/O
1	IO_L10P_1	U20	I/O
1	IO_L11N_1	T22	I/O
1	IO_L11P_1	T20	I/O
1	IO_L13N_1	T19	I/O
1	IO_L13P_1	R20	I/O
1	IO_L14N_1	R22	I/O
1	IO_L14P_1	R21	I/O
1	IO_L15N_1/VREF_1	P22	VREF
1	IO_L15P_1	P20	I/O
1	IO_L17N_1/A3	P18	DUAL
1	IO_L17P_1/A2	R19	DUAL
1	IO_L18N_1/A5	N21	DUAL
1	IO_L18P_1/A4	N22	DUAL
1	IO_L19N_1/A7	N19	DUAL
1	IO_L19P_1/A6	N20	DUAL
1	IO_L20N_1/A9	N17	DUAL
1	IO_L20P_1/A8	N18	DUAL
1	IO_L21N_1/RHCLK1	L22	RHCLK
1	IO_L21P_1/RHCLK0	M22	RHCLK
1	IO_L22N_1/TRDY1/RHCLK3	L20	RHCLK
1	IO_L22P_1/RHCLK2	L21	RHCLK
1	IO_L24N_1/RHCLK5	M20	RHCLK
1	IO_L24P_1/RHCLK4	M18	RHCLK
1	IO_L25N_1/RHCLK7	K19	RHCLK
1	IO_L25P_1/IRDY1/RHCLK6	K20	RHCLK
1	IO_L26N_1/A11	J22	DUAL

Right Half of FG484 Package (Top View)



12	13	14	15	16	17	18	19	20	21	22	
I/O L18P_0 GCLK6	I/O L16N_0	I/O L13N_0	I/O L12N_0 VREF_0	I/O L12P_0	I/O L10N_0	I/O L05N_0	I/O L06N_0	I/O L03N_0	TCK	GND	A
GND	I/O L16P_0	VCCO_0	I/O L13P_0	GND	I/O L10P_0	VCCO_0	I/O L06P_0 VREF_0	I/O L03P_0	I/O L45N_1 A23	I/O L45P_1 A22	B
I/O L17P_0 GCLK4	I/O L15N_0	I/O L09P_0	I/O L11N_0	I/O L08N_0	I/O L07N_0	I/O L05P_0	I/O L02N_0	GND	I/O L44N_1 A21	I/O L44P_1 A20	C
VCCAUX	I/O L15P_0	GND	I/O L11P_0	I/O L08P_0	I/O L07P_0	I/O L01N_0	I/O L02P_0 VREF_0	I/O L42N_1	I/O L42P_1	I/O L41N_1	D
I/O L17N_0 GCLK5	I/O L14N_0	I/O L09N_0	I/O L04P_0	INPUT	I/O L01P_0	VCCAUX	TDO	I/O L38P_1	VCCO_1	I/O L41P_1	E
INPUT	I/O L14P_0	VCCO_0	I/O L04N_0	INPUT	GND	I/O L40N_1	I/O L40P_1	I/O L38N_1	I/O L34N_1 A19	I/O L34P_1 A18	F
INPUT	INPUT	INPUT	INPUT	INPUT	I/O L46N_1 A25	I/O L46P_1 A24	I/O L36P_1	I/O L36N_1	GND	I/O L30N_1 A15	G
INPUT VREF_0	INPUT	INPUT	INPUT L47N_1	INPUT L47P_1 VREF_1	INPUT L39P_1	INPUT L39N_1	I/O L37N_1	I/O L33N_1 A17	I/O L33P_1 A16	I/O L30P_1 A14	H
VCCINT	GND	GND	INPUT L43N_1 VREF_1	INPUT L43P_1	VCCO_1	I/O L37P_1	GND	I/O L29N_1 A13	I/O L29P_1 A12	I/O L26N_1 A11	J
GND	VCCINT	INPUT L35P_1 VREF_1	INPUT L35N_1	INPUT L31N_1	I/O L32P_1	I/O L32N_1	I/O L25N_1 RHCLK7	I/O L25P_1 IRDY1 RHCLK6	VCCO_1	I/O L26P_1 A10	K
VCCINT	GND	VCCINT	INPUT L31P_1	INPUT L27N_1	GND	I/O L28P_1	I/O L28N_1	I/O L22N_1 TRDY1 RHCLK3	I/O L22P_1 RHCLK2	I/O L21N_1 RHCLK1	L
GND	VCCINT	GND	INPUT L27P_1 VREF_1	INPUT L23N_1	INPUT L23P_1	I/O L24P_1 RHCLK4	VCCAUX	I/O L24N_1 RHCLK5	GND	I/O L21P_1 RHCLK0	M
VCCINT	GND	VCCINT	INPUT L16P_1	INPUT L16N_1 VREF_1	I/O L20N_1 A9	I/O L20P_1 A8	I/O L19N_1 A7	I/O L19P_1 A6	I/O L18N_1 A5	I/O L18P_1 A4	N
INPUT	VCCINT	GND	INPUT L08P_1	INPUT L08N_1	VCCO_1	I/O L17N_1 A3	GND	I/O L15P_1	VCCO_1	I/O L15N_1 VREF_1	P
INPUT VREF_2	INPUT VREF_2	INPUT VREF_2	INPUT L04P_1	INPUT L04N_1 VREF_1	INPUT L12P_1	INPUT L12N_1 VREF_1	I/O L17P_1 A2	I/O L13P_1	I/O L14P_1	I/O L14N_1	R
GND	INPUT	INPUT	INPUT VREF_2	INPUT VREF_2	I/O L03P_1 A0	I/O L03N_1 A1	I/O L13N_1	I/O L11P_1	GND	I/O L11N_1	T
I/O L20N_2 GCLK3	I/O L26N_2 D3	VCCO_2	INPUT	INPUT ◆	GND	SUSPEND	I/O L10N_1	I/O L10P_1	I/O L09N_1	I/O L09P_1	U
I/O L20P_2 GCLK2	I/O L26P_2 INIT_B	I/O L30P_2	I/O L30N_2	I/O L31N_2	I/O L33N_2	VCCAUX	I/O L06P_1	I/O L06N_1	VCCO_1	I/O L07N_1	V
I/O L18P_2 GCLK14	I/O L23P_2	GND	I/O L25P_2	I/O L31P_2	I/O L34N_2	I/O L33P_2	I/O L02P_1 LDC1	I/O L02N_1 LDC0	I/O L05N_1	I/O L07P_1	W
I/O L18N_2 GCLK15	I/O L21N_2	I/O L23N_2	I/O L25N_2	I/O L27N_2	I/O L28N_2 D1	I/O L34P_2	DONE	GND	I/O L01N_1 LDC2	I/O L05P_1	Y
I/O L19P_2 GCLK0	VCCO_2	I/O L22P_2	I/O L24N_2 DOUT	GND	I/O L28P_2 D2	VCCO_2	I/O L32N_2	I/O L36N_2 CCLK	I/O L35N_2	I/O L01P_1 HDC	AA
I/O L19N_2 GCLK1	I/O L21P_2	I/O L22N_2 MOSI CSI_B	I/O L24P_2 AWAKE	I/O L27P_2	I/O L29P_2	I/O L29N_2	I/O L32P_2	I/O L36P_2 D0 DIN/MISO	I/O L35P_2	GND	AB

Figure 26:

FG676: 676-ball Fine-pitch Ball Grid Array

The 676-ball fine-pitch ball grid array, FG676, supports the XC3S1400A FPGA.

Table 87 lists all the FG676 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The XC3S1400A has 17 unconnected balls, indicated as N.C. (No Connection) in Table 87 and with the black diamond character (◆) in Table 87 and Figure 27.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at:

> www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 87: **Spartan-3A FG676 Pinout**

Bank	Pin Name	FG676 Ball	Type
0	IO_L01N_0	F20	I/O
0	IO_L01P_0	G20	I/O
0	IO_L02N_0	F19	I/O
0	IO_L02P_0/VREF_0	G19	VREF
0	IO_L05N_0	C22	I/O
0	IO_L05P_0	D22	I/O
0	IO_L06N_0	C23	I/O
0	IO_L06P_0	D23	I/O
0	IO_L07N_0	A22	I/O
0	IO_L07P_0	B23	I/O
0	IO_L08N_0	G17	I/O
0	IO_L08P_0	H17	I/O
0	IO_L09N_0	B21	I/O
0	IO_L09P_0	C21	I/O
0	IO_L10N_0	D21	I/O
0	IO_L10P_0	E21	I/O
0	IO_L11N_0	C20	I/O
0	IO_L11P_0	D20	I/O
0	IO_L12N_0	K16	I/O
0	IO_L12P_0	J16	I/O
0	IO_L13N_0	E17	I/O
0	IO_L13P_0	F17	I/O
0	IO_L14N_0	A20	I/O
0	IO_L14P_0/VREF_0	B20	VREF
0	IO_L15N_0	A19	I/O
0	IO_L15P_0	B19	I/O
0	IO_L16N_0	H15	I/O
0	IO_L16P_0	G15	I/O
0	IO_L17N_0	C18	I/O
0	IO_L17P_0	D18	I/O
0	IO_L18N_0	A18	I/O
0	IO_L18P_0	B18	I/O
0	IO_L19N_0	B17	I/O
0	IO_L19P_0	C17	I/O
0	IO_L20N_0/VREF_0	E15	VREF
0	IO_L20P_0	F15	I/O
0	IO_L21N_0	C16	I/O
0	IO_L21P_0	D17	I/O
0	IO_L22N_0	C15	I/O
0	IO_L22P_0	D16	I/O
0	IO_L23N_0	A15	I/O
0	IO_L23P_0	B15	I/O
0	IO_L24N_0	F14	I/O
0	IO_L24P_0	E14	I/O
0	IO_L25N_0/GCLK5	J14	GCLK
0	IO_L25P_0/GCLK4	K14	GCLK
0	IO_L26N_0/GCLK7	A14	GCLK
0	IO_L26P_0/GCLK6	B14	GCLK
0	IO_L27N_0/GCLK9	G13	GCLK
0	IO_L27P_0/GCLK8	F13	GCLK
0	IO_L28N_0/GCLK11	C13	GCLK
0	IO_L28P_0/GCLK10	B13	GCLK
0	IO_L29N_0	B12	I/O
0	IO_L29P_0	A12	I/O
0	IO_L30N_0	C12	I/O
0	IO_L30P_0	D13	I/O
0	IO_L31N_0	F12	I/O
0	IO_L31P_0	E12	I/O
0	IO_L32N_0/VREF_0	D11	VREF
0	IO_L32P_0	C11	I/O
0	IO_L33N_0	B10	I/O
0	IO_L33P_0	A10	I/O