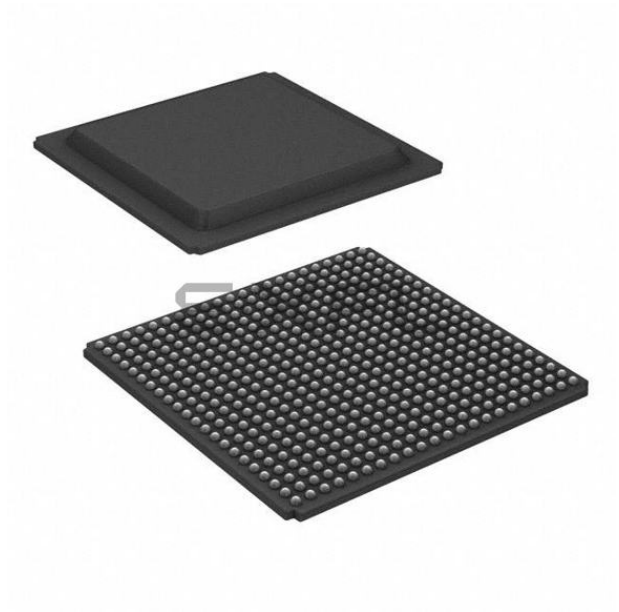
AMD Xilinx - XC3S700A-4FGG484I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1472
Number of Logic Elements/Cells	13248
Total RAM Bits	368640
Number of I/O	372
Number of Gates	700000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s700a-4fgg484i

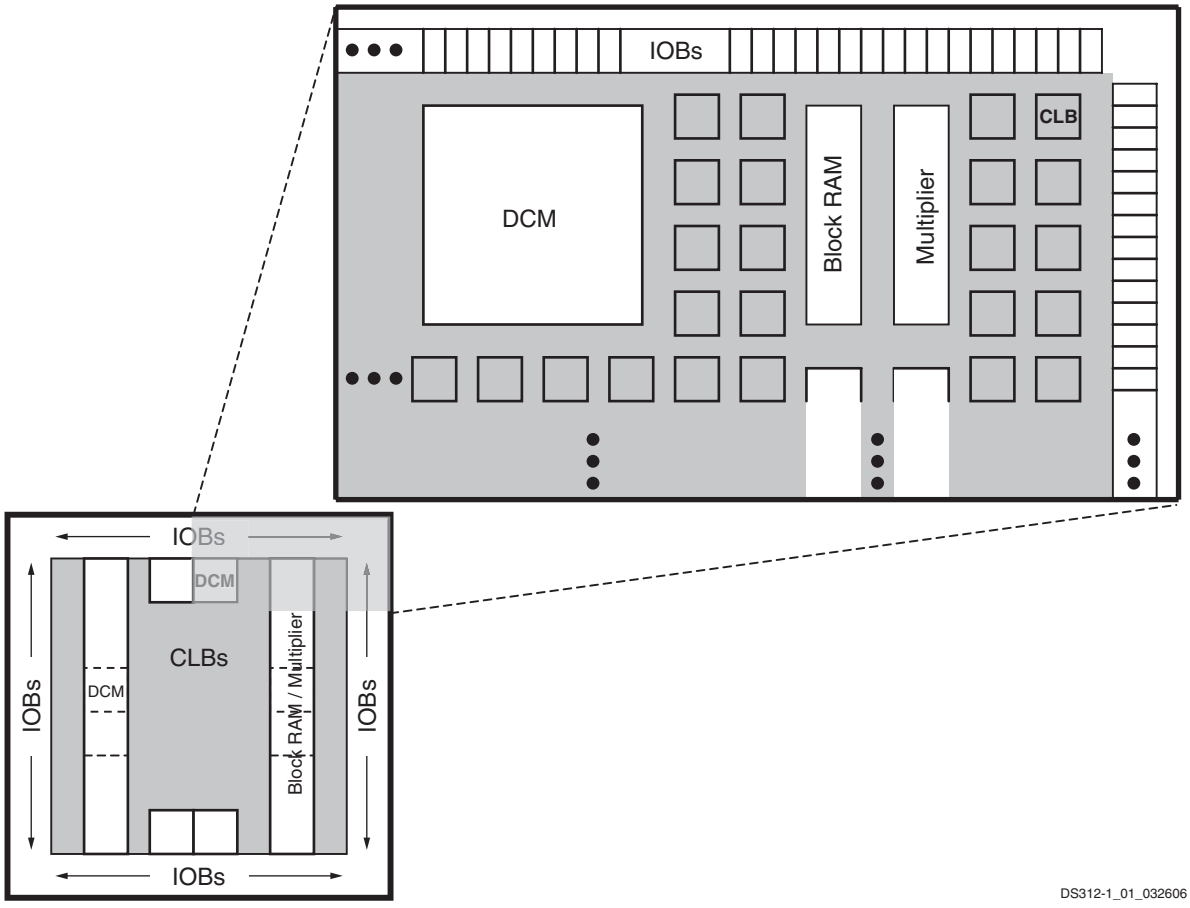
Architectural Overview

The Spartan-3A family architecture consists of five fundamental programmable functional elements:

- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. IOBs support bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including several high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A dual ring of staggered IOBs surrounds a regular array of CLBs. Each device has two columns of block RAM except for the XC3S50A, which has one column. Each RAM column consists of several 18-Kbit RAM blocks. Each block RAM is associated with a dedicated multiplier. The DCMs are positioned in the center with two at the top and two at the bottom of the device. The XC3S50A has DCMs only at the top, while the XC3S700A and XC3S1400A add two DCMs in the middle of the two columns of block RAM and multipliers.

The Spartan-3A family features a rich network of routing that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



Notes:

1. The XC3S700A and XC3S1400A have two additional DCMs on both the left and right sides as indicated by the dashed lines. The XC3S50A has only two DCMs at the top and only one Block RAM/Multiplier column.

Figure 1: **Spartan-3A FPGA Architecture**

Spartan-3A FPGA Design Documentation

The functionality of the Spartan®-3A FPGA Family is described in the following documents. The topics covered in each guide is listed below.

- **DS706: Extended Spartan-3A Family Overview**
  www.xilinx.com/support/documentation/data_sheets/ds706.pdf
- **UG331: Spartan-3 Generation FPGA User Guide**
  www.xilinx.com/support/documentation/user_guides/ug331.pdf
  - Clocking Resources
  - Digital Clock Managers (DCMs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
    - Distributed RAM
    - SRL16 Shift Registers
    - Carry and Arithmetic Logic
  - I/O Resources
  - Embedded Multiplier Blocks
  - Programmable Interconnect
  - ISE® Software Design Tools
  - IP Cores
  - Embedded Processing and Control Solutions
  - Pin Types and Package Overview
  - Package Drawings
  - Powering FPGAs
  - Power Management
- **UG332: Spartan-3 Generation Configuration User Guide**
  www.xilinx.com/support/documentation/user_guides/ug332.pdf
  - Configuration Overview
    - Configuration Pins and Behavior
    - Bitstream Sizes
  - Detailed Descriptions by Mode
    - Master Serial Mode using Xilinx® Platform Flash PROM
    - Master SPI Mode using Commodity SPI Serial Flash PROM
    - Master BPI Mode using Commodity Parallel NOR Flash PROM
    - Slave Parallel (SelectMAP) using a Processor
    - Slave Serial using a Processor
    - JTAG Mode
  - ISE iMPACT Programming Examples
  - MultiBoot Reconfiguration
  - Design Authentication using Device DNA

For application examples, see the Spartan-3A FPGA application notes.

- **Spartan-3A FPGA Application Notes**
  www.xilinx.com/support/documentation/spartan-3a_application_notes.htm

For specific hardware examples, please see the Spartan-3A FPGA Starter Kit board web page, which has links to various design examples and the user guide.

- **Spartan-3A/3AN FPGA Starter Kit Board Page**
  www.xilinx.com/s3astarter
- **UG334: Spartan-3A/3AN FPGA Starter Kit User Guide**
  www.xilinx.com/support/documentation/boards_and_kits/ug334.pdf

For information on the XA Automotive version of the Spartan-3A family, see the following data sheet.

- XA Spartan-3A Automotive FPGA Family Data Sheet
  www.xilinx.com/support/documentation/data_sheets/ds681.pdf

Create a Xilinx user account and sign up to receive automatic e-mail notification whenever this data sheet or the associated user guides are updated.

- Sign Up for Alerts
  www.xilinx.com/support/answers/18683.htm

Power Supply Specifications

Table 5: **Supply Voltage Thresholds for Power-On Reset**

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	1.0	2.0	V
V_{CCO2T}	Threshold for the V_{CCO} Bank 2 supply	1.0	2.0	V

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. Apply V_{CCINT} last for lowest overall power consumption (see UG331 chapter "Powering Spartan-3 Generation FPGAs" for more information).
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 6: **Supply Voltage Ramp Rate**

Symbol	Description	Min	Max	Units
V_{CCINTR}	Ramp rate from GND to valid V_{CCINT} supply level	0.2	100	ms
V_{CCAUXR}	Ramp rate from GND to valid V_{CCAUX} supply level	0.2	100	ms
V_{CCO2R}	Ramp rate from GND to valid V_{CCO} Bank 2 supply level	0.2	100	ms

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. Apply V_{CCINT} last for lowest overall power consumption (see UG331 chapter "Powering Spartan-3 Generation FPGAs" for more information).
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 7: **Supply Voltage Levels Necessary for Preserving CMOS Configuration Latch (CCL) Contents and RAM Data**

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain CMOS Configuration Latch (CCL) and RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain CMOS Configuration Latch (CCL) and RAM data	2.0	V

Differential I/O Standards

Differential Input Pairs

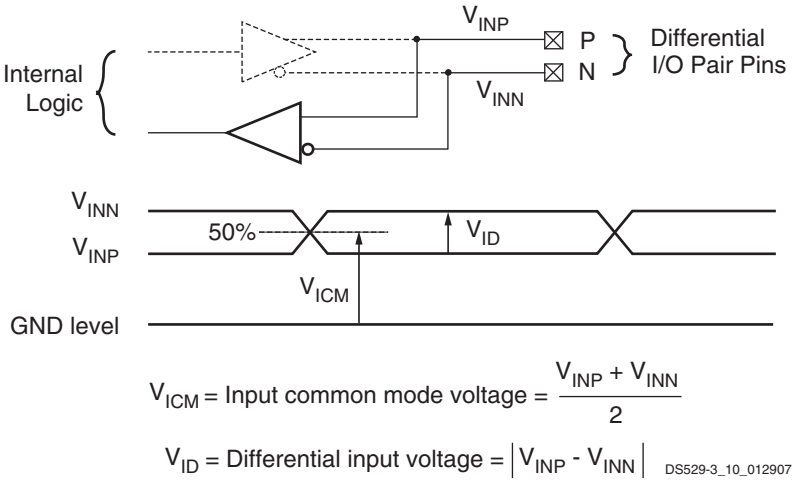


Figure 4: **Differential Input Voltages**

Table 13: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers(1)			V_{ID}			V_{ICM}(2)		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LVDS_25(3)	2.25	2.5	2.75	100	350	600	0.3	1.25	2.35
LVDS_33(3)	3.0	3.3	3.6	100	350	600	0.3	1.25	2.35
BLVDS_25(4)	2.25	2.5	2.75	100	300	–	0.3	1.3	2.35
MINI_LVDS_25(3)	2.25	2.5	2.75	200	–	600	0.3	1.2	1.95
MINI_LVDS_33(3)	3.0	3.3	3.6	200	–	600	0.3	1.2	1.95
LVPECL_25(5)	Inputs Only			100	800	1000	0.3	1.2	1.95
LVPECL_33(5)	Inputs Only			100	800	1000	0.3	1.2	2.8(6)
RSDS_25(3)	2.25	2.5	2.75	100	200	–	0.3	1.2	1.5
RSDS_33(3)	3.0	3.3	3.6	100	200	–	0.3	1.2	1.5
TMDS_33(3, 4, 7)	3.14	3.3	3.47	150	–	1200	2.7	–	3.23
PPDS_25(3)	2.25	2.5	2.75	100	–	400	0.2	–	2.3
PPDS_33(3)	3.0	3.3	3.6	100	–	400	0.2	–	2.3
DIFF_HSTL_I_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_II_18(8)	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_III_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_I	1.4	1.5	1.6	100	–	–	0.68		0.9
DIFF_HSTL_III	1.4	1.5	1.6	100	–	–	–	0.9	–
DIFF_SSTL18_I	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL18_II(8)	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL2_I	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL2_II(8)	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL3_I	3.0	3.3	3.6	100	–	–	1.1	–	1.9
DIFF_SSTL3_II	3.0	3.3	3.6	100	–	–	1.1	–	1.9

Notes:

1. The V_{CCO} rails supply only differential output drivers, not input circuits.
2. V_{ICM} must be less than V_{CCAUX}.
3. These true differential output standards are supported only on FPGA banks 0 and 2. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
4. See "External Termination Requirements for Differential I/O," page 20.
5. LVPECL is supported on inputs only, not outputs. LVPECL_33 requires V_{CCAUX}=3.3V ± 10%.
6. LVPECL_33 maximum V_{ICM} = the lower of 2.8V or $V_{CCAUX} - (V_{ID} / 2)$
7. Requires V_{CCAUX} = 3.3V ± 10% for inputs. $(V_{CCAUX} - 300\ mV) \leq V_{ICM} \leq (V_{CCAUX} - 37\ mV)$
8. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
9. All standards except for LVPECL and TMDS can have V_{CCAUX} at either 2.5V or 3.3V. Define your V_{CCAUX} level using the CONFIG VCCAUX constraint.

I/O Timing

Pin-to-Pin Clock-to-Output Times

Table 18: **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Clock-to-Output Times						
$T_{ICKOFDCM}$	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use.	LVCMOS25(2), 12mA output drive, Fast slew rate, with DCM(3)	XC3S50A	3.18	3.42	ns
			XC3S200A	3.21	3.27	ns
			XC3S400A	2.97	3.33	ns
			XC3S700A	3.39	3.50	ns
			XC3S1400A	3.51	3.99	ns
T_{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.	LVCMOS25(2), 12mA output drive, Fast slew rate, without DCM	XC3S50A	4.59	5.02	ns
			XC3S200A	4.88	5.24	ns
			XC3S400A	4.68	5.12	ns
			XC3S700A	4.97	5.34	ns
			XC3S1400A	5.06	5.69	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 23. If the latter is true, *add* the appropriate Output adjustment from Table 26.
3. DCM output jitter is included in all measurements.

Input Timing Adjustments

Table 23: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Single-Ended Standards			
LVTTL	0.62	0.62	ns
LVCMOS33	0.54	0.54	ns
LVCMOS25	0	0	ns
LVCMOS18	0.83	0.83	ns
LVCMOS15	0.60	0.60	ns
LVCMOS12	0.31	0.31	ns
PCI33_3	0.41	0.41	ns
PCI66_3	0.41	0.41	ns
HSTL_I	0.72	0.72	ns
HSTL_III	0.77	0.77	ns
HSTL_I_18	0.69	0.69	ns
HSTL_II_18	0.69	0.69	ns
HSTL_III_18	0.79	0.79	ns
SSTL18_I	0.71	0.71	ns
SSTL18_II	0.71	0.71	ns
SSTL2_I	0.68	0.68	ns
SSTL2_II	0.68	0.68	ns
SSTL3_I	0.78	0.78	ns
SSTL3_II	0.78	0.78	ns

Table 23: **Input Timing Adjustments by IOSTANDARD*(Continued)***

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Differential Standards			
LVDS_25	0.76	0.76	ns
LVDS_33	0.79	0.79	ns
BLVDS_25	0.79	0.79	ns
MINI_LVDS_25	0.78	0.78	ns
MINI_LVDS_33	0.79	0.79	ns
LVPECL_25	0.78	0.78	ns
LVPECL_33	0.79	0.79	ns
RSDS_25	0.79	0.79	ns
RSDS_33	0.77	0.77	ns
TMDS_33	0.79	0.79	ns
PPDS_25	0.79	0.79	ns
PPDS_33	0.79	0.79	ns
DIFF_HSTL_I_18	0.74	0.74	ns
DIFF_HSTL_II_18	0.72	0.72	ns
DIFF_HSTL_III_18	1.05	1.05	ns
DIFF_HSTL_I	0.72	0.72	ns
DIFF_HSTL_III	1.05	1.05	ns
DIFF_SSTL18_I	0.71	0.71	ns
DIFF_SSTL18_II	0.71	0.71	ns
DIFF_SSTL2_I	0.74	0.74	ns
DIFF_SSTL2_II	0.75	0.75	ns
DIFF_SSTL3_I	1.06	1.06	ns
DIFF_SSTL3_II	1.06	1.06	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8, Table 11, and Table 13.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Output Propagation Times

Table 24: **Timing for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Clock-to-Output Times						
T_{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OCLK input to data appearing at the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	All	2.87	3.13	ns
Propagation Times						
T_{IOOP}	The time it takes for data to travel from the IOB's O input to the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	All	2.78	2.91	ns
Set/Reset Times						
T_{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	All	3.63	3.89	ns
T_{IOGSRQ}	Time from asserting the Global Set Reset (GSR) input on the STARTUP_SPARTAN3A primitive to setting/resetting data at the Output pin			8.62	9.65	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 26.

Three-State Output Propagation Times

Table 25: **Timing for the IOB Three-State Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Synchronous Output Enable/Disable Times						
T_{IOCKHZ}	Time from the active transition at the OTCLK input of the Three-state Flip-Flop (TFF) to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	0.63	0.76	ns
T_{IOCKON}(2)	Time from the active transition at TFF's OTCLK input to when the Output pin drives valid data		All	2.80	3.06	ns
Asynchronous Output Enable/Disable Times						
T_{GTS}	Time from asserting the Global Three State (GTS) input on the STARTUP_SPARTAN3A primitive to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	9.47	10.36	ns
Set/Reset Times						
T_{IOSRHZ}	Time from asserting TFF's SR input to when the Output pin enters a high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.61	1.86	ns
T_{IOSRON}(2)	Time from asserting TFF's SR input at TFF to when the Output pin drives valid data		All	3.57	3.82	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 26.

Table 26: **Output Timing Adjustments for IOB*(Continued)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS25	Slow	2 mA	5.33	5.33	ns
		4 mA	2.81	2.81	ns
		6 mA	2.82	2.82	ns
		8 mA	1.14	1.14	ns
		12 mA	1.10	1.10	ns
		16 mA	0.83	0.83	ns
		24 mA	2.26(3)	2.26(3)	ns
	Fast	2 mA	4.36	4.36	ns
		4 mA	1.76	1.76	ns
		6 mA	1.25	1.25	ns
		8 mA	0.38	0.38	ns
		12 mA	0	0	ns
		16 mA	0.01	0.01	ns
		24 mA	0.01	0.01	ns
	QuietIO	2 mA	25.92	25.92	ns
		4 mA	25.92	25.92	ns
		6 mA	25.92	25.92	ns
		8 mA	15.57	15.57	ns
		12 mA	15.59	15.59	ns
		16 mA	14.27	14.27	ns
		24 mA	11.37	11.37	ns
LVCMOS18	Slow	2 mA	4.48	4.48	ns
		4 mA	3.69	3.69	ns
		6 mA	2.91	2.91	ns
		8 mA	1.99	1.99	ns
		12 mA	1.57	1.57	ns
		16 mA	1.19	1.19	ns
	Fast	2 mA	3.96	3.96	ns
		4 mA	2.57	2.57	ns
		6 mA	1.90	1.90	ns
		8 mA	1.06	1.06	ns
		12 mA	0.83	0.83	ns
		16 mA	0.63	0.63	ns
	QuietIO	2 mA	24.97	24.97	ns
		4 mA	24.97	24.97	ns
		6 mA	24.08	24.08	ns
		8 mA	16.43	16.43	ns
		12 mA	14.52	14.52	ns
		16 mA	13.41	13.41	ns

Table 26: **Output Timing Adjustments for IOB*(Continued)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS15	Slow	2 mA	5.82	5.82	ns
		4 mA	3.97	3.97	ns
		6 mA	3.21	3.21	ns
		8 mA	2.53	2.53	ns
		12 mA	2.06	2.06	ns
	Fast	2 mA	5.23	5.23	ns
		4 mA	3.05	3.05	ns
		6 mA	1.95	1.95	ns
		8 mA	1.60	1.60	ns
		12 mA	1.30	1.30	ns
	QuietIO	2 mA	34.11	34.11	ns
		4 mA	25.66	25.66	ns
		6 mA	24.64	24.64	ns
		8 mA	22.06	22.06	ns
		12 mA	20.64	20.64	ns
LVCMOS12	Slow	2 mA	7.14	7.14	ns
		4 mA	4.87	4.87	ns
		6 mA	5.67	5.67	ns
	Fast	2 mA	6.77	6.77	ns
		4 mA	5.02	5.02	ns
		6 mA	4.09	4.09	ns
	QuietIO	2 mA	50.76	50.76	ns
		4 mA	43.17	43.17	ns
		6 mA	37.31	37.31	ns
PCI33_3			0.34	0.34	ns
PCI66_3			0.34	0.34	ns
HSTL_I			0.78	0.78	ns
HSTL_III			1.16	1.16	ns
HSTL_I_18			0.35	0.35	ns
HSTL_II_18			0.30	0.30	ns
HSTL_III_18			0.47	0.47	ns
SSTL18_I			0.40	0.40	ns
SSTL18_II			0.30	0.30	ns
SSTL2_I			0	0	ns
SSTL2_II			–0.05	–0.05	ns
SSTL3_I			0	0	ns
SSTL3_II			0.17	0.17	ns

Miscellaneous DCM Timing

Table 42: **Miscellaneous DCM Timing**

Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN	Minimum duration of a RST pulse width	3	–	CLKIN cycles
DCM_RST_PW_MAX(2)	Maximum duration of a RST pulse width	N/A	N/A	seconds
		N/A	N/A	seconds
DCM_CONFIG_LAG_TIME(3)	Maximum duration from V_{CCINT} applied to FPGA configuration successfully completed (DONE pin goes High) and clocks applied to DCM DLL	N/A	N/A	minutes
		N/A	N/A	minutes

Notes:

1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFX180) are unaffected.
2. This specification is equivalent to the Virtex®-4 DCM_RESET specification. This specification does not apply for Spartan-3A FPGAs.
3. This specification is equivalent to the Virtex-4 TCONFIG specification. This specification does not apply for Spartan-3A FPGAs.

DNA Port Timing

Table 43: **DNA_PORT Interface Timing**

Symbol	Description	Min	Max	Units
T_{DNASSU}	Setup time on SHIFT before the rising edge of CLK	1.0	–	ns
T_{DNASH}	Hold time on SHIFT after the rising edge of CLK	0.5	–	ns
T_{DNADSU}	Setup time on DIN before the rising edge of CLK	1.0	–	ns
T_{DNADH}	Hold time on DIN after the rising edge of CLK	0.5	–	ns
T_{DNARSU}	Setup time on READ before the rising edge of CLK	5.0	10,000	ns
T_{DNARH}	Hold time on READ after the rising edge of CLK	0	–	ns
$T_{DNADCKO}$	Clock-to-output delay on DOUT after rising edge of CLK	0.5	1.5	ns
$T_{DNACLKF}$	CLK frequency	0	100	MHz
$T_{DNACLKH}$	CLK High time	1.0	∞	ns
$T_{DNACLKL}$	CLK Low time	1.0	∞	ns

Notes:

1. The minimum READ pulse width is 5 ns, the maximum READ pulse width is 10 µs.
2. The numbers in this table are based on the operating conditions set forth in Table 8.

Table 68: **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400) *(Continued)***

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
0	IO_L17P_0	IO_L17P_0	A5	I/O
0	IO_L18N_0	IO_L18N_0	B4	I/O
0	IO_L18P_0	IO_L18P_0	A4	I/O
0	IO_L19N_0	IO_L19N_0	B3	I/O
0	IO_L19P_0	IO_L19P_0	A3	I/O
0	IO_L20N_0/ PUDC_B	IO_L20N_0/ PUDC_B	D5	DUAL
0	IO_L20P_0/ VREF_0	IO_L20P_0/ VREF_0	C4	VREF
0	IP_0	IP_0	D6	INPUT
0	IP_0	IP_0	D12	INPUT
0	IP_0	IP_0	E6	INPUT
0	IP_0	IP_0	F7	INPUT
0	IP_0	IP_0	F9	INPUT
0	IP_0	IP_0	F10	INPUT
0	IP_0/VREF_0	IP_0/VREF_0	E9	VREF
0	VCCO_0	VCCO_0	B5	VCCO
0	VCCO_0	VCCO_0	B9	VCCO
0	VCCO_0	VCCO_0	B13	VCCO
0	VCCO_0	VCCO_0	E8	VCCO
1	IO_L01N_1/ LDC2	IO_L01N_1/ LDC2	N14	DUAL
1	IO_L01P_1/ HDC	IO_L01P_1/ HDC	N13	DUAL
1	IO_L02N_1/ LDC0	IO_L02N_1/ LDC0	P15	DUAL
1	IO_L02P_1/ LDC1	IO_L02P_1/ LDC1	R15	DUAL
1	IO_L03N_1	IO_L03N_1/A1	N16	DUAL
1	IO_L03P_1	IO_L03P_1/A0	P16	DUAL
1	N.C. (◆)	IO_L05N_1/ VREF_1	M14	VREF
1	N.C. (◆)	IO_L05P_1	M13	I/O
1	N.C. (◆)	IO_L06N_1/A3	K13	DUAL
1	N.C. (◆)	IO_L06P_1/A2	L13	DUAL
1	N.C. (◆)	IO_L07N_1/A5	M16	DUAL
1	N.C. (◆)	IO_L07P_1/A4	M15	DUAL
1	N.C. (◆)	IO_L08N_1/A7	L16	DUAL
1	N.C. (◆)	IO_L08P_1/A6	L14	DUAL
1	IO_L10N_1	IO_L10N_1/A9	J13	DUAL
1	IO_L10P_1	IO_L10P_1/A8	J12	DUAL
1	IO_L11N_1/ RHCLK1	IO_L11N_1/ RHCLK1	K14	RHCLK
1	IO_L11P_1/ RHCLK0	IO_L11P_1/ RHCLK0	K15	RHCLK

Table 68: **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400) *(Continued)***

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
1	IO_L12N_1/ TRDY1/RHCLK3	IO_L12N_1/ TRDY1/RHCLK3	J16	RHCLK
1	IO_L12P_1/ RHCLK2	IO_L12P_1/ RHCLK2	K16	RHCLK
1	IO_L14N_1/ RHCLK5	IO_L14N_1/ RHCLK5	H14	RHCLK
1	IO_L14P_1/ RHCLK4	IO_L14P_1/ RHCLK4	J14	RHCLK
1	IO_L15N_1/ RHCLK7	IO_L15N_1/ RHCLK7	H16	RHCLK
1	IO_L15P_1/ IRDY1/RHCLK6	IO_L15P_1/ IRDY1/RHCLK6	H15	RHCLK
1	N.C. (◆)	IO_L16N_1/A11	F16	DUAL
1	N.C. (◆)	IO_L16P_1/A10	G16	DUAL
1	N.C. (◆)	IO_L17N_1/A13	G14	DUAL
1	N.C. (◆)	IO_L17P_1/A12	H13	DUAL
1	N.C. (◆)	IO_L18N_1/A15	F15	DUAL
1	N.C. (◆)	IO_L18P_1/A14	E16	DUAL
1	N.C. (◆)	IO_L19N_1/A17	F14	DUAL
1	N.C. (◆)	IO_L19P_1/A16	G13	DUAL
1	IO_L20N_1	IO_L20N_1/A19	F13	DUAL
1	IO_L20P_1	IO_L20P_1/A18	E14	DUAL
1	IO_L22N_1	IO_L22N_1/A21	D15	DUAL
1	IO_L22P_1	IO_L22P_1/A20	D16	DUAL
1	IO_L23N_1	IO_L23N_1/A23	D14	DUAL
1	IO_L23P_1	IO_L23P_1/A22	E13	DUAL
1	IO_L24N_1	IO_L24N_1/A25	C15	DUAL
1	IO_L24P_1	IO_L24P_1/A24	C16	DUAL
1	IP_L04N_1/ VREF_1	IP_L04N_1/ VREF_1	K12	VREF
1	IP_L04P_1	IP_L04P_1	K11	INPUT
1	N.C. (◆)	IP_L09N_1	J11	INPUT
1	N.C. (◆)	IP_L09P_1/ VREF_1	J10	VREF
1	IP_L13N_1	IP_L13N_1	H11	INPUT
1	IP_L13P_1	IP_L13P_1	H10	INPUT
1	IP_L21N_1	IP_L21N_1	G11	INPUT
1	IP_L21P_1/ VREF_1	IP_L21P_1/ VREF_1	G12	VREF
1	IP_L25N_1	IP_L25N_1	F11	INPUT
1	IP_L25P_1/ VREF_1	IP_L25P_1/ VREF_1	F12	VREF
1	VCCO_1	VCCO_1	E15	VCCO
1	VCCO_1	VCCO_1	H12	VCCO
1	VCCO_1	VCCO_1	J15	VCCO
1	VCCO_1	VCCO_1	N15	VCCO

XC3S50A Differential I/O Alignment Differences

Also, some differential I/O pairs on the XC3S50A FPGA are aligned differently than the corresponding pairs on the XC3S200A or XC3S400A FPGAs, as shown in Table 74. All the mismatched pairs are in I/O Bank 2. The shading highlights the N side of each pair.

Table 74: **Differential I/O Differences in FT256**

FT256 Ball	Bank	XC3S50A	XC3S200A XC3S400A
T3	2	IO_L04P_2/VS2	IO_L03N_2/VS2
N6		IO_L03N_2/VS1	IO_L04P_2/VS1
R5		IO_L06P_2	IO_L05N_2
T5		IO_L05N_2/D7	IO_L06P_2/D7
P10		IO_L14P_2/MOSI /CSI_B	IO_L14N_2/MOSI /CSI_B
T10		IO_L14N_2	IO_L14P_2
R13		IO_L20P_2	IO_L18N_2
T14		IO_L18N_2	IO_L20P_2

XC3S50A Does Not Have BPI Mode Address Outputs

The XC3S50A FPGA does not generate the BPI-mode address pins during configuration. Table 75 summarizes these differences.

Table 75: **XC3S50A BPI Functional Differences**

FT256 Ball	Bank	XC3S50A	XC3S200A XC3S400A
N16	1	IO_L03N_1	IO_L03N_1/A1
P16		IO_L03P_1	IO_L03P_1/A0
J13		IO_L10N_1	IO_L10N_1/A9
J12		IO_L10P_1	IO_L10P_1/A8
F13		IO_L20N_1	IO_L20N_1/A19
E14		IO_L20P_1	IO_L20P_1/A18
D15		IO_L22N_1	IO_L22N_1/A21
D16		IO_L22P_1	IO_L22P_1/A20
D14		IO_L23N_1	IO_L23N_1/A23
E13		IO_L23P_1	IO_L23P_1/A22
C15		IO_L24N_1	IO_L24N_1/A25
C16		IO_L24P_1	IO_L24P_1/A24

FG320: 320-ball Fine-pitch Ball Grid Array

The 320-ball fine-pitch ball grid array package, FG320, supports two Spartan-3A FPGAs, the XC3S200A and the XC3S400A, as shown in Table 77 and Figure 23.

The FG320 package is an 18 x 18 array of solder balls minus the four center balls.

Table 77 lists all the package pins. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The shaded rows indicate pinout differences between the XC3S200A and the XC3S400A FPGAs. The XC3S200A has three unconnected balls, indicated as N.C. (No Connection) in Table 77 and with the black diamond character (◆) in Table 77 and Figure 23.

All other balls have nearly identical functionality on all three devices. Table 80 summarizes the Spartan-3A FPGA footprint migration differences for the FG320 package.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 77: **Spartan-3A FG320 Pinout**

Bank	Pin Name	FG320 Ball	Type
0	IO_L01N_0	C15	I/O
0	IO_L01P_0	C16	I/O
0	IO_L02N_0	A16	I/O
0	IO_L02P_0/VREF_0	B16	VREF
0	IO_L03N_0	A14	I/O
0	IO_L03P_0	A15	I/O
0	IO_L04N_0	C14	I/O
0	IO_L04P_0	B15	I/O
0	IO_L05N_0	D12	I/O
0	IO_L05P_0	C13	I/O
0	IO_L06N_0/VREF_0	A13	VREF
0	IO_L06P_0	B13	I/O
0	IO_L07N_0	B12	I/O
0	IO_L07P_0	C12	I/O
0	IO_L08N_0	F11	I/O
0	IO_L08P_0	E11	I/O
0	IO_L09N_0	A11	I/O
0	IO_L09P_0	B11	I/O
0	IO_L10N_0	D10	I/O
0	IO_L10P_0	C11	I/O
0	IO_L11N_0/GCLK5	C9	GCLK
0	IO_L11P_0/GCLK4	B10	GCLK
0	IO_L12N_0/GCLK7	B9	GCLK
0	IO_L12P_0/GCLK6	A10	GCLK
0	IO_L13N_0/GCLK9	B7	GCLK
0	IO_L13P_0/GCLK8	A8	GCLK
0	IO_L14N_0/GCLK11	C8	GCLK
0	IO_L14P_0/GCLK10	B8	GCLK
0	IO_L15N_0	C7	I/O
0	IO_L15P_0	D8	I/O
0	IO_L16N_0	E9	I/O
0	IO_L16P_0	D9	I/O
0	IO_L17N_0	B6	I/O
0	IO_L17P_0	A6	I/O
0	IO_L18N_0/VREF_0	A4	VREF
0	IO_L18P_0	A5	I/O
0	IO_L19N_0	E7	I/O
0	IO_L19P_0	F8	I/O
0	IO_L20N_0	D6	I/O
0	IO_L20P_0	C6	I/O
0	IO_L21N_0	A3	I/O
0	IO_L21P_0	B4	I/O
0	IO_L22N_0	D5	I/O
0	IO_L22P_0	C5	I/O
0	IO_L23N_0	A2	I/O
0	IO_L23P_0	B3	I/O
0	IO_L24N_0/PUDC_B	E5	DUAL
0	IO_L24P_0/VREF_0	E6	VREF
0	IP_0	D13	INPUT
0	IP_0	D14	INPUT
0	IP_0	E12	INPUT
0	***XC3S400A:*** IP_0 ***XC3S200A:*** N.C. (◆)	E13	INPUT
0	IP_0	F7	INPUT
0	IP_0	F9	INPUT
0	IP_0	F10	INPUT

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
0	IP_0	F12	INPUT
0	IP_0	G7	INPUT
0	IP_0	G8	INPUT
0	IP_0	G9	INPUT
0	IP_0	G11	INPUT
0	IP_0/VREF_0	E10	VREF
0	VCCO_0	B5	VCCO
0	VCCO_0	B14	VCCO
0	VCCO_0	D11	VCCO
0	VCCO_0	E8	VCCO
1	IO_L01N_1/LDC2	T17	DUAL
1	IO_L01P_1/HDC	R16	DUAL
1	IO_L02N_1/LDC0	U18	DUAL
1	IO_L02P_1/LDC1	U17	DUAL
1	IO_L03N_1/A1	R17	DUAL
1	IO_L03P_1/A0	T18	DUAL
1	IO_L05N_1	N16	I/O
1	IO_L05P_1	P16	I/O
1	IO_L06N_1	M14	I/O
1	IO_L06P_1	N15	I/O
1	IO_L07N_1/VREF_1	P18	VREF
1	IO_L07P_1	R18	I/O
1	IO_L09N_1/A3	M17	DUAL
1	IO_L09P_1/A2	M16	DUAL
1	IO_L10N_1/A5	N18	DUAL
1	IO_L10P_1/A4	N17	DUAL
1	IO_L11N_1/A7	L12	DUAL
1	IO_L11P_1/A6	L13	DUAL
1	IO_L13N_1/A9	K16	DUAL
1	IO_L13P_1/A8	L17	DUAL
1	IO_L14N_1/RHCLK1	K17	RHCLK
1	IO_L14P_1/RHCLK0	L18	RHCLK
1	IO_L15N_1/TRDY1/RHCLK3	J17	RHCLK
1	IO_L15P_1/RHCLK2	K18	RHCLK
1	IO_L17N_1/RHCLK5	K15	RHCLK
1	IO_L17P_1/RHCLK4	J16	RHCLK
1	IO_L18N_1/RHCLK7	H17	RHCLK
1	IO_L18P_1/IRDY1/RHCLK6	H18	RHCLK
1	IO_L19N_1/A11	G16	DUAL
1	IO_L19P_1/A10	H16	DUAL

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
1	IO_L21N_1	F17	I/O
1	IO_L21P_1	G17	I/O
1	IO_L22N_1/A13	E18	DUAL
1	IO_L22P_1/A12	F18	DUAL
1	IO_L23N_1/A15	H15	DUAL
1	IO_L23P_1/A14	J14	DUAL
1	IO_L25N_1	D17	I/O
1	IO_L25P_1	D18	I/O
1	IO_L26N_1/A17	E16	DUAL
1	IO_L26P_1/A16	F16	DUAL
1	IO_L27N_1/A19	F15	DUAL
1	IO_L27P_1/A18	G15	DUAL
1	IO_L29N_1/A21	E15	DUAL
1	IO_L29P_1/A20	D16	DUAL
1	IO_L30N_1/A23	B18	DUAL
1	IO_L30P_1/A22	C18	DUAL
1	IO_L31N_1/A25	B17	DUAL
1	IO_L31P_1/A24	C17	DUAL
1	IP_L04N_1/VREF_1	N14	VREF
1	IP_L04P_1	P15	INPUT
1	IP_L08N_1/VREF_1	L14	VREF
1	IP_L08P_1	M13	INPUT
1	IP_L12N_1	L16	INPUT
1	IP_L12P_1/VREF_1	M15	VREF
1	IP_L16N_1	K14	INPUT
1	IP_L16P_1	K13	INPUT
1	IP_L20N_1	J13	INPUT
1	IP_L20P_1/VREF_1	K12	VREF
1	IP_L24N_1	G14	INPUT
1	IP_L24P_1	H13	INPUT
1	IP_L28N_1	G13	INPUT
1	IP_L28P_1/VREF_1	H12	VREF
1	IP_L32N_1	F13	INPUT
1	IP_L32P_1/VREF_1	F14	VREF
1	VCCO_1	E17	VCCO
1	VCCO_1	H14	VCCO
1	VCCO_1	L15	VCCO
1	VCCO_1	P17	VCCO
2	IO_L01N_2/M0	U3	DUAL
2	IO_L01P_2/M1	T3	DUAL

Table 81: **Spartan-3A FG400 Pinout*(Continued)***

Bank	Pin Name	FG400 Ball	Type
1	IP_1/VREF_1	N14	VREF
1	IP_L04N_1/VREF_1	P15	VREF
1	IP_L04P_1	P14	INPUT
1	IP_L11N_1/VREF_1	M15	VREF
1	IP_L11P_1	M16	INPUT
1	IP_L15N_1	M13	INPUT
1	IP_L15P_1/VREF_1	M14	VREF
1	IP_L19N_1	L13	INPUT
1	IP_L19P_1	L14	INPUT
1	IP_L23N_1	K14	INPUT
1	IP_L23P_1/VREF_1	K15	VREF
1	IP_L27N_1	J15	INPUT
1	IP_L27P_1	J16	INPUT
1	IP_L31N_1	J13	INPUT
1	IP_L31P_1/VREF_1	J14	VREF
1	IP_L35N_1	H14	INPUT
1	IP_L35P_1	H15	INPUT
1	IP_L39N_1	G14	INPUT
1	IP_L39P_1/VREF_1	G15	VREF
1	VCCO_1	D19	VCCO
1	VCCO_1	H16	VCCO
1	VCCO_1	K19	VCCO
1	VCCO_1	N16	VCCO
1	VCCO_1	T19	VCCO
2	IO_L01N_2/M0	V4	DUAL
2	IO_L01P_2/M1	U4	DUAL
2	IO_L02N_2/CSO_B	Y2	DUAL
2	IO_L02P_2/M2	W3	DUAL
2	IO_L03N_2	W4	I/O
2	IO_L03P_2	Y3	I/O
2	IO_L04N_2	R7	I/O
2	IO_L04P_2	T6	I/O
2	IO_L05N_2	U5	I/O
2	IO_L05P_2	V5	I/O
2	IO_L06N_2	U6	I/O
2	IO_L06P_2	T7	I/O
2	IO_L07N_2/VS2	U7	DUAL
2	IO_L07P_2/RDWR_B	T8	DUAL
2	IO_L08N_2	Y5	I/O
2	IO_L08P_2	Y4	I/O

Table 81: **Spartan-3A FG400 Pinout*(Continued)***

Bank	Pin Name	FG400 Ball	Type
2	IO_L09N_2/VS0	W6	DUAL
2	IO_L09P_2/VS1	V6	DUAL
2	IO_L10N_2	Y7	I/O
2	IO_L10P_2	Y6	I/O
2	IO_L11N_2	U9	I/O
2	IO_L11P_2	T9	I/O
2	IO_L12N_2/D6	W8	DUAL
2	IO_L12P_2/D7	V7	DUAL
2	IO_L13N_2	V9	I/O
2	IO_L13P_2	V8	I/O
2	IO_L14N_2/D4	T10	DUAL
2	IO_L14P_2/D5	U10	DUAL
2	IO_L15N_2/GCLK13	Y9	GCLK
2	IO_L15P_2/GCLK12	W9	GCLK
2	IO_L16N_2/GCLK15	W10	GCLK
2	IO_L16P_2/GCLK14	V10	GCLK
2	IO_L17N_2/GCLK1	V11	GCLK
2	IO_L17P_2/GCLK0	Y11	GCLK
2	IO_L18N_2/GCLK3	V12	GCLK
2	IO_L18P_2/GCLK2	U11	GCLK
2	IO_L19N_2	R12	I/O
2	IO_L19P_2	T12	I/O
2	IO_L20N_2/MOSI/CSI_B	W12	DUAL
2	IO_L20P_2	Y12	I/O
2	IO_L21N_2	W13	I/O
2	IO_L21P_2	Y13	I/O
2	IO_L22N_2/DOUT	V13	DUAL
2	IO_L22P_2/AWAKE	U13	PWR MGMT
2	IO_L23N_2	R13	I/O
2	IO_L23P_2	T13	I/O
2	IO_L24N_2/D3	W14	DUAL
2	IO_L24P_2/INIT_B	Y14	DUAL
2	IO_L25N_2	T14	I/O
2	IO_L25P_2	V14	I/O
2	IO_L26N_2/D1	V15	DUAL
2	IO_L26P_2/D2	Y15	DUAL
2	IO_L27N_2	T15	I/O
2	IO_L27P_2	U15	I/O
2	IO_L28N_2	W16	I/O

Table 81: **Spartan-3A FG400 Pinout *(Continued)***

Bank	Pin Name	FG400 Ball	Type
VCCAUX	TDO	E17	JTAG
VCCAUX	TMS	E4	JTAG
VCCAUX	VCCAUX	A13	VCCAUX
VCCAUX	VCCAUX	E16	VCCAUX
VCCAUX	VCCAUX	H1	VCCAUX
VCCAUX	VCCAUX	K13	VCCAUX
VCCAUX	VCCAUX	L8	VCCAUX
VCCAUX	VCCAUX	N20	VCCAUX
VCCAUX	VCCAUX	T5	VCCAUX
VCCAUX	VCCAUX	Y8	VCCAUX
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	J12	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	N10	VCCINT

User I/Os by Bank

Table 82 indicates how the 311 available user-I/O pins are distributed between the four I/O banks on the FG400 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 82: **User I/Os Per Bank for the XC3S400A and XC3S700A in the FG400 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	77	50	12	1	6	8
Right	1	79	21	12	30	8	8
Bottom	2	76	35	6	21	6	8
Left	3	79	49	16	0	6	8
TOTAL		**311**	**155**	**46**	**52**	**26**	**32**

Footprint Migration Differences

The XC3S400A and XC3S700A FPGAs have identical footprints in the FG400 package. Designs can migrate between the XC3S400A and XC3S700A FPGAs without further consideration.

FG484: 484-ball Fine-pitch Ball Grid Array

The 484-ball fine-pitch ball grid array, FG484, supports both the XC3S700A and the XC3S1400A FPGAs. There are three pinout differences, as described in Table 86.

Table 83 lists all the FG484 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The shaded rows indicate pinout differences between the XC3S700A and the XC3S1400A FPGAs. The XC3S700A has three unconnected balls, indicated as N.C. (No Connection) in Table 83 and with the black diamond character (◆) in Table 83 and Figure 25.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 83: **Spartan-3A FG484 Pinout**

Bank	Pin Name	FG484 Ball	Type
0	IO_L01N_0	D18	I/O
0	IO_L01P_0	E17	I/O
0	IO_L02N_0	C19	I/O
0	IO_L02P_0/VREF_0	D19	VREF
0	IO_L03N_0	A20	I/O
0	IO_L03P_0	B20	I/O
0	IO_L04N_0	F15	I/O
0	IO_L04P_0	E15	I/O
0	IO_L05N_0	A18	I/O
0	IO_L05P_0	C18	I/O
0	IO_L06N_0	A19	I/O
0	IO_L06P_0/VREF_0	B19	VREF
0	IO_L07N_0	C17	I/O
0	IO_L07P_0	D17	I/O
0	IO_L08N_0	C16	I/O
0	IO_L08P_0	D16	I/O
0	IO_L09N_0	E14	I/O
0	IO_L09P_0	C14	I/O
0	IO_L10N_0	A17	I/O
0	IO_L10P_0	B17	I/O
0	IO_L11N_0	C15	I/O
0	IO_L11P_0	D15	I/O
0	IO_L12N_0/VREF_0	A15	VREF
0	IO_L12P_0	A16	I/O
0	IO_L13N_0	A14	I/O
0	IO_L13P_0	B15	I/O
0	IO_L14N_0	E13	I/O
0	IO_L14P_0	F13	I/O
0	IO_L15N_0	C13	I/O
0	IO_L15P_0	D13	I/O
0	IO_L16N_0	A13	I/O
0	IO_L16P_0	B13	I/O
0	IO_L17N_0/GCLK5	E12	GCLK
0	IO_L17P_0/GCLK4	C12	GCLK
0	IO_L18N_0/GCLK7	A11	GCLK
0	IO_L18P_0/GCLK6	A12	GCLK
0	IO_L19N_0/GCLK9	C11	GCLK
0	IO_L19P_0/GCLK8	B11	GCLK
0	IO_L20N_0/GCLK11	E11	GCLK
0	IO_L20P_0/GCLK10	D11	GCLK
0	IO_L21N_0	C10	I/O
0	IO_L21P_0	A10	I/O
0	IO_L22N_0	A8	I/O
0	IO_L22P_0	A9	I/O
0	IO_L23N_0	E10	I/O
0	IO_L23P_0	D10	I/O
0	IO_L24N_0/VREF_0	C9	VREF
0	IO_L24P_0	B9	I/O
0	IO_L25N_0	C8	I/O
0	IO_L25P_0	B8	I/O
0	IO_L26N_0	A6	I/O
0	IO_L26P_0	A7	I/O
0	IO_L27N_0	C7	I/O
0	IO_L27P_0	D7	I/O
0	IO_L28N_0	A5	I/O
0	IO_L28P_0	B6	I/O
0	IO_L29N_0	D6	I/O
0	IO_L29P_0	C6	I/O
0	IO_L30N_0	D8	I/O

Table 83: **Spartan-3A FG484 Pinout *(Continued)***

FG676: 676-ball Fine-pitch Ball Grid Array

The 676-ball fine-pitch ball grid array, FG676, supports the XC3S1400A FPGA.

Table 87 lists all the FG676 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The XC3S1400A has 17 unconnected balls, indicated as N.C. (No Connection) in Table 87 and with the black diamond character (◆) in Table 87 and Figure 27.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at:

www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 87: **Spartan-3A FG676 Pinout**

Bank	Pin Name	FG676 Ball	Type
0	IO_L01N_0	F20	I/O
0	IO_L01P_0	G20	I/O
0	IO_L02N_0	F19	I/O
0	IO_L02P_0/VREF_0	G19	VREF
0	IO_L05N_0	C22	I/O
0	IO_L05P_0	D22	I/O
0	IO_L06N_0	C23	I/O
0	IO_L06P_0	D23	I/O
0	IO_L07N_0	A22	I/O
0	IO_L07P_0	B23	I/O
0	IO_L08N_0	G17	I/O
0	IO_L08P_0	H17	I/O
0	IO_L09N_0	B21	I/O
0	IO_L09P_0	C21	I/O
0	IO_L10N_0	D21	I/O
0	IO_L10P_0	E21	I/O
0	IO_L11N_0	C20	I/O
0	IO_L11P_0	D20	I/O
0	IO_L12N_0	K16	I/O
0	IO_L12P_0	J16	I/O
0	IO_L13N_0	E17	I/O
0	IO_L13P_0	F17	I/O
0	IO_L14N_0	A20	I/O
0	IO_L14P_0/VREF_0	B20	VREF

Table 87: **Spartan-3A FG676 Pinout *(Continued)***

Bank	Pin Name	FG676 Ball	Type
0	IO_L15N_0	A19	I/O
0	IO_L15P_0	B19	I/O
0	IO_L16N_0	H15	I/O
0	IO_L16P_0	G15	I/O
0	IO_L17N_0	C18	I/O
0	IO_L17P_0	D18	I/O
0	IO_L18N_0	A18	I/O
0	IO_L18P_0	B18	I/O
0	IO_L19N_0	B17	I/O
0	IO_L19P_0	C17	I/O
0	IO_L20N_0/VREF_0	E15	VREF
0	IO_L20P_0	F15	I/O
0	IO_L21N_0	C16	I/O
0	IO_L21P_0	D17	I/O
0	IO_L22N_0	C15	I/O
0	IO_L22P_0	D16	I/O
0	IO_L23N_0	A15	I/O
0	IO_L23P_0	B15	I/O
0	IO_L24N_0	F14	I/O
0	IO_L24P_0	E14	I/O
0	IO_L25N_0/GCLK5	J14	GCLK
0	IO_L25P_0/GCLK4	K14	GCLK
0	IO_L26N_0/GCLK7	A14	GCLK
0	IO_L26P_0/GCLK6	B14	GCLK
0	IO_L27N_0/GCLK9	G13	GCLK
0	IO_L27P_0/GCLK8	F13	GCLK
0	IO_L28N_0/GCLK11	C13	GCLK
0	IO_L28P_0/GCLK10	B13	GCLK
0	IO_L29N_0	B12	I/O
0	IO_L29P_0	A12	I/O
0	IO_L30N_0	C12	I/O
0	IO_L30P_0	D13	I/O
0	IO_L31N_0	F12	I/O
0	IO_L31P_0	E12	I/O
0	IO_L32N_0/VREF_0	D11	VREF
0	IO_L32P_0	C11	I/O
0	IO_L33N_0	B10	I/O
0	IO_L33P_0	A10	I/O

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
1	IO_L53P_1	L20	I/O
1	IO_L54N_1	F24	I/O
1	IO_L54P_1	F25	I/O
1	IO_L55N_1	L17	I/O
1	IO_L55P_1	L18	I/O
1	IO_L56N_1	F23	I/O
1	IO_L56P_1	E24	I/O
1	IO_L57N_1	K18	I/O
1	IO_L57P_1	K19	I/O
1	IO_L58N_1	G22	I/O
1	IO_L58P_1/VREF_1	F22	VREF
1	IO_L59N_1	J20	I/O
1	IO_L59P_1	J19	I/O
1	IO_L60N_1	D26	I/O
1	IO_L60P_1	E26	I/O
1	IO_L61N_1	D24	I/O
1	IO_L61P_1	D25	I/O
1	IO_L62N_1/A21	H21	DUAL
1	IO_L62P_1/A20	J21	DUAL
1	IO_L63N_1/A23	C25	DUAL
1	IO_L63P_1/A22	C26	DUAL
1	IO_L64N_1/A25	G21	DUAL
1	IO_L64P_1/A24	H20	DUAL
1	IP_L16N_1	Y26	INPUT
1	IP_L16P_1	W25	INPUT
1	IP_L20N_1/VREF_1	V26	VREF
1	IP_L20P_1	W26	INPUT
1	IP_L24N_1/VREF_1	U26	VREF
1	IP_L24P_1	U25	INPUT
1	IP_L28N_1	R24	INPUT
1	IP_L28P_1/VREF_1	R23	VREF
1	IP_L32N_1	N25	INPUT
1	IP_L32P_1	N26	INPUT
1	IP_L36N_1	N23	INPUT
1	IP_L36P_1/VREF_1	M24	VREF
1	IP_L40N_1	L23	INPUT
1	IP_L40P_1	K24	INPUT
1	IP_L44N_1	H25	INPUT
1	IP_L44P_1/VREF_1	H26	VREF
1	IP_L48N_1	H24	INPUT
1	IP_L48P_1	H23	INPUT
1	IP_L52N_1/VREF_1	G25	VREF
1	IP_L52P_1	G26	INPUT
1	IP_L65N_1	B25	INPUT
1	IP_L65P_1/VREF_1	B26	VREF
1	VCCO_1	AB25	VCCO
1	VCCO_1	E25	VCCO
1	VCCO_1	H22	VCCO
1	VCCO_1	L19	VCCO
1	VCCO_1	L25	VCCO
1	VCCO_1	N22	VCCO
1	VCCO_1	T19	VCCO
1	VCCO_1	T25	VCCO
1	VCCO_1	W22	VCCO
2	IO_L01N_2/M0	AD4	DUAL
2	IO_L01P_2/M1	AC4	DUAL
2	IO_L02N_2/CSO_B	AA7	DUAL
2	IO_L02P_2/M2	Y7	DUAL
2	IO_L05N_2	Y9	I/O
2	IO_L05P_2	W9	I/O
2	IO_L06N_2	AF3	I/O
2	IO_L06P_2	AE3	I/O
2	IO_L07N_2	AF4	I/O
2	IO_L07P_2	AE4	I/O
2	IO_L08N_2	AD6	I/O
2	IO_L08P_2	AC6	I/O
2	IO_L09N_2	W10	I/O
2	IO_L09P_2	V10	I/O
2	IO_L10N_2	AE6	I/O
2	IO_L10P_2	AF5	I/O
2	IO_L11N_2	AE7	I/O
2	IO_L11P_2	AD7	I/O
2	IO_L12N_2	AA10	I/O
2	IO_L12P_2	Y10	I/O
2	IO_L13N_2	U11	I/O
2	IO_L13P_2	V11	I/O
2	IO_L14N_2	AB7	I/O
2	IO_L14P_2	AC8	I/O
2	IO_L15N_2	AC9	I/O
2	IO_L15P_2	AB9	I/O

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
3	IP_L58P_3	AA4	INPUT
3	IP_L62N_3	AB4	INPUT
3	IP_L62P_3	AB3	INPUT
3	IP_L66N_3/VREF_3	AE2	VREF
3	IP_L66P_3	AE1	INPUT
3	VCCO_3	AB2	VCCO
3	VCCO_3	E2	VCCO
3	VCCO_3	H5	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	L8	VCCO
3	VCCO_3	P5	VCCO
3	VCCO_3	T2	VCCO
3	VCCO_3	T8	VCCO
3	VCCO_3	W5	VCCO
GND	GND	A1	GND
GND	GND	A6	GND
GND	GND	A11	GND
GND	GND	A16	GND
GND	GND	A21	GND
GND	GND	A26	GND
GND	GND	AA1	GND
GND	GND	AA6	GND
GND	GND	AA11	GND
GND	GND	AA16	GND
GND	GND	AA21	GND
GND	GND	AA26	GND
GND	GND	AD3	GND
GND	GND	AD8	GND
GND	GND	AD13	GND
GND	GND	AD18	GND
GND	GND	AD24	GND
GND	GND	AF1	GND
GND	GND	AF6	GND
GND	GND	AF11	GND
GND	GND	AF16	GND
GND	GND	AF21	GND
GND	GND	AF26	GND
GND	GND	C3	GND
GND	GND	C9	GND
GND	GND	C14	GND

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
GND	GND	C19	GND
GND	GND	C24	GND
GND	GND	F1	GND
GND	GND	F6	GND
GND	GND	F11	GND
GND	GND	F16	GND
GND	GND	F21	GND
GND	GND	F26	GND
GND	GND	H3	GND
GND	GND	H8	GND
GND	GND	H14	GND
GND	GND	H19	GND
GND	GND	J24	GND
GND	GND	K10	GND
GND	GND	K17	GND
GND	GND	L1	GND
GND	GND	L6	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L15	GND
GND	GND	L21	GND
GND	GND	L26	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M16	GND
GND	GND	N3	GND
GND	GND	N8	GND
GND	GND	N11	GND
GND	GND	N15	GND
GND	GND	P12	GND
GND	GND	P16	GND
GND	GND	P19	GND
GND	GND	P24	GND
GND	GND	R11	GND
GND	GND	R13	GND
GND	GND	R15	GND
GND	GND	T1	GND
GND	GND	T6	GND
GND	GND	T12	GND
GND	GND	T14	GND

Right Half of FG676 Package (Top View)