AMD Xilinx - XC3S700A-4FTG256C Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1472
Number of Logic Elements/Cells	13248
Total RAM Bits	368640
Number of I/O	161
Number of Gates	700000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s700a-4ftg256c

Spartan-3A FPGA Design Documentation

The functionality of the Spartan®-3A FPGA Family is described in the following documents. The topics covered in each guide is listed below.

- **DS706: Extended Spartan-3A Family Overview**
  www.xilinx.com/support/documentation/data_sheets/ds706.pdf
- **UG331: Spartan-3 Generation FPGA User Guide**
  www.xilinx.com/support/documentation/user_guides/ug331.pdf
  - Clocking Resources
  - Digital Clock Managers (DCMs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
    - Distributed RAM
    - SRL16 Shift Registers
    - Carry and Arithmetic Logic
  - I/O Resources
  - Embedded Multiplier Blocks
  - Programmable Interconnect
  - ISE® Software Design Tools
  - IP Cores
  - Embedded Processing and Control Solutions
  - Pin Types and Package Overview
  - Package Drawings
  - Powering FPGAs
  - Power Management
- **UG332: Spartan-3 Generation Configuration User Guide**
  www.xilinx.com/support/documentation/user_guides/ug332.pdf
  - Configuration Overview
    - Configuration Pins and Behavior
    - Bitstream Sizes
  - Detailed Descriptions by Mode
    - Master Serial Mode using Xilinx® Platform Flash PROM
    - Master SPI Mode using Commodity SPI Serial Flash PROM
    - Master BPI Mode using Commodity Parallel NOR Flash PROM
    - Slave Parallel (SelectMAP) using a Processor
    - Slave Serial using a Processor
    - JTAG Mode
  - ISE iMPACT Programming Examples
  - MultiBoot Reconfiguration
  - Design Authentication using Device DNA

For application examples, see the Spartan-3A FPGA application notes.

- **Spartan-3A FPGA Application Notes**
  www.xilinx.com/support/documentation/spartan-3a_application_notes.htm

For specific hardware examples, please see the Spartan-3A FPGA Starter Kit board web page, which has links to various design examples and the user guide.

- **Spartan-3A/3AN FPGA Starter Kit Board Page**
  www.xilinx.com/s3astarter
- **UG334: Spartan-3A/3AN FPGA Starter Kit User Guide**
  www.xilinx.com/support/documentation/boards_and_kits/ug334.pdf

For information on the XA Automotive version of the Spartan-3A family, see the following data sheet.

- XA Spartan-3A Automotive FPGA Family Data Sheet
  www.xilinx.com/support/documentation/data_sheets/ds681.pdf

Create a Xilinx user account and sign up to receive automatic e-mail notification whenever this data sheet or the associated user guides are updated.

- Sign Up for Alerts
  www.xilinx.com/support/answers/18683.htm

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DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

Advance: Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

Production: These specifications are approved once the silicon has been characterized over numerous production lots. Parameter values are considered stable with no future changes expected.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan®-3A devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Absolute Maximum Ratings

Stresses beyond those listed under Table 4: Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 4: **Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Max	Units
V_{CCINT}	Internal supply voltage		–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage		–0.5	3.75	V
V_{CCO}	Output driver supply voltage		–0.5	3.75	V
V_{REF}	Input reference voltage		–0.5	V_{CCO} + 0.5	V
V_{IN}	Voltage applied to all User I/O pins and dual-purpose pins	Driver in a high-impedance state	–0.95	4.6	V
	Voltage applied to all Dedicated pins		–0.5	4.6	V
I_{IK}	Input clamp current per I/O pin	$-0.5V < V_{IN} < (V_{CCO} + 0.5V)$ (1)	–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model	–	±2000	V
		Charged device model	–	±500	V
		Machine model	–	±200	V
T_J	Junction temperature		–	125	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Upper clamp applies only when using PCI IOSTANDARDs.
2. For soldering guidelines, see UG112: *Device Packaging and Thermal Characteristics* and XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

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Quiescent Current Requirements

Table 10: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Typical(2)	Commercial Maximum(2)	Industrial Maximum(2)	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC3S50A	2	20	30	mA
		XC3S200A	7	50	70	mA
		XC3S400A	10	85	125	mA
		XC3S700A	13	120	185	mA
		XC3S1400A	24	220	310	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC3S50A	0.2	2	3	mA
		XC3S200A	0.2	2	3	mA
		XC3S400A	0.3	3	4	mA
		XC3S700A	0.3	3	4	mA
		XC3S1400A	0.3	3	4	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC3S50A	3	8	10	mA
		XC3S200A	5	12	15	mA
		XC3S400A	5	18	24	mA
		XC3S700A	6	28	34	mA
		XC3S1400A	10	50	58	mA

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8.
2. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using typical devices at room temperature (T_J of 25°C at V_{CCINT} = 1.2V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.6V, and V_{CCAUX} = 3.6V. The FPGA is programmed with a "blank" configuration data file (that is, a design with no functional elements instantiated). For conditions other than those described above (for example, a design including functional elements), measured quiescent current levels will be different than the values in the table.
3. For more accurate estimates for a specific design, use the Xilinx XPower tools. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3A FPGA XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer uses a netlist as input to provide maximum estimates as well as more accurate typical estimates.
4. The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.
5. For information on the power-saving Suspend mode, see XAPP480: *Using Suspend Mode in Spartan-3 Generation FPGAs*. Suspend mode typically saves 40% total power consumption compared to quiescent current.

Differential I/O Standards

Differential Input Pairs

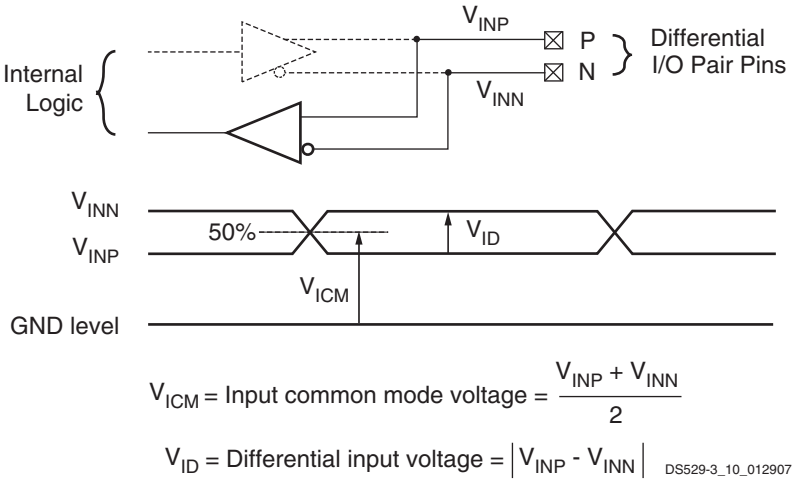


Figure 4: **Differential Input Voltages**

Table 13: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers(1)			V_{ID}			V_{ICM}(2)		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LVDS_25(3)	2.25	2.5	2.75	100	350	600	0.3	1.25	2.35
LVDS_33(3)	3.0	3.3	3.6	100	350	600	0.3	1.25	2.35
BLVDS_25(4)	2.25	2.5	2.75	100	300	–	0.3	1.3	2.35
MINI_LVDS_25(3)	2.25	2.5	2.75	200	–	600	0.3	1.2	1.95
MINI_LVDS_33(3)	3.0	3.3	3.6	200	–	600	0.3	1.2	1.95
LVPECL_25(5)	Inputs Only			100	800	1000	0.3	1.2	1.95
LVPECL_33(5)	Inputs Only			100	800	1000	0.3	1.2	2.8(6)
RSDS_25(3)	2.25	2.5	2.75	100	200	–	0.3	1.2	1.5
RSDS_33(3)	3.0	3.3	3.6	100	200	–	0.3	1.2	1.5
TMDS_33(3, 4, 7)	3.14	3.3	3.47	150	–	1200	2.7	–	3.23
PPDS_25(3)	2.25	2.5	2.75	100	–	400	0.2	–	2.3
PPDS_33(3)	3.0	3.3	3.6	100	–	400	0.2	–	2.3
DIFF_HSTL_I_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_II_18(8)	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_III_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_I	1.4	1.5	1.6	100	–	–	0.68		0.9
DIFF_HSTL_III	1.4	1.5	1.6	100	–	–	–	0.9	–
DIFF_SSTL18_I	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL18_II(8)	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL2_I	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL2_II(8)	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL3_I	3.0	3.3	3.6	100	–	–	1.1	–	1.9
DIFF_SSTL3_II	3.0	3.3	3.6	100	–	–	1.1	–	1.9

Notes:

1. The V_{CCO} rails supply only differential output drivers, not input circuits.
2. V_{ICM} must be less than V_{CCAUX}.
3. These true differential output standards are supported only on FPGA banks 0 and 2. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
4. See "External Termination Requirements for Differential I/O," page 20.
5. LVPECL is supported on inputs only, not outputs. LVPECL_33 requires V_{CCAUX}=3.3V ± 10%.
6. LVPECL_33 maximum V_{ICM} = the lower of 2.8V or $V_{CCAUX} - (V_{ID} / 2)$
7. Requires V_{CCAUX} = 3.3V ± 10% for inputs. $(V_{CCAUX} - 300\ mV) \leq V_{ICM} \leq (V_{CCAUX} - 37\ mV)$
8. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
9. All standards except for LVPECL and TMDS can have V_{CCAUX} at either 2.5V or 3.3V. Define your V_{CCAUX} level using the CONFIG VCCAUX constraint.

Table 20: **Setup and Hold Times for the IOB Input Path *(Continued)***

Symbol	Description	Conditions	IFD_DELAY_VALUE	Device	Speed Grade -5 Min	Speed Grade -4 Min	Units
$T_{IOICKPD}$	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25(3)	1	XC3S400A	–1.12	–1.12	ns
			2		–1.70	–1.70	ns
			3		–2.08	–2.08	ns
			4		–2.38	–2.38	ns
			5		–2.23	–2.23	ns
			6		–2.69	–2.69	ns
			7		–3.08	–3.08	ns
			8		–3.35	–3.35	ns
			1	XC3S700A	–1.67	–1.67	ns
			2		–2.27	–2.27	ns
			3		–2.59	–2.59	ns
			4		–2.92	–2.92	ns
			5		–2.89	–2.89	ns
			6		–3.22	–3.22	ns
			7		–3.52	–3.52	ns
			8		–3.81	–3.81	ns
			1	XC3S1400A	–1.60	–1.60	ns
			2		–2.06	–2.06	ns
			3		–2.46	–2.46	ns
			4		–2.86	–2.86	ns
			5		–2.88	–2.88	ns
			6		–3.24	–3.24	ns
			7		–3.55	–3.55	ns
			8		–3.89	–3.89	ns
Set/Reset Pulse Width							
T_{RPW_IOB}	Minimum pulse width to SR control input on IOB	-	-	All	1.33	1.61	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 23.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 23. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 21: **Sample Window (Source Synchronous)**

Symbol	Description	Max	Units
T_{SAMP}	Setup and hold capture window of an IOB flip-flop.	The input capture sample window value is highly specific to a particular application, device, package, I/O standard, I/O placement, DCM usage, and clock buffer. Please consult the appropriate Xilinx Answer Record for application-specific values. • Answer Record 30879	ps

Table 22: **Propagation Times for the IOB Input Path *(Continued)***

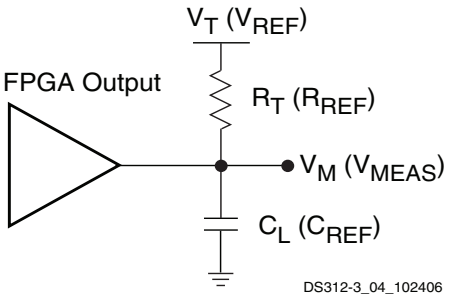
Symbol	Description	Conditions	DELAY_VALUE	Device	Speed Grade		Units
					-5	-4	
					Max	Max	
T_{IOPID}	The time it takes for data to travel from the Input pin to the I output with the input delay programmed	LVCMOS25(2)	5	XC3S1400A	3.17	3.52	ns
			6		3.52	3.92	ns
			7		3.82	4.18	ns
			8		4.10	4.57	ns
			9		3.84	4.31	ns
			10		4.20	4.79	ns
			11		4.46	5.06	ns
			12		4.87	5.51	ns
			13		5.07	5.73	ns
			14		5.43	6.08	ns
			15		5.73	6.33	ns
			16		6.01	6.77	ns
T_{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25(2)	IFD_DELAY_VALUE=0	XC3S50A	1.70	1.81	ns
				XC3S200A	1.85	2.04	ns
				XC3S400A	1.44	1.74	ns
				XC3S700A	1.48	1.74	ns
				XC3S1400A	1.50	1.97	ns
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25(2)	1	XC3S50A	2.30	2.41	ns
			2		3.24	3.35	ns
			3		3.65	3.98	ns
			4		4.18	4.55	ns
			5		4.02	4.47	ns
			6		4.86	5.32	ns
			7		5.61	6.17	ns
			8		6.11	6.75	ns
			1	XC3S200A	2.19	2.43	ns
			2		2.86	3.16	ns
			3		3.52	4.01	ns
			4		4.02	4.60	ns
			5		3.83	4.43	ns
			6		4.70	5.46	ns
			7		5.48	6.33	ns
			8		5.99	6.94	ns
			1	XC3S400A	1.93	2.25	ns
			2		2.57	2.90	ns
			3		3.16	3.66	ns
			4		3.63	4.19	ns

Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 27 lists the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H.

The Output test setup is shown in Figure 9. A termination voltage V_T is applied to the termination resistor R_T, the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (for example, LVCMOS, LVTTL), then R_T is set to 1MΩ to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



Notes:

1. The names shown in parentheses are used in the IBIS file.

Figure 9: **Output Test Setup**

Table 27: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended							
LVTTL		-	0	3.3	1M	0	1.4
LVCMOS33		-	0	3.3	1M	0	1.65
LVCMOS25		-	0	2.5	1M	0	1.25
LVCMOS18		-	0	1.8	1M	0	0.9
LVCMOS15		-	0	1.5	1M	0	0.75
LVCMOS12		-	0	1.2	1M	0	0.6
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
PCI66_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
HSTL_I		0.75	V_{REF} – 0.5	V_{REF} + 0.5	50	0.75	V_{REF}
HSTL_III		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	1.5	V_{REF}
HSTL_I_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_II_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL18_II		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
SSTL2_II		1.25	V_{REF} – 0.75	V_{REF} + 0.75	25	1.25	V_{REF}
SSTL3_I		1.5	V_{REF} – 0.75	V_{REF} + 0.75	50	1.5	V_{REF}
SSTL3_II		1.5	V_{REF} – 0.75	V_{REF} + 0.75	25	1.5	V_{REF}

Table 29: **Recommended Number of Simultaneously Switching Outputs per VCCO-GND Pair (V_{CCAUX}=3.3V)*(Continued)***

Signal Standard (IOSTANDARD)	Package Type			
	VQ100, TQ144		FT256, FG320, FG400, FG484, FG676	
	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)
Differential Standards (Number of I/O *Pairs* or Channels)				
LVDS_25	8	–	22	–
LVDS_33	8	–	27	–
BLVDS_25	1	1	4	4
MINI_LVDS_25	8	–	22	–
MINI_LVDS_33	8	–	27	–
LVPECL_25	Input Only			
LVPECL_33	Input Only			
RSDS_25	8	–	22	–
RSDS_33	8	–	27	–
TMDS_33	8	–	27	–
PPDS_25	8	–	22	–
PPDS_33	8	–	27	–
DIFF_HSTL_I	–	5	–	10
DIFF_HSTL_III	–	3	–	4
DIFF_HSTL_I_18	6	6	8	8
DIFF_HSTL_II_18	–	2	–	2
DIFF_HSTL_III_18	4	4	5	4
DIFF_SSTL18_I	3	6	3	7
DIFF_SSTL18_II	–	4	–	4
DIFF_SSTL2_I	5	5	9	9
DIFF_SSTL2_II	–	3	–	4
DIFF_SSTL3_I	3	4	4	5
DIFF_SSTL3_II	2	3	3	3

Notes:

1. Not all I/O standards are supported on all I/O banks. The left and right banks (I/O banks 1 and 3) support higher output drive current than the top and bottom banks (I/O banks 0 and 2). Similarly, true differential output standards, such as LVDS, RSDS, PPDS, miniLVDS, and TMDS, are only supported in top or bottom banks (I/O banks 0 and 2). Refer to UG331: *Spartan-3 Generation FPGA User Guide* for additional information.
2. The numbers in this table are recommendations that assume sound board lay out practice. Test limits are the V_{IL}/V_{IH} voltage limits for the respective I/O standard.
3. If more than one signal standard is assigned to the I/Os of a given bank, refer to XAPP689: *Managing Ground Bounce in Large FPGAs* for information on how to perform weighted average SSO calculations.

Clock Buffer/Multiplexer Switching Characteristics

Table 33: **Clock Distribution Switching Characteristics**

Description	Symbol	Minimum	Maximum Speed Grade		Units
			-5	-4	
Global clock buffer (BUFG, BUFGMUX, BUFGCE) I input to O-output delay	T_{GIO}	–	0.22	0.23	ns
Global clock multiplexer (BUFGMUX) select S-input setup to I0 and I1 inputs. Same as BUFGCE enable CE-input	T_{GSI}	–	0.56	0.63	ns
Frequency of signals distributed on global buffers (all sides)	F_{BUFG}	0	350	334	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.

Table 39: **Switching Characteristics for the DFS*(Continued)***

Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Lock Time								
LOCK_FX[2, 3]	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. If using both the DLL and the DFS, use the longer locking time.	5 MHz ≤ F_{CLKIN} ≤ 15 MHz	All	–	5	–	5	ms
		F_{CLKIN} > 15 MHz		–	450	–	450	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8 and Table 38.
2. DFS performance requires the additional logic automatically added by ISE 9.1i and later software revisions.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Maximum output jitter is characterized within a reasonable noise environment (150 ps input period jitter, 40 SSOs and 25% CLB switching) on an XC3S1400A FPGA. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply and PCB design. The actual maximum output jitter depends on the system application.
5. The CLKFX and CLKFX180 outputs always have an approximate 50% duty cycle.
6. Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, the data sheet specifies a maximum CLKFX jitter of "±[1% of CLKFX period + 200]". Assume the CLKFX output frequency is 100 MHz. The equivalent CLKFX period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 200 ps] = ±300 ps.

Configuration Clock (CCLK) Characteristics

Table 46: **Master Mode CCLK Output Period by *ConfigRate* Opti0on Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
T_{CCLK1}	CCLK clock period by ***ConfigRate*** setting	1 *(power-on value)*	Commercial	1,254	2,500	ns
			Industrial	1,180		ns
T_{CCLK3}		3	Commercial	413	833	ns
			Industrial	390		ns
T_{CCLK6}		6 (default)	Commercial	207	417	ns
			Industrial	195		ns
T_{CCLK7}		7	Commercial	178	357	ns
			Industrial	168		ns
T_{CCLK8}		8	Commercial	156	313	ns
			Industrial	147		ns
T_{CCLK10}		10	Commercial	123	250	ns
			Industrial	116		ns
T_{CCLK12}		12	Commercial	103	208	ns
			Industrial	97		ns
T_{CCLK13}		13	Commercial	93	192	ns
			Industrial	88		ns
T_{CCLK17}		17	Commercial	72	147	ns
			Industrial	68		ns
T_{CCLK22}		22	Commercial	54	114	ns
			Industrial	51		ns
T_{CCLK25}		25	Commercial	47	100	ns
			Industrial	45		ns
T_{CCLK27}		27	Commercial	44	93	ns
			Industrial	42		ns
T_{CCLK33}		33	Commercial	36	76	ns
			Industrial	34		ns
T_{CCLK44}		44	Commercial	26	57	ns
			Industrial	25		ns
T_{CCLK50}		50	Commercial	22	50	ns
			Industrial	21		ns
$T_{CCLK100}$		100	Commercial	11.2	25	ns
			Industrial	10.6		ns

Notes:

1. Set the ***ConfigRate*** option value when generating a configuration bitstream.

Table 47: **Master Mode CCLK Output Frequency by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
F_{CCLK1}	Equivalent CCLK clock frequency by ***ConfigRate*** setting	1 *(power-on value)*	Commercial	0.400	0.797	MHz
			Industrial		0.847	MHz
F_{CCLK3}		3	Commercial	1.20	2.42	MHz
			Industrial		2.57	MHz
F_{CCLK6}		6 (default)	Commercial	2.40	4.83	MHz
			Industrial		5.13	MHz
F_{CCLK7}		7	Commercial	2.80	5.61	MHz
			Industrial		5.96	MHz
F_{CCLK8}		8	Commercial	3.20	6.41	MHz
			Industrial		6.81	MHz
F_{CCLK10}		10	Commercial	4.00	8.12	MHz
			Industrial		8.63	MHz
F_{CCLK12}		12	Commercial	4.80	9.70	MHz
			Industrial		10.31	MHz
F_{CCLK13}		13	Commercial	5.20	10.69	MHz
			Industrial		11.37	MHz
F_{CCLK17}		17	Commercial	6.80	13.74	MHz
			Industrial		14.61	MHz
F_{CCLK22}		22	Commercial	8.80	18.44	MHz
			Industrial		19.61	MHz
F_{CCLK25}		25	Commercial	10.00	20.90	MHz
			Industrial		22.23	MHz
F_{CCLK27}		27	Commercial	10.80	22.39	MHz
			Industrial		23.81	MHz
F_{CCLK33}		33	Commercial	13.20	27.48	MHz
			Industrial		29.23	MHz
F_{CCLK44}		44	Commercial	17.60	37.60	MHz
			Industrial		40.00	MHz
F_{CCLK50}		50	Commercial	20.00	44.80	MHz
			Industrial		47.66	MHz
$F_{CCLK100}$		100	Commercial	40.00	88.68	MHz
			Industrial		94.34	MHz

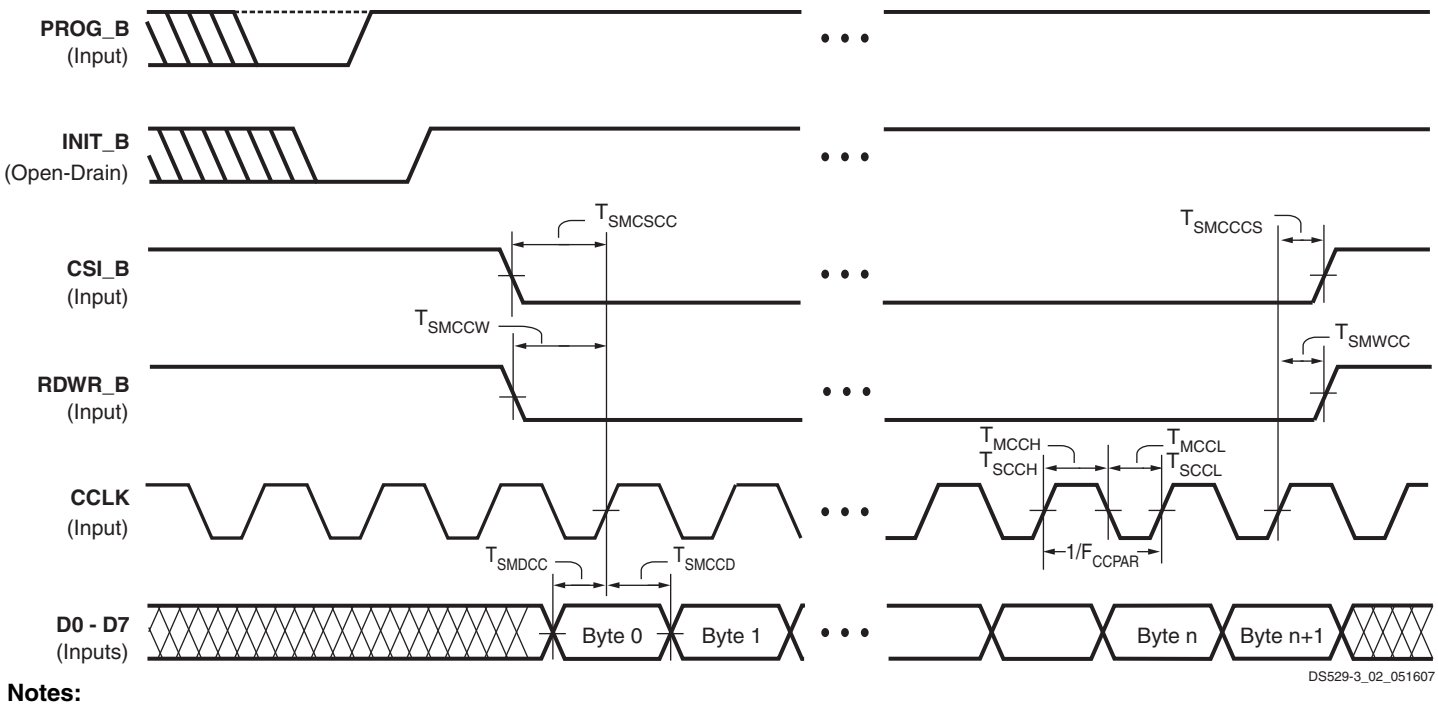
Table 48: **Master Mode CCLK Output Minimum Low and High Time**

Symbol	Description		*ConfigRate* Setting															Units
			1	3	6	7	8	10	12	13	17	22	25	27	33	44	50	100	
T_{MCCL}, T_{MCCH}	Master Mode CCLK Minimum Low and High Time	Commercial	595	196	98.3	84.5	74.1	58.4	48.9	44.1	34.2	25.6	22.3	20.9	17.1	12.3	10.4	5.3	ns
		Industrial	560	185	92.6	79.8	69.8	55.0	46.0	41.8	32.3	24.2	21.4	20.0	16.2	11.9	10.0	5.0	ns

Table 49: **Slave Mode CCLK Input Low and High Time**

Symbol	Description	Min	Max	Units
T_{SCCL}, T_{SCCH}	CCLK Low and High time	5	∞	ns

Slave Parallel Mode Timing



Notes:

1. It is possible to abort configuration by pulling CSI_B Low in a given CCLK cycle, then switching RDWR_B Low or High in any subsequent cycle for which CSI_B remains Low. The RDWR_B pin asynchronously controls the driver impedance of the D0 - D7 bus. When RDWR_B switches High, be careful to avoid contention on the D0 - D7 bus.
2. To pause configuration, pause CCLK instead of de-asserting CSI_B. See UG332 Chapter 7 section “Non-Continuous SelectMAP Data Loading” for more details.

Figure 13: **Waveforms for Slave Parallel Configuration**

Table 51: **Timing for the Slave Parallel Configuration Mode**

Symbol	Description		All Speed Grades		Units
			Min	Max	
Setup Times					
T_{SMDCC}(2)	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin		7	–	ns
T_{SMCSCC}	Setup time on the CSI_B pin before the rising transition at the CCLK pin		7	–	ns
T_{SMCCW}	Setup time on the RDWR_B pin before the rising transition at the CCLK pin		15	–	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins		1.0	–	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CSO_B pin		0	–	ns
T_{SMWCC}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	–	ns
Clock Timing					
T_{CCH}	The High pulse width at the CCLK input pin		5	–	ns
T_{CCL}	The Low pulse width at the CCLK input pin		5	–	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	0	80	MHz
		With bitstream compression	0	80	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.
2. Some Xilinx documents refer to Parallel modes as “SelectMAP” modes.

IEEE 1149.1/1532 JTAG Test Access Port Timing

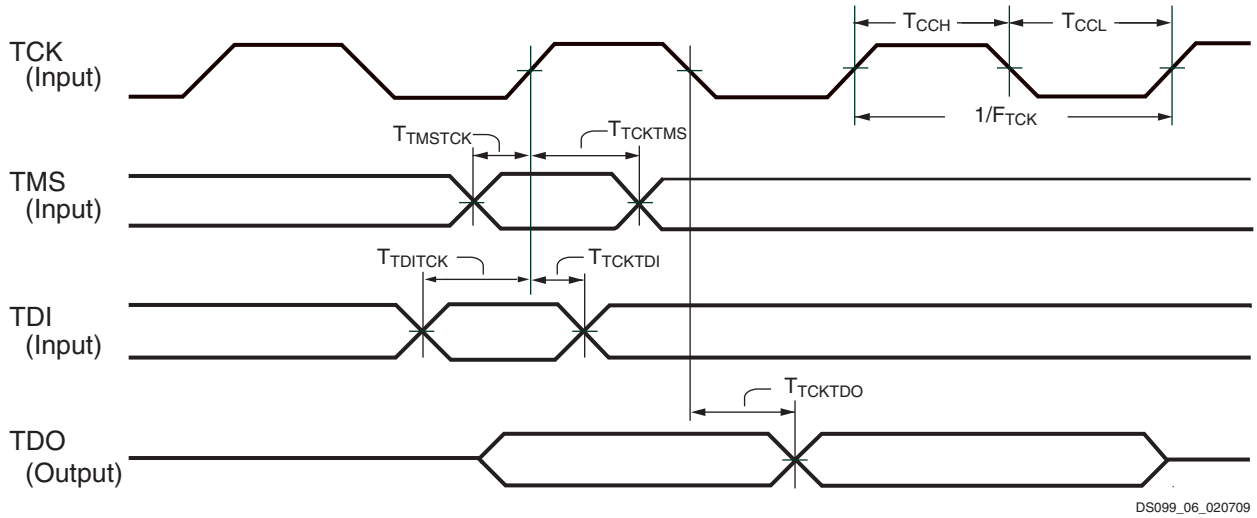


Figure 16: **JTAG Waveforms**

Table 56: **Timing for the JTAG Test Access Port**

Symbol	Description		All Speed Grades		Units
			Min	Max	
Clock-to-Output Times					
T_{TCKTDO}	The time from the falling transition on the TCK pin to data appearing at the TDO pin		1.0	11.0	ns
Setup Times					
T_{TDITCK}	The time from the setup of data at the TDI pin to the rising transition at the TCK pin	All devices and functions except those shown below	7.0	–	ns
		Boundary scan commands (INTEST, EXTEST, SAMPLE) on XC3S700A and XC3S1400A FPGAs	11.0		
T_{TMSTCK}	The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin		7.0	–	ns
Hold Times					
T_{TCKTDI}	The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin	All functions except those shown below	0	–	ns
		Configuration commands (CFG_IN, ISC_PROGRAM)	2.0		
T_{TCKTMS}	The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin		0	–	ns
Clock Timing					
T_{CCH}	The High pulse width at the TCK pin	All functions except ISC_DNA command	5	–	ns
T_{CCL}	The Low pulse width at the TCK pin		5	–	ns
T_{CCHDNA}	The High pulse width at the TCK pin	During ISC_DNA command	10	10,000	ns
T_{CCLDNA}	The Low pulse width at the TCK pin		10	10,000	ns
F_{TCK}	Frequency of the TCK signal	All operations on XC3S50A, XC3S200A, and XC3S400A FPGAs and for BYPASS or HIGHZ instructions on all FPGAs	0	33	MHz
		All operations on XC3S700A and XC3S1400A FPGAs, except for BYPASS or HIGHZ instructions		20	

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.
2. For details on JTAG see Chapter 9 “JTAG Configuration Mode and Boundary-Scan” in UG332 *Spartan-3 Generation Configuration User Guide*.

TQ144 Footprint

Note pin 1 indicator in top-left corner and logo orientation.

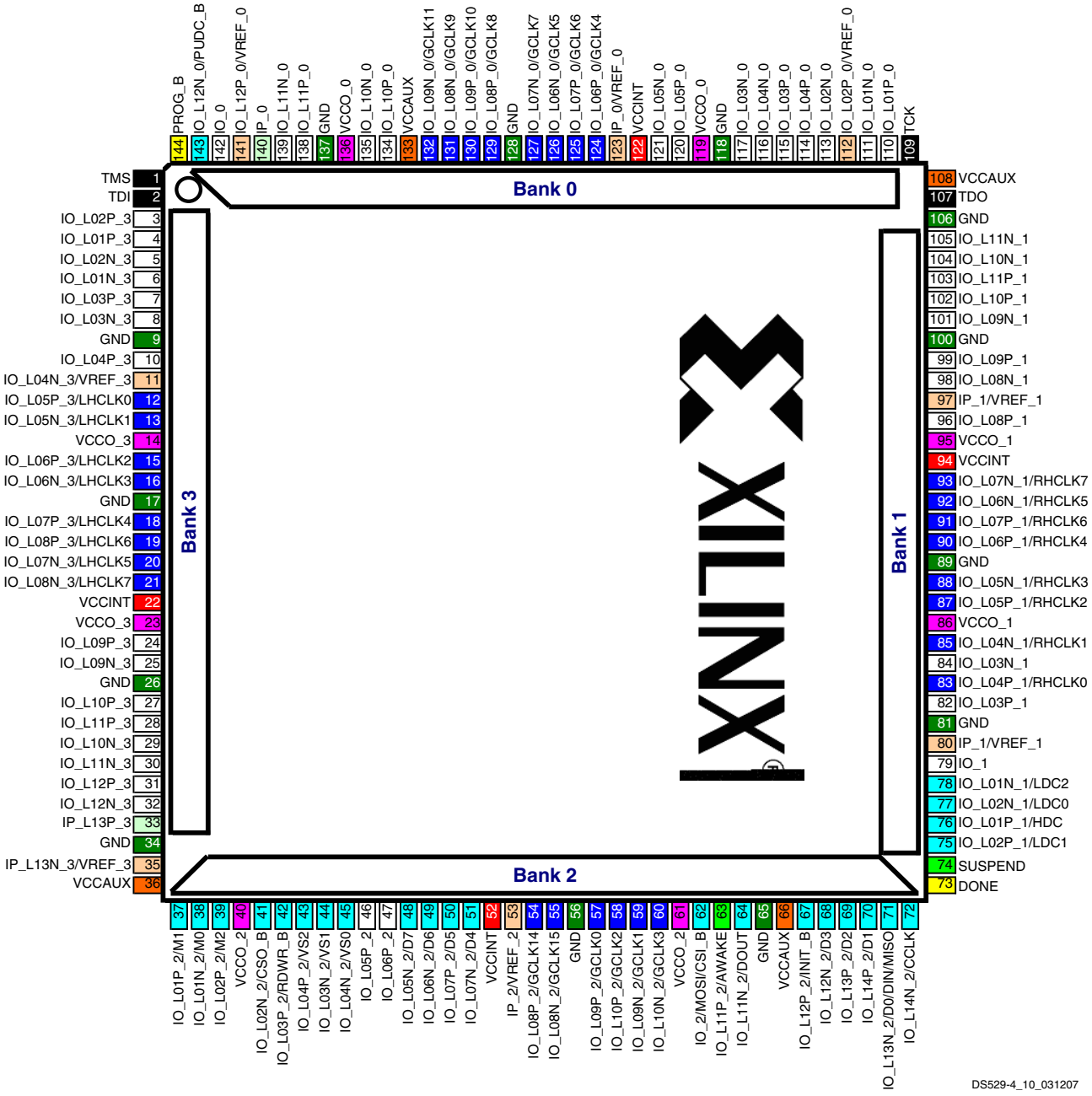


Figure 19: **TQ144 Package Footprint (Top View)**

42	**I/O:** Unrestricted, general-purpose user I/O	25	**DUAL:** Configuration pins, then possible user I/O	8	**VREF:** User I/O or input voltage reference for bank
2	**INPUT:** Unrestricted, general-purpose input pin	30	**CLK:** User I/O, input, or global buffer input	8	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core supply voltage (+1.2V)
0	**N.C.:** Not connected	13	**GND:** Ground	4	**VCCAUX:** Auxiliary supply voltage
2	**SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins				

Table 69: **Spartan-3A FT256 Pinout (XC3S700A,**

Bank	XC3S700A XC3S1400A	FT256 Ball	Type
1	IO_L20P_1/A18	E14	DUAL
1	IO_L22N_1/A21	D15	DUAL
1	IO_L22P_1/A20	D16	DUAL
1	IO_L23N_1/A23	D14	DUAL
1	IO_L23P_1/A22	E13	DUAL
1	IO_L24N_1/A25	C15	DUAL
1	IO_L24P_1/A24	C16	DUAL
1	IP_1/VREF_1	H12	VREF
1	IP_1/VREF_1	J14	VREF
1	IP_1/VREF_1	M13	VREF
1	IP_1/VREF_1	M14	VREF
1	VCCO_1	E15	VCCO
1	VCCO_1	J15	VCCO
1	VCCO_1	N15	VCCO
2	IO_L01N_2/M0	P4	DUAL
2	IO_L01P_2/M1	N4	DUAL
2	IO_L02N_2/CSO_B	T2	DUAL
2	IO_L02P_2/M2	R2	DUAL
2	IO_L03N_2/VS2	T3	DUAL
2	IO_L03P_2/RDWR_B	R3	DUAL
2	IO_L04N_2/VS0	P5	DUAL
2	IO_L04P_2/VS1	N6	DUAL
2	IO_L05N_2	R5	I/O
2	IO_L05P_2	T4	I/O
2	IO_L06N_2/D6	T6	DUAL
2	IO_L06P_2/D7	T5	DUAL
2	IO_L08N_2/D4	N8	DUAL
2	IO_L08P_2/D5	P7	DUAL
2	IO_L09N_2/GCLK13	T7	GCLK
2	IO_L09P_2/GCLK12	R7	GCLK
2	IO_L10N_2/GCLK15	T8	GCLK
2	IO_L10P_2/GCLK14	P8	GCLK
2	IO_L11N_2/GCLK1	P9	GCLK
2	IO_L11P_2/GCLK0	N9	GCLK
2	IO_L12N_2/GCLK3	T9	GCLK
2	IO_L12P_2/GCLK2	R9	GCLK
2	IO_L14N_2/MOSI/CSI_B	P10	DUAL
2	IO_L14P_2	T10	I/O
2	IO_L15N_2/DOUT	R11	DUAL
2	IO_L15P_2/AWAKE	T11	PWRMGT

Table 69: **Spartan-3A FT256 Pinout (XC3S700A,**

Bank	XC3S700A XC3S1400A	FT256 Ball	Type
2	IO_L16N_2	N11	I/O
2	IO_L16P_2	P11	I/O
2	IO_L17N_2/D3	P12	DUAL
2	IO_L17P_2/INIT_B	T12	DUAL
2	IO_L18N_2/D1	R13	DUAL
2	IO_L18P_2/D2	T13	DUAL
2	IO_L19N_2	P13	I/O
2	IO_L19P_2	N12	I/O
2	IO_L20N_2/CCLK	R14	DUAL
2	IO_L20P_2/D0/DIN/MISO	T14	DUAL
2	IP_2/VREF_2	M11	VREF
2	IP_2/VREF_2	M7	VREF
2	IP_2/VREF_2	M9	VREF
2	IP_2/VREF_2	N5	VREF
2	IP_2/VREF_2	P6	VREF
2	VCCO_2	R12	VCCO
2	VCCO_2	R4	VCCO
2	VCCO_2	R8	VCCO
3	IO_L01N_3	C1	I/O
3	IO_L01P_3	C2	I/O
3	IO_L02N_3	D3	I/O
3	IO_L02P_3	D4	I/O
3	IO_L03N_3	E1	I/O
3	IO_L03P_3	D1	I/O
3	IO_L04N_3	F4	I/O
3	IO_L04P_3	E4	I/O
3	IO_L05N_3	E2	I/O
3	IO_L05P_3	E3	I/O
3	IO_L07N_3	G3	I/O
3	IO_L07P_3	F3	I/O
3	IO_L08N_3/VREF_3	G1	VREF
3	IO_L08P_3	F1	I/O
3	IO_L11N_3/LHCLK1	H1	LHCLK
3	IO_L11P_3/LHCLK0	G2	LHCLK
3	IO_L12N_3/IRDY2/LHCLK3	J3	LHCLK
3	IO_L12P_3/LHCLK2	H3	LHCLK
3	IO_L14N_3/LHCLK5	J1	LHCLK
3	IO_L14P_3/LHCLK4	J2	LHCLK
3	IO_L15N_3/LHCLK7	K1	LHCLK
3	IO_L15P_3/TRDY2/LHCLK6	K3	LHCLK

FG320 Footprint

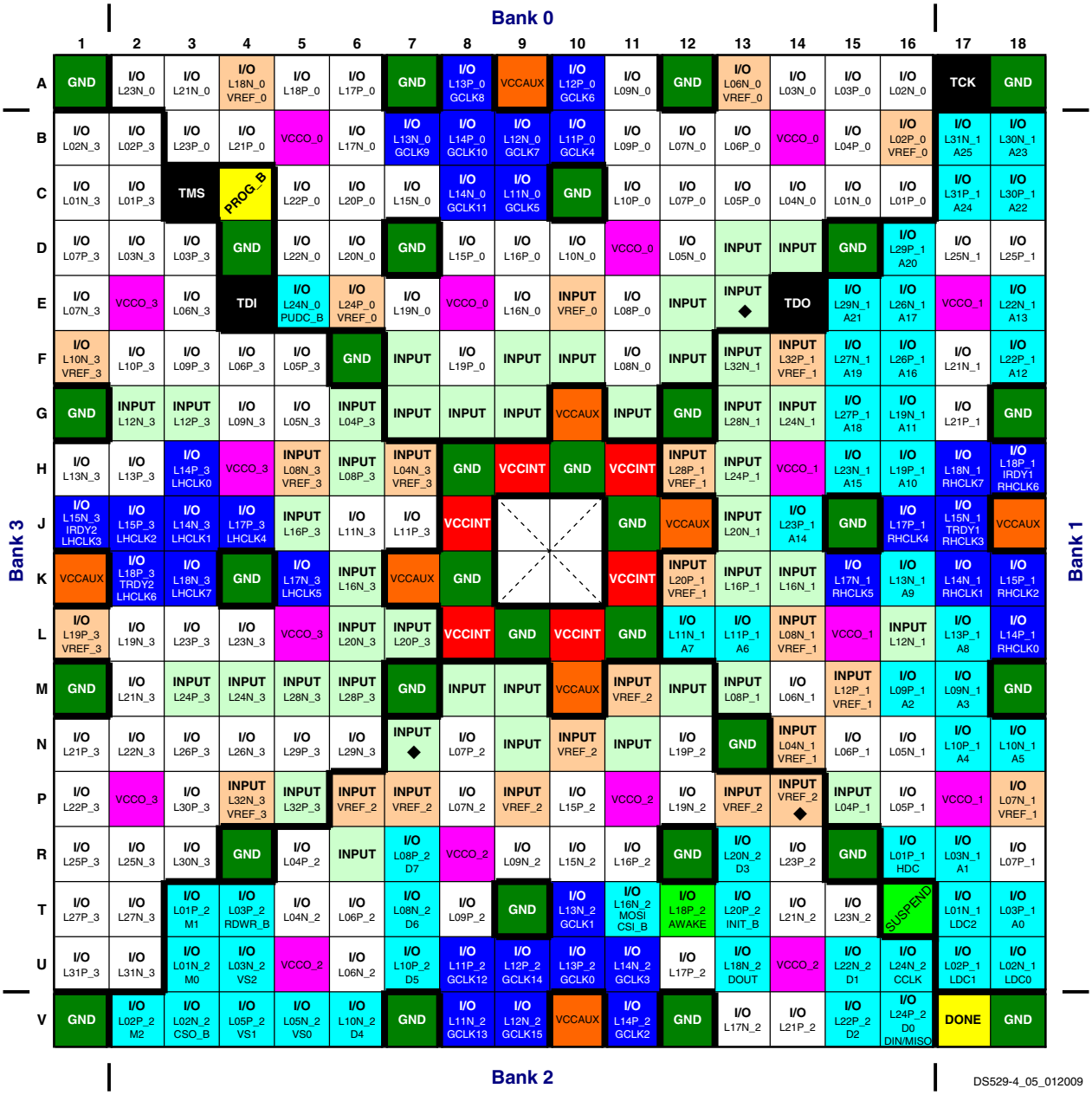


Figure 23: **FG320 Package Footprint (Top View)**

101	**I/O:** Unrestricted, general-purpose user I/O	51	**DUAL:** Configuration pins, then possible user-I/O	23 - 24	**VREF:** User I/O or input voltage reference for bank	2	**SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins
40 - 42	**INPUT:** Unrestricted, general-purpose input pin	32	**CLK:** User I/O, input, or global buffer input	16	**VCCO:** Output voltage supply for bank		
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	6	**VCCINT:** Internal core supply voltage (+1.2V)		
3	**N.C.:** Not connected. Only the XC3S200A has these pins (◆).	32	**GND:** Ground	8	**VCCAUX:** Auxiliary supply voltage		