AMD Xilinx - XC3S700A-4FTG256I Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	1472
Number of Logic Elements/Cells	13248
Total RAM Bits	368640
Number of I/O	161
Number of Gates	700000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s700a-4ftg256i

Introduction

The Spartan®-3A family of Field-Programmable Gate Arrays (FPGAs) solves the design challenges in most high-volume, cost-sensitive, I/O-intensive electronic applications. The five-member family offers densities ranging from 50,000 to 1.4 million system gates, as shown in Table 1.

The Spartan-3A FPGAs are part of the Extended Spartan-3A family, which also include the non-volatile Spartan-3AN and the higher density Spartan-3A DSP FPGAs. The Spartan-3A family builds on the success of the earlier Spartan-3E and Spartan-3 FPGA families. New features improve system performance and reduce the cost of configuration. These Spartan-3A family enhancements, combined with proven 90 nm process technology, deliver more functionality and bandwidth per dollar than ever before, setting the new standard in the programmable logic industry.

Because of their exceptionally low cost, Spartan-3A FPGAs are ideally suited to a wide range of consumer electronics applications, including broadband access, home networking, display/projection, and digital television equipment.

The Spartan-3A family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, lengthy development cycles, and the inherent inflexibility of conventional ASICs, and permit field design upgrades.

Features

- Very low cost, high-performance logic solution for high-volume, cost-conscious applications
- Dual-range V_{CCAUX} supply simplifies 3.3V-only design
- Suspend, Hibernate modes reduce system power
- Multi-voltage, multi-standard SelectIO™ interface pins
  - Up to 502 I/O pins or 227 differential signal pairs
  - LVCMOS, LVTTL, HSTL, and SSTL single-ended I/O
  - 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V signaling
  - Selectable output drive, up to 24 mA per pin
  - QUIETIO standard reduces I/O switching noise
  - Full 3.3V ± 10% compatibility and hot swap compliance
  - 640+ Mb/s data transfer rate per differential I/O
  - LVDS, RSDS, mini-LVDS, HSTL/SSTL differential I/O with integrated differential termination resistors
  - Enhanced Double Data Rate (DDR) support
  - DDR/DDR2 SDRAM support up to 400 Mb/s
  - Fully compliant 32-/64-bit, 33/66 MHz PCI® technology support
- Abundant, flexible logic resources
  - Densities up to 25,344 logic cells, including optional shift register or distributed RAM support
  - Efficient wide multiplexers, wide logic
  - Fast look-ahead carry logic
  - Enhanced 18 x 18 multipliers with optional pipeline
  - IEEE 1149.1/1532 JTAG programming/debug port
- Hierarchical SelectRAM™ memory architecture
  - Up to 576 Kbits of fast block RAM with byte write enables for processor applications
  - Up to 176 Kbits of efficient distributed RAM
- Up to eight Digital Clock Managers (DCMs)
  - Clock skew elimination (delay locked loop)
  - Frequency synthesis, multiplication, division
  - High-resolution phase shifting
  - Wide frequency range (5 MHz to over 320 MHz)
- Eight low-skew global clock networks, eight additional clocks per half device, plus abundant low-skew routing
- Configuration interface to industry-standard PROMs
  - Low-cost, space-saving SPI serial Flash PROM
  - x8 or x8/x16 BPI parallel NOR Flash PROM
  - Low-cost Xilinx® Platform Flash with JTAG
  - Unique Device DNA identifier for design authentication
  - Load multiple bitstreams under FPGA control
  - Post-configuration CRC checking
- Complete Xilinx ISE® and WebPACK™ development system software support plus Spartan-3A Starter Kit
- MicroBlaze™ and PicoBlaze™ embedded processors
- Low-cost QFP and BGA packaging, Pb-free options
  - Common footprints support easy density migration
  - Compatible with select Spartan-3AN nonvolatile FPGAs
  - Compatible with higher density Spartan-3A DSP FPGAs
- XA Automotive version available

Table 1: **Summary of Spartan-3A FPGA Attributes**

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM bits[1]	Block RAM bits[1]	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	CLBs	Slices						
XC3S50A	50K	1,584	16	12	176	704	11K	54K	3	2	144	64
XC3S200A	200K	4,032	32	16	448	1,792	28K	288K	16	4	248	112
XC3S400A	400K	8,064	40	24	896	3,584	56K	360K	20	4	311	142
XC3S700A	700K	13,248	48	32	1,472	5,888	92K	360K	20	8	372	165
XC3S1400A	1400K	25,344	72	40	2,816	11,264	176K	576K	32	8	502	227

Notes:
1. By convention, one Kb is equivalent to 1,024 bits.

General DC Characteristics for I/O Pins

Table 9: **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins**(1)

Symbol	Description	Test Conditions		Min	Typ	Max	Units
I_L(2)	Leakage current at User I/O, input-only, dual-purpose, and dedicated pins, FPGA powered	Driver is in a high-impedance state, V_{IN} = 0V or V_{CCO} max, sample-tested		–10	–	+10	µA
I_{HS}	Leakage current on pins during hot socketing, FPGA unpowered	All pins except INIT_B, PROG_B, DONE, and JTAG pins when PUDC_B = 1.		–10	–	+10	µA
		INIT_B, PROG_B, DONE, and JTAG pins or other pins when PUDC_B = 0.		Add I_{HS} + I_{RPU}			µA
I_{RPU}(3)	Current through pull-up resistor at User I/O, dual-purpose, input-only, and dedicated pins. Dedicated pins are powered by V_{CCAUX}.	V_{IN} = GND	V_{CCO} or V_{CCAUX} = 3.0V to 3.6V	–151	–315	–710	µA
			V_{CCO} or V_{CCAUX} = 2.3V to 2.7V	–82	–182	–437	µA
			V_{CCO} = 1.7V to 1.9V	–36	–88	–226	µA
			V_{CCO} = 1.4V to 1.6V	–22	–56	–148	µA
			V_{CCO} = 1.14V to 1.26V	–11	–31	–83	µA
R_{PU}(3)	Equivalent pull-up resistor value at User I/O, dual-purpose, input-only, and dedicated pins (based on I_{RPU} per Note 3)	V_{IN} = GND	V_{CCO} = 3.0V to 3.6V	5.1	11.4	23.9	kΩ
			V_{CCO} = 2.3V to 2.7V	6.2	14.8	33.1	kΩ
			V_{CCO} = 1.7V to 1.9V	8.4	21.6	52.6	kΩ
			V_{CCO} = 1.4V to 1.6V	10.8	28.4	74.0	kΩ
			V_{CCO} = 1.14V to 1.26V	15.3	41.1	119.4	kΩ
I_{RPD}(3)	Current through pull-down resistor at User I/O, dual-purpose, input-only, and dedicated pins. Dedicated pins are powered by V_{CCAUX}.	V_{IN} = V_{CCO}	V_{CCAUX} = 3.0V to 3.6V	167	346	659	µA
			V_{CCAUX} = 2.25V to 2.75V	100	225	457	µA
R_{PD}(3)	Equivalent pull-down resistor value at User I/O, dual-purpose, input-only, and dedicated pins (based on I_{RPD} per Note 3)	V_{CCAUX} = 3.0V to 3.6V	V_{IN} = 3.0V to 3.6V	5.5	10.4	20.8	kΩ
			V_{IN} = 2.3V to 2.7V	4.1	7.8	15.7	kΩ
			V_{IN} = 1.7V to 1.9V	3.0	5.7	11.1	kΩ
			V_{IN} = 1.4V to 1.6V	2.7	5.1	9.6	kΩ
			V_{IN} = 1.14V to 1.26V	2.4	4.5	8.1	kΩ
		V_{CCAUX} = 2.25V to 2.75V	V_{IN} = 3.0V to 3.6V	7.9	16.0	35.0	kΩ
			V_{IN} = 2.3V to 2.7V	5.9	12.0	26.3	kΩ
			V_{IN} = 1.7V to 1.9V	4.2	8.5	18.6	kΩ
			V_{IN} = 1.4V to 1.6V	3.6	7.2	15.7	kΩ
			V_{IN} = 1.14V to 1.26V	3.0	6.0	12.5	kΩ
I_{REF}	V_{REF} current per pin	All V_{CCO} levels		–10	–	+10	µA
C_{IN}	Input capacitance	–		–	–	10	pF
R_{DT}	Resistance of optional differential termination circuit within a differential I/O pair. Not available on Input-only pairs.	V_{CCO} = 3.3V ± 10%	LVDS_33, MINI_LVDS_33, RSDS_33	90	100	115	Ω
		V_{CCO} = 2.5V ± 10%	LVDS_25, MINI_LVDS_25, RSDS_25	90	110	–	Ω

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8.
2. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See "Parasitic Leakage" in UG331, *Spartan-3 Generation FPGA User Guide*.
3. This parameter is based on characterization. The pull-up resistance $R_{PU} = V_{CCO} / I_{RPU}$. The pull-down resistance $R_{PD} = V_{IN} / I_{RPD}$.

I/O Timing

Pin-to-Pin Clock-to-Output Times

Table 18: **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade -5 Max	Speed Grade -4 Max	Units
Clock-to-Output Times						
$T_{ICKOFDCM}$	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use.	LVCMOS25(2), 12mA output drive, Fast slew rate, with DCM(3)	XC3S50A	3.18	3.42	ns
			XC3S200A	3.21	3.27	ns
			XC3S400A	2.97	3.33	ns
			XC3S700A	3.39	3.50	ns
			XC3S1400A	3.51	3.99	ns
T_{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.	LVCMOS25(2), 12mA output drive, Fast slew rate, without DCM	XC3S50A	4.59	5.02	ns
			XC3S200A	4.88	5.24	ns
			XC3S400A	4.68	5.12	ns
			XC3S700A	4.97	5.34	ns
			XC3S1400A	5.06	5.69	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 23. If the latter is true, *add* the appropriate Output adjustment from Table 26.
3. DCM output jitter is included in all measurements.

Pin-to-Pin Setup and Hold Times

Table 19: **Pin-to-Pin Setup and Hold Times for the IOB Input Path (System Synchronous)**

Symbol	Description	Conditions	Device	Speed Grade -5 Min	Speed Grade -4 Min	Units
Setup Times						
T_{PSDCM}	When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0, with DCM(4)	XC3S50A	2.45	2.68	ns
			XC3S200A	2.59	2.84	ns
			XC3S400A	2.38	2.68	ns
			XC3S700A	2.38	2.57	ns
			XC3S1400A	1.91	2.17	ns
T_{PSFD}	When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 5, without DCM	XC3S50A	2.55	2.76	ns
			XC3S200A	2.32	2.76	ns
			XC3S400A	2.21	2.60	ns
			XC3S700A	2.28	2.63	ns
			XC3S1400A	2.33	2.41	ns
Hold Times						
T_{PHDCM}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 0, with DCM(4)	XC3S50A	-0.36	-0.36	ns
			XC3S200A	-0.52	-0.52	ns
			XC3S400A	-0.33	-0.29	ns
			XC3S700A	-0.17	-0.12	ns
			XC3S1400A	-0.07	0.00	ns
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 5, without DCM	XC3S50A	-0.63	-0.58	ns
			XC3S200A	-0.56	-0.56	ns
			XC3S400A	-0.42	-0.42	ns
			XC3S700A	-0.80	-0.75	ns
			XC3S1400A	-0.69	-0.69	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, subtract the appropriate adjustment from Table 23. If this is true of the data Input, add the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, add the appropriate Input adjustment from Table 23. If this is true of the data Input, subtract the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Table 27: **Test Methods for Timing Measurement at I/Os*(Continued)***

Signal Standard (IOSTANDARD)	Inputs			Outputs		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Differential						
LVDS_25	-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDS_33	-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
BLVDS_25	-	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
MINI_LVDS_25	-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
MINI_LVDS_33	-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVPECL_25	-	V_{ICM} – 0.3	V_{ICM} + 0.3	N/A	N/A	V_{ICM}
LVPECL_33	-	V_{ICM} – 0.3	V_{ICM} + 0.3	N/A	N/A	V_{ICM}
RSDS_25	-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
RSDS_33	-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
TMDS_33	-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	3.3	V_{ICM}
PPDS_25	-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	0.8	V_{ICM}
PPDS_33	-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	0.8	V_{ICM}
DIFF_HSTL_I	-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.75	V_{ICM}
DIFF_HSTL_III	-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.5	V_{ICM}
DIFF_HSTL_I_18	-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_HSTL_II_18	-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_HSTL_III_18	-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.8	V_{ICM}
DIFF_SSTL18_I	-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_SSTL18_II	-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_SSTL2_I	-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.25	V_{ICM}
DIFF_SSTL2_II	-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.25	V_{ICM}
DIFF_SSTL3_I	-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.5	V_{ICM}
DIFF_SSTL3_II	-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.5	V_{ICM}

Notes:

1. Descriptions of the relevant symbols are as follows:
   V_{REF} – The reference voltage for setting the input switching threshold
   V_{ICM} – The common mode input voltage
   V_M – Voltage of measurement point on signal transition
   V_L – Low-level test voltage at Input pin
   V_H – High-level test voltage at Input pin
   R_T – Effective termination resistance, which takes on a value of 1 MΩ when no parallel termination is required
   V_T – Termination voltage
2. The load capacitance (C_L) at the Output pin is 0 pF for all signal standards.
3. According to the PCI specification.

The capacitive load (C_L) is connected between the output and GND. *The Output timing for all standards, as published in the speed files and the data sheet, is always based on a C_L value of zero.* High-impedance probes (less than 1 pF) are used for all measurements. Any delay that the test fixture might contribute to test measurements is subtracted from those measurements to produce the final timing numbers as published in the speed files and data sheet.

Using IBIS Models to Simulate Load Conditions in Application

IBIS models permit the most accurate prediction of timing delays for a given application. The parameters found in the IBIS model (V_{REF}, R_{REF}, and V_{MEAS}) correspond directly with the parameters used in Table 27 (V_T, R_T, and V_M). Do not confuse V_{REF} (the termination voltage) from the IBIS model with V_{REF} (the input-switching threshold) from the table. A fourth parameter, C_{REF}, is always zero. The four parameters describe all relevant output test conditions. IBIS models are found in the Xilinx development software as well as at the following link:

www.xilinx.com/support/download/index.htm

Delays for a given application are simulated according to its specific load conditions as follows:

1. Simulate the desired signal standard with the output driver connected to the test setup shown in Figure 9. Use parameter values V_T, R_T, and V_M from Table 27. C_{REF} is zero.
2. Record the time to V_M.
3. Simulate the same signal standard with the output driver connected to the PCB trace with load. Use the appropriate IBIS model (including V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} values) or capacitive value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. Add (or subtract) the increase (or decrease) in delay to (or from) the appropriate Output standard adjustment (Table 26) to yield the worst-case delay of the PCB trace.

Simultaneously Switching Output Guidelines

This section provides guidelines for the recommended maximum allowable number of Simultaneous Switching Outputs (SSOs). These guidelines describe the maximum number of user I/O pins of a given output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of ground and power bounce.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common voltage rail. Low-to-High transitions conduct to the V_{CCO} rail; High-to-Low transitions conduct to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the die pad and the power supply or ground return. The inductance is associated with bonding wires, the package lead frame, and any other signal routing inside the package. Other variables contribute to SSO noise levels, including stray inductance on the PCB as well as capacitive loading at receivers. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

Table 28 and Table 29 provide the essential SSO guidelines. For each device/package combination, Table 28 provides the number of equivalent V_{CCO}/GND pairs. The equivalent number of pairs is based on characterization and may not match the physical number of pairs. For each output signal standard and drive strength, Table 29 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The guidelines in Table 29 are categorized by package style, slew rate, and output drive current. Furthermore, the number of SSOs is specified by I/O bank. Generally, the left and right I/O banks (Banks 1 and 3) support higher output drive current.

Multiply the appropriate numbers from Table 28 and Table 29 to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines might result in increased power or ground bounce, degraded signal integrity, or increased system jitter.

SSO_{MAX}/IO Bank = Table 28 x Table 29

The recommended maximum SSO values assume that the FPGA is soldered on the printed circuit board and that the board uses sound design practices. The SSO values do not apply for FPGAs mounted in sockets, due to the lead inductance introduced by the socket.

The SSO values assume that the V_{CCAUX} is powered at 3.3V. Setting V_{CCAUX} to 2.5V provides better SSO characteristics.

The number of SSOs allowed for quad-flat packages (VQ/TQ) is lower than for ball grid array packages (FG) due to the larger lead inductance of the quad-flat packages. Ball grid array packages are recommended for applications with a large number of simultaneously switching outputs.

Phase Shifter (PS)

Table 40: **Recommended Operating Conditions for the PS in Variable Phase Mode**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Operating Frequency Ranges						
PSCLK_FREQ (F_{PSCLK})	Frequency for the PSCLK input	1	167	1	167	MHz
Input Pulse Requirements						
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	40%	60%	40%	60%	-

Table 41: **Switching Characteristics for the PS in Variable Phase Mode**

Symbol	Description		Phase Shift Amount	Units
Phase Shifting Range				
MAX_STEPS(2)	Maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. If using CLKIN_DIVIDE_BY_2 = TRUE, double the clock effective clock period.	CLKIN < 60 MHz	±[INTEGER(10 • (T_{CLKIN} – 3 ns))]	steps
		CLKIN ≥ 60 MHz	±[INTEGER(15 • (T_{CLKIN} – 3 ns))]	
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting		±[MAX_STEPS • DCM_DELAY_STEP_MIN]	ns
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting		±[MAX_STEPS • DCM_DELAY_STEP_MAX]	ns

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 8 and Table 40.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM is has no initial fixed phase shifting, that is, the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the bottom of Table 37.

VQ100 Footprint (XC3S200A)

Note pin 1 indicator in top-left corner and logo orientation.

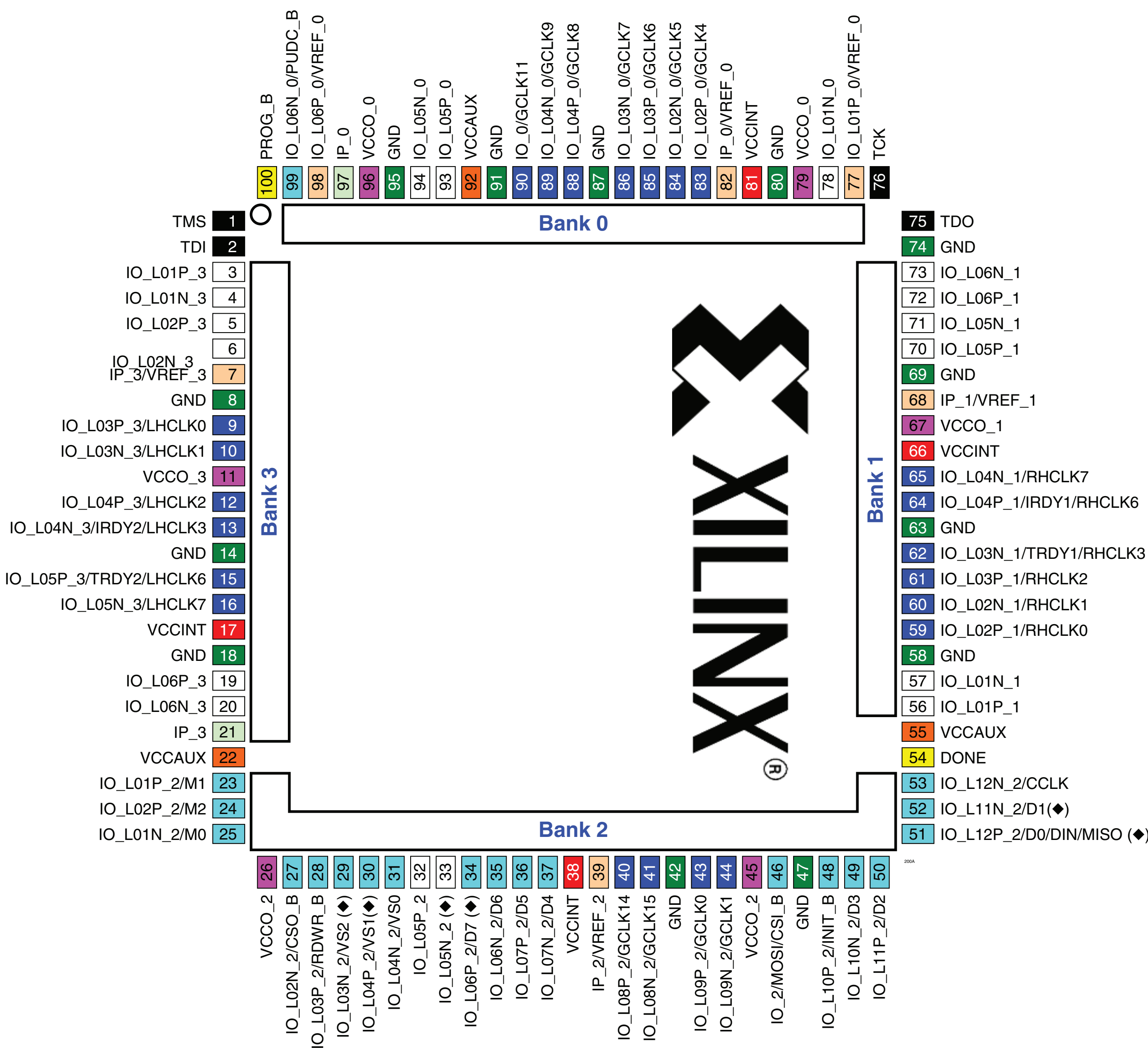

Figure 18: **VQ100 Package Footprint - XC3S200A (Top View)**

17	**I/O:** Unrestricted, general-purpose user I/O	20	**DUAL:** Configuration pins, then possible user I/O	6	**VREF:** User I/O or input voltage reference for bank
2	**INPUT:** Unrestricted, general-purpose input pin	23	**CLK:** User I/O, input, or global buffer input	6	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core supply voltage (+1.2V)
0	**N.C.:** Not connected	13	**GND:** Ground	3	**VCCAUX:** Auxiliary supply voltage

Table 68: **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400)** ***(Continued)***

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
2	IO_L01N_2/M0	IO_L01N_2/M0	P4	DUAL
2	IO_L01P_2/M1	IO_L01P_2/M1	N4	DUAL
2	IO_L02N_2/ CSO_B	IO_L02N_2/ CSO_B	T2	DUAL
2	IO_L02P_2/M2	IO_L02P_2/M2	R2	DUAL
2	IO_L04P_2/VS2	IO_L03N_2/VS2	T3	DUAL
2	IO_L03P_2/ RDWR_B	IO_L03P_2/ RDWR_B	R3	DUAL
2	IO_L04N_2/VS0	IO_L04N_2/VS0	P5	DUAL
2	IO_L03N_2/VS1	IO_L04P_2/VS1	N6	DUAL
2	IO_L06P_2	IO_L05N_2	R5	I/O
2	IO_L05P_2	IO_L05P_2	T4	I/O
2	IO_L06N_2/D6	IO_L06N_2/D6	T6	DUAL
2	IO_L05N_2/D7	IO_L06P_2/D7	T5	DUAL
2	N.C. (◆)	IO_L07N_2	P6	I/O
2	N.C. (◆)	IO_L07P_2	N7	I/O
2	IO_L08N_2/D4	IO_L08N_2/D4	N8	DUAL
2	IO_L08P_2/D5	IO_L08P_2/D5	P7	DUAL
2	N.C. (◆)	IO_L09N_2/ GCLK13	T7	GCLK
2	N.C. (◆)	IO_L09P_2/ GCLK12	R7	GCLK
2	IO_L10N_2/ GCLK15	IO_L10N_2/ GCLK15	T8	GCLK
2	IO_L10P_2/ GCLK14	IO_L10P_2/ GCLK14	P8	GCLK
2	IO_L11N_2/ GCLK1	IO_L11N_2/ GCLK1	P9	GCLK
2	IO_L11P_2/ GCLK0	IO_L11P_2/ GCLK0	N9	GCLK
2	IO_L12N_2/ GCLK3	IO_L12N_2/ GCLK3	T9	GCLK
2	IO_L12P_2/ GCLK2	IO_L12P_2/ GCLK2	R9	GCLK
2	N.C. (◆)	IO_L13N_2	M10	I/O
2	N.C. (◆)	IO_L13P_2	N10	I/O
2	IO_L14P_2/ MOSI/CSI_B	IO_L14N_2/ MOSI/CSI_B	P10	DUAL
2	IO_L14N_2	IO_L14P_2	T10	I/O
2	IO_L15N_2/ DOUT	IO_L15N_2/ DOUT	R11	DUAL
2	IO_L15P_2/ AWAKE	IO_L15P_2/ AWAKE	T11	PWR MGMT
2	IO_L16N_2	IO_L16N_2	N11	I/O
2	IO_L16P_2	IO_L16P_2	P11	I/O
2	IO_L17N_2/D3	IO_L17N_2/D3	P12	DUAL
2	IO_L17P_2/ INIT_B	IO_L17P_2/ INIT_B	T12	DUAL

Table 68: **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400)** ***(Continued)***

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
2	IO_L20P_2/D1	IO_L18N_2/D1	R13	DUAL
2	IO_L18P_2/D2	IO_L18P_2/D2	T13	DUAL
2	N.C. (◆)	IO_L19N_2	P13	I/O
2	N.C. (◆)	IO_L19P_2	N12	I/O
2	IO_L20N_2/ CCLK	IO_L20N_2/ CCLK	R14	DUAL
2	IO_L18N_2/D0/ DIN/MISO	IO_L20P_2/D0/ DIN/MISO	T14	DUAL
2	IP_2	IP_2	L7	INPUT
2	IP_2	IP_2	L8	INPUT
2	IP_2/VREF_2	IP_2/VREF_2	L9	VREF
2	IP_2/VREF_2	IP_2/VREF_2	L10	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M7	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M8	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M11	VREF
2	IP_2/VREF_2	IP_2/VREF_2	N5	VREF
2	VCCO_2	VCCO_2	M9	VCCO
2	VCCO_2	VCCO_2	R4	VCCO
2	VCCO_2	VCCO_2	R8	VCCO
2	VCCO_2	VCCO_2	R12	VCCO
3	IO_L01N_3	IO_L01N_3	C1	I/O
3	IO_L01P_3	IO_L01P_3	C2	I/O
3	IO_L02N_3	IO_L02N_3	D3	I/O
3	IO_L02P_3	IO_L02P_3	D4	I/O
3	IO_L03N_3	IO_L03N_3	E1	I/O
3	IO_L03P_3	IO_L03P_3	D1	I/O
3	N.C. (◆)	IO_L05N_3	E2	I/O
3	N.C. (◆)	IO_L05P_3	E3	I/O
3	N.C. (◆)	IO_L07N_3	G4	I/O
3	N.C. (◆)	IO_L07P_3	F3	I/O
3	IO_L08N_3/ VREF_3	IO_L08N_3/ VREF_3	G1	VREF
3	IO_L08P_3	IO_L08P_3	F1	I/O
3	N.C. (◆)	IO_L09N_3	H4	I/O
3	N.C. (◆)	IO_L09P_3	G3	I/O
3	N.C. (◆)	IO_L10N_3	H5	I/O
3	N.C. (◆)	IO_L10P_3	H6	I/O
3	IO_L11N_3/ LHCLK1	IO_L11N_3/ LHCLK1	H1	LHCLK
3	IO_L11P_3/ LHCLK0	IO_L11P_3/ LHCLK0	G2	LHCLK
3	IO_L12N_3/ IRDY2/LHCLK3	IO_L12N_3/ IRDY2/LHCLK3	J3	LHCLK
3	IO_L12P_3/ LHCLK2	IO_L12P_3/ LHCLK2	H3	LHCLK

User I/Os by Bank

Table 70, Table 71, and Table 72 indicate how the available user-I/O pins are distributed between the four I/O banks on the FT256 package. The AWAKE pin is counted as a dual-purpose I/O.

The XC3S50A FPGA in the FT256 package has 51 unconnected balls, labeled with an "N.C." type. These pins are also indicated in Figure 20.

Table 70: **User I/Os Per Bank on XC3S50A in the FT256 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	40	21	7	1	3	8
Right	1	32	12	5	4	3	8
Bottom	2	40	5	2	21	6	6
Left	3	32	15	6	0	3	8
TOTAL		**144**	**53**	**20**	**26**	**15**	**30**

Table 71: **User I/Os Per Bank on XC3S200A and XC3S400A in the FT256 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	47	27	6	1	5	8
Right	1	50	1	6	30	5	8
Bottom	2	48	11	2	21	6	8
Left	3	50	30	7	0	5	8
TOTAL		**195**	**69**	**21**	**52**	**21**	**32**

Table 72: **User I/Os Per Bank on XC3S700A and XC3S1400A in the FT256 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	41	27	1	1	4	8
Right	1	40	0	0	30	4	6
Bottom	2	41	7	0	21	5	8
Left	3	39	25	1	0	5	8
TOTAL		**161**	**59**	**2**	**52**	**18**	**30**

Differences Between XC3S200A/XC3S400A and XC3S700A/XC3S1400A

The XC3S700A and XC3S1400A FPGAs have several additional power and ground pins as compared to the XC3S200A and XC3S400A. Table 76 summarizes all the differences. All dedicated and dual-purpose configuration pins are in the same location.

Table 76: **Differences Between XC3S200A/XC3S400A and XC3S700A/XC3S1400A**

FT256 Ball	Bank	XC3S200A XC3S400A		XC3S700A XC3S1400A	
		Pin Name	Type	Pin Name	Type
F8	0	IO_L14P_0	I/O	GND	GND
D11	0	IO_L03N_0	I/O	IO_L06P_0	I/O
D10	0	IO_L06P_0	I/O	IO_L06N_0/ VREF_0	VREF
F7	0	IP_0	INPUT	GND	GND
F9	0	IP_0	INPUT	GND	GND
D12	0	IP_0	INPUT	IO_L03N_0	I/O
E9	0	IP_0/ VREF_0	INPUT	IO_L14P_0	I/O
D6	0	IP_0	INPUT	VCCAUX	VCCAUX
F10	0	IP_0	INPUT	VCCINT	VCCINT
E10	0	IO_L06N_0/ VREF_0	VREF	GND	GND
M13	1	IO_L05P_1	I/O	IP_1/ VREF_1	VREF
F11	1	IP_L25N_1	INPUT	GND	GND
H11	1	IP_L13N_1	INPUT	GND	GND
K11	1	IP_L04P_1	INPUT	GND	GND
G11	1	IP_L21N_1	INPUT	VCCINT	VCCINT
H10	1	IP_L13P_1	INPUT	VCCINT	VCCINT
J11	1	IP_L09N_1	INPUT	VCCINT	VCCINT
H14	1	IO_L14N_1/ RHCLK5	RHCLK	VCCAUX	VCCAUX
J14	1	IO_L14P_1/ RHCLK4	RHCLK	IP_1/ VREF_1	VREF
H12	1	VCCO_1	VCCO	IP_1/ VREF_1	VREF
G12	1	IP_L21P_1/ VREF_1	VREF	GND	GND
J10	1	IP_L09P_1/ VREF_1	VREF	GND	GND
K12	1	IP_L04N_1/ VREF_1	VREF	GND	GND
F12	1	IP_L25P_1/ VREF_1	VREF	VCCAUX	VCCAUX
M14	1	IO_L05N_1/ VREF_1	VREF	IP_1/ VREF_1	VREF
N7	2	IO_L07P_2	I/O	GND	GND
N10	2	IO_L13P_2	I/O	GND	GND
M10	2	IO_L13N_2	I/O	VCCAUX	VCCAUX
P6	2	IO_L07N_2	I/O	IP_2/ VREF_2	VREF
L8	2	IP_2	INPUT	GND	GND
L7	2	IP_2	INPUT	VCCINT	VCCINT
M9	2	VCCO_2	VCCO	IP_2/ VREF_2	VREF
L10	2	IP_2/ VREF_2	VREF	GND	GND
M8	2	IP_2/ VREF_2	VREF	GND	GND
L9	2	IP_2/ VREF_2	VREF	VCCINT	VCCINT
H5	3	IO_L10N_3	I/O	GND	GND
J6	3	IO_L17N_3	I/O	GND	GND
G3	3	IO_L09P_3	I/O	IO_L07N_3	I/O
J4	3	IO_L17P_3	I/O	IP_3	IP
H4	3	IO_L09N_3	I/O	VCCAUX	VCCAUX
H6	3	IO_L10P_3	I/O	VCCINT	VCCINT
N2	3	IO_L22P_3	I/O	IO_L22P_3/ VREF_3	VREF
G4	3	IO_L07N_3	I/O	IP_3/ VREF_3	VREF
G6	3	IP_L06P_3	INPUT	GND	GND
H7	3	IP_L13P_3	INPUT	GND	GND
K5	3	IP_L21P_3	INPUT	GND	GND
E4	3	IP_L04P_3	INPUT	IO_L04P_3	I/O
L5	3	IP_L25P_3	INPUT	VCCAUX	VCCAUX
J7	3	IP_L13N_3	INPUT	VCCINT	VCCINT
K6	3	IP_L21N_3	INPUT	VCCINT	VCCINT
J5	3	VCCO_3	VCCO	IP_3/ VREF_3	VREF
G5	3	IP_L06N_3/ VREF_3	VREF	GND	GND
L6	3	IP_L25N_3/ VREF_3	VREF	GND	GND
F4	3	IP_L04N_3/ VREF_3	VREF	IO_L04N_3	I/O

FG400: 400-ball Fine-pitch Ball Grid Array

The 400-ball fine-pitch ball grid array, FG400, supports two different Spartan-3A FPGAs, the XC3S400A and the XC3S700A. Both devices share a common footprint for this package as shown in Table 81 and Figure 24.

Table 81 lists all the FG400 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 81: **Spartan-3A FG400 Pinout**

Bank	Pin Name	FG400 Ball	Type
0	IO_L01N_0	A18	I/O
0	IO_L01P_0	B18	I/O
0	IO_L02N_0	C17	I/O
0	IO_L02P_0/VREF_0	D17	VREF
0	IO_L03N_0	E15	I/O
0	IO_L03P_0	D16	I/O
0	IO_L04N_0	A17	I/O
0	IO_L04P_0/VREF_0	B17	VREF
0	IO_L05N_0	A16	I/O
0	IO_L05P_0	C16	I/O
0	IO_L06N_0	C15	I/O
0	IO_L06P_0	D15	I/O
0	IO_L07N_0	A14	I/O
0	IO_L07P_0	C14	I/O
0	IO_L08N_0	A15	I/O
0	IO_L08P_0	B15	I/O
0	IO_L09N_0	F13	I/O
0	IO_L09P_0	E13	I/O
0	IO_L10N_0/VREF_0	C13	VREF
0	IO_L10P_0	D14	I/O
0	IO_L11N_0	C12	I/O
0	IO_L11P_0	B13	I/O
0	IO_L12N_0	F12	I/O
0	IO_L12P_0	D12	I/O
0	IO_L13N_0	A12	I/O
0	IO_L13P_0	B12	I/O
0	IO_L14N_0	C11	I/O
0	IO_L14P_0	B11	I/O
0	IO_L15N_0/GCLK5	E11	GCLK
0	IO_L15P_0/GCLK4	D11	GCLK
0	IO_L16N_0/GCLK7	C10	GCLK
0	IO_L16P_0/GCLK6	A10	GCLK
0	IO_L17N_0/GCLK9	E10	GCLK
0	IO_L17P_0/GCLK8	D10	GCLK
0	IO_L18N_0/GCLK11	A8	GCLK
0	IO_L18P_0/GCLK10	A9	GCLK
0	IO_L19N_0	C9	I/O
0	IO_L19P_0	B9	I/O
0	IO_L20N_0	C8	I/O
0	IO_L20P_0	B8	I/O
0	IO_L21N_0	D8	I/O
0	IO_L21P_0	C7	I/O
0	IO_L22N_0/VREF_0	F9	VREF
0	IO_L22P_0	E9	I/O
0	IO_L23N_0	F8	I/O
0	IO_L23P_0	E8	I/O
0	IO_L24N_0	A7	I/O
0	IO_L24P_0	B7	I/O
0	IO_L25N_0	C6	I/O
0	IO_L25P_0	A6	I/O
0	IO_L26N_0	B5	I/O
0	IO_L26P_0	A5	I/O
0	IO_L27N_0	F7	I/O
0	IO_L27P_0	E7	I/O
0	IO_L28N_0	D6	I/O
0	IO_L28P_0	C5	I/O
0	IO_L29N_0	C4	I/O
0	IO_L29P_0	A4	I/O
0	IO_L30N_0	B3	I/O
0	IO_L30P_0	A3	I/O
0	IO_L31N_0	F6	I/O
0	IO_L31P_0	E6	I/O
0	IO_L32N_0/PUDC_B	B2	DUAL

Table 81: **Spartan-3A FG400 Pinout*(Continued)***

Bank	Pin Name	FG400 Ball	Type
2	IO_L28P_2	Y16	I/O
2	IO_L29N_2	U16	I/O
2	IO_L29P_2	V16	I/O
2	IO_L30N_2	Y18	I/O
2	IO_L30P_2	Y17	I/O
2	IO_L31N_2	U17	I/O
2	IO_L31P_2	V17	I/O
2	IO_L32N_2/CCLK	Y19	DUAL
2	IO_L32P_2/D0/DIN/MISO	W18	DUAL
2	IP_2	P9	INPUT
2	IP_2	P12	INPUT
2	IP_2	P13	INPUT
2	IP_2	R8	INPUT
2	IP_2	R10	INPUT
2	IP_2	T11	INPUT
2	IP_2/VREF_2	N9	VREF
2	IP_2/VREF_2	N12	VREF
2	IP_2/VREF_2	P8	VREF
2	IP_2/VREF_2	P10	VREF
2	IP_2/VREF_2	P11	VREF
2	IP_2/VREF_2	R14	VREF
2	VCCO_2	R11	VCCO
2	VCCO_2	U8	VCCO
2	VCCO_2	U14	VCCO
2	VCCO_2	W5	VCCO
2	VCCO_2	W11	VCCO
2	VCCO_2	W17	VCCO
3	IO_L01N_3	D3	I/O
3	IO_L01P_3	D4	I/O
3	IO_L02N_3	C2	I/O
3	IO_L02P_3	B1	I/O
3	IO_L03N_3	D2	I/O
3	IO_L03P_3	C1	I/O
3	IO_L05N_3	E1	I/O
3	IO_L05P_3	D1	I/O
3	IO_L06N_3	G5	I/O
3	IO_L06P_3	F4	I/O
3	IO_L07N_3	J5	I/O
3	IO_L07P_3	J6	I/O
3	IO_L08N_3	H4	I/O

Table 81: **Spartan-3A FG400 Pinout*(Continued)***

Bank	Pin Name	FG400 Ball	Type
3	IO_L08P_3	H6	I/O
3	IO_L09N_3	G4	I/O
3	IO_L09P_3	F3	I/O
3	IO_L10N_3	F2	I/O
3	IO_L10P_3	E3	I/O
3	IO_L12N_3	H2	I/O
3	IO_L12P_3	G3	I/O
3	IO_L13N_3/VREF_3	G1	VREF
3	IO_L13P_3	F1	I/O
3	IO_L14N_3	H3	I/O
3	IO_L14P_3	J4	I/O
3	IO_L16N_3	J2	I/O
3	IO_L16P_3	J3	I/O
3	IO_L17N_3/LHCLK1	K2	LHCLK
3	IO_L17P_3/LHCLK0	J1	LHCLK
3	IO_L18N_3/IRDY2/LHCLK3	L3	LHCLK
3	IO_L18P_3/LHCLK2	K3	LHCLK
3	IO_L20N_3/LHCLK5	L5	LHCLK
3	IO_L20P_3/LHCLK4	K4	LHCLK
3	IO_L21N_3/LHCLK7	M1	LHCLK
3	IO_L21P_3/TRDY2/LHCLK6	L1	LHCLK
3	IO_L22N_3	M3	I/O
3	IO_L22P_3/VREF_3	M2	VREF
3	IO_L24N_3	M5	I/O
3	IO_L24P_3	M4	I/O
3	IO_L25N_3	N2	I/O
3	IO_L25P_3	N1	I/O
3	IO_L26N_3	N4	I/O
3	IO_L26P_3	N3	I/O
3	IO_L28N_3	R1	I/O
3	IO_L28P_3	P1	I/O
3	IO_L29N_3	P4	I/O
3	IO_L29P_3	P3	I/O
3	IO_L30N_3	R3	I/O
3	IO_L30P_3	R2	I/O
3	IO_L32N_3	T2	I/O
3	IO_L32P_3/VREF_3	T1	VREF
3	IO_L33N_3	R4	I/O
3	IO_L33P_3	T3	I/O
3	IO_L34N_3	U3	I/O

FG484: 484-ball Fine-pitch Ball Grid Array

The 484-ball fine-pitch ball grid array, FG484, supports both the XC3S700A and the XC3S1400A FPGAs. There are three pinout differences, as described in Table 86.

Table 83 lists all the FG484 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The shaded rows indicate pinout differences between the XC3S700A and the XC3S1400A FPGAs. The XC3S700A has three unconnected balls, indicated as N.C. (No Connection) in Table 83 and with the black diamond character (◆) in Table 83 and Figure 25.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 83: **Spartan-3A FG484 Pinout**

Bank	Pin Name	FG484 Ball	Type
0	IO_L01N_0	D18	I/O
0	IO_L01P_0	E17	I/O
0	IO_L02N_0	C19	I/O
0	IO_L02P_0/VREF_0	D19	VREF
0	IO_L03N_0	A20	I/O
0	IO_L03P_0	B20	I/O
0	IO_L04N_0	F15	I/O
0	IO_L04P_0	E15	I/O
0	IO_L05N_0	A18	I/O
0	IO_L05P_0	C18	I/O
0	IO_L06N_0	A19	I/O
0	IO_L06P_0/VREF_0	B19	VREF
0	IO_L07N_0	C17	I/O
0	IO_L07P_0	D17	I/O
0	IO_L08N_0	C16	I/O
0	IO_L08P_0	D16	I/O
0	IO_L09N_0	E14	I/O
0	IO_L09P_0	C14	I/O
0	IO_L10N_0	A17	I/O
0	IO_L10P_0	B17	I/O
0	IO_L11N_0	C15	I/O

Table 83: **Spartan-3A FG484 Pinout*(Continued)***

Bank	Pin Name	FG484 Ball	Type
0	IO_L11P_0	D15	I/O
0	IO_L12N_0/VREF_0	A15	VREF
0	IO_L12P_0	A16	I/O
0	IO_L13N_0	A14	I/O
0	IO_L13P_0	B15	I/O
0	IO_L14N_0	E13	I/O
0	IO_L14P_0	F13	I/O
0	IO_L15N_0	C13	I/O
0	IO_L15P_0	D13	I/O
0	IO_L16N_0	A13	I/O
0	IO_L16P_0	B13	I/O
0	IO_L17N_0/GCLK5	E12	GCLK
0	IO_L17P_0/GCLK4	C12	GCLK
0	IO_L18N_0/GCLK7	A11	GCLK
0	IO_L18P_0/GCLK6	A12	GCLK
0	IO_L19N_0/GCLK9	C11	GCLK
0	IO_L19P_0/GCLK8	B11	GCLK
0	IO_L20N_0/GCLK11	E11	GCLK
0	IO_L20P_0/GCLK10	D11	GCLK
0	IO_L21N_0	C10	I/O
0	IO_L21P_0	A10	I/O
0	IO_L22N_0	A8	I/O
0	IO_L22P_0	A9	I/O
0	IO_L23N_0	E10	I/O
0	IO_L23P_0	D10	I/O
0	IO_L24N_0/VREF_0	C9	VREF
0	IO_L24P_0	B9	I/O
0	IO_L25N_0	C8	I/O
0	IO_L25P_0	B8	I/O
0	IO_L26N_0	A6	I/O
0	IO_L26P_0	A7	I/O
0	IO_L27N_0	C7	I/O
0	IO_L27P_0	D7	I/O
0	IO_L28N_0	A5	I/O
0	IO_L28P_0	B6	I/O
0	IO_L29N_0	D6	I/O
0	IO_L29P_0	C6	I/O
0	IO_L30N_0	D8	I/O

Table 83: **Spartan-3A FG484 Pinout*(Continued)***

Bank	Pin Name	FG484 Ball	Type
0	IO_L30P_0	E9	I/O
0	IO_L31N_0	B4	I/O
0	IO_L31P_0	A4	I/O
0	IO_L32N_0	D5	I/O
0	IO_L32P_0	C5	I/O
0	IO_L33N_0	B3	I/O
0	IO_L33P_0	A3	I/O
0	IO_L34N_0	F8	I/O
0	IO_L34P_0	E7	I/O
0	IO_L35N_0	E6	I/O
0	IO_L35P_0	F7	I/O
0	IO_L36N_0/PUDC_B	A2	DUAL
0	IO_L36P_0/VREF_0	B2	VREF
0	IP_0	E16	INPUT
0	IP_0	E8	INPUT
0	IP_0	F10	INPUT
0	IP_0	F12	INPUT
0	IP_0	F16	INPUT
0	IP_0	G10	INPUT
0	IP_0	G11	INPUT
0	IP_0	G12	INPUT
0	IP_0	G13	INPUT
0	IP_0	G14	INPUT
0	IP_0	G15	INPUT
0	IP_0	G16	INPUT
0	IP_0	G7	INPUT
0	IP_0	G9	INPUT
0	IP_0	H10	INPUT
0	IP_0	H13	INPUT
0	IP_0	H14	INPUT
0	IP_0/VREF_0	G8	VREF
0	IP_0/VREF_0	H12	VREF
0	IP_0/VREF_0	H9	VREF
0	VCCO_0	B10	VCCO
0	VCCO_0	B14	VCCO
0	VCCO_0	B18	VCCO
0	VCCO_0	B5	VCCO
0	VCCO_0	F14	VCCO
0	VCCO_0	F9	VCCO
1	IO_L01N_1/LDC2	Y21	DUAL

Table 83: **Spartan-3A FG484 Pinout*(Continued)***

Bank	Pin Name	FG484 Ball	Type
1	IO_L01P_1/HDC	AA22	DUAL
1	IO_L02N_1/LDC0	W20	DUAL
1	IO_L02P_1/LDC1	W19	DUAL
1	IO_L03N_1/A1	T18	DUAL
1	IO_L03P_1/A0	T17	DUAL
1	IO_L05N_1	W21	I/O
1	IO_L05P_1	Y22	I/O
1	IO_L06N_1	V20	I/O
1	IO_L06P_1	V19	I/O
1	IO_L07N_1	V22	I/O
1	IO_L07P_1	W22	I/O
1	IO_L09N_1	U21	I/O
1	IO_L09P_1	U22	I/O
1	IO_L10N_1	U19	I/O
1	IO_L10P_1	U20	I/O
1	IO_L11N_1	T22	I/O
1	IO_L11P_1	T20	I/O
1	IO_L13N_1	T19	I/O
1	IO_L13P_1	R20	I/O
1	IO_L14N_1	R22	I/O
1	IO_L14P_1	R21	I/O
1	IO_L15N_1/VREF_1	P22	VREF
1	IO_L15P_1	P20	I/O
1	IO_L17N_1/A3	P18	DUAL
1	IO_L17P_1/A2	R19	DUAL
1	IO_L18N_1/A5	N21	DUAL
1	IO_L18P_1/A4	N22	DUAL
1	IO_L19N_1/A7	N19	DUAL
1	IO_L19P_1/A6	N20	DUAL
1	IO_L20N_1/A9	N17	DUAL
1	IO_L20P_1/A8	N18	DUAL
1	IO_L21N_1/RHCLK1	L22	RHCLK
1	IO_L21P_1/RHCLK0	M22	RHCLK
1	IO_L22N_1/TRDY1/RHCLK3	L20	RHCLK
1	IO_L22P_1/RHCLK2	L21	RHCLK
1	IO_L24N_1/RHCLK5	M20	RHCLK
1	IO_L24P_1/RHCLK4	M18	RHCLK
1	IO_L25N_1/RHCLK7	K19	RHCLK
1	IO_L25P_1/IRDY1/RHCLK6	K20	RHCLK
1	IO_L26N_1/A11	J22	DUAL

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
0	IO_L34N_0	D10	I/O
0	IO_L34P_0	C10	I/O
0	IO_L35N_0	H12	I/O
0	IO_L35P_0	G12	I/O
0	IO_L36N_0	B9	I/O
0	IO_L36P_0	A9	I/O
0	IO_L37N_0	D9	I/O
0	IO_L37P_0	E10	I/O
0	IO_L38N_0	B8	I/O
0	IO_L38P_0	A8	I/O
0	IO_L39N_0	K12	I/O
0	IO_L39P_0	J12	I/O
0	IO_L40N_0	D8	I/O
0	IO_L40P_0	C8	I/O
0	IO_L41N_0	C6	I/O
0	IO_L41P_0	B6	I/O
0	IO_L42N_0	C7	I/O
0	IO_L42P_0	B7	I/O
0	IO_L43N_0	K11	I/O
0	IO_L43P_0	J11	I/O
0	IO_L44N_0	D6	I/O
0	IO_L44P_0	C5	I/O
0	IO_L45N_0	B4	I/O
0	IO_L45P_0	A4	I/O
0	IO_L46N_0	H10	I/O
0	IO_L46P_0	G10	I/O
0	IO_L47N_0	H9	I/O
0	IO_L47P_0	G9	I/O
0	IO_L48N_0	E7	I/O
0	IO_L48P_0	F7	I/O
0	IO_L51N_0	B3	I/O
0	IO_L51P_0	A3	I/O
0	IO_L52N_0/PUDC_B	G8	DUAL
0	IO_L52P_0/VREF_0	F8	VREF
0	IP_0	A5	INPUT
0	IP_0	A7	INPUT
0	IP_0	A13	INPUT
0	IP_0	A17	INPUT
0	IP_0	A23	INPUT
0	IP_0	C4	INPUT

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
0	IP_0	D12	INPUT
0	IP_0	D15	INPUT
0	IP_0	D19	INPUT
0	IP_0	E11	INPUT
0	IP_0	E18	INPUT
0	IP_0	E20	INPUT
0	IP_0	F10	INPUT
0	IP_0	G14	INPUT
0	IP_0	G16	INPUT
0	IP_0	H13	INPUT
0	IP_0	H18	INPUT
0	IP_0	J10	INPUT
0	IP_0	J13	INPUT
0	IP_0	J15	INPUT
0	IP_0/VREF_0	D7	VREF
0	IP_0/VREF_0	D14	VREF
0	IP_0/VREF_0	G11	VREF
0	IP_0/VREF_0	J17	VREF
0	N.C. (◆)	A24	N.C.
0	N.C. (◆)	B24	N.C.
0	N.C. (◆)	D5	N.C.
0	N.C. (◆)	E9	N.C.
0	N.C. (◆)	F18	N.C.
0	N.C. (◆)	E6	N.C.
0	N.C. (◆)	F9	N.C.
0	N.C. (◆)	G18	N.C.
0	VCCO_0	B5	VCCO
0	VCCO_0	B11	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	B22	VCCO
0	VCCO_0	E8	VCCO
0	VCCO_0	E13	VCCO
0	VCCO_0	E19	VCCO
0	VCCO_0	H11	VCCO
0	VCCO_0	H16	VCCO
1	IO_L01N_1/LDC2	Y21	DUAL
1	IO_L01P_1/HDC	Y20	DUAL
1	IO_L02N_1/LDC0	AD25	DUAL
1	IO_L02P_1/LDC1	AE26	DUAL
1	IO_L03N_1/A1	AC24	DUAL

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
3	IO_L30P_3	N5	I/O
3	IO_L31N_3	N2	I/O
3	IO_L31P_3	N1	I/O
3	IO_L32N_3/LHCLK1	N7	LHCLK
3	IO_L32P_3/LHCLK0	N6	LHCLK
3	IO_L33N_3/IRDY2/LHCLK3	P2	LHCLK
3	IO_L33P_3/LHCLK2	P1	LHCLK
3	IO_L34N_3/LHCLK5	P3	LHCLK
3	IO_L34P_3/LHCLK4	P4	LHCLK
3	IO_L35N_3/LHCLK7	P10	LHCLK
3	IO_L35P_3/TRDY2/LHCLK6	N9	LHCLK
3	IO_L36N_3	R2	I/O
3	IO_L36P_3/VREF_3	R1	VREF
3	IO_L37N_3	R4	I/O
3	IO_L37P_3	R3	I/O
3	IO_L38N_3	T4	I/O
3	IO_L38P_3	T3	I/O
3	IO_L39N_3	P6	I/O
3	IO_L39P_3	P7	I/O
3	IO_L40N_3	R6	I/O
3	IO_L40P_3	R5	I/O
3	IO_L41N_3	P9	I/O
3	IO_L41P_3	P8	I/O
3	IO_L42N_3	U4	I/O
3	IO_L42P_3	T5	I/O
3	IO_L43N_3	R9	I/O
3	IO_L43P_3/VREF_3	R10	VREF
3	IO_L44N_3	U2	I/O
3	IO_L44P_3	U1	I/O
3	IO_L45N_3	R7	I/O
3	IO_L45P_3	R8	I/O
3	IO_L47N_3	V2	I/O
3	IO_L47P_3	V1	I/O
3	IO_L48N_3	T9	I/O
3	IO_L48P_3	T10	I/O
3	IO_L49N_3	V5	I/O
3	IO_L49P_3	U5	I/O
3	IO_L51N_3	U6	I/O
3	IO_L51P_3	T7	I/O
3	IO_L52N_3	W4	I/O

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
3	IO_L52P_3	W3	I/O
3	IO_L53N_3	Y2	I/O
3	IO_L53P_3	Y1	I/O
3	IO_L55N_3	AA3	I/O
3	IO_L55P_3	AA2	I/O
3	IO_L56N_3	U8	I/O
3	IO_L56P_3	U7	I/O
3	IO_L57N_3	Y6	I/O
3	IO_L57P_3	Y5	I/O
3	IO_L59N_3	V6	I/O
3	IO_L59P_3	V7	I/O
3	IO_L60N_3	AC1	I/O
3	IO_L60P_3	AB1	I/O
3	IO_L61N_3	V8	I/O
3	IO_L61P_3	U9	I/O
3	IO_L63N_3	W6	I/O
3	IO_L63P_3	W7	I/O
3	IO_L64N_3	AC3	I/O
3	IO_L64P_3	AC2	I/O
3	IO_L65N_3	AD2	I/O
3	IO_L65P_3	AD1	I/O
3	IP_L04N_3/VREF_3	C1	VREF
3	IP_L04P_3	C2	INPUT
3	IP_L08N_3	D1	INPUT
3	IP_L08P_3	D2	INPUT
3	IP_L12N_3/VREF_3	H4	VREF
3	IP_L12P_3	G5	INPUT
3	IP_L16N_3	G1	INPUT
3	IP_L16P_3	G2	INPUT
3	IP_L20N_3/VREF_3	J2	VREF
3	IP_L20P_3	J3	INPUT
3	IP_L24N_3	K1	INPUT
3	IP_L24P_3	J1	INPUT
3	IP_L46N_3	V4	INPUT
3	IP_L46P_3	U3	INPUT
3	IP_L50N_3/VREF_3	W2	VREF
3	IP_L50P_3	W1	INPUT
3	IP_L54N_3	Y4	INPUT
3	IP_L54P_3	Y3	INPUT
3	IP_L58N_3/VREF_3	AA5	VREF

Table 87: **Spartan-3A FG676 Pinout *(Continued)***

Bank	Pin Name	FG676 Ball	Type
3	IP_L58P_3	AA4	INPUT
3	IP_L62N_3	AB4	INPUT
3	IP_L62P_3	AB3	INPUT
3	IP_L66N_3/VREF_3	AE2	VREF
3	IP_L66P_3	AE1	INPUT
3	VCCO_3	AB2	VCCO
3	VCCO_3	E2	VCCO
3	VCCO_3	H5	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	L8	VCCO
3	VCCO_3	P5	VCCO
3	VCCO_3	T2	VCCO
3	VCCO_3	T8	VCCO
3	VCCO_3	W5	VCCO
GND	GND	A1	GND
GND	GND	A6	GND
GND	GND	A11	GND
GND	GND	A16	GND
GND	GND	A21	GND
GND	GND	A26	GND
GND	GND	AA1	GND
GND	GND	AA6	GND
GND	GND	AA11	GND
GND	GND	AA16	GND
GND	GND	AA21	GND
GND	GND	AA26	GND
GND	GND	AD3	GND
GND	GND	AD8	GND
GND	GND	AD13	GND
GND	GND	AD18	GND
GND	GND	AD24	GND
GND	GND	AF1	GND
GND	GND	AF6	GND
GND	GND	AF11	GND
GND	GND	AF16	GND
GND	GND	AF21	GND
GND	GND	AF26	GND
GND	GND	C3	GND
GND	GND	C9	GND
GND	GND	C14	GND

Table 87: **Spartan-3A FG676 Pinout *(Continued)***

Bank	Pin Name	FG676 Ball	Type
GND	GND	C19	GND
GND	GND	C24	GND
GND	GND	F1	GND
GND	GND	F6	GND
GND	GND	F11	GND
GND	GND	F16	GND
GND	GND	F21	GND
GND	GND	F26	GND
GND	GND	H3	GND
GND	GND	H8	GND
GND	GND	H14	GND
GND	GND	H19	GND
GND	GND	J24	GND
GND	GND	K10	GND
GND	GND	K17	GND
GND	GND	L1	GND
GND	GND	L6	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L15	GND
GND	GND	L21	GND
GND	GND	L26	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M16	GND
GND	GND	N3	GND
GND	GND	N8	GND
GND	GND	N11	GND
GND	GND	N15	GND
GND	GND	P12	GND
GND	GND	P16	GND
GND	GND	P19	GND
GND	GND	P24	GND
GND	GND	R11	GND
GND	GND	R13	GND
GND	GND	R15	GND
GND	GND	T1	GND
GND	GND	T6	GND
GND	GND	T12	GND
GND	GND	T14	GND

User I/Os by Bank

Table 88 indicates how the 502 available user-I/O pins are distributed between the four I/O banks on the FG676 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 88: **User I/Os Per Bank for the XC3S1400A in the FG676 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	120	82	20	1	9	8
Right	1	130	67	15	30	10	8
Bottom	2	120	67	14	21	10	8
Left	3	132	97	18	0	9	8
TOTAL		**502**	**313**	**67**	**52**	**38**	**32**

Footprint Migration Differences

The XC3S1400A FPGA is the only Spartan-3A device offered in the FG676 package. However, Table 89 summarizes footprint and functionality differences between the XC3S1400A and the XC3SD1800A in the Spartan-3A DSP family. There are 17 unconnected balls in the XC3S1400A that become 16 input-only pins and one I/O pin in the XC3SD1800A. All other pins not listed in Table 89 unconditionally migrate between the Spartan-3A devices and the Spartan-3A DSP devices available in the FG676 package. The arrows indicate the direction for easy migration. For more details on the Spartan-3A DSP family and pinouts, and additional differences in the FG676 pinout for the XC3SD3400A device, see DS610.

Table 89: **FG676 Footprint Differences**

Pin	Bank	XC3S1400A	Migration	XC3SD1800A
A24	0	N.C.	→	INPUT
B24	0	N.C.	→	INPUT
D5	0	N.C.	→	INPUT
E6	0	N.C.	→	VREF (INPUT)
E9	0	N.C.	→	INPUT
F9	0	N.C.	→	VREF (INPUT)
F18	0	N.C.	→	INPUT
G18	0	N.C.	→	VREF (INPUT)
W18	2	N.C.	→	VREF (INPUT)
Y8	2	N.C.	→	VREF (INPUT)
Y18	2	N.C.	→	INPUT
Y19	2	N.C.	→	INPUT
AA8	2	N.C.	→	INPUT
AC5	2	N.C.	→	INPUT
AC22	2	N.C.	→	I/O
AD5	2	N.C.	→	INPUT
AD23	2	N.C.	→	VREF(INPUT)
DIFFERENCES			**17**	

Legend:

→ This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction is possible depending on how the pin is configured for the device on the right.

Right Half of FG676 Package (Top View)

Bank 0 (top) · Bank 1 (right) · Bank 2 (bottom)

	14	15	16	17	18	19	20	21	22	23	24	25	26
A	I/O L26N_0 GCLK7	I/O L23N_0	GND	INPUT	I/O L18N_0	I/O L15N_0	I/O L14N_0	GND	I/O L07N_0	INPUT	N.C. ◆	TCK	GND
B	I/O L26P_0 GCLK6	I/O L23P_0	VCCO_0	I/O L19N_0	I/O L18P_0	I/O L15P_0	I/O L14P_0 VREF_0	I/O L09N_0	VCCO_0	I/O L07P_0	N.C. ◆	INPUT L65N_1	INPUT L65P_1 VREF_1
C	GND	I/O L22N_0	I/O L21N_0	I/O L19P_0	I/O L17N_0	GND	I/O L11N_0	I/O L09P_0	I/O L05N_0	I/O L06N_0	GND	I/O L63N_1 A23	I/O L63P_1 A22
D	INPUT VREF_0	INPUT	I/O L22P_0	I/O L21P_0	I/O L17P_0	INPUT	I/O L11P_0	I/O L10N_0	I/O L05P_0	I/O L06P_0	I/O L61N_1	I/O L61P_1	I/O L60N_1
E	I/O L24P_0	I/O L20N_0 VREF_0	VCCAUX	I/O L13N_0	INPUT	VCCO_0	INPUT	I/O L10P_0	VCCAUX	TDO	I/O L56P_1	VCCO_1	I/O L60P_1
F	I/O L24N_0	I/O L20P_0	GND	I/O L13P_0	N.C. ◆	I/O L02N_0	I/O L01N_0	GND	I/O L58P_1 VREF_1	I/O L56N_1	I/O L54N_1	I/O L54P_1	GND
G	INPUT	I/O L16P_0	INPUT	I/O L08N_0	N.C. ◆	I/O L02P_0 VREF_0	I/O L01P_0	I/O L64N_1 A25	I/O L58N_1	I/O L51P_1	I/O L51N_1	INPUT L52N_1 VREF_1	INPUT L52P_1
H	GND	I/O L16N_0	VCCO_0	I/O L08P_0	INPUT	GND	I/O L64P_1 A24	I/O L62N_1 A21	VCCO_1	INPUT L48P_1	INPUT L48N_1	INPUT L44N_1	INPUT L44P_1 VREF_1
J	I/O L25N_0 GCLK5	INPUT	I/O L12P_0	INPUT VREF_0	VCCAUX	I/O L59P_1	I/O L59N_1	I/O L62P_1 A20	I/O L49N_1	I/O L49P_1	GND	I/O L43N_1 A19	I/O L43P_1 A18
K	I/O L25P_0 GCLK4	VCCINT	I/O L12N_0	GND	I/O L57N_1	I/O L57P_1	I/O L53N_1	I/O L50N_1	I/O L46N_1	I/O L46P_1	INPUT L40P_1	I/O L41P_1	I/O L41N_1
L	VCCINT	GND	VCCINT	I/O L55N_1	I/O L55P_1	VCCO_1	I/O L53P_1	GND	I/O L50P_1	INPUT L40N_1	I/O L38P_1 A12	VCCO_1	GND
M	GND	VCCINT	GND	VCCINT	I/O L47N_1	I/O L47P_1	I/O L42N_1 A17	I/O L45P_1	I/O L45N_1	I/O L38N_1 A13	INPUT L36P_1 VREF_1	I/O L35N_1 A11	I/O L35P_1 A10
N	VCCINT	GND	VCCINT	I/O L39N_1 A15	I/O L39P_1 A14	I/O L34N_1 RHCLK7	I/O L42P_1 A16	I/O L37N_1	VCCO_1	INPUT L36N_1	I/O L33N_1 RHCLK5	INPUT L32N_1	INPUT L32P_1
P	VCCINT	VCCINT	GND	VCCAUX	I/O L34P_1 IRDY1 RHCLK6	GND	I/O L30N_1 RHCLK1	I/O L30P_1 RHCLK0	I/O L37P_1	I/O L33P_1 RHCLK4	GND	I/O L31N_1 TRDY1 RHCLK3	I/O L31P_1 RHCLK2
R	VCCINT	GND	VCCINT	I/O L27N_1 A7	I/O L27P_1 A6	I/O L22P_1	I/O L22N_1	I/O L25P_1 A2	I/O L25N_1 A3	INPUT L28P_1 VREF_1	INPUT L28N_1	I/O L29P_1 A8	I/O L29N_1 A9
T	GND	VCCINT	GND	I/O L17N_1	I/O L17P_1	VCCO_1	I/O L14N_1	GND	VCCAUX	I/O L26P_1 A4	I/O L26N_1 A5	VCCO_1	GND
U	VCCAUX	I/O L35N_2	I/O L42N_2	GND	I/O L12N_1	I/O L12P_1	I/O L10N_1	I/O L14P_1	I/O L21N_1	I/O L23P_1	I/O L23N_1 VREF_1	INPUT L24P_1	INPUT L24N_1 VREF_1
V	I/O L31P_2	I/O L35P_2	I/O L42P_2	I/O L46N_2	I/O L08P_1	I/O L08N_1	SUSPEND	I/O L10P_1	I/O L18N_1	I/O L21P_1	I/O L19P_1	I/O L19N_1	INPUT L20N_1 VREF_1
W	GND	I/O L31N_2	VCCO_2	I/O L46P_2	N.C. ◆	GND	I/O L04P_1	I/O L04N_1	VCCO_1	I/O L18P_1	GND	INPUT L16P_1	INPUT L20P_1
Y	I/O L27P_2 GCLK0	I/O L34N_2 D3	INPUT 2 VREF_2	I/O L43N_2	N.C. ◆	N.C. ◆	I/O L01P_1 HDC	I/O L01N_1 LDC2	I/O L13P_1	I/O L13N_1	I/O L15P_1	I/O L15N_1	INPUT L16N_1
AA	I/O L27N_2 GCLK1	I/O L34P_2 INIT_B	GND	I/O L43P_2	I/O L47N_2	INPUT	INPUT VREF_2	GND	I/O L09P_1	I/O L09N_1	I/O L11P_1	I/O L11N_1	GND
AB	VCCO_2	I/O L30N_2 MOSI CSI_B	I/O L38N_2	INPUT	I/O L47P_2	VCCO_2	INPUT	DONE	VCCAUX	I/O L07P_1	I/O L07N_1 VREF_1	VCCO_1	I/O L06N_1
AC	I/O L29N_2	I/O L30P_2	I/O L38P_2	INPUT	INPUT	I/O L40N_2	I/O L41N_2	I/O L45N_2	N.C. ◆	I/O L03P_1 A0	I/O L03N_1 A1	I/O L05N_1	I/O L06P_1
AD	I/O L29P_2	I/O L32P_2 AWAKE	INPUT	I/O L33N_2	GND	I/O L40P_2	I/O L41P_2	I/O L44N_2	I/O L45P_2	N.C. ◆	GND	I/O L02N_1 LDC0	I/O L05P_1
AE	I/O L28N_2 GCLK3	I/O L32N_2 DOUT	VCCO_2	I/O L33P_2	I/O L36N_2 D1	I/O L37N_2	I/O L39N_2	I/O L44P_2	VCCO_2	I/O L48N_2	I/O L52N_2 CCLK	I/O L51N_2	I/O L02P_1 LDC1
AF	I/O L28P_2 GCLK2	INPUT VREF_2	GND	INPUT VREF_2	I/O L36P_2 D2	I/O L37P_2	I/O L39P_2	GND	INPUT VREF_2	I/O L48P_2	I/O L52P_2 D0 DIN/MISO	I/O L51P_2	GND

DS529-4_08_012009