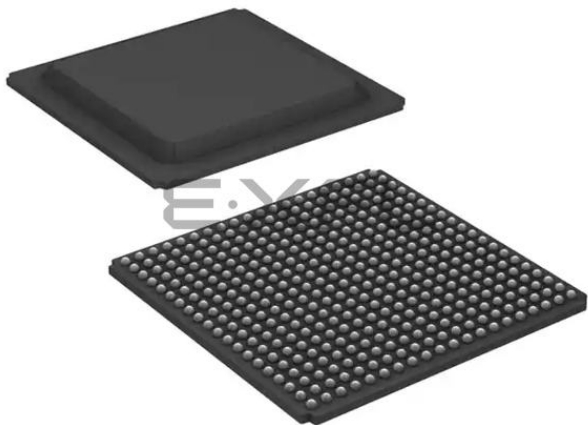




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	1472
Number of Logic Elements/Cells	13248
Total RAM Bits	368640
Number of I/O	311
Number of Gates	700000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	400-BGA
Supplier Device Package	400-FBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s700a-5fgg400c

Architectural Overview

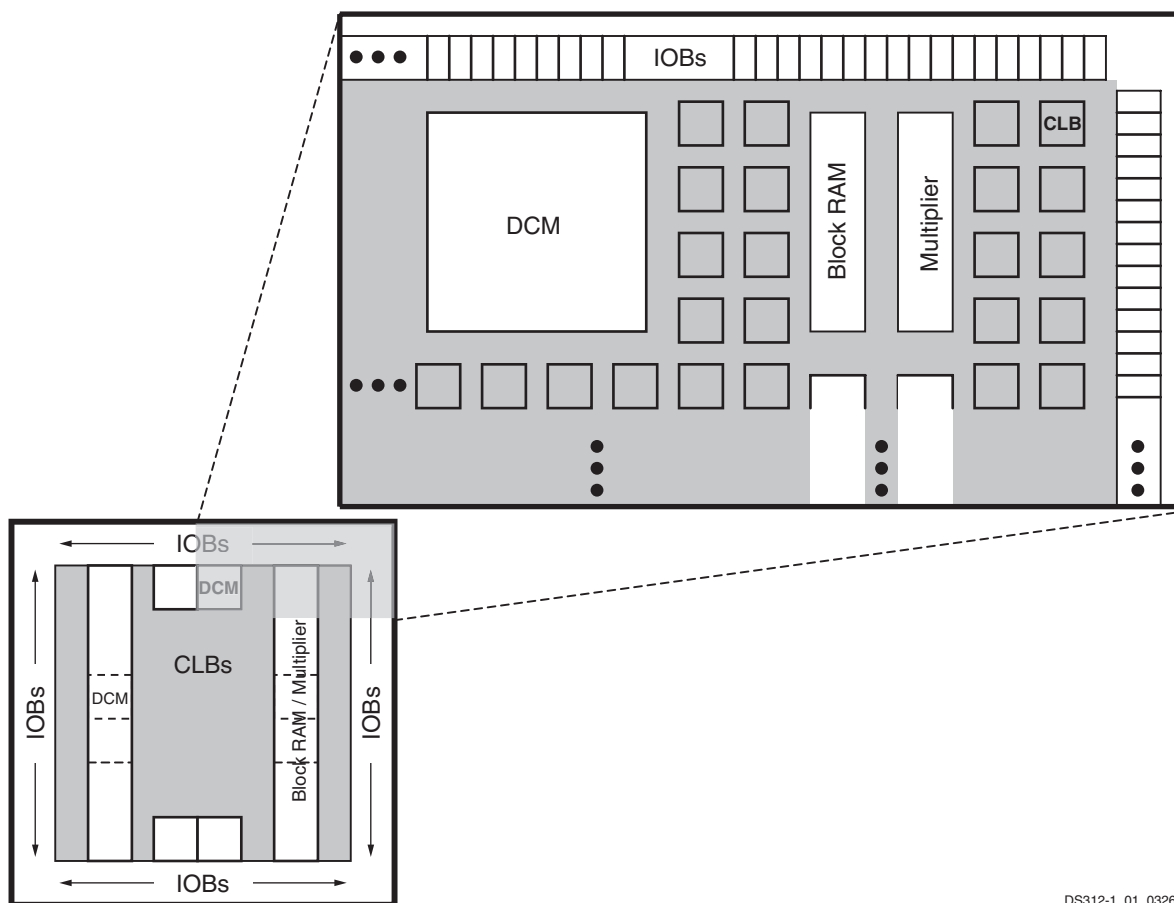
The Spartan-3A family architecture consists of five fundamental programmable functional elements:

- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. IOBs support bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including several high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product.

- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A dual ring of staggered IOBs surrounds a regular array of CLBs. Each device has two columns of block RAM except for the XC3S50A, which has one column. Each RAM column consists of several 18-Kbit RAM blocks. Each block RAM is associated with a dedicated multiplier. The DCMs are positioned in the center with two at the top and two at the bottom of the device. The XC3S50A has DCMs only at the top, while the XC3S700A and XC3S1400A add two DCMs in the middle of the two columns of block RAM and multipliers.

The Spartan-3A family features a rich network of routing that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



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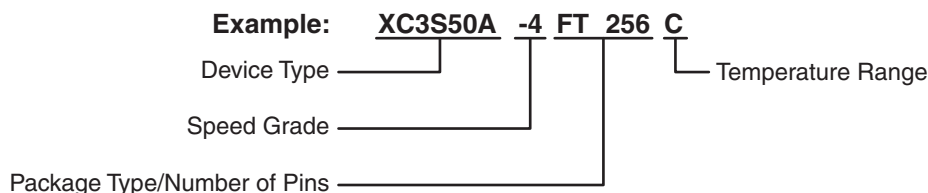
Notes:

1. The XC3S700A and XC3S1400A have two additional DCMs on both the left and right sides as indicated by the dashed lines. The XC3S50A has only two DCMs at the top and only one Block RAM/Multiplier column.

Figure 1: Spartan-3A FPGA Architecture

Ordering Information

Spartan-3A FPGAs are available in both standard and Pb-free packaging options for all device/package combinations. The Pb-free packages include a 'G' character in the ordering code.



DS529-1_05_011309

Device	Speed Grade		Package Type / Number of Pins ⁽¹⁾		Temperature Range (T _J)	
XC3S50A	–4	Standard Performance	VQ100/ VQG100	100-pin Very Thin Quad Flat Pack (VQFP)	C	Commercial (0°C to 85°C)
XC3S200A	–5	High Performance (Commercial only)	TQ144/ TQG144	144-pin Thin Quad Flat Pack (TQFP)	I	Industrial (–40°C to 100°C)
XC3S400A			FT256/ FTG256	256-ball Fine-Pitch Thin Ball Grid Array (FTBGA)		
XC3S700A			FG320/ FGG320	320-ball Fine-Pitch Ball Grid Array (FBGA)		
XC3S1400A			FG400/ FGG400	400-ball Fine-Pitch Ball Grid Array (FBGA)		
			FG484/ FGG484	484-ball Fine-Pitch Ball Grid Array (FBGA)		
			FG676/ FGG676	676-ball Fine-Pitch Ball Grid Array (FBGA)		

Notes:

- See [Table 2](#) for specific device/package combinations.
- See [DS681](#) for the XA Automotive Spartan-3A FPGAs.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/05/06	1.0	Initial release.
02/02/07	1.1	Promoted to Preliminary status. Updated maximum differential I/O count for XC3S50A in Table 1 . Updated differential input-only pin counts in Table 2 .
03/16/07	1.2	Minor formatting updates.
04/23/07	1.3	Added " Production Status " section.
05/08/07	1.4	Updated XC3S400A to Production.
07/10/07	1.4.1	Minor updates.
04/15/08	1.6	Added VQ100 for XC3S50A and XC3S200A and extended FT256 to XC3S700A and XC3S1400A. Added reference to SCD 4103 for 750 Mbps performance.
05/28/08	1.7	Added reference to XA Automotive version.
03/06/09	1.8	Simplified Ordering Information. Added references to Extended Spartan-3A Family. Removed reference to SCD 4103.
08/19/10	2.0	Updated Table 2 to clarify TQ/VQ size.

General Recommended Operating Conditions

Table 8: General Recommended Operating Conditions

Symbol	Description			Min	Nominal	Max	Units
T _J	Junction temperature	Commercial		0	—	85	°C
		Industrial		−40	—	100	°C
V _{CCINT}	Internal supply voltage			1.14	1.20	1.26	V
V _{CCO} ⁽¹⁾	Output driver supply voltage			1.10	—	3.60	V
V _{CCAUX}	Auxiliary supply voltage ⁽²⁾	V _{CCAUX} = 2.5		2.25	2.50	2.75	V
		V _{CCAUX} = 3.3		3.00	3.30	3.60	V
V _{IN}	Input voltage ⁽³⁾	PCI IOSTANDARD		−0.5	—	V _{CCO} +0.5	V
		All other IOSTANDARDS	IP or IO_#	−0.5	—	4.10	V
			IO_Lxxy_# ⁽⁴⁾	−0.5	—	4.10	V
T _{IN}	Input signal transition time ⁽⁵⁾			—	—	500	ns

Notes:

1. This V_{CCO} range spans the lowest and highest operating voltages for all supported I/O standards. [Table 11](#) lists the recommended V_{CCO} range specific to each of the single-ended I/O standards, and [Table 13](#) lists that specific to the differential standards.
2. Define V_{CCAUX} selection using CONFIG VCCAUX constraint.
3. See [XAPP459](#), “Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins.”
4. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in [UG331](#), *Spartan-3 Generation FPGA User Guide*.
5. Measured between 10% and 90% V_{CCO} . Follow [Signal Integrity](#) recommendations.

Differential Output Pairs

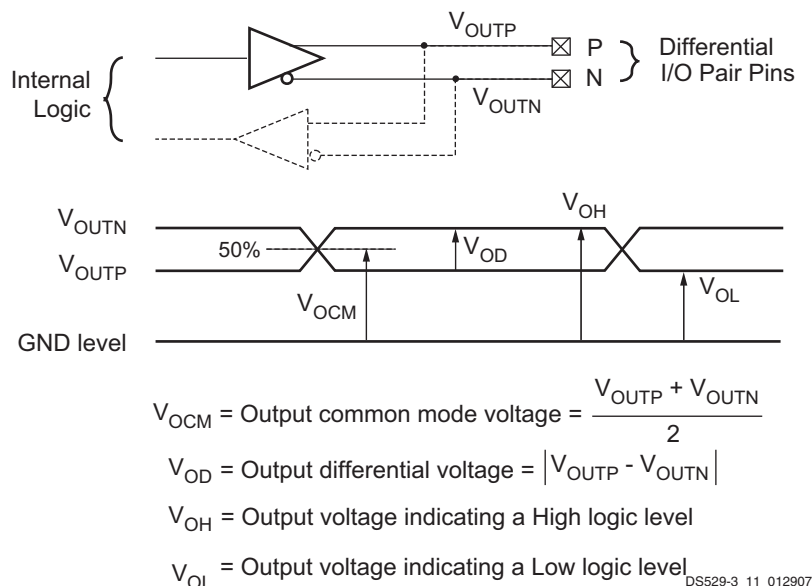


Figure 5: Differential Output Voltages

Table 14: DC Characteristics of User I/Os Using Differential Signal Standards

IOSTANDARD Attribute	V_{OD}			V_{OCM}			V_{OH}	V_{OL}
	Min (mV)	Typ (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (V)	Max (V)
LVDS_25	247	350	454	1.125	—	1.375	—	—
LVDS_33	247	350	454	1.125	—	1.375	—	—
BLVDS_25	240	350	460	—	1.30	—	—	—
MINI_LVDS_25	300	—	600	1.0	—	1.4	—	—
MINI_LVDS_33	300	—	600	1.0	—	1.4	—	—
RSDS_25	100	—	400	1.0	—	1.4	—	—
RSDS_33	100	—	400	1.0	—	1.4	—	—
TMDS_33	400	—	800	$V_{CCO} - 0.405$	—	$V_{CCO} - 0.190$	—	—
PPDS_25	100	—	400	0.5	0.8	1.4	—	—
PPDS_33	100	—	400	0.5	0.8	1.4	—	—
DIFF_HSTL_I_18	—	—	—	—	—	—	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_II_18	—	—	—	—	—	—	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_III_18	—	—	—	—	—	—	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_I	—	—	—	—	—	—	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_III	—	—	—	—	—	—	$V_{CCO} - 0.4$	0.4
DIFF_SSTL18_I	—	—	—	—	—	—	$V_{TT} + 0.475$	$V_{TT} - 0.475$
DIFF_SSTL18_II	—	—	—	—	—	—	$V_{TT} + 0.603$	$V_{TT} - 0.603$
DIFF_SSTL2_I	—	—	—	—	—	—	$V_{TT} + 0.61$	$V_{TT} - 0.61$
DIFF_SSTL2_II	—	—	—	—	—	—	$V_{TT} + 0.81$	$V_{TT} - 0.81$
DIFF_SSTL3_I	—	—	—	—	—	—	$V_{TT} + 0.6$	$V_{TT} - 0.6$
DIFF_SSTL3_II	—	—	—	—	—	—	$V_{TT} + 0.8$	$V_{TT} - 0.8$

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8 and Table 13.
2. See "External Termination Requirements for Differential I/O," page 20.
3. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100 Ω across the N and P pins of the differential signal pair.
4. At any given time, no more than two of the following differential output standards can be assigned to an I/O bank: LVDS_25, RSDS_25, MINI_LVDS_25, PPDS_25 when $V_{CCO}=2.5V$, or LVDS_33, RSDS_33, MINI_LVDS_33, TMDS_33, PPDS_33 when $V_{CCO} = 3.3V$

Table 22: Propagation Times for the IOB Input Path(Continued)

Symbol	Description	Conditions	DELAY_VALUE	Device	Speed Grade		Units
					-5	-4	
					Max	Max	
T _{IOPID}	The time it takes for data to travel from the Input pin to the I output with the input delay programmed	LVCMOS25 ⁽²⁾	15	XC3S200A	5.43	6.24	ns
			16		5.75	6.59	ns
			1	XC3S400A	1.32	1.43	ns
			2		1.67	1.83	ns
			3		1.90	2.07	ns
			4		2.33	2.52	ns
			5		2.60	2.91	ns
			6		2.94	3.20	ns
			7		3.23	3.51	ns
			8		3.50	3.85	ns
			9		3.18	3.55	ns
			10		3.53	3.95	ns
			11		3.76	4.20	ns
			12		4.26	4.67	ns
			13		4.51	4.97	ns
			14		4.85	5.32	ns
			15		5.14	5.64	ns
			16		5.40	5.95	ns
			1	XC3S700A	1.84	1.87	ns
			2		2.20	2.27	ns
			3		2.46	2.60	ns
			4		2.93	3.15	ns
			5		3.21	3.45	ns
			6		3.54	3.80	ns
			7		3.86	4.16	ns
			8		4.13	4.48	ns
			9		3.82	4.19	ns
			10		4.17	4.58	ns
			11		4.43	4.89	ns
			12		4.95	5.49	ns
			13		5.22	5.83	ns
			14		5.57	6.21	ns
			15		5.89	6.55	ns
			16		6.16	6.89	ns
			1	XC3S1400A	1.95	2.18	ns
			2		2.29	2.59	ns
			3		2.54	2.84	ns
			4		2.96	3.30	ns

Table 26: Output Timing Adjustments for IOB(Continued)

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS25	Slow	2 mA	5.33	5.33	ns
		4 mA	2.81	2.81	ns
		6 mA	2.82	2.82	ns
		8 mA	1.14	1.14	ns
		12 mA	1.10	1.10	ns
		16 mA	0.83	0.83	ns
		24 mA	2.26 ⁽³⁾	2.26 ⁽³⁾	ns
	Fast	2 mA	4.36	4.36	ns
		4 mA	1.76	1.76	ns
		6 mA	1.25	1.25	ns
		8 mA	0.38	0.38	ns
		12 mA	0	0	ns
		16 mA	0.01	0.01	ns
		24 mA	0.01	0.01	ns
	QuietIO	2 mA	25.92	25.92	ns
		4 mA	25.92	25.92	ns
		6 mA	25.92	25.92	ns
		8 mA	15.57	15.57	ns
		12 mA	15.59	15.59	ns
		16 mA	14.27	14.27	ns
		24 mA	11.37	11.37	ns
LVCMOS18	Slow	2 mA	4.48	4.48	ns
		4 mA	3.69	3.69	ns
		6 mA	2.91	2.91	ns
		8 mA	1.99	1.99	ns
		12 mA	1.57	1.57	ns
		16 mA	1.19	1.19	ns
	Fast	2 mA	3.96	3.96	ns
		4 mA	2.57	2.57	ns
		6 mA	1.90	1.90	ns
		8 mA	1.06	1.06	ns
		12 mA	0.83	0.83	ns
		16 mA	0.63	0.63	ns
	QuietIO	2 mA	24.97	24.97	ns
		4 mA	24.97	24.97	ns
		6 mA	24.08	24.08	ns
		8 mA	16.43	16.43	ns
12 mA		14.52	14.52	ns	
		16 mA	13.41	13.41	ns

Table 26: Output Timing Adjustments for IOB(Continued)

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS15	Slow	2 mA	5.82	5.82	ns
		4 mA	3.97	3.97	ns
		6 mA	3.21	3.21	ns
		8 mA	2.53	2.53	ns
		12 mA	2.06	2.06	ns
	Fast	2 mA	5.23	5.23	ns
		4 mA	3.05	3.05	ns
		6 mA	1.95	1.95	ns
		8 mA	1.60	1.60	ns
		12 mA	1.30	1.30	ns
	QuietIO	2 mA	34.11	34.11	ns
		4 mA	25.66	25.66	ns
		6 mA	24.64	24.64	ns
		8 mA	22.06	22.06	ns
		12 mA	20.64	20.64	ns
LVCMOS12	Slow	2 mA	7.14	7.14	ns
		4 mA	4.87	4.87	ns
		6 mA	5.67	5.67	ns
	Fast	2 mA	6.77	6.77	ns
		4 mA	5.02	5.02	ns
		6 mA	4.09	4.09	ns
	QuietIO	2 mA	50.76	50.76	ns
		4 mA	43.17	43.17	ns
		6 mA	37.31	37.31	ns
PCI33_3			0.34	0.34	ns
PCI66_3			0.34	0.34	ns
HSTL_I			0.78	0.78	ns
HSTL_III			1.16	1.16	ns
HSTL_I_18			0.35	0.35	ns
HSTL_II_18			0.30	0.30	ns
HSTL_III_18			0.47	0.47	ns
SSTL18_I			0.40	0.40	ns
SSTL18_II			0.30	0.30	ns
SSTL2_I			0	0	ns
SSTL2_II			-0.05	-0.05	ns
SSTL3_I			0	0	ns
SSTL3_II			0.17	0.17	ns

18 x 18 Embedded Multiplier Timing

Table 34: 18 x 18 Embedded Multiplier Timing

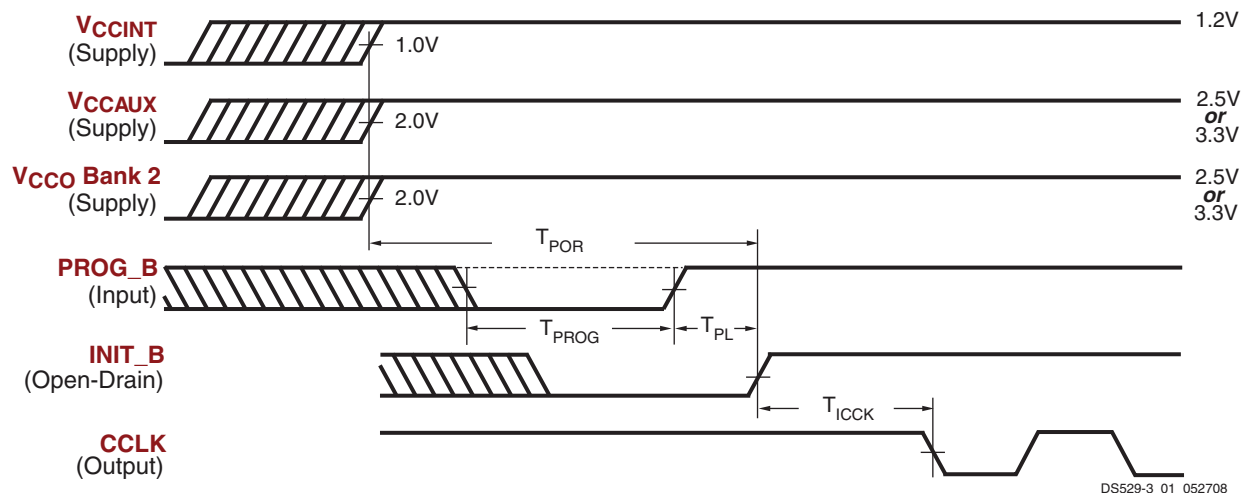
Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Combinatorial Delay						
T _{MULT}	Combinational multiplier propagation delay from the A and B inputs to the P outputs, assuming 18-bit inputs and a 36-bit product (AREG, BREG, and PREG registers unused)	–	4.36	–	4.88	ns
Clock-to-Output Times						
T _{MSCKP_P}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using the PREG register ^(2,3)	–	0.84	–	1.30	ns
T _{MSCKP_A} T _{MSCKP_B}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using either the AREG or BREG register ^(2,4)	–	4.44	–	4.97	ns
Setup Times						
T _{MSDCK_P}	Data setup time at the A or B input before the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused) ⁽³⁾	3.56	–	3.98	–	ns
T _{MSDCK_A}	Data setup time at the A input before the active transition at the CLK when using the AREG input register ⁽⁴⁾	0.00	–	0.00	–	ns
T _{MSDCK_B}	Data setup time at the B input before the active transition at the CLK when using the BREG input register ⁽⁴⁾	0.00	–	0.00	–	ns
Hold Times						
T _{MSCKD_P}	Data hold time at the A or B input after the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused) ⁽³⁾	0.00	–	0.00	–	ns
T _{MSCKD_A}	Data hold time at the A input after the active transition at the CLK when using the AREG input register ⁽⁴⁾	0.35	–	0.45	–	ns
T _{MSCKD_B}	Data hold time at the B input after the active transition at the CLK when using the BREG input register ⁽⁴⁾	0.35	–	0.45	–	ns
Clock Frequency						
F _{MULT}	Internal operating frequency for a two-stage 18x18 multiplier using the AREG and BREG input registers and the PREG output register ⁽¹⁾	0	280	0	250	MHz

Notes:

1. Combinational delay is less and pipelined performance is higher when multiplying input data with less than 18 bits.
2. The PREG register is typically used in both single-stage and two-stage pipelined multiplier implementations.
3. The PREG register is typically used when inferring a single-stage multiplier.
4. Input registers AREG or BREG are typically used when inferring a two-stage multiplier.
5. The numbers in this table are based on the operating conditions set forth in [Table 8](#).

Configuration and JTAG Timing

General Configuration Power-On/Reconfigure Timing


Notes:

1. The V_{CCINT} , V_{CCAUX} , and V_{CCO} supplies can be applied in any order.
2. The Low-going pulse on $PROG_B$ is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of $INIT_B$ samples the voltage levels applied to the mode pins (M0 - M2).

Figure 11: Waveforms for Power-On and the Beginning of Configuration

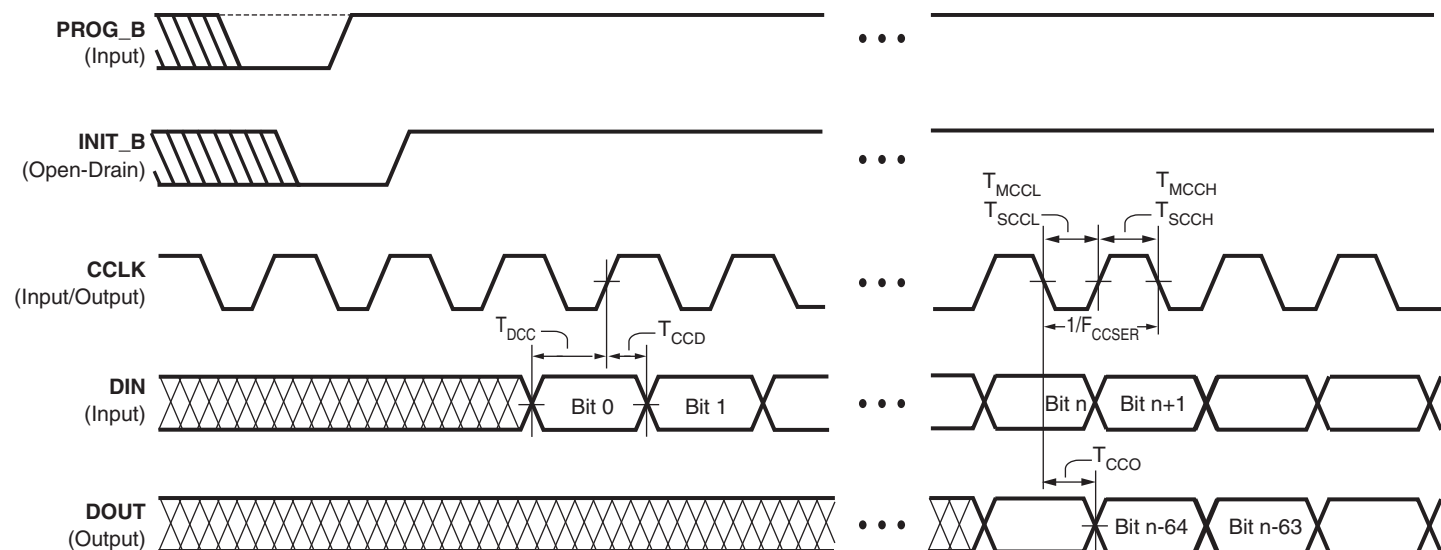
Table 45: Power-On Timing and the Beginning of Configuration

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
$T_{POR}^{(2)}$	The time from the application of V_{CCINT} , V_{CCAUX} , and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the $INIT_B$ pin	All	—	18	ms
T_{PROG}	The width of the low-going pulse on the $PROG_B$ pin	All	0.5	—	μ s
$T_{PL}^{(2)}$	The time from the rising edge of the $PROG_B$ pin to the rising transition on the $INIT_B$ pin	XC3S50A	—	0.5	ms
		XC3S200A	—	0.5	ms
		XC3S400A	—	1	ms
		XC3S700A	—	2	ms
		XC3S1400A	—	2	ms
T_{INIT}	Minimum Low pulse width on $INIT_B$ output	All	250	—	ns
$T_{ICCK}^{(3)}$	The time from the rising edge of the $INIT_B$ pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4	μ s

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8. This means power must be applied to all V_{CCINT} , V_{CCO} , and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, and BPI modes.
4. For details on configuration, see [UG332](#) *Spartan-3 Generation Configuration User Guide*.

Master Serial and Slave Serial Mode Timing



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Figure 12: Waveforms for Master Serial and Slave Serial Configuration

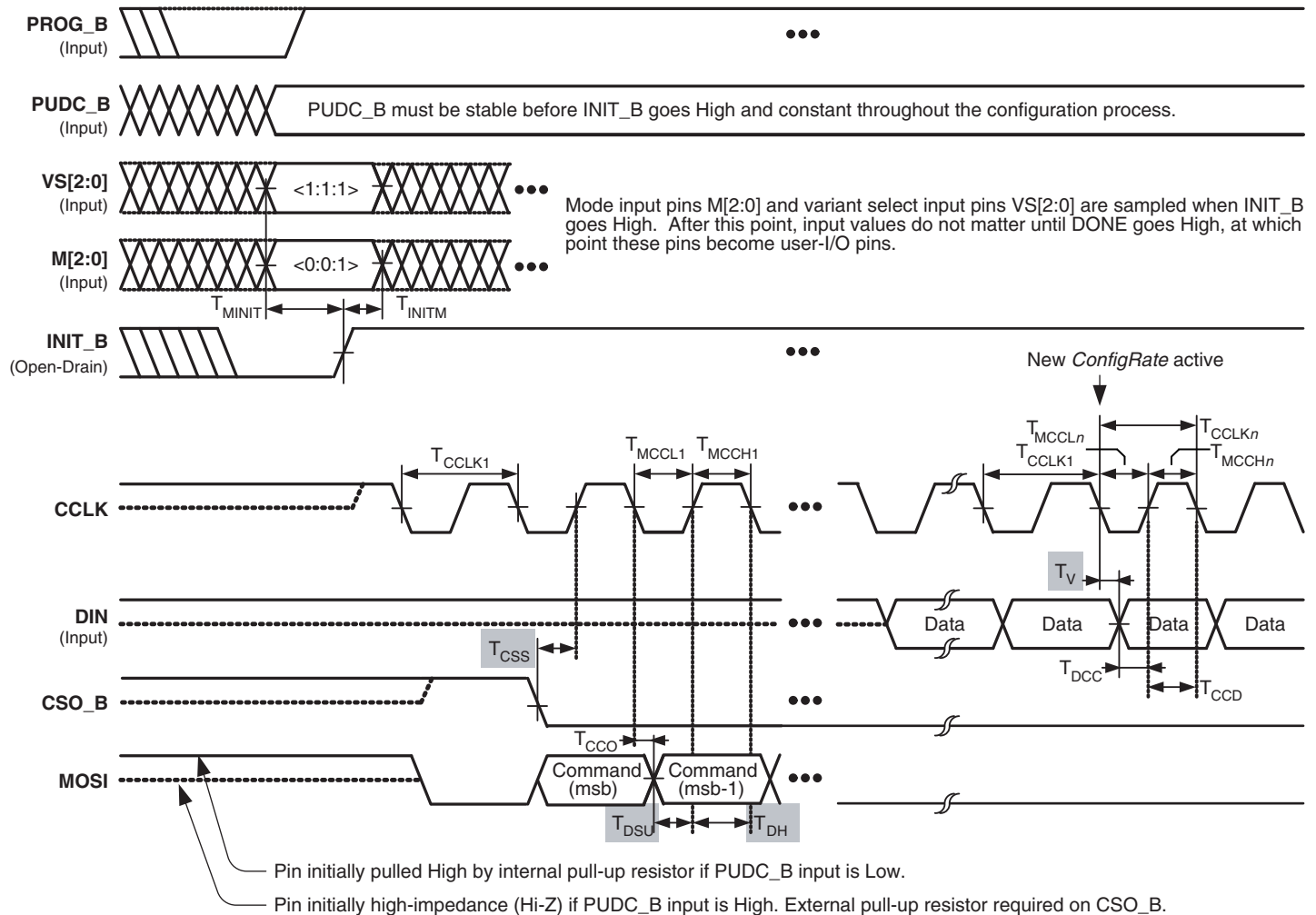
Table 50: Timing for the Master Serial and Slave Serial Configuration Modes

Symbol	Description	Slave/ Master	All Speed Grades		Units
			Min	Max	
Clock-to-Output Times					
T _{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin	Both	1.5	10	ns
Setup Times					
T _{DCC}	The time from the setup of data at the DIN pin to the rising transition at the CCLK pin	Both	7	—	ns
Hold Times					
T _{CCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin	Master	0	—	ns
		Slave	1.0		
Clock Timing					
T _{CCH}	High pulse width at the CCLK input pin	Master	See Table 48		
		Slave	See Table 49		
T _{CCL}	Low pulse width at the CCLK input pin	Master	See Table 48		
		Slave	See Table 49		
F _{CCSER}	Frequency of the clock signal at the CCLK input pin	Slave	0	100	MHz
	No bitstream compression				
	With bitstream compression		0	100	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Serial Peripheral Interface (SPI) Configuration Timing



DS529-3_06_102506

Figure 14: Waveforms for Serial Peripheral Interface (SPI) Configuration

Table 52: Timing for Serial Peripheral Interface (SPI) Configuration Mode

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	See Table 46		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate bitstream option setting	See Table 46		
T_{MINIT}	Setup time on VS[2:0] variant-select pins and M[2:0] mode pins before the rising edge of INIT_B	50	—	ns
T_{INITM}	Hold time on VS[2:0] variant-select pins and M[2:0] mode pins after the rising edge of INIT_B	0	—	ns
T_{CCO}	MOSI output valid delay after CCLK falling clock edge	See Table 50		
T_{DCC}	Setup time on the DIN data input before CCLK rising clock edge	See Table 50		
T_{CCD}	Hold time on the DIN data input after CCLK rising clock edge	See Table 50		

Table 53: Configuration Timing Requirements for Attached SPI Serial Flash

Symbol	Description	Requirement	Units
T_{CCS}	SPI serial Flash PROM chip-select time	$T_{CCS} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DSU}	SPI serial Flash PROM data input setup time	$T_{DSU} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DH}	SPI serial Flash PROM data input hold time	$T_{DH} \leq T_{MCCH1}$	ns
T_V	SPI serial Flash PROM data clock-to-output time	$T_V \leq T_{MCCLn} - T_{DCC}$	ns
f_C or f_R	Maximum SPI serial Flash PROM clock frequency (also depends on specific read command used)	$f_C \geq \frac{1}{T_{CCLKn(min)}}$	MHz

Notes:

1. These requirements are for successful FPGA configuration in SPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.

TQ144: 144-lead Thin Quad Flat Package

The XC3S50A is available in the 144-lead thin quad flat package, TQ144.

Table 66 lists all the package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The XC3S50A does not support the address output pins for the Byte-wide Peripheral Interface (BPI) configuration mode.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip

Pinout Table

Table 66: Spartan-3A TQ144 Pinout

Bank	Pin Name	Pin	Type
0	IO_0	P142	I/O
0	IO_L01N_0	P111	I/O
0	IO_L01P_0	P110	I/O
0	IO_L02N_0	P113	I/O
0	IO_L02P_0/VREF_0	P112	VREF
0	IO_L03N_0	P117	I/O
0	IO_L03P_0	P115	I/O
0	IO_L04N_0	P116	I/O
0	IO_L04P_0	P114	I/O
0	IO_L05N_0	P121	I/O
0	IO_L05P_0	P120	I/O
0	IO_L06N_0/GCLK5	P126	GCLK
0	IO_L06P_0/GCLK4	P124	GCLK
0	IO_L07N_0/GCLK7	P127	GCLK
0	IO_L07P_0/GCLK6	P125	GCLK
0	IO_L08N_0/GCLK9	P131	GCLK
0	IO_L08P_0/GCLK8	P129	GCLK
0	IO_L09N_0/GCLK11	P132	GCLK
0	IO_L09P_0/GCLK10	P130	GCLK
0	IO_L10N_0	P135	I/O
0	IO_L10P_0	P134	I/O
0	IO_L11N_0	P139	I/O
0	IO_L11P_0	P138	I/O
0	IO_L12N_0/PUDC_B	P143	DUAL
0	IO_L12P_0/VREF_0	P141	VREF
0	IP_0	P140	INPUT

Table 66: Spartan-3A TQ144 Pinout(Continued)

Bank	Pin Name	Pin	Type
0	IP_0/VREF_0	P123	VREF
0	VCCO_0	P119	VCCO
0	VCCO_0	P136	VCCO
1	IO_1	P79	I/O
1	IO_L01N_1/LDC2	P78	DUAL
1	IO_L01P_1/HDC	P76	DUAL
1	IO_L02N_1/LDC0	P77	DUAL
1	IO_L02P_1/LDC1	P75	DUAL
1	IO_L03N_1	P84	I/O
1	IO_L03P_1	P82	I/O
1	IO_L04N_1/RHCLK1	P85	RHCLK
1	IO_L04P_1/RHCLK0	P83	RHCLK
1	IO_L05N_1/TRDY1/RHCLK3	P88	RHCLK
1	IO_L05P_1/RHCLK2	P87	RHCLK
1	IO_L06N_1/RHCLK5	P92	RHCLK
1	IO_L06P_1/RHCLK4	P90	RHCLK
1	IO_L07N_1/RHCLK7	P93	RHCLK
1	IO_L07P_1/IRDY1/RHCLK6	P91	RHCLK
1	IO_L08N_1	P98	I/O
1	IO_L08P_1	P96	I/O
1	IO_L09N_1	P101	I/O
1	IO_L09P_1	P99	I/O
1	IO_L10N_1	P104	I/O
1	IO_L10P_1	P102	I/O
1	IO_L11N_1	P105	I/O
1	IO_L11P_1	P103	I/O
1	IP_1/VREF_1	P80	VREF
1	IP_1/VREF_1	P97	VREF
1	VCCO_1	P86	VCCO
1	VCCO_1	P95	VCCO
2	IO_2/MOSI/CSI_B	P62	DUAL
2	IO_L01N_2/M0	P38	DUAL
2	IO_L01P_2/M1	P37	DUAL
2	IO_L02N_2/CSO_B	P41	DUAL
2	IO_L02P_2/M2	P39	DUAL
2	IO_L03N_2/VS1	P44	DUAL
2	IO_L03P_2/RDWR_B	P42	DUAL
2	IO_L04N_2/VS0	P45	DUAL
2	IO_L04P_2/VS2	P43	DUAL
2	IO_L05N_2/D7	P48	DUAL

FT256 Footprint (XC3S50A)

		(Differential Outputs)					Bank 0				(Differential Outputs)						
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
(High Output Drive)	A	GND	PROG_B	I/O L19P_0	I/O L18P_0	I/O L17P_0	I/O L15P_0	N.C.	I/O L12P_0 GCLK10	I/O L10N_0 GCLK7	I/O L08N_0	I/O L07N_0	N.C.	I/O L04N_0	I/O L04P_0	TCK	GND
	B	TDI	TMS	I/O L19N_0	I/O L18N_0	VCCO_0	I/O L15N_0	GND	I/O L12N_0 GCLK11	VCCO_0	I/O L08P_0	GND	INPUT	VCCO_0	I/O L02N_0	I/O L02P_0 VREF_0	TDO
	C	I/O L01N_3	I/O L01P_3	GND	I/O L20P_0 VREF_0	I/O L17N_0	I/O L16N_0	N.C.	I/O L11P_0 GCLK8	I/O L10P_0 GCLK6	I/O L09P_0 GCLK4	I/O L07P_0	I/O L03P_0	I/O L01N_0	GND	I/O L24N_1	I/O L24P_1
	D	I/O L03P_3	VCCO_3	I/O L02N_3	I/O L02P_3	I/O L20N_0 PUDC_B	INPUT	I/O L16P_0	I/O L11N_0 GCLK9	I/O L09N_0 GCLK5	N.C.	I/O L03N_0	INPUT	I/O L01P_0	I/O L23N_1	I/O L22N_1	I/O L22P_1
(High Output Drive)	E	I/O L03N_3	N.C.	N.C.	INPUT L04P_3	GND	INPUT	N.C.	VCCO_0	INPUT VREF_0	N.C.	VCCAUX	GND	I/O L23P_1	I/O L20P_1	VCCO_1	N.C.
	F	I/O L08P_3	GND	N.C.	INPUT L04N_3 VREF_3	VCCAUX	GND	INPUT	N.C.	INPUT	INPUT	INPUT L25N_1	INPUT L25P_1 VREF_1	I/O L20N_1	N.C.	N.C.	N.C.
	G	I/O L08N_3 VREF_3	I/O L11P_3 LHCLK0	N.C.	N.C.	N.C.	N.C.	VCCINT	GND	VCCINT	GND	INPUT L21N_1	INPUT L21P_1 VREF_1	N.C.	N.C.	GND	N.C.
	H	I/O L11N_3 LHCLK1	VCCO_3	I/O L12P_3 LHCLK2	N.C.	N.C.	N.C.	INPUT L13P_3	VCCINT	GND	INPUT L13P_1	INPUT L13N_1	VCCO_1	N.C.	I/O L14N_1 RHCLK5	I/O L15P_1 IRDY1 RHCLK6	I/O L15N_1 RHCLK7
(High Output Drive)	J	I/O L14N_3 LHCLK5	I/O L14P_3 LHCLK4	I/O L12N_3 IRDY2 LHCLK3	N.C.	VCCO_3	N.C.	INPUT L13N_3	GND	VCCINT	N.C.	N.C.	I/O L10P_1	I/O L10N_1	I/O L14P_1 RHCLK4	VCCO_1	I/O L12N_1 TRDY1 RHCLK3
	K	I/O L15N_3 LHCLK7	GND	I/O L15P_3 TRDY2 LHCLK6	N.C.	INPUT L21P_3	INPUT L21N_3	GND	VCCINT	GND	VCCINT	INPUT L04P_1	INPUT L04N_1 VREF_1	N.C.	I/O L11N_1 RHCLK1	I/O L11P_1 RHCLK0	I/O L12P_1 RHCLK2
	L	N.C.	N.C.	N.C.	N.C.	INPUT L25P_3	INPUT L25N_3 VREF_3	INPUT	INPUT	INPUT VREF_2	INPUT VREF_2	GND	VCCAUX	N.C.	N.C.	GND	N.C.
	M	I/O L20P_3	VCCO_3	N.C.	I/O L24N_3	GND	VCCAUX	INPUT VREF_2	INPUT VREF_2	VCCO_2	N.C.	INPUT VREF_2	GND	N.C.	N.C.	N.C.	N.C.
(High Output Drive)	N	I/O L20N_3	I/O L22P_3	I/O L24P_3	I/O L01P_2 M1	INPUT VREF_2	I/O L03N_2 VS1	N.C.	I/O L08N_2 D4	I/O L11P_2 GCLK0	N.C.	I/O L16N_2	N.C.	I/O L01P_1 HDC	I/O L01N_1 LDC2	VCCO_1	I/O L03N_1
	P	I/O L22N_3	I/O L23N_3	GND	I/O L01N_2 M0	I/O L04N_2 VS0	N.C.	I/O L08P_2 D5	I/O L10P_2 GCLK14	I/O L11N_2 GCLK1	I/O L14P_2 MOSI CSI_B	I/O L16P_2	I/O L17N_2 D3	N.C.	GND	I/O L02N_1 LDC0	I/O L03P_1
	R	I/O L23P_3	I/O L02P_2 M2	I/O L03P_2 RDWR_B	VCCO_2	I/O L06P_2	GND	N.C.	VCCO_2	I/O L12P_2 GCLK2	GND	I/O L15N_2 DOUT	VCCO_2	I/O L20P_2 D1	I/O L20N_2 CCLK	I/O L02P_1 LDC1	SUSPEND
	T	GND	I/O L02N_2 CSO_B	I/O L04P_2 VS2	I/O L05P_2	I/O L05N_2 D7	I/O L06N_2 D6	N.C.	I/O L10N_2 GCLK15	I/O L12N_2 GCLK3	I/O L14N_2	I/O L15P_2 AWAKE	I/O L17P_2 INIT_B	I/O L18P_2 D2	I/O L18N_2 D0 DIN/MISO	DONE	GND
		(Differential Outputs)					Bank 2				(Differential Outputs)						

Figure 20: XC3S50A FT256 Package Footprint (Top View)

53	I/O: Unrestricted, general-purpose user I/O	25	DUAL: Configuration pins, then possible user I/O	15	VREF: User I/O or input voltage reference for bank	2	SUSPEND: Dedicated SUSPEND and dual-purpose AWAKE Power Management pins
20	INPUT: Unrestricted, general-purpose input pin	30	CLK: User I/O, input, or global buffer input	16	VCCO: Output voltage supply for bank		
2	CONFIG: Dedicated configuration pins	4	JTAG: Dedicated JTAG port pins	6	VCCINT: Internal core supply voltage (+1.2V)		
51	N.C.: Not connected (XC3S50A only)	28	GND: Ground	4	VCCAUX: Auxiliary supply voltage		

Bank 0																			
11	12	13	14	15	16	17	18	19	20										
GND	I/O L13N_0	VCCAUX	I/O L07N_0	I/O L08N_0	I/O L05N_0	I/O L04N_0	I/O L01N_0	TCK	GND										
I/O L14P_0	I/O L13P_0	I/O L11P_0	GND	I/O L08P_0	VCCO_0	I/O L04P_0 VREF_0	I/O L01P_0	I/O L38N_1 A25	I/O L38P_1 A24										
I/O L14N_0	I/O L11N_0	I/O L10N_0 VREF_0	I/O L07P_0	I/O L06N_0	I/O L05P_0	I/O L02N_0	GND	I/O L37N_1 A23	I/O L37P_1 A22										
I/O L15P_0 GCLK4	I/O L12P_0	VCCO_0	I/O L10P_0	I/O L06P_0	I/O L03P_0	I/O L02P_0 VREF_0	I/O L34N_1	VCCO_1	I/O L34P_1										
I/O L15N_0 GCLK5	GND	I/O L09P_0	INPUT	I/O L03N_0	VCCAUX	TDO	I/O L33P_1	I/O L32N_1	I/O L32P_1										
INPUT	I/O L12N_0	I/O L09N_0	INPUT	GND	I/O L36N_1 A21	I/O L33N_1	I/O L30N_1 A19	I/O L29N_1 A17	I/O L29P_1 A16										
INPUT VREF_0	INPUT	INPUT	INPUT L39N_1	INPUT L39P_1 VREF_1	I/O L36P_1 A20	I/O L30P_1 A18	I/O L28P_1	GND	I/O L26N_1 A15										
INPUT	INPUT	GND	INPUT L35N_1	INPUT L35P_1	VCCO_1	I/O L28N_1	I/O L25N_1 A13	I/O L25P_1 A12	I/O L26P_1 A14										
GND	VCCINT	INPUT L31N_1	INPUT L31P_1 VREF_1	INPUT L27N_1	INPUT L27P_1	I/O L24P_1	I/O L22N_1 A11	I/O L22P_1 A10	I/O L21N_1 RHCLK7										
VCCINT	GND	VCCAUX	INPUT L23N_1	INPUT L23P_1 VREF_1	I/O L24N_1	GND	I/O L20P_1 RHCLK4	VCCO_1	I/O L21P_1 IRDY1 RHCLK6										
GND	VCCINT	INPUT L19N_1	INPUT L19P_1	I/O L16P_1 A8	I/O L16N_1 A9	I/O L20N_1 RHCLK5	I/O L18N_1 TRDY1 RHCLK3	I/O L18P_1 RHCLK2	GND										
VCCINT	GND	INPUT L15N_1	INPUT L15P_1 VREF_1	INPUT L11N_1 VREF_1	INPUT L11P_1	I/O L14P_1 A6	I/O L14N_1 A7	I/O L17P_1 RHCLK0	I/O L17N_1 RHCLK1										
GND	INPUT VREF_2	GND	INPUT VREF_1	I/O L12P_1 A2	VCCO_1	I/O L12N_1 A3	I/O L13P_1 A4	I/O L13N_1 A5	VCCAUX										
INPUT VREF_2	INPUT	INPUT	INPUT L04P_1	INPUT L04N_1 VREF_1	I/O L07P_1	I/O L07N_1	I/O L10P_1	GND	I/O L10N_1 VREF_1										
VCCO_2	I/O L19N_2	I/O L23N_2	INPUT VREF_2	SUSPEND	I/O L03N_1 A1	I/O L08N_1	I/O L08P_1	I/O L09P_1	I/O L09N_1										
INPUT	I/O L19P_2	I/O L23P_2	I/O L25N_2	I/O L27N_2	GND	I/O L03P_1 A0	I/O L05P_1	VCCO_1	I/O L05N_1										
I/O L18P_2 GCLK2	GND	I/O L22P_2 AWAKE	VCCO_2	I/O L27P_2	I/O L29N_2	I/O L31N_2	I/O L02N_1 LDC0	I/O L06P_1	I/O L06N_1										
I/O L17N_2 GCLK1	I/O L18N_2 GCLK3	I/O L22N_2 DOUT	I/O L25P_2	I/O L26N_2 D1	I/O L29P_2	I/O L31P_2	GND	I/O L02P_1 LDC1	I/O L01N_1 LDC2										
VCCO_2	I/O L20N_2 MOSI CSL_B	I/O L21N_2	I/O L24N_2 D3	GND	I/O L28N_2	VCCO_2	I/O L32P_2 D0 DIN/MISO	DONE	I/O L01P_1 HDC										
I/O L17P_2 GCLK0	I/O L20P_2	I/O L21P_2	I/O L24P_2 INIT_B	I/O L26P_2 D2	I/O L28P_2	I/O L30P_2	I/O L30N_2	I/O L32N_2 CCLK	GND										
Bank 2																			

Right Half of FG400
Package (Top View)

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Table 83: Spartan-3A FG484 Pinout(Continued)

Bank	Pin Name	FG484 Ball	Type
2	VCCO_2	AA18	VCCO
2	VCCO_2	AA5	VCCO
2	VCCO_2	AA9	VCCO
2	VCCO_2	U14	VCCO
2	VCCO_2	U9	VCCO
3	IO_L01N_3	D2	I/O
3	IO_L01P_3	C1	I/O
3	IO_L02N_3	C2	I/O
3	IO_L02P_3	B1	I/O
3	IO_L03N_3	E4	I/O
3	IO_L03P_3	D3	I/O
3	IO_L05N_3	G5	I/O
3	IO_L05P_3	G6	I/O
3	IO_L06N_3	E1	I/O
3	IO_L06P_3	D1	I/O
3	IO_L07N_3	E3	I/O
3	IO_L07P_3	F4	I/O
3	IO_L08N_3	G4	I/O
3	IO_L08P_3	F3	I/O
3	IO_L09N_3	H6	I/O
3	IO_L09P_3	H5	I/O
3	IO_L10N_3	J5	I/O
3	IO_L10P_3	K6	I/O
3	IO_L12N_3	F1	I/O
3	IO_L12P_3	F2	I/O
3	IO_L13N_3	G1	I/O
3	IO_L13P_3	G3	I/O
3	IO_L14N_3	H3	I/O
3	IO_L14P_3	H4	I/O
3	IO_L16N_3	H1	I/O
3	IO_L16P_3	H2	I/O
3	IO_L17N_3/VREF_3	J1	VREF
3	IO_L17P_3	J3	I/O
3	IO_L18N_3	K4	I/O
3	IO_L18P_3	K5	I/O
3	IO_L20N_3	K2	I/O
3	IO_L20P_3	K3	I/O
3	IO_L21N_3/LHCLK1	L3	LHCLK
3	IO_L21P_3/LHCLK0	L5	LHCLK
3	IO_L22N_3/IRDY2/LHCLK3	L1	LHCLK

Table 83: Spartan-3A FG484 Pinout(Continued)

Bank	Pin Name	FG484 Ball	Type
3	IO_L22P_3/LHCLK2	K1	LHCLK
3	IO_L24N_3/LHCLK5	M2	LHCLK
3	IO_L24P_3/LHCLK4	M1	LHCLK
3	IO_L25N_3/LHCLK7	M4	LHCLK
3	IO_L25P_3/TRDY2/LHCLK6	M3	LHCLK
3	IO_L26N_3	N3	I/O
3	IO_L26P_3/VREF_3	N1	VREF
3	IO_L28N_3	P2	I/O
3	IO_L28P_3	P1	I/O
3	IO_L29N_3	P5	I/O
3	IO_L29P_3	P3	I/O
3	IO_L30N_3	N4	I/O
3	IO_L30P_3	M5	I/O
3	IO_L32N_3	R2	I/O
3	IO_L32P_3	R1	I/O
3	IO_L33N_3	R4	I/O
3	IO_L33P_3	R3	I/O
3	IO_L34N_3	T4	I/O
3	IO_L34P_3	R5	I/O
3	IO_L36N_3	T3	I/O
3	IO_L36P_3/VREF_3	T1	VREF
3	IO_L37N_3	U2	I/O
3	IO_L37P_3	U1	I/O
3	IO_L38N_3	V3	I/O
3	IO_L38P_3	V1	I/O
3	IO_L40N_3	U5	I/O
3	IO_L40P_3	T5	I/O
3	IO_L41N_3	U4	I/O
3	IO_L41P_3	U3	I/O
3	IO_L42N_3	W2	I/O
3	IO_L42P_3	W1	I/O
3	IO_L43N_3	W3	I/O
3	IO_L43P_3	V4	I/O
3	IO_L44N_3	Y2	I/O
3	IO_L44P_3	Y1	I/O
3	IO_L45N_3	AA2	I/O
3	IO_L45P_3	AA1	I/O
3	IP_3/VREF_3	J8	VREF
3	IP_3/VREF_3	R6	VREF
3	IP_L04N_3/VREF_3	H7	VREF

User I/Os by Bank

Table 84 and Table 85 indicate how the user-I/O pins are distributed between the four I/O banks on the FG484 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 84: User I/Os Per Bank for the XC3S700A in the FG484 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	92	58	17	1	8	8
Right	1	94	33	15	30	8	8
Bottom	2	92	43	11	21	9	8
Left	3	94	61	17	0	8	8
TOTAL		372	195	60	52	33	32

Table 85: User I/Os Per Bank for the XC3S1400A in the FG484 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	92	58	17	1	8	8
Right	1	94	33	15	30	8	8
Bottom	2	95	43	13	21	10	8
Left	3	94	61	17	0	8	8
TOTAL		375	195	62	52	34	32

Footprint Migration Differences

Table 86 summarizes any footprint and functionality differences between the XC3S700A and the XC3S1400A FPGAs that might affect easy migration between devices available in the FG484 package. There are three such balls. All other pins not listed in Table 86 unconditionally migrate between Spartan-3A devices available in the FG484 package.

The arrows indicate the direction for easy migration.

Table 86: FG484 Footprint Migration Differences

Pin	Bank	XC3S700A	Migration	XC3S1400A
T8	2	N.C.	→	INPUT/VREF
U7	2	N.C.	→	INPUT
U16	2	N.C.	→	INPUT
DIFFERENCES			3	

Legend:

- This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction is possible depending on how the pin is configured for the device on the right.

Bank 0												
12	13	14	15	16	17	18	19	20	21	22		
I/O L18P_0 GCLK6	I/O L16N_0	I/O L13N_0	I/O L12N_0 VREF_0	I/O L12P_0	I/O L10N_0	I/O L05N_0	I/O L06N_0	I/O L03N_0	TCK	GND	A	
GND	I/O L16P_0	VCCO_0	I/O L13P_0	GND	I/O L10P_0	VCCO_0	I/O L06P_0 VREF_0	I/O L03P_0	I/O L45N_1 A23	I/O L45P_1 A22	B	
I/O L17P_0 GCLK4	I/O L15N_0	I/O L09P_0	I/O L11N_0	I/O L08N_0	I/O L07N_0	I/O L05P_0	I/O L02N_0	GND	I/O L44N_1 A21	I/O L44P_1 A20	C	
VCCAUX	I/O L15P_0	GND	I/O L11P_0	I/O L08P_0	I/O L07P_0	I/O L01N_0	I/O L02P_0 VREF_0	I/O L42N_1	I/O L42P_1	I/O L41N_1	D	
I/O L17N_0 GCLK5	I/O L14N_0	I/O L09N_0	I/O L04P_0	INPUT	I/O L01P_0	VCCAUX	TDO	I/O L38P_1	VCCO_1	I/O L41P_1	E	
INPUT	I/O L14P_0	VCCO_0	I/O L04N_0	INPUT	GND	I/O L40N_1	I/O L40P_1	I/O L38N_1	I/O L34N_1 A19	I/O L34P_1 A18	F	
INPUT	INPUT	INPUT	INPUT	INPUT	I/O L46N_1 A25	I/O L46P_1 A24	I/O L36P_1	I/O L36N_1	GND	I/O L30N_1 A15	G	
INPUT VREF_0	INPUT	INPUT	INPUT L47N_1	INPUT L47P_1 VREF_1	INPUT L39P_1	INPUT L39N_1	I/O L37N_1	I/O L33N_1 A17	I/O L33P_1 A16	I/O L30P_1 A14	H	
VCCINT	GND	GND	INPUT L43N_1 VREF_1	INPUT L43P_1	VCCO_1	I/O L37P_1	GND	I/O L29N_1 A13	I/O L29P_1 A12	I/O L26N_1 A11	J	
GND	VCCINT	INPUT L35P_1 VREF_1	INPUT L35N_1	INPUT L31N_1	I/O L32P_1	I/O L32N_1	I/O L25N_1 RHCLK7	I/O L25P_1 IRDY1 RHCLK6	VCCO_1	I/O L26P_1 A10	K	
VCCINT	GND	VCCINT	INPUT L31P_1	INPUT L27N_1	GND	I/O L28P_1	I/O L28N_1	I/O L22N_1 TRDY1 RHCLK3	I/O L22P_1 RHCLK2	I/O L21N_1 RHCLK1	L	Bank 1
GND	VCCINT	GND	INPUT L27P_1 VREF_1	INPUT L23N_1	INPUT L23P_1	I/O L24P_1 RHCLK4	VCCAUX	I/O L24N_1 RHCLK5	GND	I/O L21P_1 RHCLK0	M	
VCCINT	GND	VCCINT	INPUT L16P_1	INPUT L16N_1 VREF_1	I/O L20N_1 A9	I/O L20P_1 A8	I/O L19N_1 A7	I/O L19P_1 A6	I/O L18N_1 A5	I/O L18P_1 A4	N	
INPUT	VCCINT	GND	INPUT L08P_1	INPUT L08N_1	VCCO_1	I/O L17N_1 A3	GND	I/O L15P_1	VCCO_1	I/O L15N_1 VREF_1	P	
INPUT VREF_2	INPUT VREF_2	INPUT VREF_2	INPUT L04P_1	INPUT L04N_1 VREF_1	INPUT L12P_1	INPUT L12N_1 VREF_1	I/O L17P_1 A2	I/O L13P_1	I/O L14P_1	I/O L14N_1	R	
GND	INPUT	INPUT	INPUT VREF_2	INPUT VREF_2	I/O L03P_1 A0	I/O L03N_1 A1	I/O L13N_1	I/O L11P_1	GND	I/O L11N_1	T	
I/O L20N_2 GCLK3	I/O L26N_2 D3	VCCO_2	INPUT	INPUT	GND	SUSPEND	I/O L10N_1	I/O L10P_1	I/O L09N_1	I/O L09P_1	U	
I/O L20P_2 GCLK2	I/O L26P_2 INIT_B	I/O L30P_2	I/O L30N_2	I/O L31N_2	I/O L33N_2	VCCAUX	I/O L06P_1	I/O L06N_1	VCCO_1	I/O L07N_1	V	
I/O L18P_2 GCLK14	I/O L23P_2	GND	I/O L25P_2	I/O L31P_2	I/O L34N_2	I/O L33P_2	I/O L02P_1 LDC1	I/O L02N_1 LDC0	I/O L05N_1	I/O L07P_1	W	
I/O L18N_2 GCLK15	I/O L21N_2	I/O L23N_2	I/O L25N_2	I/O L27N_2	I/O L28N_2 D1	I/O L34P_2	DONE	GND	I/O L01N_1 LDC2	I/O L05P_1	Y	
I/O L19P_2 GCLK0	VCCO_2	I/O L22P_2	I/O L24N_2 DOUT	GND	I/O L28P_2 D2	VCCO_2	I/O L32N_2	I/O L36N_2 CLK	I/O L35N_2	I/O L01P_1 HDC	A A	
I/O L19N_2 GCLK1	I/O L21P_2	I/O L22N_2 MOSI CSI_B	I/O L24P_2 AWAKE	I/O L27P_2	I/O L29P_2	I/O L29N_2	I/O L32P_2	I/O L36P_2 D0 DIN/MISO	I/O L35P_2	GND	A B	

Right Half of FG484
Package (Top View)

Figure 26:

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Table 87: Spartan-3A FG676 Pinout(Continued)

Bank	Pin Name	FG676 Ball	Type
1	IO_L03P_1/A0	AC23	DUAL
1	IO_L04N_1	W21	I/O
1	IO_L04P_1	W20	I/O
1	IO_L05N_1	AC25	I/O
1	IO_L05P_1	AD26	I/O
1	IO_L06N_1	AB26	I/O
1	IO_L06P_1	AC26	I/O
1	IO_L07N_1/VREF_1	AB24	VREF
1	IO_L07P_1	AB23	I/O
1	IO_L08N_1	V19	I/O
1	IO_L08P_1	V18	I/O
1	IO_L09N_1	AA23	I/O
1	IO_L09P_1	AA22	I/O
1	IO_L10N_1	U20	I/O
1	IO_L10P_1	V21	I/O
1	IO_L11N_1	AA25	I/O
1	IO_L11P_1	AA24	I/O
1	IO_L12N_1	U18	I/O
1	IO_L12P_1	U19	I/O
1	IO_L13N_1	Y23	I/O
1	IO_L13P_1	Y22	I/O
1	IO_L14N_1	T20	I/O
1	IO_L14P_1	U21	I/O
1	IO_L15N_1	Y25	I/O
1	IO_L15P_1	Y24	I/O
1	IO_L17N_1	T17	I/O
1	IO_L17P_1	T18	I/O
1	IO_L18N_1	V22	I/O
1	IO_L18P_1	W23	I/O
1	IO_L19N_1	V25	I/O
1	IO_L19P_1	V24	I/O
1	IO_L21N_1	U22	I/O
1	IO_L21P_1	V23	I/O
1	IO_L22N_1	R20	I/O
1	IO_L22P_1	R19	I/O
1	IO_L23N_1/VREF_1	U24	VREF
1	IO_L23P_1	U23	I/O
1	IO_L25N_1/A3	R22	DUAL
1	IO_L25P_1/A2	R21	DUAL
1	IO_L26N_1/A5	T24	DUAL

Table 87: Spartan-3A FG676 Pinout(Continued)

Bank	Pin Name	FG676 Ball	Type
1	IO_L26P_1/A4	T23	DUAL
1	IO_L27N_1/A7	R17	DUAL
1	IO_L27P_1/A6	R18	DUAL
1	IO_L29N_1/A9	R26	DUAL
1	IO_L29P_1/A8	R25	DUAL
1	IO_L30N_1/RHCLK1	P20	RHCLK
1	IO_L30P_1/RHCLK0	P21	RHCLK
1	IO_L31N_1/TRDY1/RHCLK3	P25	RHCLK
1	IO_L31P_1/RHCLK2	P26	RHCLK
1	IO_L33N_1/RHCLK5	N24	RHCLK
1	IO_L33P_1/RHCLK4	P23	RHCLK
1	IO_L34N_1/RHCLK7	N19	RHCLK
1	IO_L34P_1/IRDY1/RHCLK6	P18	RHCLK
1	IO_L35N_1/A11	M25	DUAL
1	IO_L35P_1/A10	M26	DUAL
1	IO_L37N_1	N21	I/O
1	IO_L37P_1	P22	I/O
1	IO_L38N_1/A13	M23	DUAL
1	IO_L38P_1/A12	L24	DUAL
1	IO_L39N_1/A15	N17	DUAL
1	IO_L39P_1/A14	N18	DUAL
1	IO_L41N_1	K26	I/O
1	IO_L41P_1	K25	I/O
1	IO_L42N_1/A17	M20	DUAL
1	IO_L42P_1/A16	N20	DUAL
1	IO_L43N_1/A19	J25	DUAL
1	IO_L43P_1/A18	J26	DUAL
1	IO_L45N_1	M22	I/O
1	IO_L45P_1	M21	I/O
1	IO_L46N_1	K22	I/O
1	IO_L46P_1	K23	I/O
1	IO_L47N_1	M18	I/O
1	IO_L47P_1	M19	I/O
1	IO_L49N_1	J22	I/O
1	IO_L49P_1	J23	I/O
1	IO_L50N_1	K21	I/O
1	IO_L50P_1	L22	I/O
1	IO_L51N_1	G24	I/O
1	IO_L51P_1	G23	I/O
1	IO_L53N_1	K20	I/O

Table 87: Spartan-3A FG676 Pinout(Continued)

Bank	Pin Name	FG676 Ball	Type
1	IO_L53P_1	L20	I/O
1	IO_L54N_1	F24	I/O
1	IO_L54P_1	F25	I/O
1	IO_L55N_1	L17	I/O
1	IO_L55P_1	L18	I/O
1	IO_L56N_1	F23	I/O
1	IO_L56P_1	E24	I/O
1	IO_L57N_1	K18	I/O
1	IO_L57P_1	K19	I/O
1	IO_L58N_1	G22	I/O
1	IO_L58P_1/VREF_1	F22	VREF
1	IO_L59N_1	J20	I/O
1	IO_L59P_1	J19	I/O
1	IO_L60N_1	D26	I/O
1	IO_L60P_1	E26	I/O
1	IO_L61N_1	D24	I/O
1	IO_L61P_1	D25	I/O
1	IO_L62N_1/A21	H21	DUAL
1	IO_L62P_1/A20	J21	DUAL
1	IO_L63N_1/A23	C25	DUAL
1	IO_L63P_1/A22	C26	DUAL
1	IO_L64N_1/A25	G21	DUAL
1	IO_L64P_1/A24	H20	DUAL
1	IP_L16N_1	Y26	INPUT
1	IP_L16P_1	W25	INPUT
1	IP_L20N_1/VREF_1	V26	VREF
1	IP_L20P_1	W26	INPUT
1	IP_L24N_1/VREF_1	U26	VREF
1	IP_L24P_1	U25	INPUT
1	IP_L28N_1	R24	INPUT
1	IP_L28P_1/VREF_1	R23	VREF
1	IP_L32N_1	N25	INPUT
1	IP_L32P_1	N26	INPUT
1	IP_L36N_1	N23	INPUT
1	IP_L36P_1/VREF_1	M24	VREF
1	IP_L40N_1	L23	INPUT
1	IP_L40P_1	K24	INPUT
1	IP_L44N_1	H25	INPUT
1	IP_L44P_1/VREF_1	H26	VREF
1	IP_L48N_1	H24	INPUT

Table 87: Spartan-3A FG676 Pinout(Continued)

Bank	Pin Name	FG676 Ball	Type
1	IP_L48P_1	H23	INPUT
1	IP_L52N_1/VREF_1	G25	VREF
1	IP_L52P_1	G26	INPUT
1	IP_L65N_1	B25	INPUT
1	IP_L65P_1/VREF_1	B26	VREF
1	VCCO_1	AB25	VCCO
1	VCCO_1	E25	VCCO
1	VCCO_1	H22	VCCO
1	VCCO_1	L19	VCCO
1	VCCO_1	L25	VCCO
1	VCCO_1	N22	VCCO
1	VCCO_1	T19	VCCO
1	VCCO_1	T25	VCCO
1	VCCO_1	W22	VCCO
2	IO_L01N_2/M0	AD4	DUAL
2	IO_L01P_2/M1	AC4	DUAL
2	IO_L02N_2/CSO_B	AA7	DUAL
2	IO_L02P_2/M2	Y7	DUAL
2	IO_L05N_2	Y9	I/O
2	IO_L05P_2	W9	I/O
2	IO_L06N_2	AF3	I/O
2	IO_L06P_2	AE3	I/O
2	IO_L07N_2	AF4	I/O
2	IO_L07P_2	AE4	I/O
2	IO_L08N_2	AD6	I/O
2	IO_L08P_2	AC6	I/O
2	IO_L09N_2	W10	I/O
2	IO_L09P_2	V10	I/O
2	IO_L10N_2	AE6	I/O
2	IO_L10P_2	AF5	I/O
2	IO_L11N_2	AE7	I/O
2	IO_L11P_2	AD7	I/O
2	IO_L12N_2	AA10	I/O
2	IO_L12P_2	Y10	I/O
2	IO_L13N_2	U11	I/O
2	IO_L13P_2	V11	I/O
2	IO_L14N_2	AB7	I/O
2	IO_L14P_2	AC8	I/O
2	IO_L15N_2	AC9	I/O
2	IO_L15P_2	AB9	I/O