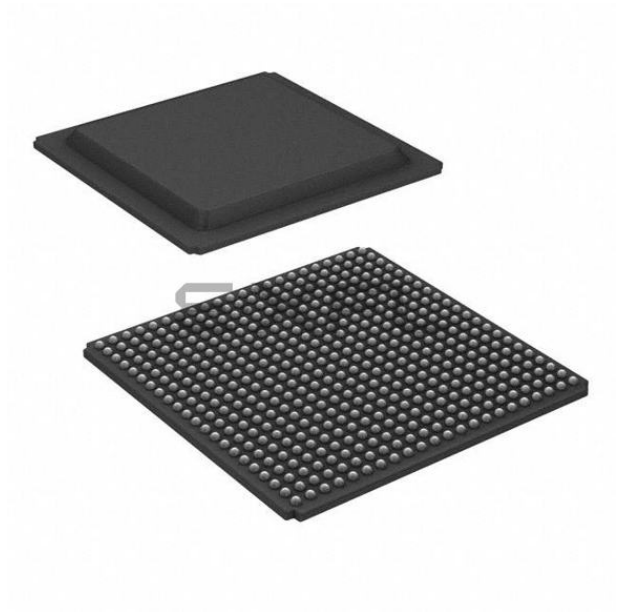
AMD Xilinx - XC3S700A-5FGG484C Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1472
Number of Logic Elements/Cells	13248
Total RAM Bits	368640
Number of I/O	372
Number of Gates	700000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s700a-5fgg484c

Production Status

Table 3 indicates the production status of each Spartan-3A FPGA by temperature range and speed grade. The table also lists the earliest speed file version required for creating a production configuration bitstream. Later versions are also supported.

Table 3: **Spartan-3A FPGA Production Status (Production Speed File)**

Temperature Range		Commercial (C)		Industrial
Speed Grade		Standard (–4)	High-Performance (–5)	Standard (–4)
Part Number	XC3S50A	**Production** (v1.35)	**Production** (v1.35)	**Production** (v1.35)
	XC3S200A	**Production** (v1.35)	**Production** (v1.35)	**Production** (v1.35)
	XC3S400A	**Production** (v1.36)	**Production** (v1.36)	**Production** (v1.36)
	XC3S700A	**Production** (v1.34)	**Production** (v1.35)	**Production** (v1.34)
	XC3S1400A	**Production** (v1.34)	**Production** (v1.35)	**Production** (v1.34)

Package Marking

Figure 2 provides a top marking example for Spartan-3A FPGAs in the quad-flat packages. Figure 3 shows the top marking for Spartan-3A FPGAs in BGA packages. The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator.

The "5C" and "4I" Speed Grade/Temperature Range part combinations may be dual marked as "5C/4I". Devices with a single mark are only guaranteed for the marked speed grade and temperature range.

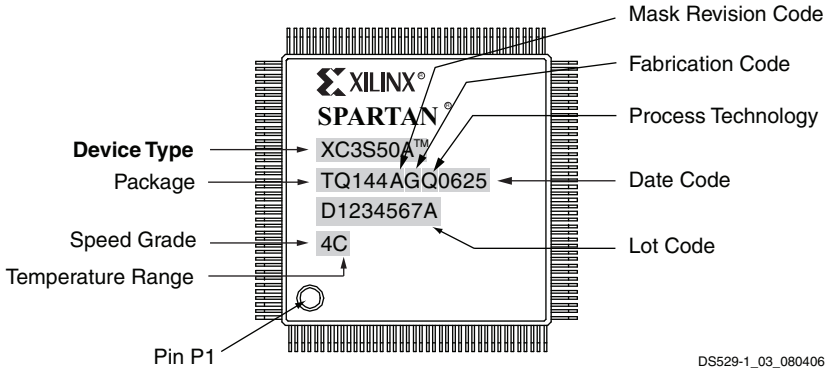


Figure 2: **Spartan-3A QFP Package Marking Example**

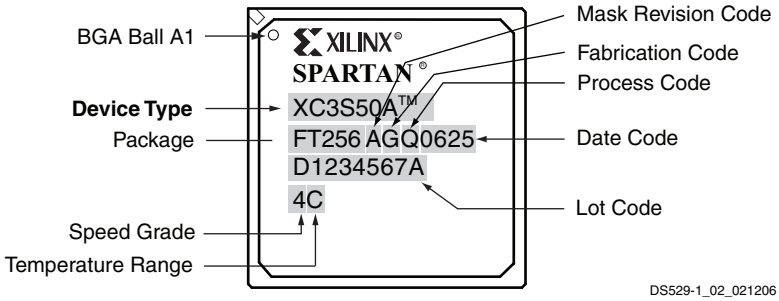


Figure 3: **Spartan-3A BGA Package Marking Example**

Related Product Families

The Spartan-3AN nonvolatile FPGA family is architecturally identical to the Spartan-3A FPGA family, except that it has in-system flash memory and is offered in select pin-compatible package options.

- **DS557: Spartan-3AN Family Data Sheet**
  www.xilinx.com/support/documentation/data_sheets/ds557.pdf

The compatible Spartan-3A DSP FPGA family replaces the 18-bit multiplier with the DSP48A block, while also increasing the block RAM capability and quantity. The two members of the Spartan-3A DSP FPGA family extend the Spartan-3A density range up to 37,440 and 53,712 logic cells.

- **DS610: Spartan-3A DSP FPGA Family Data Sheet**
  www.xilinx.com/support/documentation/data_sheets/ds610.pdf
- **UG431: XtremeDSP DSP48A for Spartan-3A DSP FPGAs**
  www.xilinx.com/support/documentation/user_guides/ug431.pdf

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/05/06	1.0	Initial release.
02/02/07	1.1	Promoted to Preliminary status.
03/16/07	1.2	Added cross-reference to nonvolatile Spartan-3AN FPGA family.
04/23/07	1.3	Added cross-reference to compatible Spartan-3A DSP family.
07/10/07	1.4	Updated Starter Kit reference to new UG334.
04/15/08	1.6	Updated trademarks.
05/28/08	1.7	Added reference to XA Automotive version.
03/06/09	1.8	Added link to DS706 on Extended Spartan-3A family.
08/19/10	2.0	Updated link to sign up for Alerts.

General Recommended Operating Conditions

Table 8: **General Recommended Operating Conditions**

Symbol	Description			Min	Nominal	Max	Units
T_J	Junction temperature	Commercial		0	–	85	°C
		Industrial		–40	–	100	°C
V_{CCINT}	Internal supply voltage			1.14	1.20	1.26	V
V_{CCO} (1)	Output driver supply voltage			1.10	–	3.60	V
V_{CCAUX}	Auxiliary supply voltage(2)	V_{CCAUX} = 2.5		2.25	2.50	2.75	V
		V_{CCAUX} = 3.3		3.00	3.30	3.60	V
V_{IN}	Input voltage(3)	PCI IOSTANDARD		–0.5	–	V_{CCO}+0.5	V
		All other IOSTANDARDs	IP or IO_#	–0.5	–	4.10	V
			IO_Lxxy_#(4)	–0.5	–	4.10	V
T_{IN}	Input signal transition time(5)			–	–	500	ns

Notes:

1. This V_{CCO} range spans the lowest and highest operating voltages for all supported I/O standards. Table 11 lists the recommended V_{CCO} range specific to each of the single-ended I/O standards, and Table 13 lists that specific to the differential standards.
2. Define V_{CCAUX} selection using CONFIG VCCAUX constraint.
3. See XAPP459, "Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins."
4. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in UG331, *Spartan-3 Generation FPGA User Guide*.
5. Measured between 10% and 90% V_{CCO}. Follow Signal Integrity recommendations.

Single-Ended I/O Standards

Table 11: **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers(2)			V_{REF}			V_{IL}	V_{IH}
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
LVTTL	3.0	3.3	3.6	V_{REF} is not used for these I/O standards			0.8	2.0
LVCMOS33(4)	3.0	3.3	3.6				0.8	2.0
LVCMOS25(4,5)	2.3	2.5	2.7				0.7	1.7
LVCMOS18	1.65	1.8	1.95				0.4	0.8
LVCMOS15	1.4	1.5	1.6				0.4	0.8
LVCMOS12	1.1	1.2	1.3				0.4	0.7
PCI33_3(6)	3.0	3.3	3.6				0.3 • V_{CCO}	0.5 • V_{CCO}
PCI66_3(6)	3.0	3.3	3.6				0.3 • V_{CCO}	0.5 • V_{CCO}
HSTL_I	1.4	1.5	1.6	0.68	0.75	0.9	V_{REF} – 0.1	V_{REF} + 0.1
HSTL_III	1.4	1.5	1.6	–	0.9	-	V_{REF} – 0.1	V_{REF} + 0.1
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1	V_{REF} – 0.1	V_{REF} + 0.1
HSTL_II_18	1.7	1.8	1.9	–	0.9	–	V_{REF} – 0.1	V_{REF} + 0.1
HSTL_III_18	1.7	1.8	1.9	–	1.1	–	V_{REF} – 0.1	V_{REF} + 0.1
SSTL18_I	1.7	1.8	1.9	0.833	0.900	0.969	V_{REF} – 0.125	V_{REF} + 0.125
SSTL18_II	1.7	1.8	1.9	0.833	0.900	0.969	V_{REF} – 0.125	V_{REF} + 0.125
SSTL2_I	2.3	2.5	2.7	1.13	1.25	1.38	V_{REF} – 0.150	V_{REF} + 0.150
SSTL2_II	2.3	2.5	2.7	1.13	1.25	1.38	V_{REF} – 0.150	V_{REF} + 0.150
SSTL3_I	3.0	3.3	3.6	1.3	1.5	1.7	V_{REF} – 0.2	V_{REF} + 0.2
SSTL3_II	3.0	3.3	3.6	1.3	1.5	1.7	V_{REF} – 0.2	V_{REF} + 0.2

Notes:

1. Descriptions of the symbols used in this table are as follows:
   V_{CCO} – the supply voltage for output drivers
   V_{REF} – the reference voltage for setting the input switching threshold
   V_{IL} – the input voltage that indicates a Low logic level
   V_{IH} – the input voltage that indicates a High logic level
2. In general, the V_{CCO} rails supply only output drivers, not input circuits. The exceptions are for LVCMOS25 inputs when V_{CCAUX} = 3.3V range and for PCI I/O standards.
3. For device operation, the maximum signal voltage (V_{IH} max) can be as high as V_{IN} max. See Table 8.
4. There is approximately 100 mV of hysteresis on inputs using LVCMOS33 and LVCMOS25 I/O standards.
5. All Dedicated pins (PROG_B, DONE, SUSPEND, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail and use the LVCMOS25 or LVCMOS33 standard depending on V_{CCAUX}. The dual-purpose configuration pins use the LVCMOS standard before the User mode. When using these pins as part of a standard 2.5V configuration interface, apply 2.5V to the V_{CCO} lines of Banks 0, 1, and 2 at power-on as well as throughout configuration.
6. For information on PCI IP solutions, see www.xilinx.com/pci. The PCI IOSTANDARD is not supported on input-only pins. The PCIX IOSTANDARD is available and has equivalent characteristics but no PCI-X IP is supported.

Differential Output Pairs

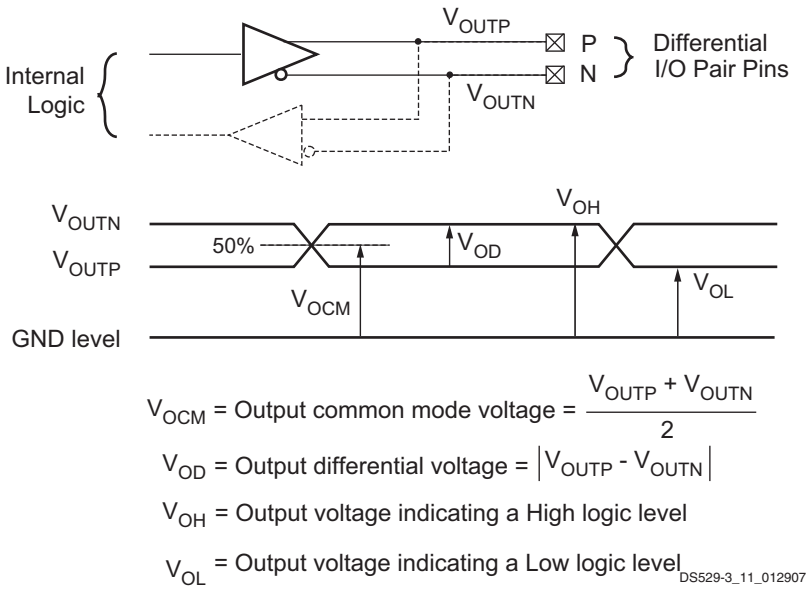


Figure 5: **Differential Output Voltages**

Table 14: **DC Characteristics of User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{OD}			V_{OCM}			V_{OH}	V_{OL}
	Min (mV)	Typ (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (V)	Max (V)
LVDS_25	247	350	454	1.125	–	1.375	–	–
LVDS_33	247	350	454	1.125	–	1.375	–	–
BLVDS_25	240	350	460	–	1.30	–	–	–
MINI_LVDS_25	300	–	600	1.0	–	1.4	–	–
MINI_LVDS_33	300	–	600	1.0	–	1.4	–	–
RSDS_25	100	–	400	1.0	–	1.4	–	–
RSDS_33	100	–	400	1.0	–	1.4	–	–
TMDS_33	400	–	800	V_{CCO} – 0.405	–	V_{CCO} – 0.190	–	–
PPDS_25	100	–	400	0.5	0.8	1.4	–	–
PPDS_33	100	–	400	0.5	0.8	1.4	–	–
DIFF_HSTL_I_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_II_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_I	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_SSTL18_I	–	–	–	–	–	–	V_{TT} + 0.475	V_{TT} – 0.475
DIFF_SSTL18_II	–	–	–	–	–	–	V_{TT} + 0.603	V_{TT} – 0.603
DIFF_SSTL2_I	–	–	–	–	–	–	V_{TT} + 0.61	V_{TT} – 0.61
DIFF_SSTL2_II	–	–	–	–	–	–	V_{TT} + 0.81	V_{TT} – 0.81
DIFF_SSTL3_I	–	–	–	–	–	–	V_{TT} + 0.6	V_{TT} – 0.6
DIFF_SSTL3_II	–	–	–	–	–	–	V_{TT} + 0.8	V_{TT} – 0.8

Notes:

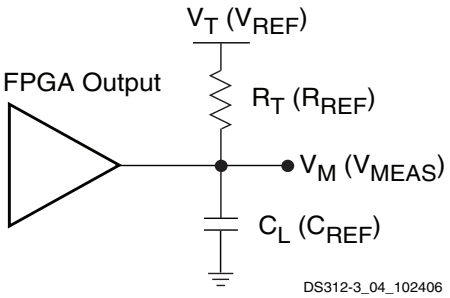
1. The numbers in this table are based on the conditions set forth in Table 8 and Table 13.
2. See "External Termination Requirements for Differential I/O," page 20.
3. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair.
4. At any given time, no more than two of the following differential output standards can be assigned to an I/O bank: LVDS_25, RSDS_25, MINI_LVDS_25, PPDS_25 when V_{CCO}=2.5V, or LVDS_33, RSDS_33, MINI_LVDS_33, TMDS_33, PPDS_33 when V_{CCO} = 3.3V

Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 27 lists the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H.

The Output test setup is shown in Figure 9. A termination voltage V_T is applied to the termination resistor R_T, the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (for example, LVCMOS, LVTTL), then R_T is set to 1MΩ to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



Notes:

1. The names shown in parentheses are used in the IBIS file.

Figure 9: **Output Test Setup**

Table 27: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended							
LVTTL		-	0	3.3	1M	0	1.4
LVCMOS33		-	0	3.3	1M	0	1.65
LVCMOS25		-	0	2.5	1M	0	1.25
LVCMOS18		-	0	1.8	1M	0	0.9
LVCMOS15		-	0	1.5	1M	0	0.75
LVCMOS12		-	0	1.2	1M	0	0.6
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
PCI66_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
HSTL_I		0.75	V_{REF} – 0.5	V_{REF} + 0.5	50	0.75	V_{REF}
HSTL_III		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	1.5	V_{REF}
HSTL_I_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_II_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL18_II		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
SSTL2_II		1.25	V_{REF} – 0.75	V_{REF} + 0.75	25	1.25	V_{REF}
SSTL3_I		1.5	V_{REF} – 0.75	V_{REF} + 0.75	50	1.5	V_{REF}
SSTL3_II		1.5	V_{REF} – 0.75	V_{REF} + 0.75	25	1.5	V_{REF}

Digital Clock Manager (DCM) Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables (Table 36 and Table 37) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables (Table 38 through Table 41) supersede any corresponding ones in the DLL tables. DLL specifications that do not change with the addition of DFS or PS functions are presented in Table 36 and Table 37.

Period jitter and cycle-cycle jitter are two of many different ways of specifying clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the ideal clock period over a collection of millions of samples. In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

Spread Spectrum

DCMs accept typical spread spectrum clocks as long as they meet the input requirements. The DLL will track the frequency changes created by the spread spectrum clock to drive the global clocks to the FPGA logic. See XAPP469, *Spread-Spectrum Clocking Reception for Displays* for details.

Delay-Locked Loop (DLL)

Table 36: **Recommended Operating Conditions for the DLL**

Symbol		Description		Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges								
F_{CLKIN}	CLKIN_FREQ_DLL	Frequency of the CLKIN clock input		5(2)	280(3)	5(2)	250(3)	MHz
Input Pulse Requirements								
CLKIN_PULSE		CLKIN pulse width as a percentage of the CLKIN period	$F_{CLKIN} \leq 150$ MHz	40%	60%	40%	60%	–
			$F_{CLKIN} > 150$ MHz	45%	55%	45%	55%	–
Input Clock Jitter Tolerance and Delay Path Variation(4)								
CLKIN_CYC_JITT_DLL_LF		Cycle-to-cycle jitter at the CLKIN input	$F_{CLKIN} \leq 150$ MHz	–	±300	–	±300	ps
CLKIN_CYC_JITT_DLL_HF			$F_{CLKIN} > 150$ MHz	–	±150	–	±150	ps
CLKIN_PER_JITT_DLL		Period jitter at the CLKIN input		–	±1	–	±1	ns
CLKFB_DELAY_VAR_EXT		Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input		–	±1	–	±1	ns

Notes:

1. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
2. The DFS, when operating independently of the DLL, supports lower FCLKIN frequencies. See Table 38.
3. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM. The CLK2X output reproduces the clock frequency provided on the CLKIN input.
4. CLKIN input jitter beyond these limits might cause the DCM to lose lock.
5. The DCM specifications are guaranteed when both adjacent DCMs are locked.

Phase Shifter (PS)

Table 40: **Recommended Operating Conditions for the PS in Variable Phase Mode**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Operating Frequency Ranges						
PSCLK_FREQ (F_{PSCLK})	Frequency for the PSCLK input	1	167	1	167	MHz
Input Pulse Requirements						
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	40%	60%	40%	60%	-

Table 41: **Switching Characteristics for the PS in Variable Phase Mode**

Symbol	Description		Phase Shift Amount	Units
Phase Shifting Range				
MAX_STEPS(2)	Maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. If using CLKIN_DIVIDE_BY_2 = TRUE, double the clock effective clock period.	CLKIN < 60 MHz	±[INTEGER(10 • (T_{CLKIN} – 3 ns))]	steps
		CLKIN ≥ 60 MHz	±[INTEGER(15 • (T_{CLKIN} – 3 ns))]	
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting		±[MAX_STEPS • DCM_DELAY_STEP_MIN]	ns
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting		±[MAX_STEPS • DCM_DELAY_STEP_MAX]	ns

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 8 and Table 40.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM is has no initial fixed phase shifting, that is, the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the bottom of Table 37.

Table 53: **Configuration Timing Requirements for Attached SPI Serial Flash**

Symbol	Description	Requirement	Units
T_{CCS}	SPI serial Flash PROM chip-select time	$T_{CCS} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DSU}	SPI serial Flash PROM data input setup time	$T_{DSU} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DH}	SPI serial Flash PROM data input hold time	$T_{DH} \leq T_{MCCH1}$	ns
T_V	SPI serial Flash PROM data clock-to-output time	$T_V \leq T_{MCCLn} - T_{DCC}$	ns
f_C or f_R	Maximum SPI serial Flash PROM clock frequency (also depends on specific read command used)	$f_C \geq \frac{1}{T_{CCLKn(min)}}$	MHz

Notes:

1. These requirements are for successful FPGA configuration in SPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/05/06	1.0	Initial release.
02/02/07	1.1	Promoted to Preliminary status. Moved Table 15 to under "DC Electrical Characteristics" section. Updated all timing specifications for the v1.32 speed files. Added recommended Simultaneous Switching Output (SSO) limits in Table 29. Set a 10 µs maximum pulse width for the DNA_PORT READ signal and the JTAG clock input during the ISC_DNA command, affecting both Table 43 and Table 56. Described "External Termination Requirements for Differential I/O." Added separate DIN hold time for Slave mode in Table 50. Corrected wording in Table 52 and Table 54; no specifications affected.
03/16/07	1.2	Updated all AC timing specifications to the v1.34 speeds file. Promoted the XC3S700A and XC3S1400A FPGAs offered in the -4 speed grade to Production status, as shown in Table 16. Added Note 2 to Table 39 regarding the extra logic (one LUT) automatically added by ISE 9.1i and later software revisions for any DCM application that leverages the Digital Frequency Synthesizer (DFS). Separated some JTAG specifications by array size or function, as shown in Table 56. Updated quiescent current limits in Table 10.
04/23/07	1.3	Updated all AC timing specifications to the v1.35 speeds file. Promoted all devices except the XC3S400A to Production status, as shown in Table 16.
05/08/07	1.4	Updated XC3S400A to Production and v1.36 speeds file. Added banking rules and other explanatory footnotes to Table 12 and Table 13. Corrected DIFF_SSTL3_II V_{OL} Max in Table 14. Improved XC3S400A Pin-to-Pin Clock-to-Output times in Table 18. Updated XC3S400A Pin-to-Pin Setup Times in Table 19. Updated TIOICKPD for -5 in Table 20. Added SSO numbers to Table 28 and Table 29. Removed invalid Embedded Multiplier Hold Times in Table 34. Improved CLKOUT_FREQ_CLK90 in Table 37. Improved T_{TDITCK} and F_{TCK} performance for XC3S400A in Table 56.
07/10/07	1.5	Added DIFF_HSTL_I and DIFF_HSTL_III to Table 13, Table 14, Table 27, and Table 29. Updated TMDS DC characteristics in Table 14. Updated for speed file v1.37 in ISE 9.2.01i as shown in Table 17. Updated pin-to-pin setup and hold times in Table 19. Updated TMDS output adjustment in Table 26. Updated I/O Test Method values in Table 27. Added BLVDS SSO numbers inTable 29. For Multiplier block, updated setup times and added hold times to Table 34. Updated block RAM clock width in Table 35. Updated CLKOUT_PER_JITT_2X and CLKOUT_PER_JITT_DV2 in Table 37. Added CCLK specifications for Commercial in Table 46 through Table 48.
04/15/08	1.6	Added V_{IN} to Recommended Operating Conditions in Table 8 and added reference to XAPP459, "Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins." Reduced typical I_{CCINTQ} and I_{CCAUXQ} quiescent current values by 12%-58% in Table 10. Increased V_{IL} max to 0.4V for LVCMOS12/15/18 and improved V_{IH} min to 0.7V for LVCMOS12 in Table 11. Changed V_{OL} max to 0.4V and V_{OH} min to V_{CCO}-0.4V for LVCMOS15/18 in Table 12. Noted latest speed file v1.39 in ISE 10.1 software in Table 16. Added new packages to SSO limits in Table 28 and Table 29. Improved SSTL18_II SSO limit for FG packages in Table 29. Improved F_{BUFG} for -4 to 334 MHz in Table 33. Added references to 375 MHz performance via SCD 4103 in Table 33,Table 38, Table 39, and Table 40. Restored Units column to Table 44. Updated CCLK output maximum period in Table 46 to match minimum frequency in Table 47. Corrected BPI active clock edge in Figure 15 and Table 54.
05/28/08	1.7	Improved V_{CCAUXT} and V_{CCO2T} POR minimum in Table 5 and updated V_{CCO} POR levels in Figure 11. Clarified recommended V_{IN} in Table 8. Added reference to V_{CCAUX} in "Simultaneously Switching Output Guidelines". Added reference to Sample Window in Table 21. Removed DNA_RETENTION limit of 10 years in Table 15 since number of Read cycles is the only unique limit. Added references to UG332.
03/06/09	1.8	Changed typical quiescent current temperature from ambient to junction. Updated BPI configuration waveforms in Figure 15 and updated Table 55. Updated selected I/O standard DC characteristics. Added TIOPI and TIOPID in Table 22. Removed references to SCD 4103.
08/19/10	2.0	Added I_{IK} to Table 4. Updated V_{IN} in Table 8 and footnoted I_L in Table 9 to note potential leakage between pins of a differential pair. Clarified LVPECL notes to Table 13. Corrected symbols for TSUSPEND_GTS and TSUSPEND_GWE in Table 44.

Table 59: **Maximum User I/O by Package**

Device	Package	Maximum User I/Os and Input-Only	Maximum Input-Only	Maximum Differential Pairs	All Possible I/Os by Type					
					I/O	INPUT	DUAL	VREF	CLK	N.C.
XC3S50A	VQ100	68	6	60	17	2	20	6	23	0
XC3S200A		68	6	60	17	2	20	6	23	0
XC3S50A	TQ144	108	7	50	42	2	26	8	30	0
XC3S50A	FT256	144	32	64	53	20	26	15	30	51
XC3S200A		195	35	90	69	21	52	21	32	0
XC3S400A		195	35	90	69	21	52	21	32	0
XC3S700A		161	13	60	59	2	52	18	30	0
XC3S1400A		161	13	60	59	2	52	18	30	0
XC3S200A	FG320	248	56	112	101	40	52	23	32	3
XC3S400A		251	59	112	101	42	52	24	32	0
XC3S400A	FG400	311	63	142	155	46	52	26	32	0
XC3S700A		311	63	142	155	46	52	26	32	0
XC3S700A	FG484	372	84	165	194	61	52	33	32	3
XC3S1400A		375	87	165	195	62	52	34	32	0
XC3S1400A	FG676	502	94	227	313	67	52	38	32	17

Notes:

1. Some VREFs are on INPUT pins. See pinout tables for details.

Electronic versions of the package pinout tables and footprints are available for download from the Xilinx website. Using a spreadsheet program, the data can be sorted and reformatted according to any specific needs. Similarly, the ASCII-text file is easily parsed by most scripting programs.

http://www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip

User I/Os by Bank

Table 67 indicates how the 108 available user-I/O pins are distributed between the four I/O banks on the TQ144 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 67: **User I/Os Per Bank for the XC3S50A in the TQ144 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	27	14	1	1	3	8
Right	1	25	11	0	4	2	8
Bottom	2	30	2	0	21	1	6
Left	3	26	15	1	0	2	8
TOTAL		**108**	**42**	**2**	**26**	**8**	**30**

Footprint Migration Differences

The XC3S50A FPGA is the only Spartan-3A device offered in the TQ144 package.

TQ144 Footprint

Note pin 1 indicator in top-left corner and logo orientation.

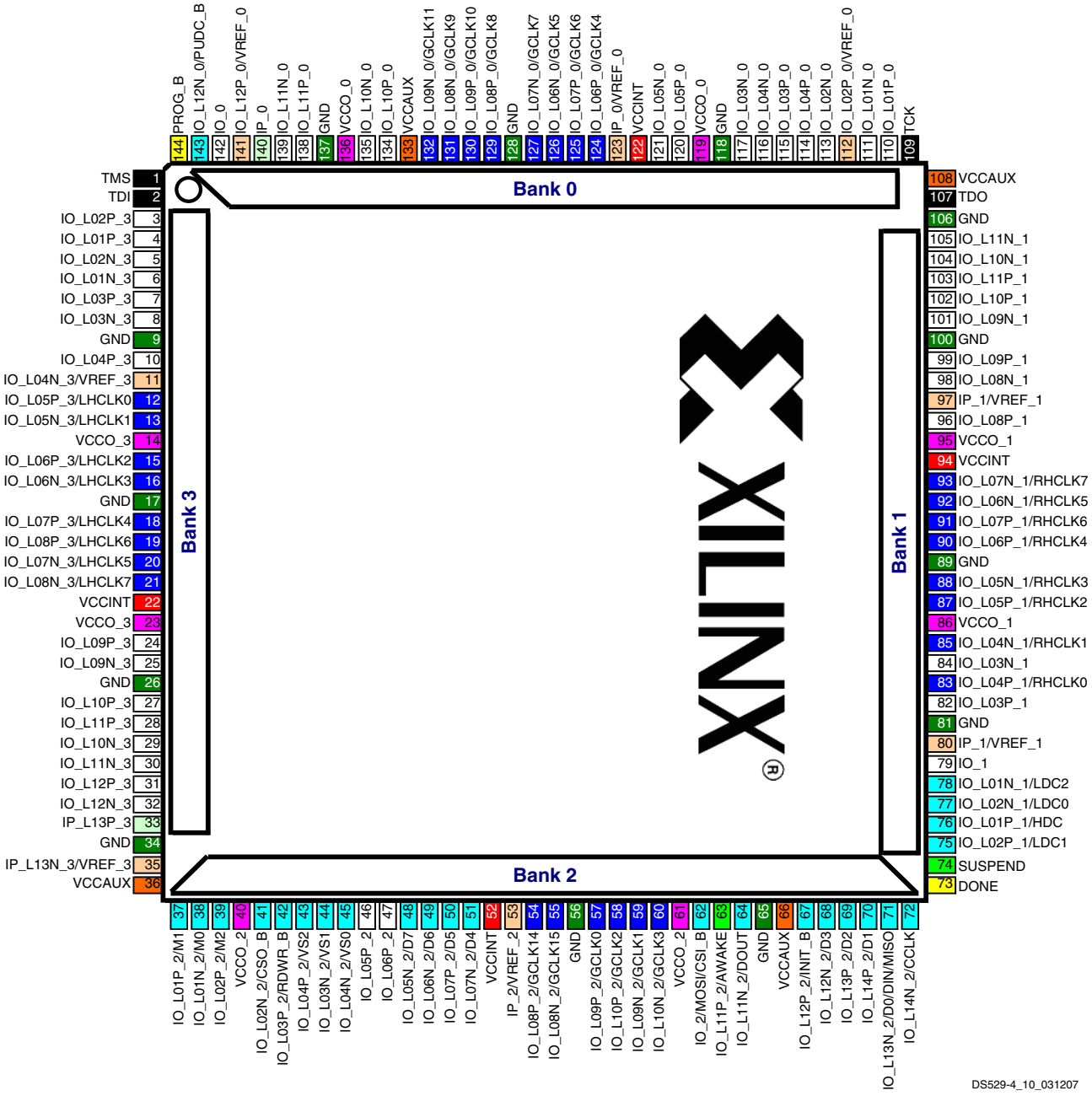


Figure 19: **TQ144 Package Footprint (Top View)**

42	**I/O:** Unrestricted, general-purpose user I/O	25	**DUAL:** Configuration pins, then possible user I/O	8	**VREF:** User I/O or input voltage reference for bank
2	**INPUT:** Unrestricted, general-purpose input pin	30	**CLK:** User I/O, input, or global buffer input	8	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core supply voltage (+1.2V)
0	**N.C.:** Not connected	13	**GND:** Ground	4	**VCCAUX:** Auxiliary supply voltage
2	**SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins				

Table 68: **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400) *(Continued)***

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
2	IO_L01N_2/M0	IO_L01N_2/M0	P4	DUAL
2	IO_L01P_2/M1	IO_L01P_2/M1	N4	DUAL
2	IO_L02N_2/ CSO_B	IO_L02N_2/ CSO_B	T2	DUAL
2	IO_L02P_2/M2	IO_L02P_2/M2	R2	DUAL
2	IO_L04P_2/VS2	IO_L03N_2/VS2	T3	DUAL
2	IO_L03P_2/ RDWR_B	IO_L03P_2/ RDWR_B	R3	DUAL
2	IO_L04N_2/VS0	IO_L04N_2/VS0	P5	DUAL
2	IO_L03N_2/VS1	IO_L04P_2/VS1	N6	DUAL
2	IO_L06P_2	IO_L05N_2	R5	I/O
2	IO_L05P_2	IO_L05P_2	T4	I/O
2	IO_L06N_2/D6	IO_L06N_2/D6	T6	DUAL
2	IO_L05N_2/D7	IO_L06P_2/D7	T5	DUAL
2	N.C. (◆)	IO_L07N_2	P6	I/O
2	N.C. (◆)	IO_L07P_2	N7	I/O
2	IO_L08N_2/D4	IO_L08N_2/D4	N8	DUAL
2	IO_L08P_2/D5	IO_L08P_2/D5	P7	DUAL
2	N.C. (◆)	IO_L09N_2/ GCLK13	T7	GCLK
2	N.C. (◆)	IO_L09P_2/ GCLK12	R7	GCLK
2	IO_L10N_2/ GCLK15	IO_L10N_2/ GCLK15	T8	GCLK
2	IO_L10P_2/ GCLK14	IO_L10P_2/ GCLK14	P8	GCLK
2	IO_L11N_2/ GCLK1	IO_L11N_2/ GCLK1	P9	GCLK
2	IO_L11P_2/ GCLK0	IO_L11P_2/ GCLK0	N9	GCLK
2	IO_L12N_2/ GCLK3	IO_L12N_2/ GCLK3	T9	GCLK
2	IO_L12P_2/ GCLK2	IO_L12P_2/ GCLK2	R9	GCLK
2	N.C. (◆)	IO_L13N_2	M10	I/O
2	N.C. (◆)	IO_L13P_2	N10	I/O
2	IO_L14P_2/ MOSI/CSI_B	IO_L14N_2/ MOSI/CSI_B	P10	DUAL
2	IO_L14N_2	IO_L14P_2	T10	I/O
2	IO_L15N_2/ DOUT	IO_L15N_2/ DOUT	R11	DUAL
2	IO_L15P_2/ AWAKE	IO_L15P_2/ AWAKE	T11	PWR MGMT
2	IO_L16N_2	IO_L16N_2	N11	I/O
2	IO_L16P_2	IO_L16P_2	P11	I/O
2	IO_L17N_2/D3	IO_L17N_2/D3	P12	DUAL
2	IO_L17P_2/ INIT_B	IO_L17P_2/ INIT_B	T12	DUAL

Table 68: **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400) *(Continued)***

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
2	IO_L20P_2/D1	IO_L18N_2/D1	R13	DUAL
2	IO_L18P_2/D2	IO_L18P_2/D2	T13	DUAL
2	N.C. (◆)	IO_L19N_2	P13	I/O
2	N.C. (◆)	IO_L19P_2	N12	I/O
2	IO_L20N_2/ CCLK	IO_L20N_2/ CCLK	R14	DUAL
2	IO_L18N_2/D0/ DIN/MISO	IO_L20P_2/D0/ DIN/MISO	T14	DUAL
2	IP_2	IP_2	L7	INPUT
2	IP_2	IP_2	L8	INPUT
2	IP_2/VREF_2	IP_2/VREF_2	L9	VREF
2	IP_2/VREF_2	IP_2/VREF_2	L10	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M7	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M8	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M11	VREF
2	IP_2/VREF_2	IP_2/VREF_2	N5	VREF
2	VCCO_2	VCCO_2	M9	VCCO
2	VCCO_2	VCCO_2	R4	VCCO
2	VCCO_2	VCCO_2	R8	VCCO
2	VCCO_2	VCCO_2	R12	VCCO
3	IO_L01N_3	IO_L01N_3	C1	I/O
3	IO_L01P_3	IO_L01P_3	C2	I/O
3	IO_L02N_3	IO_L02N_3	D3	I/O
3	IO_L02P_3	IO_L02P_3	D4	I/O
3	IO_L03N_3	IO_L03N_3	E1	I/O
3	IO_L03P_3	IO_L03P_3	D1	I/O
3	N.C. (◆)	IO_L05N_3	E2	I/O
3	N.C. (◆)	IO_L05P_3	E3	I/O
3	N.C. (◆)	IO_L07N_3	G4	I/O
3	N.C. (◆)	IO_L07P_3	F3	I/O
3	IO_L08N_3/ VREF_3	IO_L08N_3/ VREF_3	G1	VREF
3	IO_L08P_3	IO_L08P_3	F1	I/O
3	N.C. (◆)	IO_L09N_3	H4	I/O
3	N.C. (◆)	IO_L09P_3	G3	I/O
3	N.C. (◆)	IO_L10N_3	H5	I/O
3	N.C. (◆)	IO_L10P_3	H6	I/O
3	IO_L11N_3/ LHCLK1	IO_L11N_3/ LHCLK1	H1	LHCLK
3	IO_L11P_3/ LHCLK0	IO_L11P_3/ LHCLK0	G2	LHCLK
3	IO_L12N_3/ IRDY2/LHCLK3	IO_L12N_3/ IRDY2/LHCLK3	J3	LHCLK
3	IO_L12P_3/ LHCLK2	IO_L12P_3/ LHCLK2	H3	LHCLK

FT256 Footprint (XC3S200A, XC3S400A)

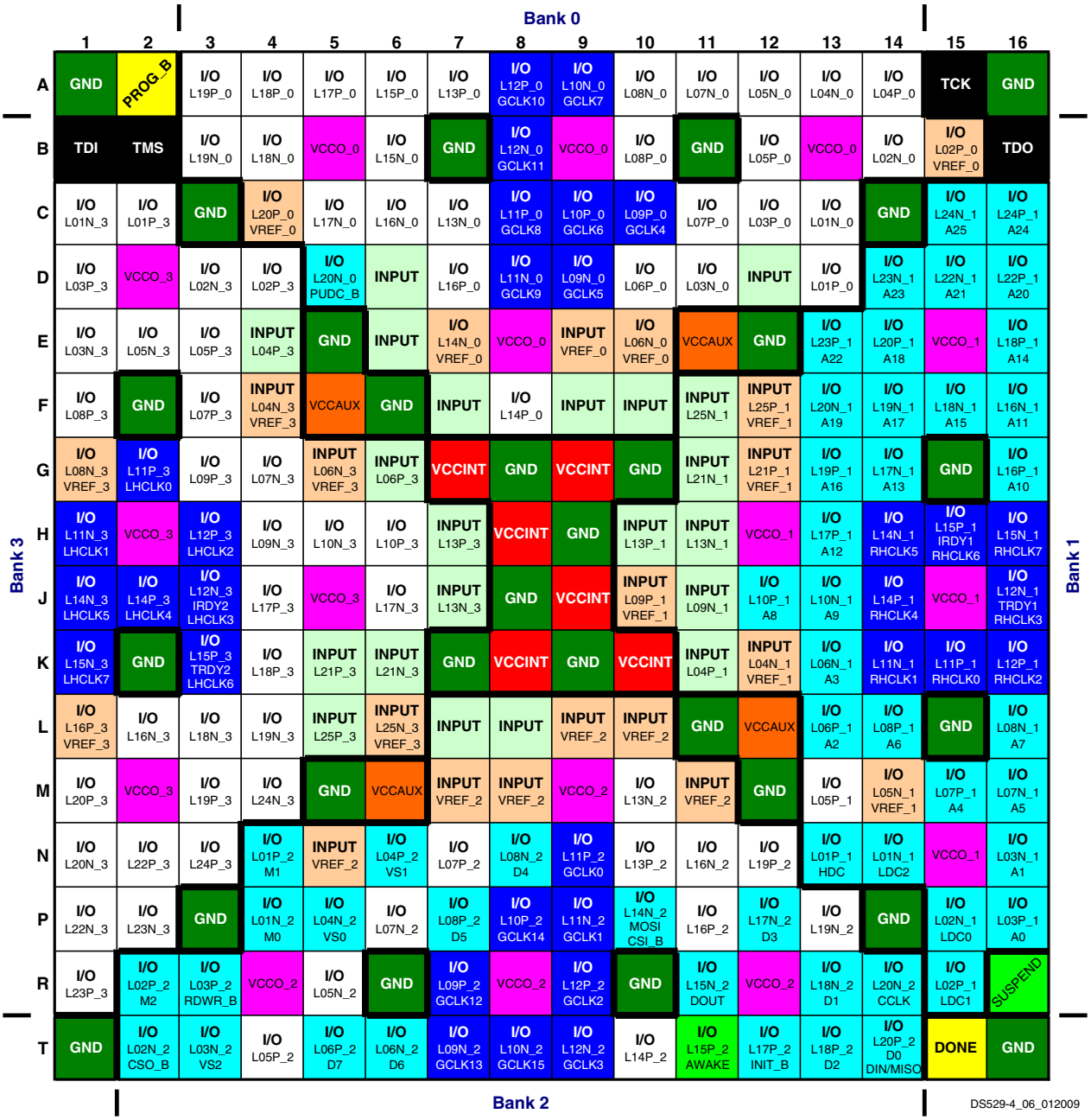


Figure 21: **XC3S200A and XC3S400A FT256 Package Footprint (Top View)**

69	**I/O:** Unrestricted, general-purpose user I/O	51	**DUAL:** Configuration pins, then possible user I/O	21	**VREF:** User I/O or input voltage reference for bank	2	**SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins
21	**INPUT:** Unrestricted, general-purpose input pin	32	**CLK:** User I/O, input, or global buffer input	16	**VCCO:** Output voltage supply for bank		
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	6	**VCCINT:** Internal core supply voltage (+1.2V)		
0	**N.C.:** Not connected	28	**GND:** Ground	4	**VCCAUX:** Auxiliary supply voltage		

User I/Os by Bank

Table 78 and Table 79 indicate how the available user-I/O pins are distributed between the four I/O banks on the FG320 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 78: **User I/Os Per Bank for XC3S200A in the FG320 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	60	35	11	1	5	8
Right	1	64	9	10	30	7	8
Bottom	2	60	19	6	21	6	8
Left	3	64	38	13	0	5	8
TOTAL		**248**	**101**	**40**	**52**	**23**	**32**

Table 79: **User I/Os Per Bank for XC3S400A in the FG320 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	61	35	12	1	5	8
Right	1	64	9	10	30	7	8
Bottom	2	62	19	7	21	7	8
Left	3	64	38	13	0	5	8
TOTAL		**251**	**101**	**42**	**52**	**24**	**32**

Footprint Migration Differences

Table 80 summarizes any footprint and functionality differences between the XC3S200A and the XC3S400A FPGAs that might affect easy migration between devices available in the FG320 package. There are three such balls. All other pins not listed in Table 80 unconditionally migrate between Spartan-3A devices available in the FG320 package.

The arrows indicate the direction for easy migration.

Table 80: **FG320 Footprint Migration Differences**

Pin	Bank	XC3S200A	Migration	XC3S400A
E13	0	N.C.	→	INPUT
N7	2	N.C.	→	INPUT
P14	2	N.C.	→	INPUT/VREF
DIFFERENCES			**3**	

Legend:

→ This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction is possible depending on how the pin is configured for the device on the right.

Table 81: **Spartan-3A FG400 Pinout *(Continued)***

Bank	Pin Name	FG400 Ball	Type
VCCAUX	TDO	E17	JTAG
VCCAUX	TMS	E4	JTAG
VCCAUX	VCCAUX	A13	VCCAUX
VCCAUX	VCCAUX	E16	VCCAUX
VCCAUX	VCCAUX	H1	VCCAUX
VCCAUX	VCCAUX	K13	VCCAUX
VCCAUX	VCCAUX	L8	VCCAUX
VCCAUX	VCCAUX	N20	VCCAUX
VCCAUX	VCCAUX	T5	VCCAUX
VCCAUX	VCCAUX	Y8	VCCAUX
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	J12	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	N10	VCCINT

User I/Os by Bank

Table 82 indicates how the 311 available user-I/O pins are distributed between the four I/O banks on the FG400 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 82: **User I/Os Per Bank for the XC3S400A and XC3S700A in the FG400 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	77	50	12	1	6	8
Right	1	79	21	12	30	8	8
Bottom	2	76	35	6	21	6	8
Left	3	79	49	16	0	6	8
TOTAL		**311**	**155**	**46**	**52**	**26**	**32**

Footprint Migration Differences

The XC3S400A and XC3S700A FPGAs have identical footprints in the FG400 package. Designs can migrate between the XC3S400A and XC3S700A FPGAs without further consideration.

Table 83: **Spartan-3A FG484 Pinout*(Continued)***

Bank	Pin Name	FG484 Ball	Type
2	VCCO_2	AA18	VCCO
2	VCCO_2	AA5	VCCO
2	VCCO_2	AA9	VCCO
2	VCCO_2	U14	VCCO
2	VCCO_2	U9	VCCO
3	IO_L01N_3	D2	I/O
3	IO_L01P_3	C1	I/O
3	IO_L02N_3	C2	I/O
3	IO_L02P_3	B1	I/O
3	IO_L03N_3	E4	I/O
3	IO_L03P_3	D3	I/O
3	IO_L05N_3	G5	I/O
3	IO_L05P_3	G6	I/O
3	IO_L06N_3	E1	I/O
3	IO_L06P_3	D1	I/O
3	IO_L07N_3	E3	I/O
3	IO_L07P_3	F4	I/O
3	IO_L08N_3	G4	I/O
3	IO_L08P_3	F3	I/O
3	IO_L09N_3	H6	I/O
3	IO_L09P_3	H5	I/O
3	IO_L10N_3	J5	I/O
3	IO_L10P_3	K6	I/O
3	IO_L12N_3	F1	I/O
3	IO_L12P_3	F2	I/O
3	IO_L13N_3	G1	I/O
3	IO_L13P_3	G3	I/O
3	IO_L14N_3	H3	I/O
3	IO_L14P_3	H4	I/O
3	IO_L16N_3	H1	I/O
3	IO_L16P_3	H2	I/O
3	IO_L17N_3/VREF_3	J1	VREF
3	IO_L17P_3	J3	I/O
3	IO_L18N_3	K4	I/O
3	IO_L18P_3	K5	I/O
3	IO_L20N_3	K2	I/O
3	IO_L20P_3	K3	I/O
3	IO_L21N_3/LHCLK1	L3	LHCLK
3	IO_L21P_3/LHCLK0	L5	LHCLK
3	IO_L22N_3/IRDY2/LHCLK3	L1	LHCLK

Table 83: **Spartan-3A FG484 Pinout*(Continued)***

Bank	Pin Name	FG484 Ball	Type
3	IO_L22P_3/LHCLK2	K1	LHCLK
3	IO_L24N_3/LHCLK5	M2	LHCLK
3	IO_L24P_3/LHCLK4	M1	LHCLK
3	IO_L25N_3/LHCLK7	M4	LHCLK
3	IO_L25P_3/TRDY2/LHCLK6	M3	LHCLK
3	IO_L26N_3	N3	I/O
3	IO_L26P_3/VREF_3	N1	VREF
3	IO_L28N_3	P2	I/O
3	IO_L28P_3	P1	I/O
3	IO_L29N_3	P5	I/O
3	IO_L29P_3	P3	I/O
3	IO_L30N_3	N4	I/O
3	IO_L30P_3	M5	I/O
3	IO_L32N_3	R2	I/O
3	IO_L32P_3	R1	I/O
3	IO_L33N_3	R4	I/O
3	IO_L33P_3	R3	I/O
3	IO_L34N_3	T4	I/O
3	IO_L34P_3	R5	I/O
3	IO_L36N_3	T3	I/O
3	IO_L36P_3/VREF_3	T1	VREF
3	IO_L37N_3	U2	I/O
3	IO_L37P_3	U1	I/O
3	IO_L38N_3	V3	I/O
3	IO_L38P_3	V1	I/O
3	IO_L40N_3	U5	I/O
3	IO_L40P_3	T5	I/O
3	IO_L41N_3	U4	I/O
3	IO_L41P_3	U3	I/O
3	IO_L42N_3	W2	I/O
3	IO_L42P_3	W1	I/O
3	IO_L43N_3	W3	I/O
3	IO_L43P_3	V4	I/O
3	IO_L44N_3	Y2	I/O
3	IO_L44P_3	Y1	I/O
3	IO_L45N_3	AA2	I/O
3	IO_L45P_3	AA1	I/O
3	IP_3/VREF_3	J8	VREF
3	IP_3/VREF_3	R6	VREF
3	IP_L04N_3/VREF_3	H7	VREF

Table 83: **Spartan-3A FG484 Pinout*(Continued)***

Bank	Pin Name	FG484 Ball	Type
3	IP_L04P_3	H8	INPUT
3	IP_L11N_3	K8	INPUT
3	IP_L11P_3	J7	INPUT
3	IP_L15N_3/VREF_3	L8	VREF
3	IP_L15P_3	K7	INPUT
3	IP_L19N_3	M8	INPUT
3	IP_L19P_3	L7	INPUT
3	IP_L23N_3	M6	INPUT
3	IP_L23P_3	M7	INPUT
3	IP_L27N_3	N9	INPUT
3	IP_L27P_3	N8	INPUT
3	IP_L31N_3	N5	INPUT
3	IP_L31P_3	N6	INPUT
3	IP_L35N_3	P8	INPUT
3	IP_L35P_3	N7	INPUT
3	IP_L39N_3	R8	INPUT
3	IP_L39P_3	P7	INPUT
3	IP_L46N_3/VREF_3	T6	VREF
3	IP_L46P_3	R7	INPUT
3	VCCO_3	E2	VCCO
3	VCCO_3	J2	VCCO
3	VCCO_3	J6	VCCO
3	VCCO_3	N2	VCCO
3	VCCO_3	P6	VCCO
3	VCCO_3	V2	VCCO
GND	GND	A1	GND
GND	GND	A22	GND
GND	GND	AA11	GND
GND	GND	AA16	GND
GND	GND	AA7	GND
GND	GND	AB1	GND
GND	GND	AB22	GND
GND	GND	B12	GND
GND	GND	B16	GND
GND	GND	B7	GND
GND	GND	C20	GND
GND	GND	C3	GND
GND	GND	D14	GND
GND	GND	D9	GND
GND	GND	F11	GND

Table 83: **Spartan-3A FG484 Pinout*(Continued)***

Bank	Pin Name	FG484 Ball	Type
GND	GND	F17	GND
GND	GND	F6	GND
GND	GND	G2	GND
GND	GND	G21	GND
GND	GND	J11	GND
GND	GND	J13	GND
GND	GND	J14	GND
GND	GND	J19	GND
GND	GND	J4	GND
GND	GND	J9	GND
GND	GND	K10	GND
GND	GND	K12	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L17	GND
GND	GND	L2	GND
GND	GND	L6	GND
GND	GND	L9	GND
GND	GND	M10	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M21	GND
GND	GND	N11	GND
GND	GND	N13	GND
GND	GND	P10	GND
GND	GND	P14	GND
GND	GND	P19	GND
GND	GND	P4	GND
GND	GND	P9	GND
GND	GND	T12	GND
GND	GND	T2	GND
GND	GND	T21	GND
GND	GND	U17	GND
GND	GND	U6	GND
GND	GND	W10	GND
GND	GND	W14	GND
GND	GND	Y20	GND
GND	GND	Y3	GND
VCCAUX	SUSPEND	U18	PWR MGMT

FG676 Footprint

Left Half of FG676 Package (Top View)

313 **I/O:** Unrestricted, general-purpose user I/O

67 **INPUT:** Unrestricted, general-purpose input pin

51 **DUAL:** Configuration pins, then possible user I/O

2 **SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins

38 **VREF:** User I/O or input voltage reference for bank

32 **CLK:** User I/O, input, or clock buffer input

2 **CONFIG:** Dedicated configuration pins

4 **JTAG:** Dedicated JTAG port pins

77 **GND:** Ground

36 **VCCO:** Output voltage supply for bank

23 **VCCINT:** Internal core supply voltage (+1.2V)

14 **VCCAUX:** Auxiliary supply voltage

17 ◆ **N.C.:** Not connected

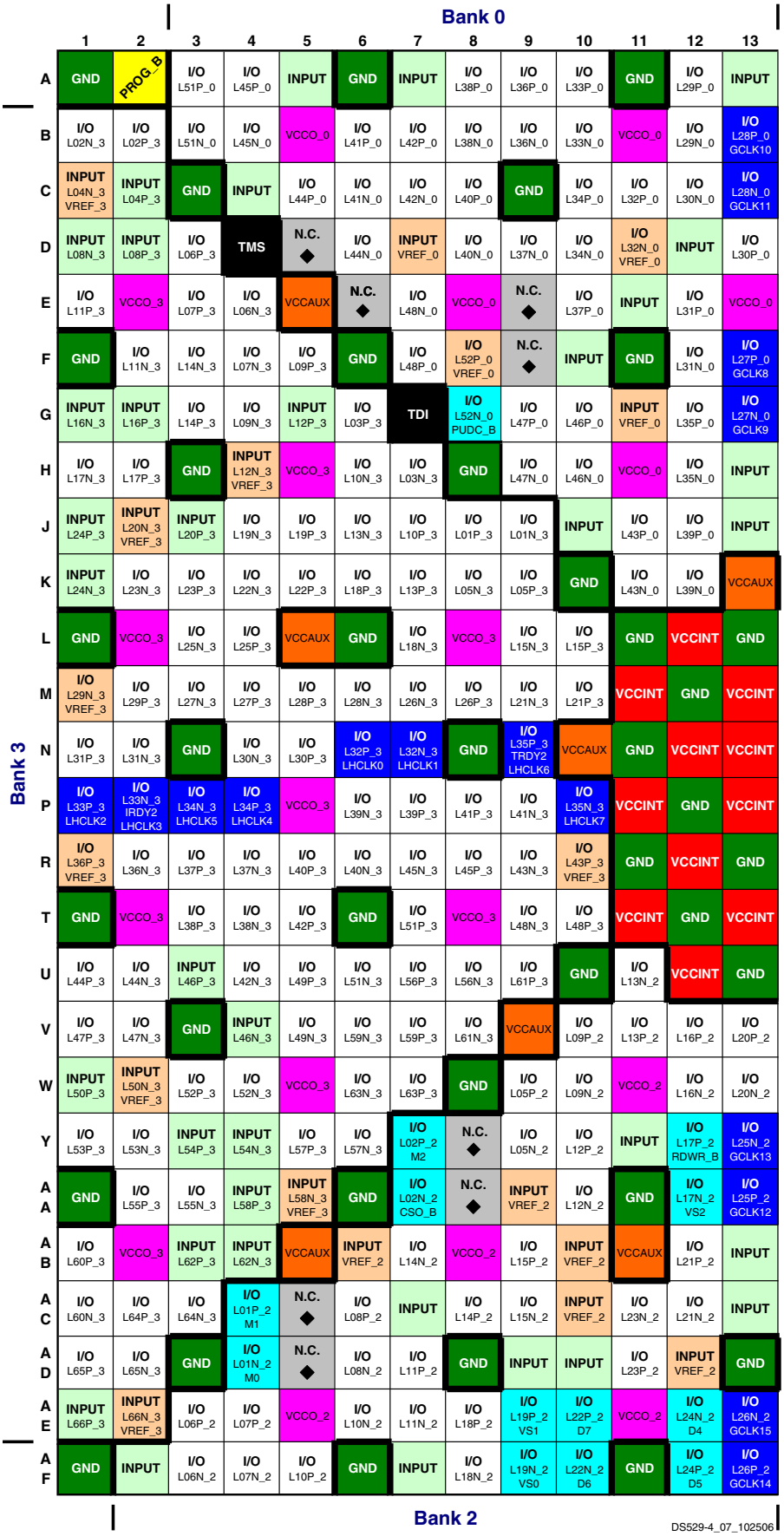


Figure 27: **FG676 Package Footprint (Top View)**