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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	1472
Number of Logic Elements/Cells	13248
Total RAM Bits	368640
Number of I/O	161
Number of Gates	700000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s700a-5ftg256c

Production Status

Table 3 indicates the production status of each Spartan-3A FPGA by temperature range and speed grade. The table also lists the earliest speed file version required for creating a production configuration bitstream. Later versions are also supported.

Table 3: **Spartan-3A FPGA Production Status (Production Speed File)**

Temperature Range		Commercial (C)		Industrial
Speed Grade		Standard (–4)	High-Performance (–5)	Standard (–4)
Part Number	XC3S50A	Production (v1.35)	Production (v1.35)	Production (v1.35)
	XC3S200A	Production (v1.35)	Production (v1.35)	Production (v1.35)
	XC3S400A	Production (v1.36)	Production (v1.36)	Production (v1.36)
	XC3S700A	Production (v1.34)	Production (v1.35)	Production (v1.34)
	XC3S1400A	Production (v1.34)	Production (v1.35)	Production (v1.34)

Package Marking

Figure 2 provides a top marking example for Spartan-3A FPGAs in the quad-flat packages. Figure 3 shows the top marking for Spartan-3A FPGAs in BGA packages. The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator.

The "5C" and "4I" Speed Grade/Temperature Range part combinations may be dual marked as "5C/4I". Devices with a single mark are only guaranteed for the marked speed grade and temperature range.

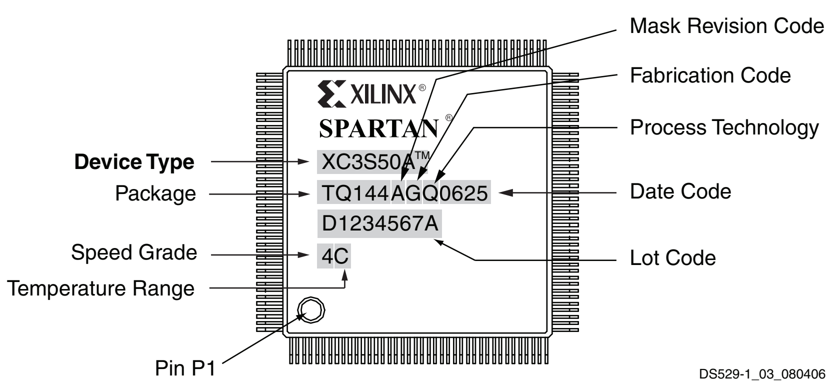

Figure 2: **Spartan-3A QFP Package Marking Example**

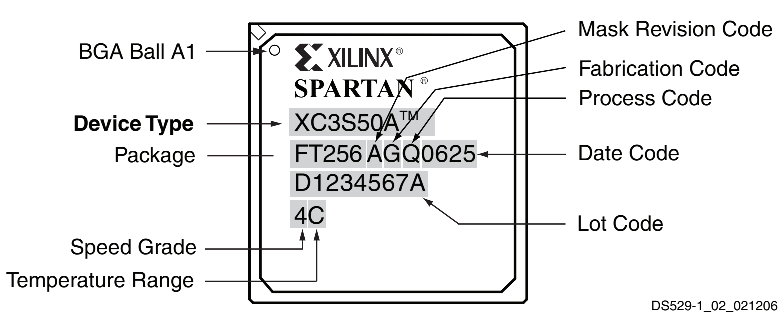

Figure 3: **Spartan-3A BGA Package Marking Example**

Output Propagation Times

Table 24: **Timing for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade -5 Max	Speed Grade -4 Max	Units
Clock-to-Output Times						
T_{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OCLK input to data appearing at the Output pin	LVCMOS25[(2)], 12 mA output drive, Fast slew rate	All	2.87	3.13	ns
Propagation Times						
T_{IOOP}	The time it takes for data to travel from the IOB's O input to the Output pin	LVCMOS25[(2)], 12 mA output drive, Fast slew rate	All	2.78	2.91	ns
Set/Reset Times						
T_{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the Output pin	LVCMOS25[(2)], 12 mA output drive, Fast slew rate	All	3.63	3.89	ns
T_{IOGSRQ}	Time from asserting the Global Set Reset (GSR) input on the STARTUP_SPARTAN3A primitive to setting/resetting data at the Output pin			8.62	9.65	ns

Notes:
1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 26.

Three-State Output Propagation Times

Table 25: **Timing for the IOB Three-State Path**

Symbol	Description	Conditions	Device	Speed Grade -5 Max	Speed Grade -4 Max	Units
Synchronous Output Enable/Disable Times						
T_{IOCKHZ}	Time from the active transition at the OTCLK input of the Three-state Flip-Flop (TFF) to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	0.63	0.76	ns
T_{IOCKON}[(2)]	Time from the active transition at TFF's OTCLK input to when the Output pin drives valid data		All	2.80	3.06	ns
Asynchronous Output Enable/Disable Times						
T_{GTS}	Time from asserting the Global Three State (GTS) input on the STARTUP_SPARTAN3A primitive to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	9.47	10.36	ns
Set/Reset Times						
T_{IOSRHZ}	Time from asserting TFF's SR input to when the Output pin enters a high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.61	1.86	ns
T_{IOSRON}[(2)]	Time from asserting TFF's SR input at TFF to when the Output pin drives valid data		All	3.57	3.82	ns

Notes:
1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 26.

Table 29: **Recommended Number of Simultaneously Switching Outputs per VCCO-GND Pair (V_{CCAUX}=3.3V)*(Continued)***

Signal Standard (IOSTANDARD)	Package Type			
	VQ100, TQ144		FT256, FG320, FG400, FG484, FG676	
	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)
Differential Standards (Number of I/O *Pairs* or Channels)				
LVDS_25	8	–	22	–
LVDS_33	8	–	27	–
BLVDS_25	1	1	4	4
MINI_LVDS_25	8	–	22	–
MINI_LVDS_33	8	–	27	–
LVPECL_25	Input Only			
LVPECL_33	Input Only			
RSDS_25	8	–	22	–
RSDS_33	8	–	27	–
TMDS_33	8	–	27	–
PPDS_25	8	–	22	–
PPDS_33	8	–	27	–
DIFF_HSTL_I	–	5	–	10
DIFF_HSTL_III	–	3	–	4
DIFF_HSTL_I_18	6	6	8	8
DIFF_HSTL_II_18	–	2	–	2
DIFF_HSTL_III_18	4	4	5	4
DIFF_SSTL18_I	3	6	3	7
DIFF_SSTL18_II	–	4	–	4
DIFF_SSTL2_I	5	5	9	9
DIFF_SSTL2_II	–	3	–	4
DIFF_SSTL3_I	3	4	4	5
DIFF_SSTL3_II	2	3	3	3

Notes:

1. Not all I/O standards are supported on all I/O banks. The left and right banks (I/O banks 1 and 3) support higher output drive current than the top and bottom banks (I/O banks 0 and 2). Similarly, true differential output standards, such as LVDS, RSDS, PPDS, miniLVDS, and TMDS, are only supported in top or bottom banks (I/O banks 0 and 2). Refer to UG331: *Spartan-3 Generation FPGA User Guide* for additional information.
2. The numbers in this table are recommendations that assume sound board lay out practice. Test limits are the V_{IL}/V_{IH} voltage limits for the respective I/O standard.
3. If more than one signal standard is assigned to the I/Os of a given bank, refer to XAPP689: *Managing Ground Bounce in Large FPGAs* for information on how to perform weighted average SSO calculations.

Table 37: **Switching Characteristics for the DLL**

Symbol	Description		Device	Speed Grade -5 Min	Speed Grade -5 Max	Speed Grade -4 Min	Speed Grade -4 Max	Units
Output Frequency Ranges								
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs		All	5	280	5	250	MHz
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs			5	200	5	200	MHz
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs			10	334	10	334	MHz
CLKOUT_FREQ_DV	Frequency for the CLKDV output			0.3125	186	0.3125	166	MHz
Output Clock Jitter(2,3,4)								
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output		All	–	±100	–	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs			–	±[0.5% of CLKIN period + 100]	–	±[0.5% of CLKIN period + 100]	ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division			–	±150	–	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division			–	±[0.5% of CLKIN period + 100]	–	±[0.5% of CLKIN period + 100]	ps
Duty Cycle(4)								
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	–	±[1% of CLKIN period + 350]	–	±[1% of CLKIN period + 350]	ps
Phase Alignment(4)								
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs		All	–	±150	–	±150	ps
CLKOUT_PHASE_DLL	Phase offset between DLL outputs	CLK0 to CLK2X (not CLK2X180)		–	±[1% of CLKIN period + 100]	–	±[1% of CLKIN period + 100]	ps
		All others		–	±[1% of CLKIN period + 150]	–	±[1% of CLKIN period + 150]	ps
Lock Time								
LOCK_DLL(3)	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	5 MHz ≤ F_{CLKIN} ≤ 15 MHz	All	–	5	–	5	ms
		F_{CLKIN} > 15 MHz		–	600	–	600	µs
Delay Lines								
DCM_DELAY_STEP(5)	Finest delay resolution, averaged over all steps		All	15	35	15	35	ps

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8 and Table 36.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, the data sheet specifies a maximum jitter of "±[1% of CLKIN period + 150]". Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250ps.
5. The typical delay step size is 23 ps.

Digital Frequency Synthesizer (DFS)

Table 38: **Recommended Operating Conditions for the DFS**

Symbol		Description		Speed Grade -5 Min	-5 Max	-4 Min	-4 Max	Units
Input Frequency Ranges(2)								
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input		0.200	333(4)	0.200	333(4)	MHz
Input Clock Jitter Tolerance(3)								
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency	$F_{CLKFX} \leq 150$ MHz	–	±300	–	±300	ps
CLKIN_CYC_JITT_FX_HF			$F_{CLKFX} > 150$ MHz	–	±150	–	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input		–	±1	–	±1	ns

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 36.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.
4. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM.

Table 39: **Switching Characteristics for the DFS**

Symbol	Description		Device	Speed Grade -5 Min	-5 Max	-4 Min	-4 Max	Units
Output Frequency Ranges								
CLKOUT_FREQ_FX(2)	Frequency for the CLKFX and CLKFX180 outputs		All	5	350	5	320	MHz
Output Clock Jitter(3,4)								
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.		All	**Typ**	**Max**	**Typ**	**Max**	
		CLKIN ≤ 20 MHz		Use the Spartan-3A Jitter Calculator: www.xilinx.com/support/documentation/data_sheets/s3a_jitter_calc.zip				ps
		CLKIN > 20 MHz		±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	ps
Duty Cycle(5,6)								
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	–	±[1% of CLKFX period + 350]	–	±[1% of CLKFX period + 350]	ps
Phase Alignment(6)								
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used		All	–	±200	–	±200	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used		All	–	±[1% of CLKFX period + 200]	–	±[1% of CLKFX period + 200]	ps

Table 47: **Master Mode CCLK Output Frequency by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
F_{CCLK1}	Equivalent CCLK clock frequency by ***ConfigRate*** setting	1 *(power-on value)*	Commercial	0.400	0.797	MHz
			Industrial		0.847	MHz
F_{CCLK3}		3	Commercial	1.20	2.42	MHz
			Industrial		2.57	MHz
F_{CCLK6}		6 (default)	Commercial	2.40	4.83	MHz
			Industrial		5.13	MHz
F_{CCLK7}		7	Commercial	2.80	5.61	MHz
			Industrial		5.96	MHz
F_{CCLK8}		8	Commercial	3.20	6.41	MHz
			Industrial		6.81	MHz
F_{CCLK10}		10	Commercial	4.00	8.12	MHz
			Industrial		8.63	MHz
F_{CCLK12}		12	Commercial	4.80	9.70	MHz
			Industrial		10.31	MHz
F_{CCLK13}		13	Commercial	5.20	10.69	MHz
			Industrial		11.37	MHz
F_{CCLK17}		17	Commercial	6.80	13.74	MHz
			Industrial		14.61	MHz
F_{CCLK22}		22	Commercial	8.80	18.44	MHz
			Industrial		19.61	MHz
F_{CCLK25}		25	Commercial	10.00	20.90	MHz
			Industrial		22.23	MHz
F_{CCLK27}		27	Commercial	10.80	22.39	MHz
			Industrial		23.81	MHz
F_{CCLK33}		33	Commercial	13.20	27.48	MHz
			Industrial		29.23	MHz
F_{CCLK44}		44	Commercial	17.60	37.60	MHz
			Industrial		40.00	MHz
F_{CCLK50}		50	Commercial	20.00	44.80	MHz
			Industrial		47.66	MHz
$F_{CCLK100}$		100	Commercial	40.00	88.68	MHz
			Industrial		94.34	MHz

Table 48: **Master Mode CCLK Output Minimum Low and High Time**

Symbol	Description		*ConfigRate* Setting																Units
			1	3	6	7	8	10	12	13	17	22	25	27	33	44	50	100	
T_{MCCL}, T_{MCCH}	Master Mode CCLK Minimum Low and High Time	Commercial	595	196	98.3	84.5	74.1	58.4	48.9	44.1	34.2	25.6	22.3	20.9	17.1	12.3	10.4	5.3	ns
		Industrial	560	185	92.6	79.8	69.8	55.0	46.0	41.8	32.3	24.2	21.4	20.0	16.2	11.9	10.0	5.0	ns

Table 49: **Slave Mode CCLK Input Low and High Time**

Symbol	Description	Min	Max	Units
T_{SCCL}, T_{SCCH}	CCLK Low and High time	5	∞	ns

Master Serial and Slave Serial Mode Timing

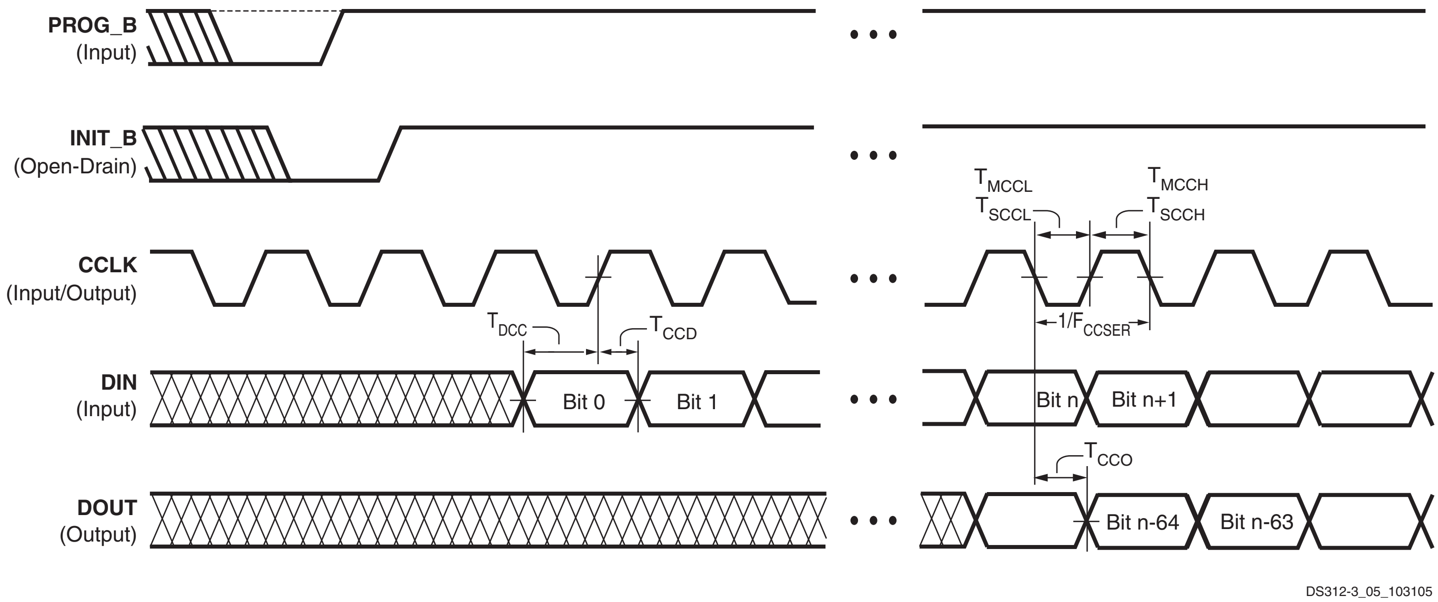

Figure 12: **Waveforms for Master Serial and Slave Serial Configuration**

Table 50: **Timing for the Master Serial and Slave Serial Configuration Modes**

Symbol	Description	Slave/ Master	All Speed Grades Min	All Speed Grades Max	Units
Clock-to-Output Times					
T_{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin	Both	1.5	10	ns
Setup Times					
T_{DCC}	The time from the setup of data at the DIN pin to the rising transition at the CCLK pin	Both	7	–	ns
Hold Times					
T_{CCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin	Master	0	–	ns
		Slave	1.0		
Clock Timing					
T_{CCH}	High pulse width at the CCLK input pin	Master	See Table 48		
		Slave	See Table 49		
T_{CCL}	Low pulse width at the CCLK input pin	Master	See Table 48		
		Slave	See Table 49		
F_{CCSER}	Frequency of the clock signal at the CCLK input pin: No bitstream compression	Slave	0	100	MHz
	Frequency of the clock signal at the CCLK input pin: With bitstream compression		0	100	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Package Thermal Characteristics

The power dissipated by an FPGA application has implications on package selection and system design. The power consumed by a Spartan-3A FPGA is reported using either the XPower Power Estimator or the XPower Analyzer calculator integrated in the Xilinx® ISE® development software. Table 62 provides the thermal characteristics for the various Spartan-3A FPGA package offerings. This information is also available using the Thermal Query tool on xilinx.com (www.xilinx.com/cgi-bin/thermal/thermal.pl).

The junction-to-case thermal resistance (θ_{JC}) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board (θ_{JB}) value similarly reports the difference between the board and junction temperature. The junction-to-ambient (θ_{JA}) value reports the temperature difference between the ambient environment and the junction temperature. The θ_{JA} value is reported at different air velocities, measured in linear feet per minute (LFM). The "Still Air (0 LFM)" column shows the θ_{JA} value in a system without a fan. The thermal resistance drops with increasing air flow.

Table 62: **Spartan-3A Package Thermal Characteristics**

Package	Device	Junction-to-Case (θ_{JC})	Junction-to-Board (θ_{JB})	Junction-to-Ambient (θ_{JA}) at Different Air Flows				Units
				Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	
VQ100 VQG100	XC3S50A	12.9	30.1	48.5	40.4	37.6	36.6	°C/Watt
	XC3S200A	10.9	25.7	42.9	35.7	33.2	32.4	°C/Watt
TQ144 TQG144	XC3S50A	16.5	32.0	42.4	36.3	35.8	34.9	°C/Watt
FT256 FTG256	XC3S50A	16.0	33.5	42.3	35.6	35.5	34.5	°C/Watt
	XC3S200A	10.3	23.8	32.7	26.6	26.1	25.2	°C/Watt
	XC3S400A	8.4	19.3	29.9	24.9	23.0	22.3	°C/Watt
	XC3S700A	7.8	18.6	28.1	22.3	21.2	20.7	°C/Watt
	XC3S1400A	5.4	14.1	24.2	18.7	17.5	17.0	°C/Watt
FG320 FGG320	XC3S200A	11.7	18.5	27.8	22.3	21.1	20.3	°C/Watt
	XC3S400A	9.9	15.4	25.2	19.8	18.6	17.8	°C/Watt
FG400 FGG400	XC3S400A	9.8	15.5	25.6	19.2	18.0	17.3	°C/Watt
	XC3S700A	8.2	13.0	23.1	17.9	16.7	16.0	°C/Watt
FG484 FGG484	XC3S700A	7.9	12.8	22.3	17.4	16.2	15.5	°C/Watt
	XC3S1400A	6.0	9.9	19.5	14.7	13.5	12.8	°C/Watt
FG676 FGG676	XC3S1400A	5.8	9.4	17.8	13.5	12.4	11.8	°C/Watt

FT256: 256-ball Fine-pitch, Thin Ball Grid Array

The 256-ball fine-pitch, thin ball grid array package, FT256, supports all five Spartan-3A FPGAs. The XC3S200A and XC3S400A have identical footprints, and the XC3S700A and XC3S1400A have identical footprints. The XC3S50A is compatible with the XC3S200A/XC3S400A but has 51 unconnected balls. The XC3S200A/XC3S400A is similar to the XC3S700A/XC3S1400A, but the XC3S700A/ XC3S1400A adds more power and ground pins and therefore is not compatible.

Table 68 lists all the package pins for the XC3S50A, XC3S200A, and XC3S400A. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The highlighted rows indicate pinout differences between the XC3S50A, the XC3S200A, and the XC3S400A FPGAs. The XC3S50A has 51 unconnected balls, indicated as N.C. (No Connection) in Table 68 and Figure 20 and with the black diamond character (◆) in Table 68. Figure 21 provides the common footprint for the XC3S200A and XC3S400A.

Table 68 also indicates that some differential I/O pairs have different assignments between the XC3S50A and the XC3S200A/XC3S400A, highlighted in light blue. See "Footprint Migration Differences," page 99 for additional information.

All other balls have nearly identical functionality on all three devices. Table 73 summarizes the XC3S50A FPGA footprint migration differences for the FT256 package.

The XC3S50A does not support the address output pins for the Byte-wide Peripheral Interface (BPI) configuration mode.

Table 69 lists all the package pins for the XC3S700A and XC3S1400A. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier. Figure 22 provides the common footprint for the XC3S200A and XC3S400A.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 68: **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400)**

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
0	IO_L01N_0	IO_L01N_0	C13	I/O
0	IO_L01P_0	IO_L01P_0	D13	I/O
0	IO_L02N_0	IO_L02N_0	B14	I/O
0	IO_L02P_0/ VREF_0	IO_L02P_0/ VREF_0	B15	VREF
0	IO_L03N_0	IO_L03N_0	D11	I/O
0	IO_L03P_0	IO_L03P_0	C12	I/O
0	IO_L04N_0	IO_L04N_0	A13	I/O
0	IO_L04P_0	IO_L04P_0	A14	I/O
0	N.C. (◆)	IO_L05N_0	A12	I/O
0	IP_0	IO_L05P_0	B12	I/O
0	N.C. (◆)	IO_L06N_0/ VREF_0	E10	VREF
0	N.C. (◆)	IO_L06P_0	D10	I/O
0	IO_L07N_0	IO_L07N_0	A11	I/O
0	IO_L07P_0	IO_L07P_0	C11	I/O
0	IO_L08N_0	IO_L08N_0	A10	I/O
0	IO_L08P_0	IO_L08P_0	B10	I/O
0	IO_L09N_0/ GCLK5	IO_L09N_0/ GCLK5	D9	GCLK
0	IO_L09P_0/ GCLK4	IO_L09P_0/ GCLK4	C10	GCLK
0	IO_L10N_0/ GCLK7	IO_L10N_0/ GCLK7	A9	GCLK
0	IO_L10P_0/ GCLK6	IO_L10P_0/ GCLK6	C9	GCLK
0	IO_L11N_0/ GCLK9	IO_L11N_0/ GCLK9	D8	GCLK
0	IO_L11P_0/ GCLK8	IO_L11P_0/ GCLK8	C8	GCLK
0	IO_L12N_0/ GCLK11	IO_L12N_0/ GCLK11	B8	GCLK
0	IO_L12P_0/ GCLK10	IO_L12P_0/ GCLK10	A8	GCLK
0	N.C. (◆)	IO_L13N_0	C7	I/O
0	N.C. (◆)	IO_L13P_0	A7	I/O
0	N.C. (◆)	IO_L14N_0/ VREF_0	E7	VREF
0	N.C. (◆)	IO_L14P_0	F8	I/O
0	IO_L15N_0	IO_L15N_0	B6	I/O
0	IO_L15P_0	IO_L15P_0	A6	I/O
0	IO_L16N_0	IO_L16N_0	C6	I/O
0	IO_L16P_0	IO_L16P_0	D7	I/O
0	IO_L17N_0	IO_L17N_0	C5	I/O

Table 68: **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400)** ***(Continued)***

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
3	IO_L14N_3/ LHCLK5	IO_L14N_3/ LHCLK5	J1	LHCLK
3	IO_L14P_3/ LHCLK4	IO_L14P_3/ LHCLK4	J2	LHCLK
3	IO_L15N_3/ LHCLK7	IO_L15N_3/ LHCLK7	K1	LHCLK
3	IO_L15P_3/ TRDY2/LHCLK6	IO_L15P_3/ TRDY2/LHCLK6	K3	LHCLK
3	N.C. (◆)	IO_L16N_3	L2	I/O
3	N.C. (◆)	IO_L16P_3/ VREF_3	L1	VREF
3	N.C. (◆)	IO_L17N_3	J6	I/O
3	N.C. (◆)	IO_L17P_3	J4	I/O
3	N.C. (◆)	IO_L18N_3	L3	I/O
3	N.C. (◆)	IO_L18P_3	K4	I/O
3	N.C. (◆)	IO_L19N_3	L4	I/O
3	N.C. (◆)	IO_L19P_3	M3	I/O
3	IO_L20N_3	IO_L20N_3	N1	I/O
3	IO_L20P_3	IO_L20P_3	M1	I/O
3	IO_L22N_3	IO_L22N_3	P1	I/O
3	IO_L22P_3	IO_L22P_3	N2	I/O
3	IO_L23N_3	IO_L23N_3	P2	I/O
3	IO_L23P_3	IO_L23P_3	R1	I/O
3	IO_L24N_3	IO_L24N_3	M4	I/O
3	IO_L24P_3	IO_L24P_3	N3	I/O
3	IP_L04N_3/ VREF_3	IP_L04N_3/ VREF_3	F4	VREF
3	IP_L04P_3	IP_L04P_3	E4	INPUT
3	N.C. (◆)	IP_L06N_3/ VREF_3	G5	VREF
3	N.C. (◆)	IP_L06P_3	G6	INPUT
3	IP_L13N_3	IP_L13N_3	J7	INPUT
3	IP_L13P_3	IP_L13P_3	H7	INPUT
3	IP_L21N_3	IP_L21N_3	K6	INPUT
3	IP_L21P_3	IP_L21P_3	K5	INPUT
3	IP_L25N_3/ VREF_3	IP_L25N_3/ VREF_3	L6	VREF
3	IP_L25P_3	IP_L25P_3	L5	INPUT
3	VCCO_3	VCCO_3	D2	VCCO
3	VCCO_3	VCCO_3	H2	VCCO
3	VCCO_3	VCCO_3	J5	VCCO
3	VCCO_3	VCCO_3	M2	VCCO
GND	GND	GND	A1	GND
GND	GND	GND	A16	GND
GND	GND	GND	B7	GND

Table 68: **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400)** ***(Continued)***

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
GND	GND	GND	B11	GND
GND	GND	GND	C3	GND
GND	GND	GND	C14	GND
GND	GND	GND	E5	GND
GND	GND	GND	E12	GND
GND	GND	GND	F2	GND
GND	GND	GND	F6	GND
GND	GND	GND	G8	GND
GND	GND	GND	G10	GND
GND	GND	GND	G15	GND
GND	GND	GND	H9	GND
GND	GND	GND	J8	GND
GND	GND	GND	K2	GND
GND	GND	GND	K7	GND
GND	GND	GND	K9	GND
GND	GND	GND	L11	GND
GND	GND	GND	L15	GND
GND	GND	GND	M5	GND
GND	GND	GND	M12	GND
GND	GND	GND	P3	GND
GND	GND	GND	P14	GND
GND	GND	GND	R6	GND
GND	GND	GND	R10	GND
GND	GND	GND	T1	GND
GND	GND	GND	T16	GND
VCCAUX	SUSPEND	SUSPEND	R16	PWR MGMT
VCCAUX	DONE	DONE	T15	CONFIG
VCCAUX	PROG_B	PROG_B	A2	CONFIG
VCCAUX	TCK	TCK	A15	JTAG
VCCAUX	TDI	TDI	B1	JTAG
VCCAUX	TDO	TDO	B16	JTAG
VCCAUX	TMS	TMS	B2	JTAG
VCCAUX	VCCAUX	VCCAUX	E11	VCCAUX
VCCAUX	VCCAUX	VCCAUX	F5	VCCAUX
VCCAUX	VCCAUX	VCCAUX	L12	VCCAUX
VCCAUX	VCCAUX	VCCAUX	M6	VCCAUX
VCCINT	VCCINT	VCCINT	G7	VCCINT
VCCINT	VCCINT	VCCINT	G9	VCCINT
VCCINT	VCCINT	VCCINT	H8	VCCINT
VCCINT	VCCINT	VCCINT	J9	VCCINT

Table 68: **Spartan-3A FT256 Pinout (XC3S50A, XC3S200A, XC3S400)** ***(Continued)***

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
VCCINT	VCCINT	VCCINT	K8	VCCINT
VCCINT	VCCINT	VCCINT	K10	VCCINT

Table 69: **Spartan-3A FT256 Pinout (XC3S700A, XC3S1400A)**

Bank	XC3S700A XC3S1400A	FT256 Ball	Type
0	IO_L01N_0	C13	I/O
0	IO_L01P_0	D13	I/O
0	IO_L02N_0	B14	I/O
0	IO_L02P_0/VREF_0	B15	VREF
0	IO_L03N_0	D12	I/O
0	IO_L03P_0	C12	I/O
0	IO_L04N_0	A13	I/O
0	IO_L04P_0	A14	I/O
0	IO_L05N_0	A12	I/O
0	IO_L05P_0	B12	I/O
0	IO_L06N_0/VREF_0	D10	VREF
0	IO_L06P_0	D11	I/O
0	IO_L07N_0	A11	I/O
0	IO_L07P_0	C11	I/O
0	IO_L08N_0	A10	I/O
0	IO_L08P_0	B10	I/O
0	IO_L09N_0/GCLK5	D9	GCLK
0	IO_L09P_0/GCLK4	C10	GCLK
0	IO_L10N_0/GCLK7	A9	GCLK
0	IO_L10P_0/GCLK6	C9	GCLK
0	IO_L11N_0/GCLK9	D8	GCLK
0	IO_L11P_0/GCLK8	C8	GCLK
0	IO_L12N_0/GCLK11	B8	GCLK
0	IO_L12P_0/GCLK10	A8	GCLK
0	IO_L13N_0	C7	I/O
0	IO_L13P_0	A7	I/O
0	IO_L14N_0/VREF_0	E7	VREF
0	IO_L14P_0	E9	I/O
0	IO_L15N_0	B6	I/O
0	IO_L15P_0	A6	I/O
0	IO_L16N_0	C6	I/O
0	IO_L16P_0	D7	I/O
0	IO_L17N_0	C5	I/O
0	IO_L17P_0	A5	I/O

Table 69: **Spartan-3A FT256 Pinout (XC3S700A,**

Bank	XC3S700A XC3S1400A	FT256 Ball	Type
0	IO_L18N_0	B4	I/O
0	IO_L18P_0	A4	I/O
0	IO_L19N_0	B3	I/O
0	IO_L19P_0	A3	I/O
0	IO_L20N_0/PUDC_B	D5	DUAL
0	IO_L20P_0/VREF_0	C4	VREF
0	IP_0	E6	INPUT
0	VCCO_0	B13	VCCO
0	VCCO_0	B5	VCCO
0	VCCO_0	B9	VCCO
0	VCCO_0	E8	VCCO
1	IO_L01N_1/LDC2	N14	DUAL
1	IO_L01P_1/HDC	N13	DUAL
1	IO_L02N_1/LDC0	P15	DUAL
1	IO_L02P_1/LDC1	R15	DUAL
1	IO_L03N_1/A1	N16	DUAL
1	IO_L03P_1/A0	P16	DUAL
1	IO_L06N_1/A3	K13	DUAL
1	IO_L06P_1/A2	L13	DUAL
1	IO_L07N_1/A5	M16	DUAL
1	IO_L07P_1/A4	M15	DUAL
1	IO_L08N_1/A7	L16	DUAL
1	IO_L08P_1/A6	L14	DUAL
1	IO_L10N_1/A9	J13	DUAL
1	IO_L10P_1/A8	J12	DUAL
1	IO_L11N_1/RHCLK1	K14	RHCLK
1	IO_L11P_1/RHCLK0	K15	RHCLK
1	IO_L12N_1/TRDY1/RHCLK3	J16	RHCLK
1	IO_L12P_1/RHCLK2	K16	RHCLK
1	IO_L15N_1/RHCLK7	H16	RHCLK
1	IO_L15P_1/IRDY1/RHCLK6	H15	RHCLK
1	IO_L16N_1/A11	F16	DUAL
1	IO_L16P_1/A10	G16	DUAL
1	IO_L17N_1/A13	G14	DUAL
1	IO_L17P_1/A12	H13	DUAL
1	IO_L18N_1/A15	F15	DUAL
1	IO_L18P_1/A14	E16	DUAL
1	IO_L19N_1/A17	F14	DUAL
1	IO_L19P_1/A16	G13	DUAL
1	IO_L20N_1/A19	F13	DUAL

Table 69: **Spartan-3A FT256 Pinout (XC3S700A,**

Bank	XC3S700A XC3S1400A	FT256 Ball	Type
VCCAUX	VCCAUX	F5	VCCAUX
VCCAUX	VCCAUX	H14	VCCAUX
VCCAUX	VCCAUX	H4	VCCAUX
VCCAUX	VCCAUX	L12	VCCAUX
VCCAUX	VCCAUX	L5	VCCAUX
VCCAUX	VCCAUX	M10	VCCAUX
VCCAUX	VCCAUX	M6	VCCAUX
VCCINT	VCCINT	F10	VCCINT
VCCINT	VCCINT	G11	VCCINT
VCCINT	VCCINT	G7	VCCINT
VCCINT	VCCINT	G9	VCCINT
VCCINT	VCCINT	H10	VCCINT
VCCINT	VCCINT	H6	VCCINT
VCCINT	VCCINT	H8	VCCINT
VCCINT	VCCINT	J11	VCCINT
VCCINT	VCCINT	J7	VCCINT
VCCINT	VCCINT	J9	VCCINT
VCCINT	VCCINT	K10	VCCINT
VCCINT	VCCINT	K6	VCCINT
VCCINT	VCCINT	K8	VCCINT
VCCINT	VCCINT	L7	VCCINT
VCCINT	VCCINT	L9	VCCINT

Differences Between XC3S200A/XC3S400A and XC3S700A/XC3S1400A

The XC3S700A and XC3S1400A FPGAs have several additional power and ground pins as compared to the XC3S200A and XC3S400A. Table 76 summarizes all the differences. All dedicated and dual-purpose configuration pins are in the same location.

Table 76: **Differences Between XC3S200A/XC3S400A and XC3S700A/XC3S1400A**

FT256 Ball	Bank	XC3S200A XC3S400A		XC3S700A XC3S1400A	
		Pin Name	Type	Pin Name	Type
F8	0	IO_L14P_0	I/O	GND	GND
D11	0	IO_L03N_0	I/O	IO_L06P_0	I/O
D10	0	IO_L06P_0	I/O	IO_L06N_0/ VREF_0	VREF
F7	0	IP_0	INPUT	GND	GND
F9	0	IP_0	INPUT	GND	GND
D12	0	IP_0	INPUT	IO_L03N_0	I/O
E9	0	IP_0/ VREF_0	INPUT	IO_L14P_0	I/O
D6	0	IP_0	INPUT	VCCAUX	VCCAUX
F10	0	IP_0	INPUT	VCCINT	VCCINT
E10	0	IO_L06N_0/ VREF_0	VREF	GND	GND
M13	1	IO_L05P_1	I/O	IP_1/ VREF_1	VREF
F11	1	IP_L25N_1	INPUT	GND	GND
H11	1	IP_L13N_1	INPUT	GND	GND
K11	1	IP_L04P_1	INPUT	GND	GND
G11	1	IP_L21N_1	INPUT	VCCINT	VCCINT
H10	1	IP_L13P_1	INPUT	VCCINT	VCCINT
J11	1	IP_L09N_1	INPUT	VCCINT	VCCINT
H14	1	IO_L14N_1/ RHCLK5	RHCLK	VCCAUX	VCCAUX
J14	1	IO_L14P_1/ RHCLK4	RHCLK	IP_1/ VREF_1	VREF
H12	1	VCCO_1	VCCO	IP_1/ VREF_1	VREF
G12	1	IP_L21P_1/ VREF_1	VREF	GND	GND
J10	1	IP_L09P_1/ VREF_1	VREF	GND	GND
K12	1	IP_L04N_1/ VREF_1	VREF	GND	GND
F12	1	IP_L25P_1/ VREF_1	VREF	VCCAUX	VCCAUX
M14	1	IO_L05N_1/ VREF_1	VREF	IP_1/ VREF_1	VREF
N7	2	IO_L07P_2	I/O	GND	GND
N10	2	IO_L13P_2	I/O	GND	GND
M10	2	IO_L13N_2	I/O	VCCAUX	VCCAUX
P6	2	IO_L07N_2	I/O	IP_2/ VREF_2	VREF
L8	2	IP_2	INPUT	GND	GND
L7	2	IP_2	INPUT	VCCINT	VCCINT
M9	2	VCCO_2	VCCO	IP_2/ VREF_2	VREF
L10	2	IP_2/ VREF_2	VREF	GND	GND
M8	2	IP_2/ VREF_2	VREF	GND	GND
L9	2	IP_2/ VREF_2	VREF	VCCINT	VCCINT
H5	3	IO_L10N_3	I/O	GND	GND
J6	3	IO_L17N_3	I/O	GND	GND
G3	3	IO_L09P_3	I/O	IO_L07N_3	I/O
J4	3	IO_L17P_3	I/O	IP_3	IP
H4	3	IO_L09N_3	I/O	VCCAUX	VCCAUX
H6	3	IO_L10P_3	I/O	VCCINT	VCCINT
N2	3	IO_L22P_3	I/O	IO_L22P_3/ VREF_3	VREF
G4	3	IO_L07N_3	I/O	IP_3/ VREF_3	VREF
G6	3	IP_L06P_3	INPUT	GND	GND
H7	3	IP_L13P_3	INPUT	GND	GND
K5	3	IP_L21P_3	INPUT	GND	GND
E4	3	IP_L04P_3	INPUT	IO_L04P_3	I/O
L5	3	IP_L25P_3	INPUT	VCCAUX	VCCAUX
J7	3	IP_L13N_3	INPUT	VCCINT	VCCINT
K6	3	IP_L21N_3	INPUT	VCCINT	VCCINT
J5	3	VCCO_3	VCCO	IP_3/ VREF_3	VREF
G5	3	IP_L06N_3/ VREF_3	VREF	GND	GND
L6	3	IP_L25N_3/ VREF_3	VREF	GND	GND
F4	3	IP_L04N_3/ VREF_3	VREF	IO_L04N_3	I/O

Table 77: **Spartan-3A FG320 Pinout*(Continued)***

Bank	Pin Name	FG320 Ball	Type
2	IO_L02N_2/CSO_B	V3	DUAL
2	IO_L02P_2/M2	V2	DUAL
2	IO_L03N_2/VS2	U4	DUAL
2	IO_L03P_2/RDWR_B	T4	DUAL
2	IO_L04N_2	T5	I/O
2	IO_L04P_2	R5	I/O
2	IO_L05N_2/VS0	V5	DUAL
2	IO_L05P_2/VS1	V4	DUAL
2	IO_L06N_2	U6	I/O
2	IO_L06P_2	T6	I/O
2	IO_L07N_2	P8	I/O
2	IO_L07P_2	N8	I/O
2	IO_L08N_2/D6	T7	DUAL
2	IO_L08P_2/D7	R7	DUAL
2	IO_L09N_2	R9	I/O
2	IO_L09P_2	T8	I/O
2	IO_L10N_2/D4	V6	DUAL
2	IO_L10P_2/D5	U7	DUAL
2	IO_L11N_2/GCLK13	V8	GCLK
2	IO_L11P_2/GCLK12	U8	GCLK
2	IO_L12N_2/GCLK15	V9	GCLK
2	IO_L12P_2/GCLK14	U9	GCLK
2	IO_L13N_2/GCLK1	T10	GCLK
2	IO_L13P_2/GCLK0	U10	GCLK
2	IO_L14N_2/GCLK3	U11	GCLK
2	IO_L14P_2/GCLK2	V11	GCLK
2	IO_L15N_2	R10	I/O
2	IO_L15P_2	P10	I/O
2	IO_L16N_2/MOSI/CSI_B	T11	DUAL
2	IO_L16P_2	R11	I/O
2	IO_L17N_2	V13	I/O
2	IO_L17P_2	U12	I/O
2	IO_L18N_2/DOUT	U13	DUAL
2	IO_L18P_2/AWAKE	T12	PWR MGMT
2	IO_L19N_2	P12	I/O
2	IO_L19P_2	N12	I/O
2	IO_L20N_2/D3	R13	DUAL
2	IO_L20P_2/INIT_B	T13	DUAL
2	IO_L21N_2	T14	I/O
2	IO_L21P_2	V14	I/O
2	IO_L22N_2/D1	U15	DUAL
2	IO_L22P_2/D2	V15	DUAL
2	IO_L23N_2	T15	I/O
2	IO_L23P_2	R14	I/O
2	IO_L24N_2/CCLK	U16	DUAL
2	IO_L24P_2/D0/DIN/MISO	V16	DUAL
2	IP_2	M8	INPUT
2	IP_2	M9	INPUT
2	IP_2	M12	INPUT
2	***XC3S400A:*** IP_2 ***XC3S200A:*** N.C. (◆)	N7	INPUT
2	IP_2	N9	INPUT
2	IP_2	N11	INPUT
2	IP_2	R6	INPUT
2	IP_2/VREF_2	M11	VREF
2	IP_2/VREF_2	N10	VREF
2	IP_2/VREF_2	P6	VREF
2	IP_2/VREF_2	P7	VREF
2	IP_2/VREF_2	P9	VREF
2	IP_2/VREF_2	P13	VREF
2	***XC3S400A:*** IP_2/VREF_2 ***XC3S200A:*** N.C. (◆)	P14	VREF
2	VCCO_2	P11	VCCO
2	VCCO_2	R8	VCCO
2	VCCO_2	U5	VCCO
2	VCCO_2	U14	VCCO
3	IO_L01N_3	C1	I/O
3	IO_L01P_3	C2	I/O
3	IO_L02N_3	B1	I/O
3	IO_L02P_3	B2	I/O
3	IO_L03N_3	D2	I/O
3	IO_L03P_3	D3	I/O
3	IO_L05N_3	G5	I/O
3	IO_L05P_3	F5	I/O
3	IO_L06N_3	E3	I/O
3	IO_L06P_3	F4	I/O
3	IO_L07N_3	E1	I/O
3	IO_L07P_3	D1	I/O
3	IO_L09N_3	G4	I/O
3	IO_L09P_3	F3	I/O

FG400: 400-ball Fine-pitch Ball Grid Array

The 400-ball fine-pitch ball grid array, FG400, supports two different Spartan-3A FPGAs, the XC3S400A and the XC3S700A. Both devices share a common footprint for this package as shown in Table 81 and Figure 24.

Table 81 lists all the FG400 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at

> www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 81: **Spartan-3A FG400 Pinout**

Bank	Pin Name	FG400 Ball	Type
0	IO_L01N_0	A18	I/O
0	IO_L01P_0	B18	I/O
0	IO_L02N_0	C17	I/O
0	IO_L02P_0/VREF_0	D17	VREF
0	IO_L03N_0	E15	I/O
0	IO_L03P_0	D16	I/O
0	IO_L04N_0	A17	I/O
0	IO_L04P_0/VREF_0	B17	VREF
0	IO_L05N_0	A16	I/O
0	IO_L05P_0	C16	I/O
0	IO_L06N_0	C15	I/O
0	IO_L06P_0	D15	I/O
0	IO_L07N_0	A14	I/O
0	IO_L07P_0	C14	I/O
0	IO_L08N_0	A15	I/O
0	IO_L08P_0	B15	I/O
0	IO_L09N_0	F13	I/O
0	IO_L09P_0	E13	I/O
0	IO_L10N_0/VREF_0	C13	VREF
0	IO_L10P_0	D14	I/O
0	IO_L11N_0	C12	I/O
0	IO_L11P_0	B13	I/O
0	IO_L12N_0	F12	I/O
0	IO_L12P_0	D12	I/O
0	IO_L13N_0	A12	I/O
0	IO_L13P_0	B12	I/O
0	IO_L14N_0	C11	I/O
0	IO_L14P_0	B11	I/O
0	IO_L15N_0/GCLK5	E11	GCLK
0	IO_L15P_0/GCLK4	D11	GCLK
0	IO_L16N_0/GCLK7	C10	GCLK
0	IO_L16P_0/GCLK6	A10	GCLK
0	IO_L17N_0/GCLK9	E10	GCLK
0	IO_L17P_0/GCLK8	D10	GCLK
0	IO_L18N_0/GCLK11	A8	GCLK
0	IO_L18P_0/GCLK10	A9	GCLK
0	IO_L19N_0	C9	I/O
0	IO_L19P_0	B9	I/O
0	IO_L20N_0	C8	I/O
0	IO_L20P_0	B8	I/O
0	IO_L21N_0	D8	I/O
0	IO_L21P_0	C7	I/O
0	IO_L22N_0/VREF_0	F9	VREF
0	IO_L22P_0	E9	I/O
0	IO_L23N_0	F8	I/O
0	IO_L23P_0	E8	I/O
0	IO_L24N_0	A7	I/O
0	IO_L24P_0	B7	I/O
0	IO_L25N_0	C6	I/O
0	IO_L25P_0	A6	I/O
0	IO_L26N_0	B5	I/O
0	IO_L26P_0	A5	I/O
0	IO_L27N_0	F7	I/O
0	IO_L27P_0	E7	I/O
0	IO_L28N_0	D6	I/O
0	IO_L28P_0	C5	I/O
0	IO_L29N_0	C4	I/O
0	IO_L29P_0	A4	I/O
0	IO_L30N_0	B3	I/O
0	IO_L30P_0	A3	I/O
0	IO_L31N_0	F6	I/O
0	IO_L31P_0	E6	I/O
0	IO_L32N_0/PUDC_B	B2	DUAL

Table 81: **Spartan-3A FG400 Pinout*(Continued)***

Bank	Pin Name	FG400 Ball	Type
VCCAUX	TDO	E17	JTAG
VCCAUX	TMS	E4	JTAG
VCCAUX	VCCAUX	A13	VCCAUX
VCCAUX	VCCAUX	E16	VCCAUX
VCCAUX	VCCAUX	H1	VCCAUX
VCCAUX	VCCAUX	K13	VCCAUX
VCCAUX	VCCAUX	L8	VCCAUX
VCCAUX	VCCAUX	N20	VCCAUX
VCCAUX	VCCAUX	T5	VCCAUX
VCCAUX	VCCAUX	Y8	VCCAUX
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	J12	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	N10	VCCINT

User I/Os by Bank

Table 82 indicates how the 311 available user-I/O pins are distributed between the four I/O banks on the FG400 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 82: **User I/Os Per Bank for the XC3S400A and XC3S700A in the FG400 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	77	50	12	1	6	8
Right	1	79	21	12	30	8	8
Bottom	2	76	35	6	21	6	8
Left	3	79	49	16	0	6	8
TOTAL		**311**	**155**	**46**	**52**	**26**	**32**

Footprint Migration Differences

The XC3S400A and XC3S700A FPGAs have identical footprints in the FG400 package. Designs can migrate between the XC3S400A and XC3S700A FPGAs without further consideration.

FG400 Footprint

Left Half of FG400 Package (Top View)

- **155** — **I/O:** Unrestricted, general-purpose user I/O
- **46** — **INPUT:** Unrestricted, general-purpose input pin
- **51** — **DUAL:** Configuration pins, then possible user I/O
- **26** — **VREF:** User I/O or input voltage reference for bank
- **32** — **CLK:** User I/O, input, or clock buffer input
- **2** — **CONFIG:** Dedicated configuration pins
- **4** — **JTAG:** Dedicated JTAG port pins
- **2** — **SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins
- **43** — **GND:** Ground
- **22** — **VCCO:** Output voltage supply for bank
- **9** — **VCCINT:** Internal core supply voltage (+1.2V)
- **8** — **VCCAUX:** Auxiliary supply voltage

Bank 0 (top), Bank 3 (left), Bank 2 (bottom)

	1	2	3	4	5	6	7	8	9	10
A	GND	I/O L32P_0 VREF_0	I/O L30P_0	I/O L29P_0	I/O L26P_0	I/O L25P_0	I/O L24N_0	I/O L18N_0 GCLK11	I/O L18P_0 GCLK10	I/O L16P_0 GCLK6
B	I/O L02P_3	I/O L32N_0 PUDC_B	I/O L30N_0	VCCO_0	I/O L26N_0	GND	I/O L24P_0	I/O L20P_0	I/O L19P_0	VCCO_0
C	I/O L03P_3	I/O L02N_3	GND	I/O L29N_0	I/O L28P_0	I/O L25N_0	I/O L21P_0	I/O L20N_0	I/O L19N_0	I/O L16N_0 GCLK7
D	I/O L05P_3	I/O L03N_3	I/O L01N_3	I/O L01P_3	PROG_B	I/O L28N_0	VCCO_0	I/O L21N_0	GND	I/O L17P_0 GCLK8
E	I/O L05N_3	VCCO_3	I/O L10P_3	TMS	GND	I/O L31P_0	I/O L27P_0	I/O L23P_0	I/O L22P_0	I/O L17N_0 GCLK9
F	I/O L13P_3	I/O L10N_3	I/O L09P_3	I/O L06P_3	TDI	I/O L31N_0	I/O L27N_0	I/O L23N_0	I/O L22N_0 VREF_0	VCCO_0
G	I/O L13N_3 VREF_3	GND	I/O L12P_3	I/O L09N_3	I/O L06N_3	INPUT L04N_3 VREF_3	INPUT L04P_3	INPUT	INPUT	INPUT
H	VCCAUX	I/O L12N_3	I/O L14N_3	I/O L08N_3	VCCO_3	I/O L08P_3	INPUT	GND	INPUT	INPUT
J	I/O L17P_3 LHCLK0	I/O L16N_3	I/O L16P_3	I/O L14P_3	I/O L07N_3	I/O L07P_3	INPUT L11N_3 VREF_3	INPUT L11P_3	GND	VCCINT
K	GND	I/O L17N_3 LHCLK1	I/O L18P_3 LHCLK2	I/O L20P_3 LHCLK4	INPUT L19N_3	INPUT L19P_3	INPUT L15N_3	INPUT L15P_3	VCCINT	GND
L	I/O L21P_3 TRDY2 LHCLK6	VCCO_3	I/O L18N_3 IRDY2 LHCLK3	GND	I/O L20N_3 LHCLK5	INPUT L23N_3	INPUT L23P_3	VCCAUX	GND	VCCINT
M	I/O L21N_3 LHCLK7	I/O L22P_3 VREF_3	I/O L22N_3	I/O L24P_3	I/O L24N_3	INPUT L31P_3	INPUT L27N_3	INPUT L27P_3	VCCINT	GND
N	I/O L25P_3	I/O L25N_3	I/O L26P_3	I/O L26N_3	VCCO_3	INPUT L35N_3	INPUT L31N_3	GND	INPUT VREF_2	VCCINT
P	I/O L28P_3	GND	I/O L29P_3	I/O L29N_3	INPUT L35P_3	INPUT L39P_3	INPUT L39N_3 VREF_3	INPUT VREF_2	INPUT	INPUT VREF_2
R	I/O L28N_3	I/O L30P_3	I/O L30N_3	I/O L33N_3	I/O L36P_3	GND	I/O L04N_2	INPUT	GND	INPUT
T	I/O L32P_3 VREF_3	I/O L32N_3	I/O L33P_3	I/O L36N_3	VCCAUX	I/O L04P_2	I/O L06P_2	I/O L07P_2 RDWR_B	I/O L11P_2	I/O L14N_2 D4
U	I/O L34P_3	VCCO_3	I/O L34N_3	I/O L01P_2 M1	I/O L05N_2	I/O L06N_2	I/O L07N_2 VS2	VCCO_2	I/O L11N_2	I/O L14P_2 D5
V	I/O L37P_3	I/O L37N_3	GND	I/O L01N_2 M0	I/O L05P_2	I/O L09P_2 VS1	I/O L12P_2 D7	I/O L13P_2	I/O L13N_2	I/O L16P_2 GCLK14
W	I/O L38P_3	I/O L38N_3	I/O L02P_2 M2	I/O L03N_2	VCCO_2	I/O L09N_2 VS0	GND	I/O L12N_2 D6	I/O L15P_2 GCLK12	I/O L16N_2 GCLK15
Y	GND	I/O L02N_2 CSO_B	I/O L03P_2	I/O L08P_2	I/O L08N_2	I/O L10P_2	I/O L10N_2	VCCAUX	I/O L15N_2 GCLK13	GND

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Figure 24: **FG400 Package Footprint (Top View)**

Table 83: **Spartan-3A FG484 Pinout*(Continued)***

Bank	Pin Name	FG484 Ball	Type
2	VCCO_2	AA18	VCCO
2	VCCO_2	AA5	VCCO
2	VCCO_2	AA9	VCCO
2	VCCO_2	U14	VCCO
2	VCCO_2	U9	VCCO
3	IO_L01N_3	D2	I/O
3	IO_L01P_3	C1	I/O
3	IO_L02N_3	C2	I/O
3	IO_L02P_3	B1	I/O
3	IO_L03N_3	E4	I/O
3	IO_L03P_3	D3	I/O
3	IO_L05N_3	G5	I/O
3	IO_L05P_3	G6	I/O
3	IO_L06N_3	E1	I/O
3	IO_L06P_3	D1	I/O
3	IO_L07N_3	E3	I/O
3	IO_L07P_3	F4	I/O
3	IO_L08N_3	G4	I/O
3	IO_L08P_3	F3	I/O
3	IO_L09N_3	H6	I/O
3	IO_L09P_3	H5	I/O
3	IO_L10N_3	J5	I/O
3	IO_L10P_3	K6	I/O
3	IO_L12N_3	F1	I/O
3	IO_L12P_3	F2	I/O
3	IO_L13N_3	G1	I/O
3	IO_L13P_3	G3	I/O
3	IO_L14N_3	H3	I/O
3	IO_L14P_3	H4	I/O
3	IO_L16N_3	H1	I/O
3	IO_L16P_3	H2	I/O
3	IO_L17N_3/VREF_3	J1	VREF
3	IO_L17P_3	J3	I/O
3	IO_L18N_3	K4	I/O
3	IO_L18P_3	K5	I/O
3	IO_L20N_3	K2	I/O
3	IO_L20P_3	K3	I/O
3	IO_L21N_3/LHCLK1	L3	LHCLK
3	IO_L21P_3/LHCLK0	L5	LHCLK
3	IO_L22N_3/IRDY2/LHCLK3	L1	LHCLK

Table 83: **Spartan-3A FG484 Pinout*(Continued)***

Bank	Pin Name	FG484 Ball	Type
3	IO_L22P_3/LHCLK2	K1	LHCLK
3	IO_L24N_3/LHCLK5	M2	LHCLK
3	IO_L24P_3/LHCLK4	M1	LHCLK
3	IO_L25N_3/LHCLK7	M4	LHCLK
3	IO_L25P_3/TRDY2/LHCLK6	M3	LHCLK
3	IO_L26N_3	N3	I/O
3	IO_L26P_3/VREF_3	N1	VREF
3	IO_L28N_3	P2	I/O
3	IO_L28P_3	P1	I/O
3	IO_L29N_3	P5	I/O
3	IO_L29P_3	P3	I/O
3	IO_L30N_3	N4	I/O
3	IO_L30P_3	M5	I/O
3	IO_L32N_3	R2	I/O
3	IO_L32P_3	R1	I/O
3	IO_L33N_3	R4	I/O
3	IO_L33P_3	R3	I/O
3	IO_L34N_3	T4	I/O
3	IO_L34P_3	R5	I/O
3	IO_L36N_3	T3	I/O
3	IO_L36P_3/VREF_3	T1	VREF
3	IO_L37N_3	U2	I/O
3	IO_L37P_3	U1	I/O
3	IO_L38N_3	V3	I/O
3	IO_L38P_3	V1	I/O
3	IO_L40N_3	U5	I/O
3	IO_L40P_3	T5	I/O
3	IO_L41N_3	U4	I/O
3	IO_L41P_3	U3	I/O
3	IO_L42N_3	W2	I/O
3	IO_L42P_3	W1	I/O
3	IO_L43N_3	W3	I/O
3	IO_L43P_3	V4	I/O
3	IO_L44N_3	Y2	I/O
3	IO_L44P_3	Y1	I/O
3	IO_L45N_3	AA2	I/O
3	IO_L45P_3	AA1	I/O
3	IP_3/VREF_3	J8	VREF
3	IP_3/VREF_3	R6	VREF
3	IP_L04N_3/VREF_3	H7	VREF

Table 83: **Spartan-3A FG484 Pinout*(Continued)***

Bank	Pin Name	FG484 Ball	Type
3	IP_L04P_3	H8	INPUT
3	IP_L11N_3	K8	INPUT
3	IP_L11P_3	J7	INPUT
3	IP_L15N_3/VREF_3	L8	VREF
3	IP_L15P_3	K7	INPUT
3	IP_L19N_3	M8	INPUT
3	IP_L19P_3	L7	INPUT
3	IP_L23N_3	M6	INPUT
3	IP_L23P_3	M7	INPUT
3	IP_L27N_3	N9	INPUT
3	IP_L27P_3	N8	INPUT
3	IP_L31N_3	N5	INPUT
3	IP_L31P_3	N6	INPUT
3	IP_L35N_3	P8	INPUT
3	IP_L35P_3	N7	INPUT
3	IP_L39N_3	R8	INPUT
3	IP_L39P_3	P7	INPUT
3	IP_L46N_3/VREF_3	T6	VREF
3	IP_L46P_3	R7	INPUT
3	VCCO_3	E2	VCCO
3	VCCO_3	J2	VCCO
3	VCCO_3	J6	VCCO
3	VCCO_3	N2	VCCO
3	VCCO_3	P6	VCCO
3	VCCO_3	V2	VCCO
GND	GND	A1	GND
GND	GND	A22	GND
GND	GND	AA11	GND
GND	GND	AA16	GND
GND	GND	AA7	GND
GND	GND	AB1	GND
GND	GND	AB22	GND
GND	GND	B12	GND
GND	GND	B16	GND
GND	GND	B7	GND
GND	GND	C20	GND
GND	GND	C3	GND
GND	GND	D14	GND
GND	GND	D9	GND
GND	GND	F11	GND

Table 83: **Spartan-3A FG484 Pinout*(Continued)***

Bank	Pin Name	FG484 Ball	Type
GND	GND	F17	GND
GND	GND	F6	GND
GND	GND	G2	GND
GND	GND	G21	GND
GND	GND	J11	GND
GND	GND	J13	GND
GND	GND	J14	GND
GND	GND	J19	GND
GND	GND	J4	GND
GND	GND	J9	GND
GND	GND	K10	GND
GND	GND	K12	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L17	GND
GND	GND	L2	GND
GND	GND	L6	GND
GND	GND	L9	GND
GND	GND	M10	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M21	GND
GND	GND	N11	GND
GND	GND	N13	GND
GND	GND	P10	GND
GND	GND	P14	GND
GND	GND	P19	GND
GND	GND	P4	GND
GND	GND	P9	GND
GND	GND	T12	GND
GND	GND	T2	GND
GND	GND	T21	GND
GND	GND	U17	GND
GND	GND	U6	GND
GND	GND	W10	GND
GND	GND	W14	GND
GND	GND	Y20	GND
GND	GND	Y3	GND
VCCAUX	SUSPEND	U18	PWR MGMT

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
GND	GND	T16	GND
GND	GND	T21	GND
GND	GND	T26	GND
GND	GND	U10	GND
GND	GND	U13	GND
GND	GND	U17	GND
GND	GND	V3	GND
GND	GND	W8	GND
GND	GND	W14	GND
GND	GND	W19	GND
GND	GND	W24	GND
VCCAUX	SUSPEND	V20	PWR MGMT
VCCAUX	DONE	AB21	CONFIG
VCCAUX	PROG_B	A2	CONFIG
VCCAUX	TCK	A25	JTAG
VCCAUX	TDI	G7	JTAG
VCCAUX	TDO	E23	JTAG
VCCAUX	TMS	D4	JTAG
VCCAUX	VCCAUX	AB5	VCCAUX
VCCAUX	VCCAUX	AB11	VCCAUX
VCCAUX	VCCAUX	AB22	VCCAUX
VCCAUX	VCCAUX	E5	VCCAUX
VCCAUX	VCCAUX	E16	VCCAUX
VCCAUX	VCCAUX	E22	VCCAUX
VCCAUX	VCCAUX	J18	VCCAUX
VCCAUX	VCCAUX	K13	VCCAUX
VCCAUX	VCCAUX	L5	VCCAUX
VCCAUX	VCCAUX	N10	VCCAUX
VCCAUX	VCCAUX	P17	VCCAUX
VCCAUX	VCCAUX	T22	VCCAUX
VCCAUX	VCCAUX	U14	VCCAUX
VCCAUX	VCCAUX	V9	VCCAUX
VCCINT	VCCINT	K15	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	L14	VCCINT
VCCINT	VCCINT	L16	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	M13	VCCINT
VCCINT	VCCINT	M15	VCCINT

Table 87: **Spartan-3A FG676 Pinout*(Continued)***

Bank	Pin Name	FG676 Ball	Type
VCCINT	VCCINT	M17	VCCINT
VCCINT	VCCINT	N12	VCCINT
VCCINT	VCCINT	N13	VCCINT
VCCINT	VCCINT	N14	VCCINT
VCCINT	VCCINT	N16	VCCINT
VCCINT	VCCINT	P11	VCCINT
VCCINT	VCCINT	P13	VCCINT
VCCINT	VCCINT	P14	VCCINT
VCCINT	VCCINT	P15	VCCINT
VCCINT	VCCINT	R12	VCCINT
VCCINT	VCCINT	R14	VCCINT
VCCINT	VCCINT	R16	VCCINT
VCCINT	VCCINT	T11	VCCINT
VCCINT	VCCINT	T13	VCCINT
VCCINT	VCCINT	T15	VCCINT
VCCINT	VCCINT	U12	VCCINT