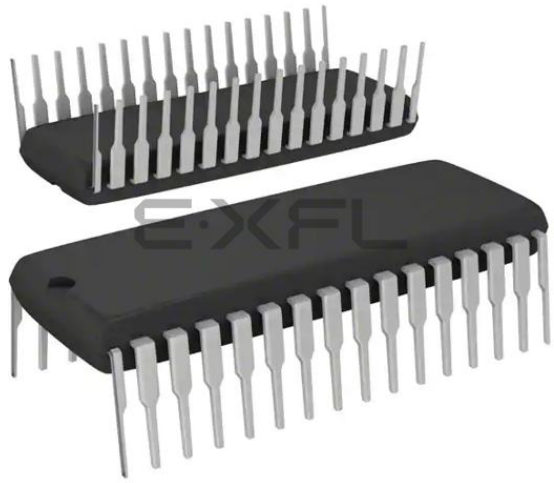

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	32-SDIP (0.400", 10.16mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72f324bk4b6

2 Pin description

Figure 2. 44-pin LQFP package pinout

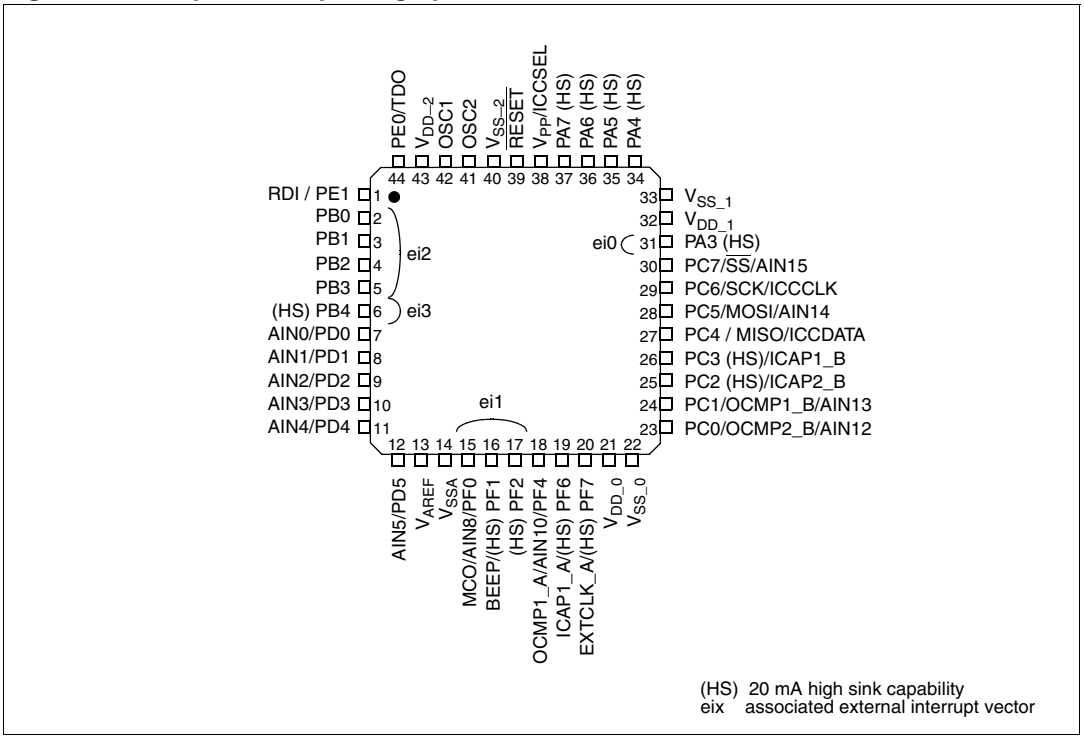


Figure 3. 42-pin SDIP package pinout

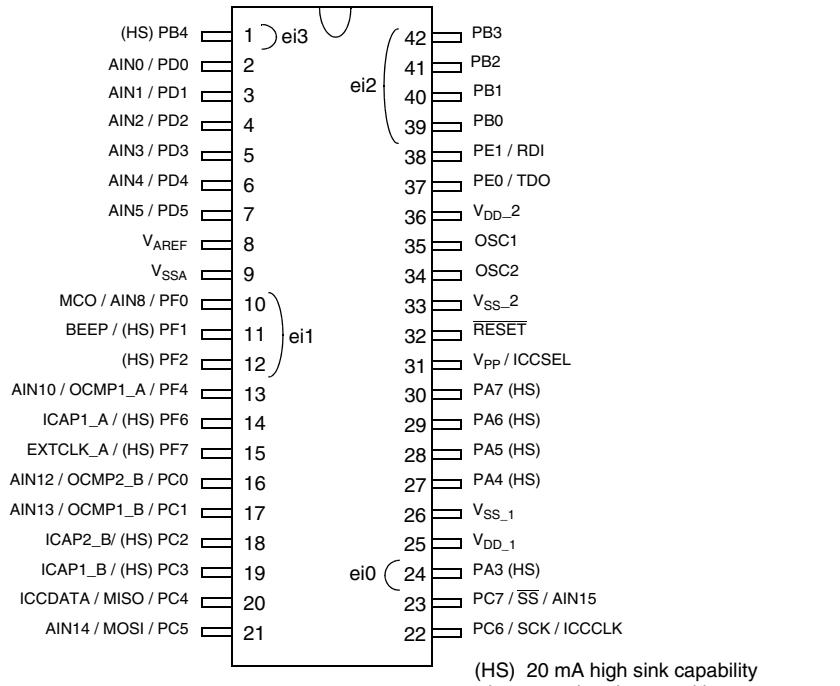


Figure 4. 32-pin LQFP package pinout

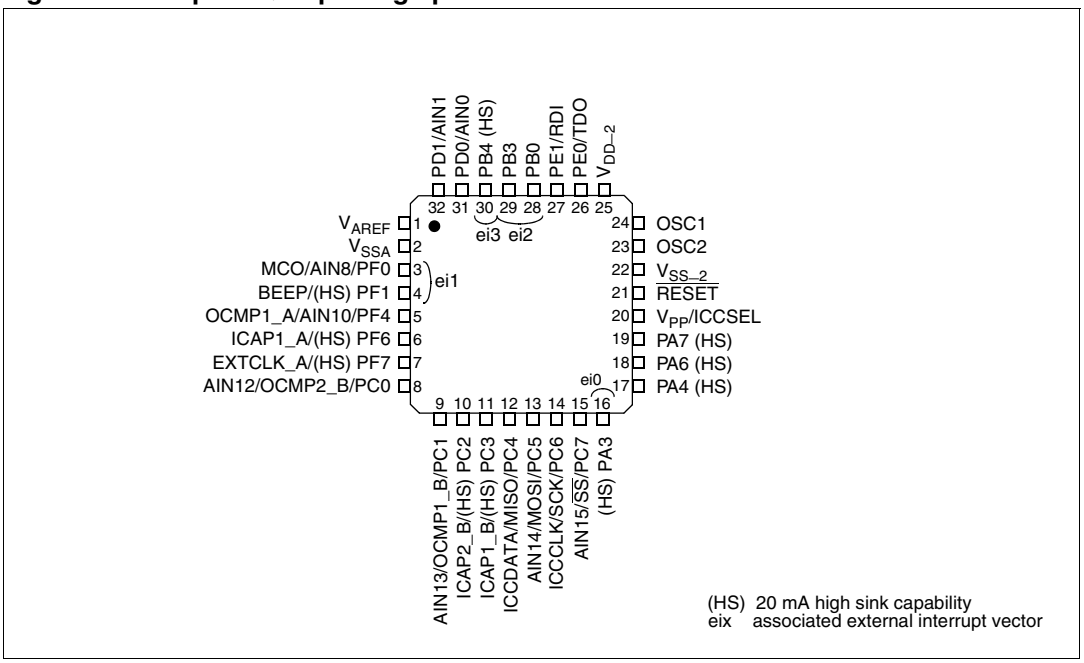
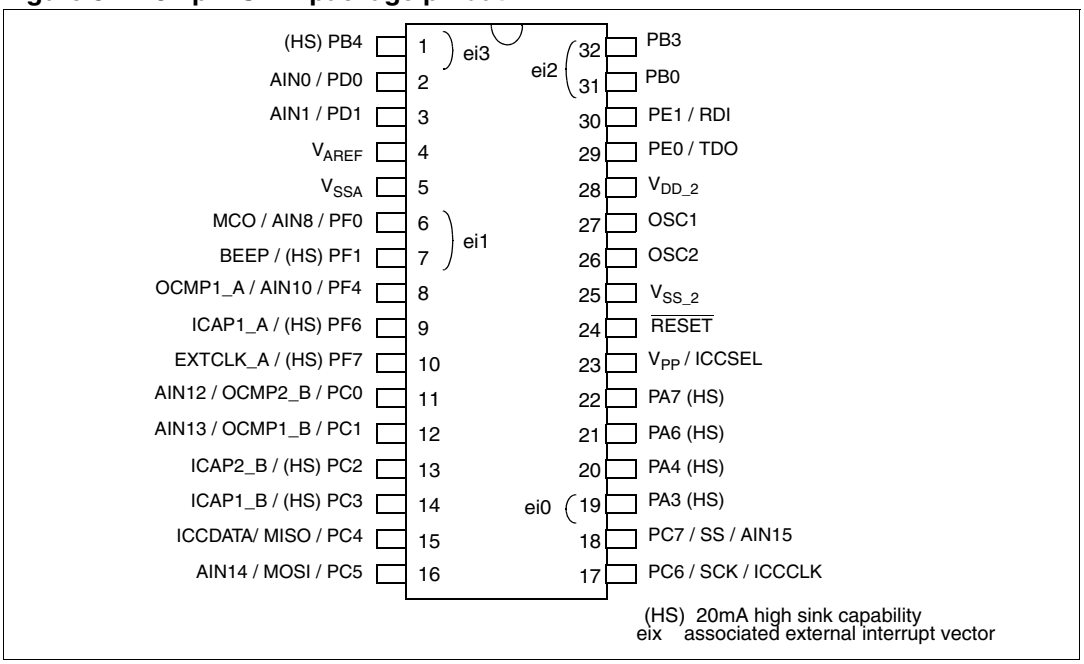


Figure 5. 32-pin SDIP package pinout



See *Section 12: Electrical characteristics on page 141* for external pin connection guidelines.

Refer to *Section 9: I/O ports on page 58* for more details on the software configuration of the I/O ports.

The reset configuration of each pin is shown in bold. This configuration is valid as long as the device is in reset state.

Provided the minimum V_{DD} value (guaranteed for the oscillator frequency) is above V_{IT-}, the MCU can only be in two modes:

- under full software control
- in static safe reset

In these conditions, secure operation is always ensured for the application without the need for external reset hardware.

During an LVD reset, the $\overline{\text{RESET}}$ pin is held low, thus permitting the MCU to reset other devices.

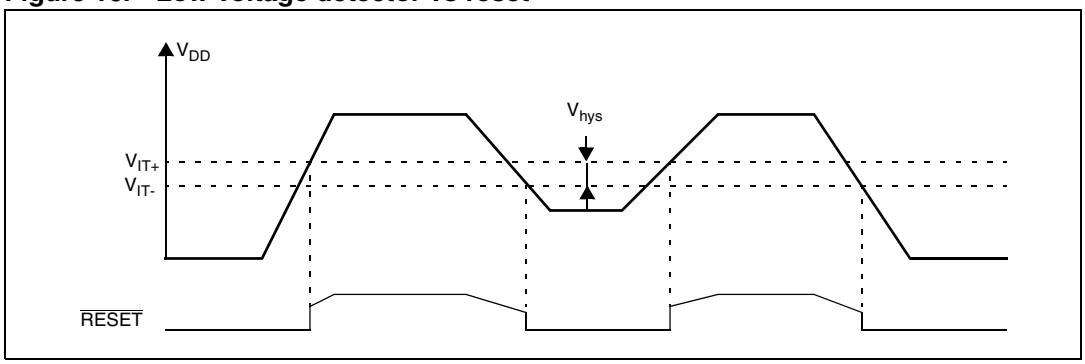
Note: 1 The LVD allows the device to be used without any external reset circuitry.

2 If the medium or low thresholds are selected, the detection may occur outside the specified operating voltage range. Below 3.8 V, device operation is not guaranteed.

3 The LVD is an optional function which can be selected by option byte.

4 It is recommended to make sure that the V_{DD} supply voltage rises monotonously when the device is exiting from reset, to ensure the application functions properly.

Figure 16. Low voltage detector vs reset



6.5.2 AVD (auxiliary voltage detector)

The AVD is based on an analog comparison between a $V_{IT-(AVD)}$ and $V_{IT+(AVD)}$ reference value and the V_{DD} main supply. The V_{IT-} reference value for falling voltage is lower than the V_{IT+} reference value for rising voltage in order to avoid parasitic detection (hysteresis).

The output of the AVD comparator is directly readable by the application software through a real-time status bit (AVDF) in the SICSR register. This bit is read only.

Caution: The AVD function is active only if the LVD is enabled through the option byte (see *Section 14.1 on page 179*).

Monitoring the V_{DD} main supply

The AVD voltage threshold value is relative to the selected LVD threshold configured by option byte (see *Section 14.1 on page 179*).

If the AVD interrupt is enabled, an interrupt is generated when the voltage crosses the $V_{IT+(AVD)}$ or $V_{IT-(AVD)}$ threshold (AVDF bit toggles).

In the case of a drop in voltage, the AVD interrupt acts as an early warning, allowing software to shut down safely before the LVD resets the microcontroller. See *Figure 17*.

6.6 SI registers

6.6.1 System integrity (SI) control/status register (SICSR)

SICSR Reset value: 000x 000x (00h)

7	6	5	4	3	2	1	0
Res	AVDIE	AVDF	LVDRF	Reserved			WDGRF
-	R/W	RO	R/W	-			R/W

Table 12. SICSR register description

Bit	Name	Function
7	-	Reserved, must be kept cleared
6	AVDIE	Voltage detector interrupt enable This bit is set and cleared by software. It enables an interrupt to be generated when the AVDF flag changes (toggles). The pending interrupt information is automatically cleared when software enters the AVD interrupt routine 0: AVD interrupt disabled 1: AVD interrupt enabled
5	AVDF	Voltage detector flag This read-only bit is set and cleared by hardware. If the AVDIE bit is set, an interrupt request is generated when the AVDF bit changes value. Refer to *Figure 17* and to *Section 6.5.2: AVD (auxiliary voltage detector)* for additional details. 0: V_{DD} over $V_{IT+(AVD)}$ threshold 1: V_{DD} under $V_{IT-(AVD)}$ threshold
4	LVDRF	LVD Reset flag This bit indicates that the last reset was generated by the LVD block. It is set by hardware (LVD reset) and cleared by software (writing zero). See WDGRF flag description for more details. When the LVD is disabled by option byte, the LVDRF bit value is undefined.
3:1	-	Reserved, must be kept cleared
0	WDGRF	Watchdog Reset flag This bit indicates that the last reset was generated by the Watchdog peripheral. It is set by hardware (watchdog reset) and cleared by software (writing zero) or an LVD reset (to ensure a stable cleared state of the WDGRF flag when CPU starts). Combined with the LVDRF information, the flag description is given in *Table 13*.

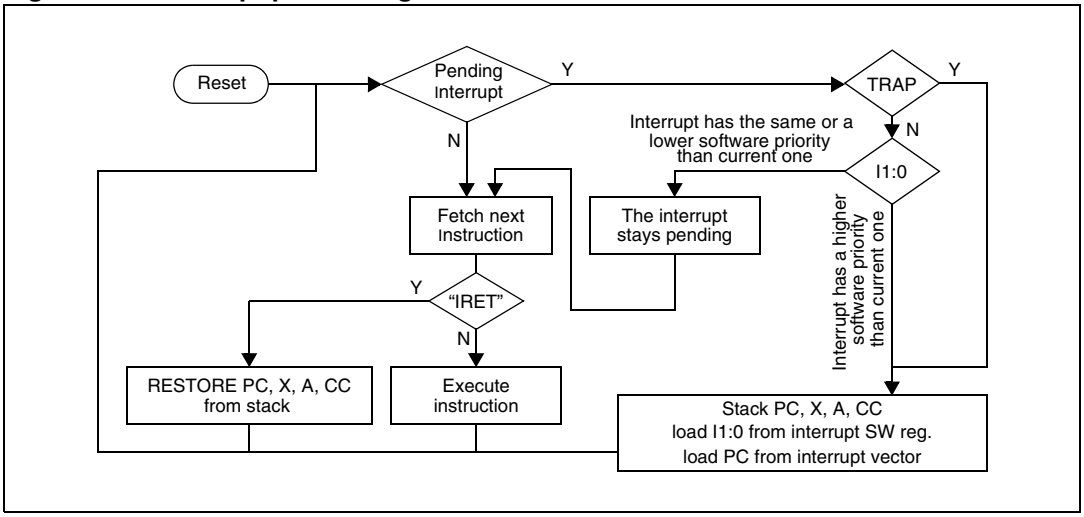
Table 13. Reset source flags

Reset sources	LVDRF	WDGRF
External $\overline{\text{RESET}}$ pin	0	0
Watchdog	0	1
LVD	1	X

Table 14. Interrupt software priority levels

Interrupt software priority	Level	I1	I0
Level 0 (main)	Low	1	0
Level 1	↓	0	1
Level 2	↓	0	0
Level 3 (= interrupt disable)	High	1	1

Figure 18. Interrupt processing flowchart



7.2.1 Servicing pending interrupts

As several interrupts can be pending at the same time, the interrupt to be taken into account is determined by the following two-step process:

- the highest software priority interrupt is serviced,
- if several interrupts have the same software priority then the interrupt with the highest hardware priority is serviced first.

Figure 19 describes this decision process.

Figure 19. Priority decision process flowchart

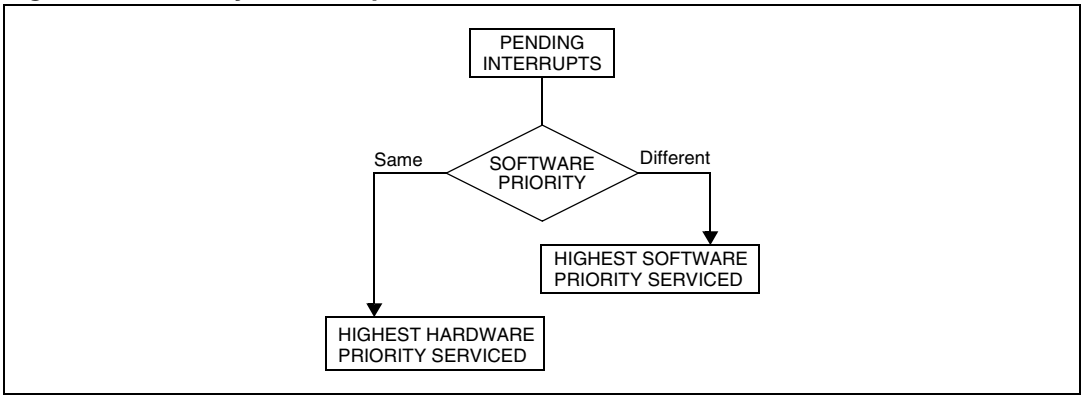
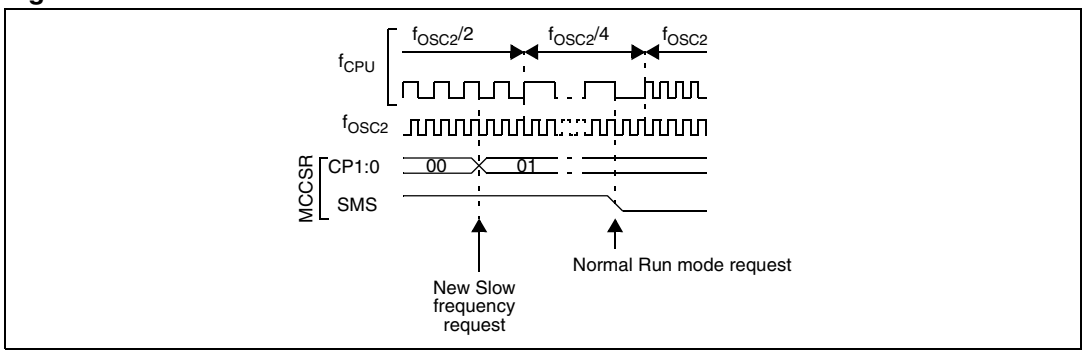


Figure 24. Slow mode clock transitions



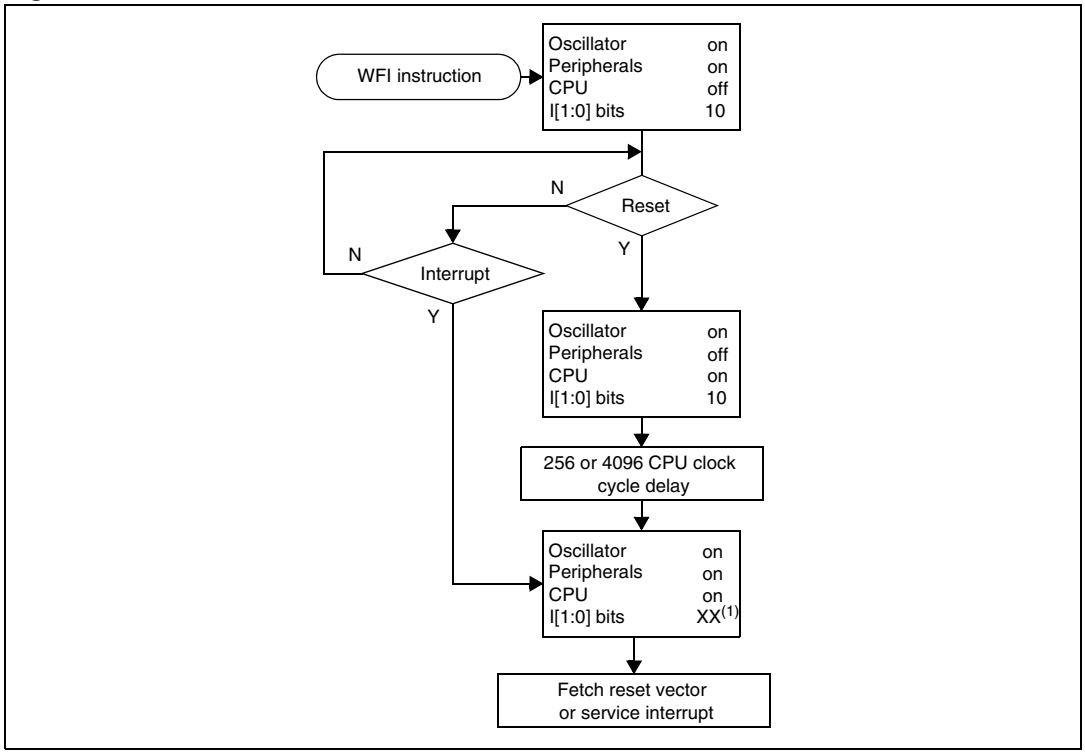
8.3 Wait mode

Wait mode places the MCU in a low power consumption mode by stopping the CPU.

This power saving mode is selected by calling the 'WFI' instruction.

All peripherals remain active. During Wait mode, the I[1:0] bits of the CC register are forced to '10', to enable all interrupts. All other registers and memory remain unchanged. The MCU remains in Wait mode until an interrupt or reset occurs, whereupon the Program Counter branches to the starting address of the interrupt or reset service routine. The MCU will remain in Wait mode until a reset or an interrupt occurs, causing it to wake up. Refer to *Figure 25*.

Figure 25. Wait mode flowchart



1. Before servicing an interrupt, the CC register is pushed on the stack. The I[1:0] bits of the CC register are set to the current software priority level of the interrupt routine and recovered when the CC register is popped.

Figure 28. Halt timing overview

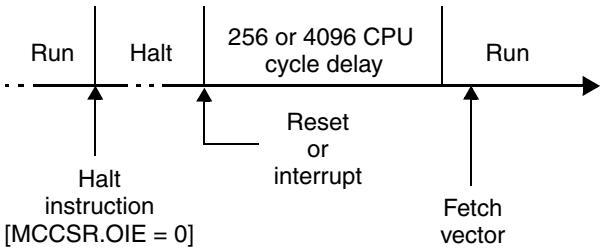
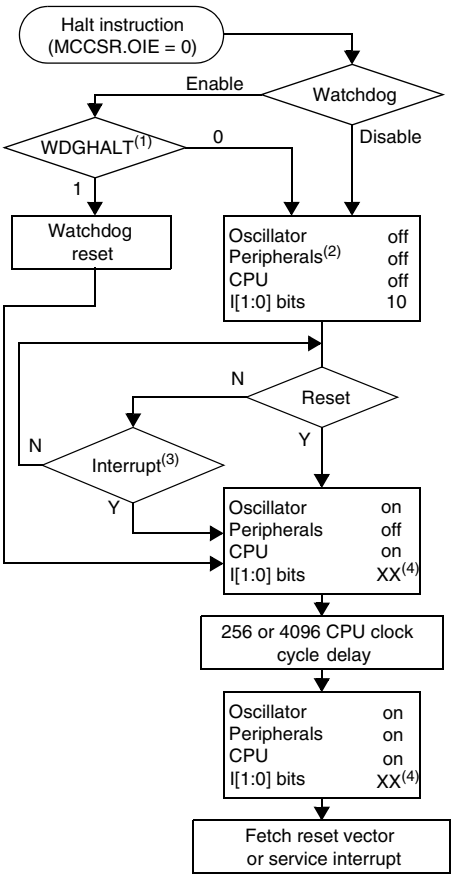


Figure 29. Halt mode flowchart



1. WDGHALT is an option bit. See *Section 14.1 on page 179* for more details.
2. Peripheral clocked with an external clock source can still be active.
3. Only some specific interrupts can exit the MCU from Halt mode (such as external interrupt). Refer to *Table 25: Interrupt mapping* for more details.
4. Before servicing an interrupt, the CC register is pushed on the stack. The I[1:0] bits of the CC register are set to the current software priority level of the interrupt routine and recovered when the CC register is popped.

MCC beep control register (MCCBCR)

MCCBCR Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
Reserved						BC[1:0]	
-						R/W	

Table 41. MCCBCR register description

Bit	Name	Function
7:2	-	Reserved, must be kept cleared
1:0	BC[1:0]	Beep Control These 2 bits select the PF1 pin beep capability (see *Table 42*). The beep output signal is available in Active-halt mode but has to be disabled to reduce the consumption.

Table 42. Beep frequency selection

BC1	BC0	Beep mode with f_{OSC2} = 8 MHz	
0	0	Off	
0	1	~2 kHz	Output Beep signal ~50% duty cycle
1	0	~1 kHz	
1	1	~500 Hz	

Table 43. Main clock controller register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
002Bh	SICSR Reset value	0	AVDIE 0	AVDF 0	LVDRF x	0	0	0	WDGRF x
002Ch	MCCSR Reset value	MCO 0	CP1 0	CP0 0	SMS 0	TB1 0	TB0 0	OIE 0	OIF 0
002Dh	MCCBCR Reset value	0	0	0	0	0	0	BC1 0	BC0 0

Note: 1 After reading the ICiHR register, transfer of input capture data is inhibited and ICFi will never be set until the ICiLR register is also read.

2 The ICiR register contains the free running counter value which corresponds to the most recent input capture.

3 The two input capture functions can be used together even if the timer also uses the two output compare functions.

4 In One pulse mode and PWM mode only Input Capture 2 can be used.

5 The alternate inputs (ICAP1 and ICAP2) are always directly connected to the timer. So any transitions on these pins activates the input capture function.
Moreover if one of the ICAPi pins is configured as an input and the second one as an output, an interrupt can be generated if the user toggles the output pin and if the ICIE bit is set.
This can be avoided if the input capture function i is disabled by reading the ICiHR (see note 1).

6 The TOF bit can be used with interrupt generation in order to measure events that go beyond the timer range (FFFFh).

Figure 41. Input capture block diagram

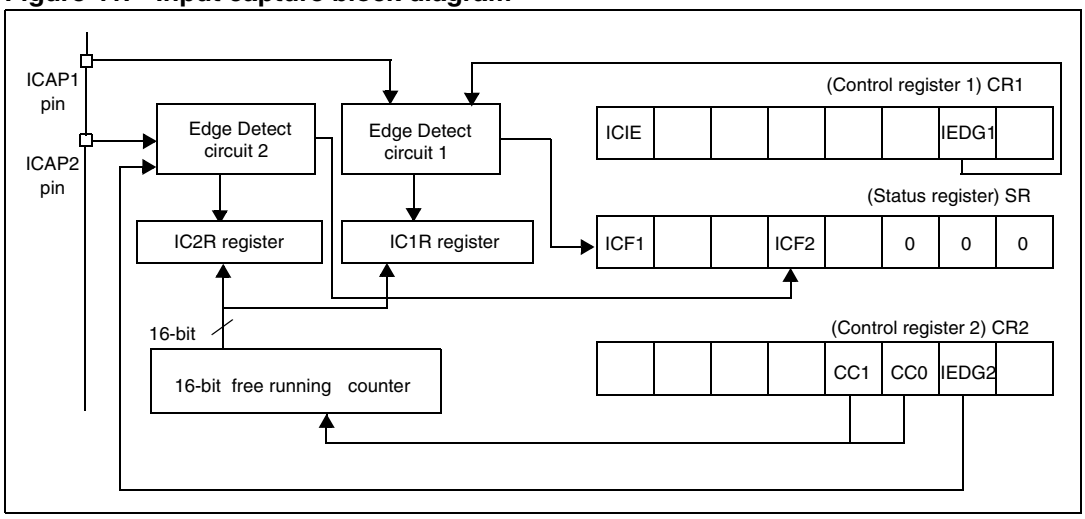
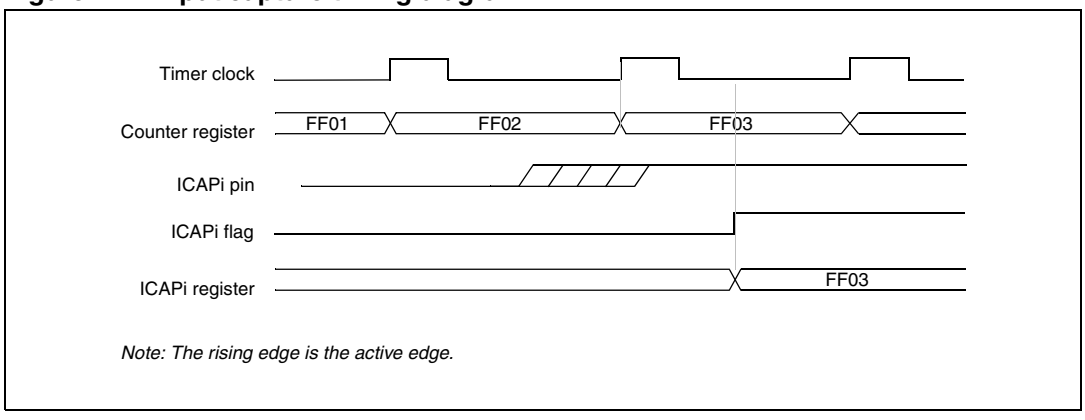


Figure 42. Input capture timing diagram



Note: The rising edge is the active edge.

Output compare

In this section, the index, *i*, may be 1 or 2 because there are two output compare functions in the 16-bit timer.

This function can be used to control an output waveform or indicate when a period of time has elapsed.

When a match is found between the Output Compare register and the free running counter, the output compare function:

- Assigns pins with a programmable value if the OC*i*E bit is set
- Sets a flag in the status register
- Generates an interrupt if enabled

Two 16-bit registers Output Compare register 1 (OC1R) and Output Compare register 2 (OC2R) contain the value to be compared to the counter register each timer clock cycle.

Table 45. Output compare byte distribution

Register	MS byte	LS byte
OCiR	OC*i*HR	OC*i*LR

These registers are readable and witable and are not affected by the timer hardware. A reset event changes the OC*i*R value to 8000h.

Timing resolution is one count of the free running counter: (f_{CPU}/CC[1:0]).

Procedure

To use the Output Compare function, select the following in the CR2 register:

- Set the OC*i*E bit if an output is needed then the OCMP*i* pin is dedicated to the output compare *i* signal.
- Select the timer clock (CC[1:0]) (see *Table 50*).

And select the following in the CR1 register:

- Select the OLVL*i* bit to applied to the OCMP*i* pins after the match occurs.
- Set the OCIE bit to generate an interrupt if it is needed.

When a match is found between OCRi register and CR register:

- OCF*i* bit is set
- The OCMP*i* pin takes OLVL*i* bit value (OCMP*i* pin latch is forced low during reset)
- A timer interrupt is generated if the OCIE bit is set in the CR1 register and the I bit is cleared in the CC register (CC).

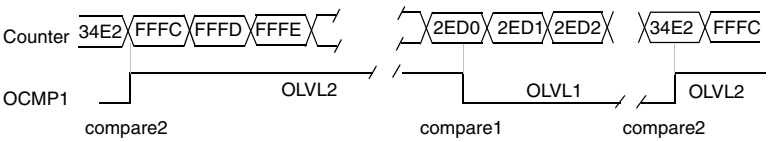
The OC*i*R register value required for a specific timing application can be calculated using the following formula:

$$\Delta \text{ OC}i\text{R} = \frac{\Delta t * f_{CPU}}{\text{PRESC}}$$

Where:

Δt = Output compare period (in seconds)
f_{CPU} = CPU clock frequency (in hertz)
PRESC = Timer prescaler factor (2, 4 or 8 depending on CC[1:0] bits; see *Table 50*)

Figure 48. Pulse width modulation mode timing example with two output compare functions(1)(2)



1. OC1R = 2ED0h, OC2R = 34E2, OLVL1 = 0, OLVL2 = 1
2. On timers with only one Output Compare register, a fixed frequency PWM signal can be generated using the output compare and the counter overflow to define the pulse length.

Pulse Width Modulation mode

Pulse Width Modulation (PWM) mode enables the generation of a signal with a frequency and pulse length determined by the value of the OC1R and OC2R registers.

Pulse Width Modulation mode uses the complete Output Compare 1 function plus the OC2R register, and so this functionality can not be used when PWM mode is activated.

In PWM mode, double buffering is implemented on the output compare registers. Any new values written in the OC1R and OC2R registers are taken into account only at the end of the PWM period (OC2) to avoid spikes on the PWM output pin (OCMP1).

Procedure

To use Pulse Width Modulation mode:

1. Load the OC2R register with the value corresponding to the period of the signal using the formula below.
2. Load the OC1R register with the value corresponding to the period of the pulse if (OLVL1 = 0 and OLVL2 = 1) using the formula in the opposite column.
3. Select the following in the CR1 register:
   - Using the OLVL1 bit, select the level to be applied to the OCMP1 pin after a successful comparison with the OC1R register.
   - Using the OLVL2 bit, select the level to be applied to the OCMP1 pin after a successful comparison with the OC2R register.
4. Select the following in the CR2 register:
   - Set OC1E bit: the OCMP1 pin is then dedicated to the output compare 1 function.
   - Set the PWM bit.
   - Select the timer clock (CC[1:0]) (see *Table 50*).

Table 55. SPICR register description

Bit	Name	Function
7	SPIE	Serial Peripheral Interrupt Enable This bit is set and cleared by software. 0: Interrupt is inhibited. 1: An SPI interrupt is generated whenever SPIF = 1, MODF = 1 or OVR = 1 in the SPICSR register.
6	SPE	Serial Peripheral Output Enable This bit is set and cleared by software. It is also cleared by hardware when, in master mode, $\overline{SS}$ = 0 (see *Master mode fault (MODF) on page 102*). The SPE bit is cleared by reset, so the SPI peripheral is not initially connected to the external pins. 0: I/O pins free for general purpose I/O 1: SPI I/O pin alternate functions enabled
5	SPR2	Divider Enable This bit is set and cleared by software and is cleared by reset. It is used with the SPR[1:0] bits to set the baud rate. Refer to *Table 56: SPI master mode SCK frequency*. 0: Divider by 2 enabled 1: Divider by 2 disabled *Note: This bit has no effect in slave mode.*
4	MSTR	Master mode This bit is set and cleared by software. It is also cleared by hardware when, in master mode, $\overline{SS}$ = 0 (see *Master mode fault (MODF) on page 102*). 0: Slave mode 1: Master mode. The function of the SCK pin changes from an input to an output and the functions of the MISO and MOSI pins are reversed.
3	CPOL	Clock Polarity This bit is set and cleared by software. This bit determines the idle state of the serial Clock. The CPOL bit affects both the master and slave modes. 0: SCK pin has a low level idle state 1: SCK pin has a high level idle state *Note: If CPOL is changed at the communication byte boundaries, the SPI must be disabled by resetting the SPE bit.*
2	CPHA	Clock Phase This bit is set and cleared by software. 0: The first clock transition is the first data capture edge. 1: The second clock transition is the first capture edge. *Note: The slave must have the same CPOL and CPHA settings as the master.*
1:0	SPR[1:0]	Serial clock frequency These bits are set and cleared by software. Used with the SPR2 bit, they select the baud rate of the SPI serial clock SCK output by the SPI in master mode (see *Table 56*). *Note: These 2 bits have no effect in slave mode.*

Table 56. SPI master mode SCK frequency

Serial clock	SPR2	SPR1	SPR0
$f_{CPU}/4$	1	0	0
$f_{CPU}/8$	0	0	0

Table 58. SPI register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0021h	SPIDR Reset value	MSB x	x	x	x	x	x	x	LSB x
0022h	SPICR Reset value	SPIE 0	SPE 0	SPR2 0	MSTR 0	CPOL x	CPHA x	SPR1 x	SPR0 x
0023h	SPICSR Reset value	SPIF 0	WCOL 0	OVR 0	MODF 0	0	SOD 0	SSM 0	SSI 0

10.5 Serial communications interface (SCI)

10.5.1 Introduction

The serial communications interface (SCI) offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. The SCI offers a very wide range of baud rates using two baud rate generator systems.

10.5.2 Main features

- Full duplex, asynchronous communications
- NRZ standard format (mark/space)
- Dual baud rate generator systems
- Independently programmable transmit and receive baud rates up to 500K baud.
- Programmable data word length (8 or 9 bits)
- Receive buffer full, Transmit buffer empty and End of Transmission flags
- 2 receiver wakeup modes
  - Address bit (MSB)
  - Idle line
- Muting function for multiprocessor configurations
- Separate enable bits for Transmitter and Receiver
- 4 error detection flags
  - Overrun error
  - Noise error
  - Frame error
  - Parity error
- 5 interrupt sources with flags
  - Transmit data register empty
  - Transmission complete
  - Receive data register full
  - Idle line received
  - Overrun error detected

- Parity control
  - Transmits parity bit
  - Checks parity of received data byte
- Reduced power consumption mode

10.5.3 General description

The interface is externally connected to another device by two pins (see *Figure 58*):

- TDO: Transmit Data Output. When the transmitter and the receiver are disabled, the output pin returns to its I/O port configuration. When the transmitter and/or the receiver are enabled and nothing is to be transmitted, the TDO pin is at high level.
- RDI: Receive Data Input is the serial data input. Oversampling techniques are used for data recovery by discriminating between valid incoming data and noise.

Through these pins, serial data is transmitted and received as frames comprising:

- an Idle Line prior to transmission or reception
- a start bit
- a data word (8 or 9 bits) least significant bit first
- a Stop bit indicating that the frame is complete

This interface uses two types of baud rate generator:

- a conventional type for commonly-used baud rates
- an extended type with a prescaler offering a very wide range of baud rates even with non-standard oscillator frequencies

10.6 10-bit A/D converter (ADC)

10.6.1 Introduction

The on-chip analog-to-digital converter (ADC) peripheral is a 10-bit, successive approximation converter with internal sample and hold circuitry. This peripheral has up to 16 multiplexed analog input channels (refer to device pin out description) that allow the peripheral to convert the analog voltage levels from up to 16 different sources.

The result of the conversion is stored in a 10-bit Data Register. The A/D converter is controlled through a Control/Status Register.

10.6.2 Main features

- 10-bit conversion
- Up to 16 channels with multiplexed input
- Linear successive approximation
- Data register (DR) which contains the results
- Conversion complete status flag
- On/off bit (to reduce consumption)

The block diagram is shown in *Figure 61*.

Figure 61. ADC block diagram

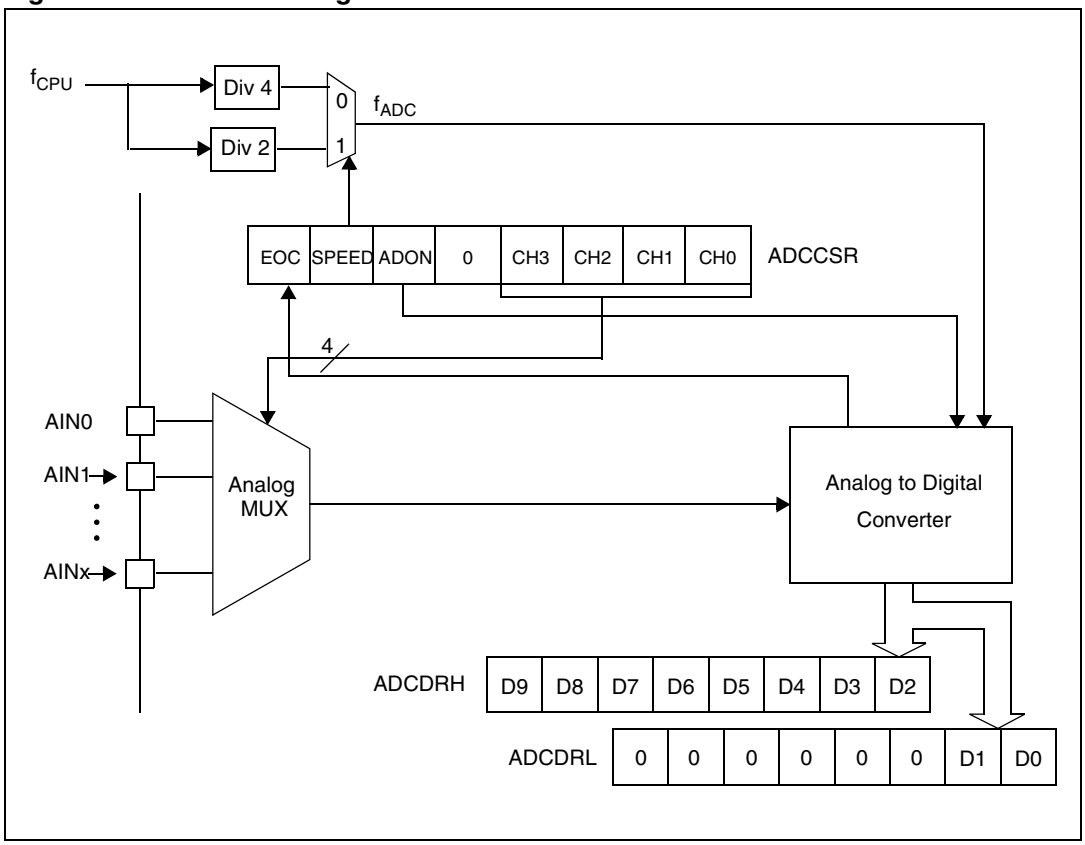


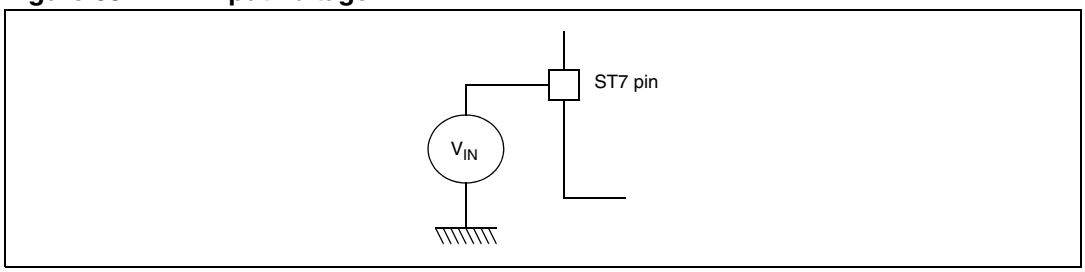
Table 82. Instruction set overview (continued)

Mnemo	Description	Function/example	Dst	Src	I1	H	I0	N	Z	C
JRUGT	Jump if (C + Z = 0)	Unsigned >								
JRULE	Jump if (C + Z = 1)	Unsigned <=								
LD	Load	dst <= src	reg, M	M, reg				N	Z	
MUL	Multiply	X,A = X * A	A, X, Y	X, Y, A		0				0
NEG	Negate (2's compl)	neg $10	reg, M					N	Z	C
NOP	No Operation									
OR	OR operation	A = A + M	A	M				N	Z	
POP	Pop from the Stack	pop reg	reg	M						
		pop CC	CC	M	I1	H	I0	N	Z	C
PUSH	Push onto the Stack	push Y	M	reg, CC						
RCF	Reset carry flag	C = 0								0
RIM	Enable Interrupts	I1:0 = 10 (level 0)			1		0			
RLC	Rotate Left true C	C <= A <= C	reg, M					N	Z	C
RRC	Rotate Right true C	C => A => C	reg, M					N	Z	C
RSP	Reset Stack Pointer	S = Max allowed								
SBC	Subtract with Carry	A = A - M - C	A	M				N	Z	C
SCF	Set CARRY FLAG	C = 1								1
SIM	Disable Interrupts	I1:0 = 11 (level 3)			1		1			
SLA	Shift Left Arithmetic	C <= A <= 0	reg, M					N	Z	C
SLL	Shift Left Logic	C <= A <= 0	reg, M					N	Z	C
SRL	Shift Right Logic	0 => A => C	reg, M					0	Z	C
SRA	Shift Right Arithmetic	A7 => A => C	reg, M					N	Z	C
SUB	Subtraction	A = A - M	A	M				N	Z	C
SWAP	SWAP nibbles	A7-A4 <=> A3-A0	reg, M					N	Z	
TNZ	Test for Neg and Zero	tnz lbl1						N	Z	
TRAP	S/W TRAP	S/W interrupt			1		1			
WFI	Wait for Interrupt				1		0			
XOR	Exclusive OR	A = A XOR M	A	M				N	Z	

12.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 63*.

Figure 63. Pin input voltage



12.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

12.2.1 Voltage characteristics

Table 83. Voltage characteristics

Symbol	Ratings	Maximum value	Unit
V_{DD} - V_{SS}	Supply voltage	6.5	V
V_{PP} - V_{SS}	Programming voltage	13	
V_{IN} (1)(2)	Input voltage on true open drain pin	V_{SS} - 0.3 to 6.5	
	Input voltage on any other pin	V_{SS} - 0.3 to V_{DD} + 0.3	
$\lvert\Delta V_{DDx}\rvert$ and $\lvert\Delta V_{SSx}\rvert$	Variations between different digital power pins	50	mV
$\lvert V_{SSA} - V_{SSx}\rvert$	Variations between digital and analog ground pins	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 12.8.3 on page 157*	
$V_{ESD(MM)}$	Electrostatic discharge voltage (machine model)		

1. Directly connecting the $\overline{\text{RESET}}$ and I/O pins to V_{DD} or V_{SS} could damage the device if an unintentional internal reset is generated or an unexpected change of the I/O configuration occurs (for example, due to a corrupted program counter). To guarantee safe operation, this connection has to be done through a pull-up or pull-down resistor (typical: 4.7 kΩ for $\overline{\text{RESET}}$, 10 kΩ for I/Os). For the same reason, unused I/O pins must not be directly tied to V_{DD} or V_{SS}.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly ensured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected.

12.4 LVD/AVD characteristics

12.4.1 Operating conditions with LVD

Subject to general operating conditions for T_A.

Table 87. Operating conditions with LVD

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IT+(LVD)}$	Reset release threshold (V_{DD} rise)	VD level = high in option byte	4.0(1)	4.2	4.5	V
		VD level = med. in option byte(2)	3.55(1)	3.75	4.0(1)	
		VD level = low in option byte(2)	2.95(1)	3.15	3.35(1)	
$V_{IT-(LVD)}$	Reset generation threshold (V_{DD} fall)	VD level = high in option byte	3.8	4.0	4.25(1)	
		VD level = med. in option byte(2)	3.35(1)	3.55	3.75(1)	
		VD level = low in option byte(2)	2.8(1)	3.0	3.15(1)	
$V_{hys(LVD)}$	LVD voltage threshold hysteresis(1)	$V_{IT+(LVD)}$-$V_{IT-(LVD)}$	150	200	250	mV
Vt_{POR}	V_{DD} rise time(1)	Flash devices	6µs/V		100ms/V	
		8/16 Kbyte ROM devices			20ms/V	
		32 Kbyte ROM devices			∝ ms/V	
$t_{g(VDD)}$	Filtered glitch delay on V_{DD}(1)	Not detected by the LVD			40	ns

1. Data based on characterization results, tested in production for ROM devices only.
2. If the medium or low thresholds are selected, the detection may occur outside the specified operating voltage range.

12.4.2 Auxiliary voltage detector (AVD) thresholds

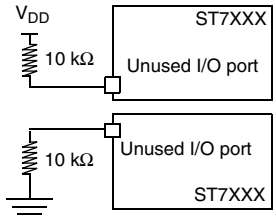
Subject to general operating conditions for T_A.

Table 88. AVD thresholds

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IT+(AVD)}$	1 ⇒0 AVDF flag toggle threshold (V_{DD} rise)	VD level = high in option byte	4.4(1)	4.6	4.9	V
		VD level = med. in option byte	3.95(1)	4.15	4.4(1)	
		VD level = low in option byte	3.4(1)	3.6	3.8(1)	
$V_{IT-(AVD)}$	0 ⇒1 AVDF flag toggle threshold (V_{DD} fall)	VD level = high in option byte	4.2	4.4	4.65(1)	
		VD level = med. in option byte	3.75(1)	4.0	4.2(1)	
		VD level = low in option byte	3.2(1)	3.4	3.6(1)	
$V_{hys(AVD)}$	AVD voltage threshold hysteresis	$V_{IT+(AVD)}$-$V_{IT-(AVD)}$		200		mV
ΔV_{IT-}	Voltage drop between AVD flag set and LVD reset activated	$V_{IT-(AVD)}$-$V_{IT-(LVD)}$		450		

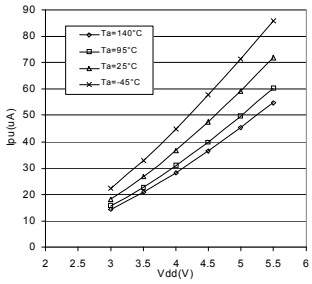
1. Data based on characterization results, tested in production for ROM devices only.

Figure 70. Unused I/O pins configured as input(1)



1. I/O can be left unconnected if it is configured as output (0 or 1) by the software. This has the advantage of greater EMC robustness and lower cost.

Figure 71. Typical I_{PU} vs. V_{DD} with $V_{IN} = V_{SS}$



12.9.2 Output driving current

Subject to general operating conditions for V_{DD}, f_{CPU}, and T_A unless otherwise specified.

Table 107. Output driving current

Symbol	Parameter	Conditions		Min	Max	Unit
V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time (see *Figure 72*)	V_{DD} = 5V	I_{IO} = +5 mA		1.2	V
			I_{IO} = +2 mA		0.5	
	Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time (see *Figure 73* and *Figure 75*)		I_{IO} = +20 mA $T_A \leq 85$ °C $T_A > 85$ °C		 1.3 1.5	
			I_{IO} = +8 mA		0.6	
V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time (see *Figure 74* and *Figure 77*)		I_{IO} = -5 mA, $T_A \leq 85$ °C $T_A > 85$ °C	 V_{DD} - 1.4 V_{DD} - 1.6		
			I_{IO} = -2 mA	V_{DD} - 0.7		

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Section 12.2.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Section 12.2.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}. True open drain I/O pins do not have V_{OH}.

16 Revision history

Table 126. Document revision history

Date	Revision	Changes
05-May-2004	2.0	Merged ST72F324 Flash with ST72324B ROM datasheet. Vt POR max modified in *Section 12.4 on page 145* Added *Figure 79 on page 164* Modified V_{AREF} min in *"10-bit ADC characteristics" on page 168* Modified I INJ for PB0 in *Section 12.9 on page 158* Added *"Clearing active interrupts outside interrupt routine" on page 187* Modified "32K ROM DEVICES ONLY" on page 165
30-Mar-2005	3	Removed Clock Security System (CSS) throughout document Added notes on ST72F324B 8K/16K Flash devices in Table 27 Corrected MCO description in *Section 10.2 on page 69* Modified VtPOR in *Section 12.4 on page 145* Static current consumption modified in *Section 12.9 on page 158* Updated footnote and *Figure 78 on page 163* and *Figure 79 on page 164* Modified Soldering information in *Section 13.6* Updated *Section 14 on page 178* Added Table 27 Modified *Figure 8 on page 25* and note 4 in *"Flash program memory" on page 23* Added limitation on ICC entry mode with 39 pulses to *"Known limitations" on page 185* Added Section 16 on page 166 for ST72F324B 8K/16K Flash devices Modified "Internal Sales Types on box label" in Table 29 on page 157
12-Sep-2005	4	Removed notes related to ST72F324, refer to datasheet rev 3 for specifications on older devices. Note: This datasheet rev refers only to ST72F324B and ST72324B. Changed character transmission procedure in *Section on page 112* Updated Vt POR max in *Section 12.4 on page 145* Updated Current Consumption for in *Section 12.5 on page 146* Added oscillator diagram and table to *Section 12.6.3 on page 150* Increased Data retention max. parameter in *Section 12.7.2 on page 154* Updated ordering Section 14.3 on page 155 and Section 14.5 on page 157 Updated Development tools *Section 14.3 on page 183* Added "external interrupt missed" in *Section 15.1 on page 185*
06-Feb-2006	5	Added description of SICSR register at address 2Bh in *Table 3 on page 20* Changed description on port PF2 to add internal pull-up in *Section 9.5.1 on page 63* Highlighted note in SPI *"Master mode operation" on page 99* Changed *"Static latch-up" on page 157* Added note 5 on analog input static current consumption *"General characteristics" on page 158* Updated notes in *"Thermal characteristics" on page 177*