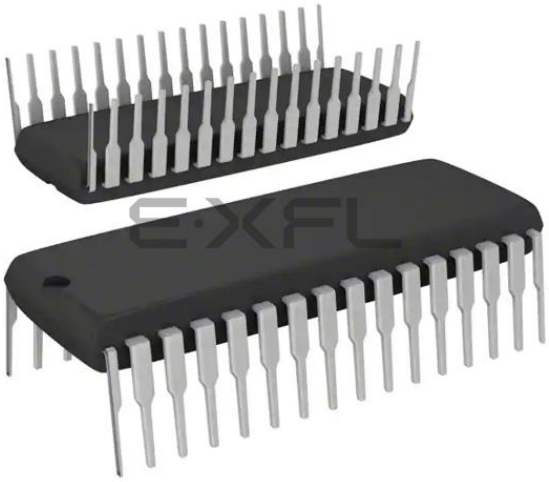


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72f324bk4m6

Table 3. Hardware register map (continued)

Address	Block	Register label	Register name	Reset status	Remarks
0041h	Timer B	TBCR2	Timer B control register 2	00h	R/W
0042h		TBCR1	Timer B control register 1	00h	R/W
0043h		TBCSR	Timer B control/status register	xxxx x0xxb	R/W
0044h		TBIC1HR	Timer B input capture 1 high register	xxh	Read only
0045h		TBIC1LR	Timer B input capture 1 low register	xxh	Read only
0046h		TBOC1HR	Timer B output compare 1 high register	80h	R/W
0047h		TBOC1LR	Timer B output compare 1 low register	00h	R/W
0048h		TBCHR	Timer B counter high register	FFh	Read only
0049h		TBCLR	Timer B counter low register	FCh	Read only
004Ah		TBACHR	Timer B alternate counter high register	FFh	Read only
004Bh		TBACLR	Timer B alternate counter low register	FCh	Read only
004Ch		TBIC2HR	Timer B input capture 2 high register	xxh	Read only
004Dh		TBIC2LR	Timer B input capture 2 low register	xxh	Read only
004Eh		TBOC2HR	Timer B output compare 2 high register	80h	R/W
004Fh		TBOC2LR	Timer B output compare 2 low register	00h	R/W
0050h	SCI	SCISR	SCI status register	C0h	Read only
0051h		SCIDR	SCI data register	xxh	R/W
0052h		SCIBRR	SCI baud rate register	00h	R/W
0053h		SCICR1	SCI control register 1	x000 0000b	R/W
0054h		SCICR2	SCI control register 2	00h	R/W
0055h		SCIERPR	SCI extended receive prescaler register	00h	R/W
0056h			Reserved area	---	
0057h		SCIETPR	SCI extended transmit prescaler register	00h	R/W
0058h to 006Fh	Reserved area (24 bytes)				
0070h	ADC	ADCCSR	Control/status register	00h	R/W
0071h		ADCDRH	Data high register	00h	Read only
0072h		ADCDRL	Data low register	00h	Read only
0073h 007Fh	Reserved area (13 bytes)				

1. The bits associated with unavailable pins must always keep their reset value.
2. The contents of the I/O port DR registers are readable only in output configuration. In input configuration, the values of the I/O pins are returned instead of the DR register contents.

Legend: x = undefined, R/W = read/write

4.5 ICP (in-circuit programming)

To perform ICP the microcontroller must be switched to ICC (in-circuit communication) mode by an external controller or programming tool.

Depending on the ICP code downloaded in RAM, Flash memory programming can be fully customized (number of bytes to program, program locations, or selection serial communication interface for downloading).

When using an STMicroelectronics or third-party programming tool that supports ICP and the specific microcontroller device, the user needs only to implement the ICP hardware interface on the application board (see *Figure 8*). For more details on the pin locations, refer to the device pinout description.

4.6 IAP (in-application programming)

This mode uses a BootLoader program previously stored in Sector 0 by the user (in ICP mode or by plugging the device in a programming tool).

This mode is fully controlled by user software. This allows it to be adapted to the user application, (such as user-defined strategy for entering programming mode, choice of communications protocol used to fetch the data to be stored). For example, it is possible to download code from the SPI, SCI, USB or CAN interface and program it in the Flash. IAP mode can be used to program any of the Flash sectors except Sector 0, which is write/erase protected to allow recovery in case errors occur during the programming operation.

4.7 Related documentation

For details on Flash programming and ICC protocol, refer to the *ST7 Flash Programming Reference Manual* and to the *ST7 ICC Protocol Reference Manual*.

4.7.1 Flash Control/Status Register (FCSR)

This register is reserved for use by programming tool software. It controls the Flash programming and erasing operations.

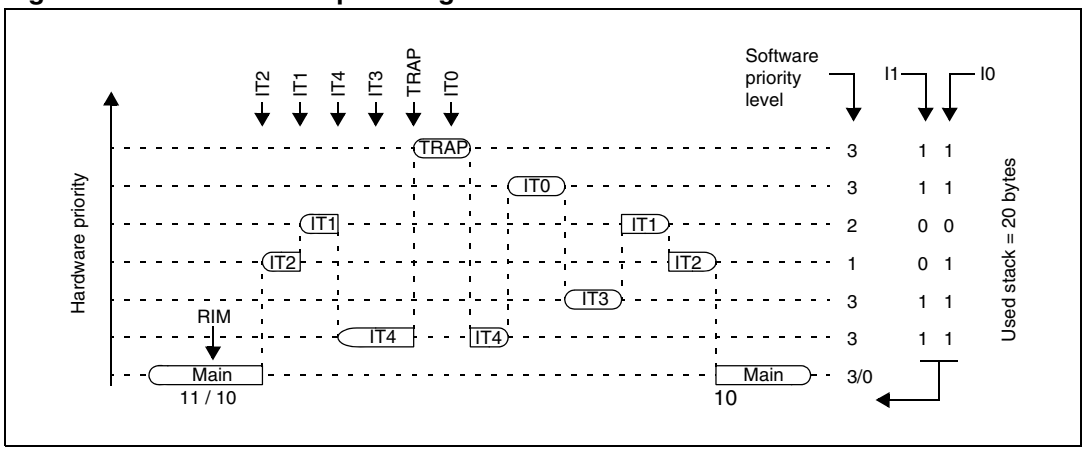
FCSR Reset value:0000 0000 (00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 5. Flash control/status register address and reset value

Address (Hex)	Register label	7	6	5	4	3	2	1	0
0029h	FCSR reset value	0	0	0	0	0	0	0	0

Figure 21. Nested interrupt management



7.5 Interrupt registers

7.5.1 CPU CC register interrupt bits

CPU CC Reset value: 111x 1010(xAh)

7	6	5	4	3	2	1	0
1	1	**I1**	H	**I0**	N	Z	C
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 15. CPU CC register interrupt bits description

Bit	Name	Function
5	I1	Software Interrupt Priority 1
3	I0	Software Interrupt Priority 0

Table 16. Interrupt software priority levels

Interrupt software priority	Level	I1	I0
Level 0 (main)	Low	1	0
Level 1	↓	0	1
Level 2	↓	0	0
Level 3 (= interrupt disable)(1)	High	1	1

1. TRAP and RESET events can interrupt a level 3 program.

These two bits indicate the current interrupt software priority (see *Table 16*) and are set/cleared by hardware when entering in interrupt. The loaded value is given by the corresponding bits in the interrupt software priority registers (ISPRx).

They can be also set/cleared by software with the RIM, SIM, HALT, WFI, IRET and PUSH/POP instructions (see *Table 18: Dedicated interrupt instruction set*).

10.2.2 Clock-out capability

The clock-out capability is an alternate function of an I/O port pin that outputs the f_{CPU} clock to drive external devices. It is controlled by the MCO bit in the MCCSR register.

Caution: When selected, the clock out pin suspends the clock during Active-halt mode.

10.2.3 Real-time clock (RTC) timer

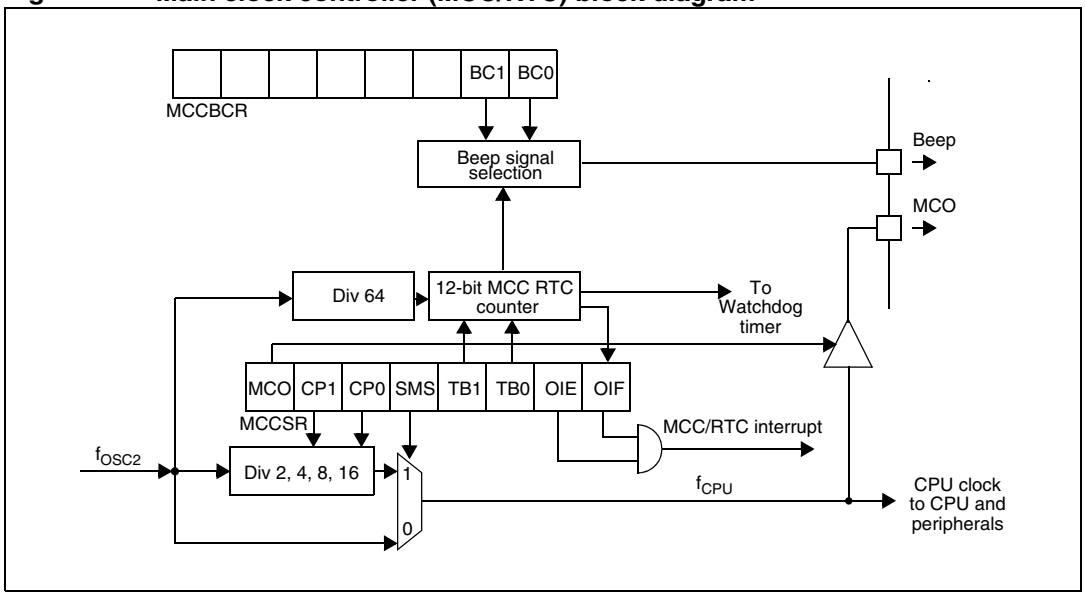
The counter of the real-time clock timer allows an interrupt to be generated based on an accurate real-time clock. Four different time bases depending directly on f_{OSC2} are available. The whole functionality is controlled by four bits of the MCCSR register: TB[1:0], OIE and OIF.

When the RTC interrupt is enabled (OIE bit set), the ST7 enters Active-halt mode when the HALT instruction is executed. See *Section 8.4: Active-halt and Halt modes on page 54* for more details.

10.2.4 Beeper

The beep function is controlled by the MCCBCR register. It can output three selectable frequencies on the Beep pin (I/O port alternate function).

Figure 35. Main clock controller (MCC/RTC) block diagram



10.3 16-bit timer

10.3.1 Introduction

The timer consists of a 16-bit free-running counter driven by a programmable prescaler.

It may be used for a variety of purposes, including pulse length measurement of up to two input signals (input capture) or generation of up to two output waveforms (output compare and PWM).

Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler and the CPU clock prescaler.

Some ST7 devices have two on-chip 16-bit timers. They are completely independent, and do not share any resources. They are synchronized after a MCU reset as long as the timer clock frequencies are not modified.

This description covers one or two 16-bit timers. In ST7 devices with two timers, register names are prefixed with TA (Timer A) or TB (Timer B).

10.3.2 Main features

- Programmable prescaler: f_{CPU} divided by 2, 4 or 8
- Overflow status flag and maskable interrupt
- External clock input (must be at least four times slower than the CPU clock speed) with the choice of active edge
- 1 or 2 output compare functions each with:
  - 2 dedicated 16-bit registers
  - 2 dedicated programmable signals
  - 2 dedicated status flags
  - 1 dedicated maskable interrupt
- 1 or 2 input capture functions each with:
  - 2 dedicated 16-bit registers
  - 2 dedicated active edge selection signals
  - 2 dedicated status flags
  - 1 dedicated maskable interrupt
- Pulse width modulation mode (PWM)
- One pulse mode
- Reduced power mode
- 5 alternate functions on I/O ports (ICAP1, ICAP2, OCMP1, OCMP2, EXTCLK)(c)

The timer block diagram is shown in *Figure 36*.

c. Some timer pins may not be available (not bonded) in some ST7 devices. Refer to *Section 2: Pin description*. When reading an input signal on a non-bonded pin, the value will always be '1'.

Table 51. CSR register description (continued)

Bit	Name	Function
6	OCF1	Output compare flag 1 0: No match (reset value). 1: The content of the free running counter has matched the content of the OC1R register. To clear this bit, first read the SR register, then read or write the low byte of the OC1R (OC1LR) register.
5	TOF	Timer overflow flag 0: No timer overflow (reset value). 1: The free running counter rolled over from FFFFh to 0000h. To clear this bit, first read the SR register, then read or write the low byte of the CR (CLR) register. *Note: Reading or writing the ACLR register does not clear TOF.*
4	ICF2	Input capture flag 2 0: No input capture (reset value). 1: An Input Capture has occurred on the ICAP2 pin. To clear this bit, first read the SR register, then read or write the low byte of the IC2R (IC2LR) register.
3	OCF2	Output compare flag 2 0: No match (reset value). 1: The content of the free running counter has matched the content of the OC2R register. To clear this bit, first read the SR register, then read or write the low byte of the OC2R (OC2LR) register.
2	TIMD	Timer disable This bit is set and cleared by software. When set, it freezes the timer prescaler and counter and disabled the output functions (OCMP1 and OCMP2 pins) to reduce power consumption. Access to the timer registers is still available, allowing the timer configuration to be changed, or the counter reset, while it is disabled. 0: Timer enabled. 1: Timer prescaler, counter and outputs disabled.
1:0	-	Reserved, must be kept cleared.

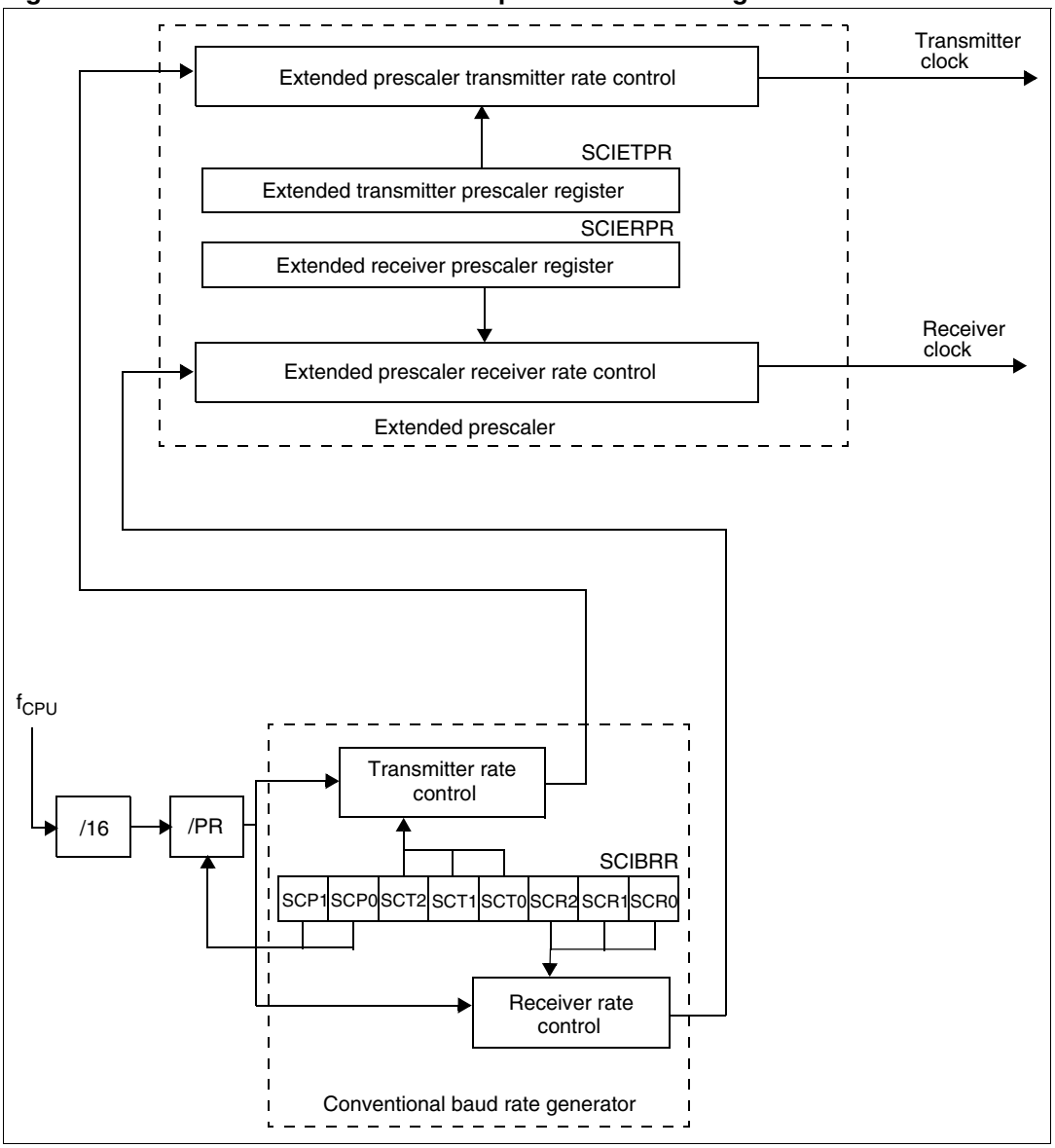
Input capture 1 high register (IC1HR)

This is an 8-bit register that contains the high part of the counter value (transferred by the input capture 1 event).

IC1HR — Reset value: undefined

7	6	5	4	3	2	1	0
MSB							LSB
RO	RO	RO	RO	RO	RO	RO	RO

Figure 59. SCI baud rate and extended prescaler block diagram



Framing error

A framing error is detected when:

- The stop bit is not recognized on reception at the expected time, following either a de-synchronization or excessive noise.
- A break is received.

When the framing error is detected:

- the FE bit is set by hardware
- Data is transferred from the Shift register to the SCIDR register.
- No interrupt is generated. However this bit rises at the same time as the RDRF bit which itself generates an interrupt.

The FE bit is reset by a SCISR register read operation followed by a SCIDR register read operation.

Receiver muting and wakeup feature

In multiprocessor configurations it is often desirable that only the intended message recipient should actively receive the full message contents, thus reducing redundant SCI service overhead for all non-addressed receivers.

The non-addressed devices may be placed in sleep mode by means of the muting function.

Setting the RWU bit by software puts the SCI in sleep mode:

All the reception status bits cannot be set.

All the receive interrupts are inhibited.

A muted receiver may be awakened by one of the following two ways:

- by Idle Line detection if the Wake bit is reset,
- by Address Mark detection if the Wake bit is set.

A receiver wakes up by Idle Line detection when the Receive line has recognized an Idle Frame. Then the RWU bit is reset by hardware but the Idle bit is not set.

A receiver wakes up by Address Mark detection when it received a ‘1’ as the most significant bit of a word, thus indicating that the message is an address. The reception of this particular word wakes up the receiver, resets the RWU bit and sets the RDRF bit, which allows the receiver to receive this word normally and to use it as an address word.

Caution: In Mute mode, do not write to the SCICR2 register. If the SCI is in Mute mode during the read operation (RWU = 1) and an address mark wakeup event occurs (RWU is reset) before the write operation, the RWU bit will be set again by this write operation. Consequently the address byte is lost and the SCI is not woken up from Mute mode.

Parity control

Parity control (generation of parity bit in transmission and parity checking in reception) can be enabled by setting the PCE bit in the SCICR1 register. Depending on the frame length defined by the M bit, the possible SCI frame formats are as listed in *Table 59*.

Table 59. Frame formats(1)(2)

M bit	PCE bit	SCI frame
0	0	| SB | 8 bit data | STB |
0	1	| SB | 7-bit data | PB | STB |
1	0	| SB | 9-bit data | STB |
1	1	| SB | 8-bit data PB | STB |

1. SB = Start bit, STB = Stop bit, and PB = Parity bit.
2. In case of wakeup by an address mark, the MSB bit of the data is taken into account and not the Parity bit.

Table 62. SCISR register description (continued)

Bit	Name	Function
0	PE	Parity error This bit is set by hardware when a parity error occurs in receiver mode. It is cleared by a software sequence (a read to the status register followed by an access to the SCIDR data register). An interrupt is generated if PIE = 1 in the SCICR1 register. 0: No parity error 1: Parity error

SCI Control Register 1 (SCICR1)

SCICR1 Reset value: x000 0000 (x0h)

7	6	5	4	3	2	1	0
R8	T8	SCID	M	WAKE	PCE	PS	PIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 63. SCICR1 register description

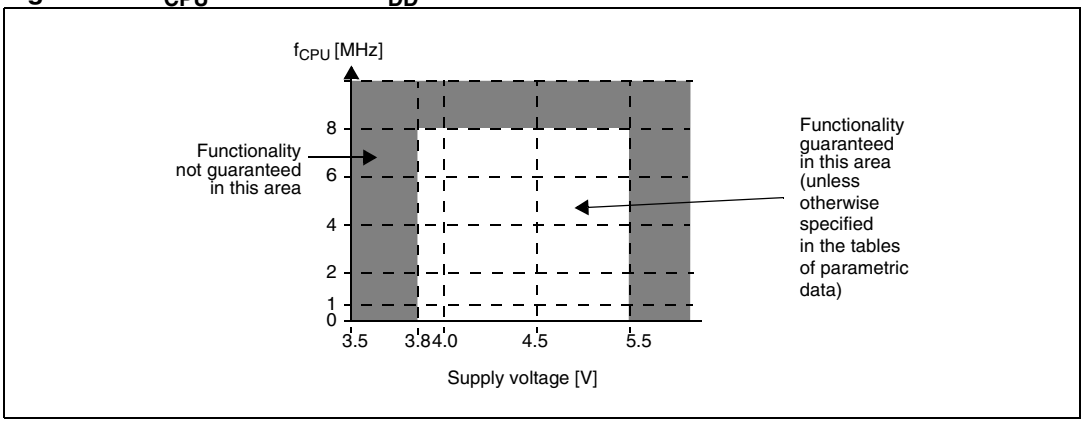
Bit	Name	Function
7	R8	Receive data bit 8 This bit is used to store the 9th bit of the received word when M = 1.
6	T8	Transmit data bit 8 This bit is used to store the 9th bit of the transmitted word when M = 1.
5	SCID	Disabled for low power consumption When this bit is set the SCI prescalers and outputs are stopped and the end of the current byte transfer in order to reduce power consumption.This bit is set and cleared by software. 0: SCI enabled 1: SCI prescaler and outputs disabled
4	M	Word length This bit determines the word length. It is set or cleared by software. 0: 1 Start bit, 8 data bits, 1 Stop bit 1: 1 Start bit, 9 data bits, 1 Stop bit *Note: The M bit must not be modified during a data transfer (both transmission and reception).*
3	WAKE	Wakeup method This bit determines the SCI wakeup method, it is set or cleared by software. 0: Idle line 1: Address mark
2	PCE	Parity control enable This bit selects the hardware parity control (generation and detection). When the parity control is enabled, the computed parity is inserted at the MSB position (9th bit if M = 1; 8th bit if M = 0) and parity is checked on the received data. This bit is set and cleared by software. Once it is set, PCE is active after the current byte (in reception and in transmission). 0: Parity control disabled 1: Parity control enabled

12.3 Operating conditions

Table 86. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal clock frequency		0	8	MHz
V_{DD}	Operating voltage (except Flash Write/Erase)		3.8	5.5	V
	Operating Voltage for Flash Write/Erase	V_{PP} = 11.4 to 12.6 V	4.5	5.5	
T_A	Ambient temperature range	1-suffix version	0	70	°C
		5-suffix version	-10	85	
		6-suffix version	-40	85	
		7-suffix version	-40	105	
		3-suffix version	-40	125	

Figure 64. f_{CPU} max versus V_{DD}



Note: Some temperature ranges are only available with a specific package and memory size. Refer to Section 14: Device configuration and ordering information.

Warning: Do not connect 12 V to V_{PP} before V_{DD} is powered on, as this may damage the device.

13 Package characteristics

13.1 ECOPACK

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

13.2 Package mechanical data

13.2.1 LQFP44 package mechanical data

Figure 89. 44-pin low profile quad flat package outline

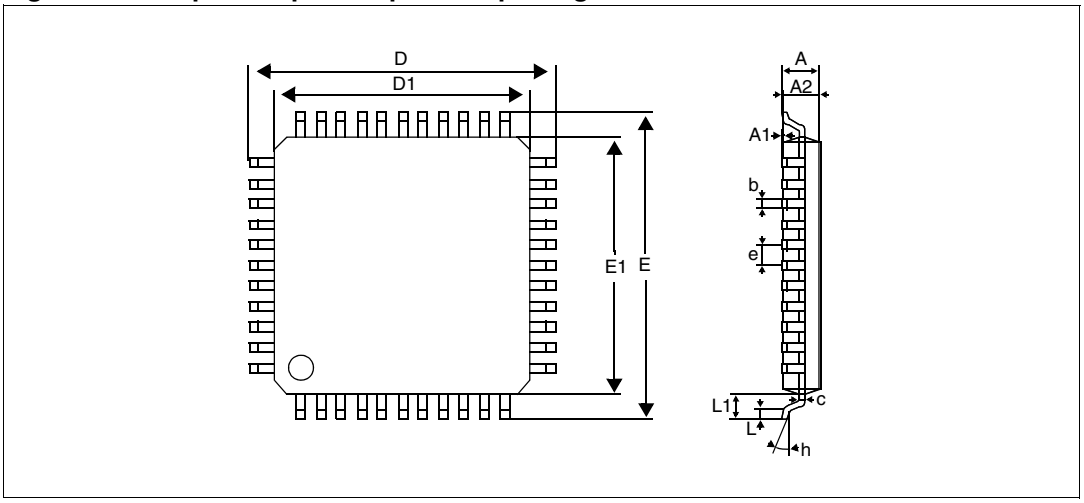


Table 114. 44-pin low profile quad flat package mechanical data

Dim.	mm			inches (1)		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.30	0.37	0.45	0.0118	0.0146	0.0177
C	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	

Table 115. 42-pin dual in line package mechanical data

Dim.	mm			inches (1)		
	Min	Typ	Max	Min	Typ	Max
E	15.24		16.00	0.6000		0.6299
E1	12.70	13.72	14.48	0.5000	0.5402	0.5701
e		1.78			0.0701	
eA		15.24			0.6000	
eB			18.54			0.7299
eC			1.52			0.0598
L	2.54	3.30	3.56	0.1000	0.1299	0.1402
Number of pins						
N	42					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

13.2.3 LQFP32 package mechanical data

Figure 91. 32-pin low profile quad flat package outline

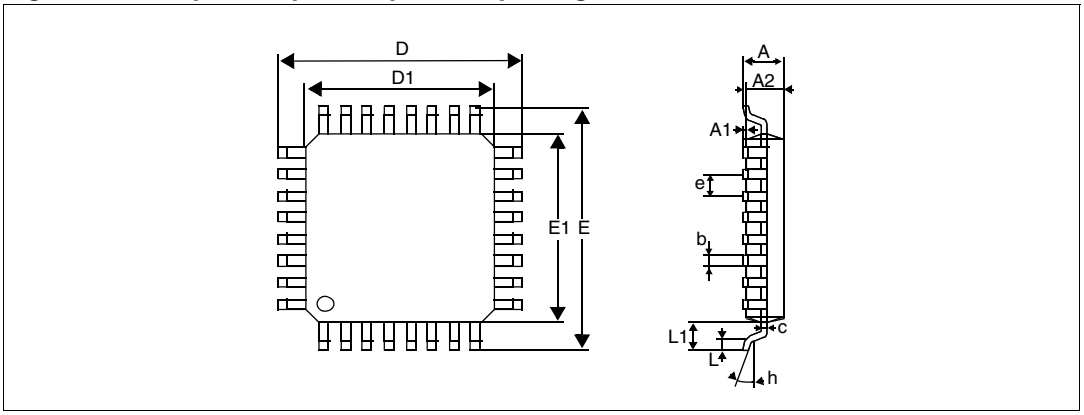


Table 116. 32-pin low profile quad flat package mechanical data

Dim.	mm			inches (1)		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.30	0.37	0.45	0.0118	0.0146	0.0177
C	0.09		0.20	0.0035		0.0079
D		9.00			0.3543	
D1		7.00			0.2756	

Table 117. 32-pin dual in-line package mechanical data (continued)

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E	9.91	10.41	11.05	0.3902	0.4098	0.4350
E1	7.62	8.89	9.40	0.3000	0.3500	0.3701
e		1.78			0.0701	
eA		10.16			0.4000	
eB			12.70			0.5000
eC			1.40			0.0551
L	2.54	3.05	3.81	0.1000	0.1201	0.1500
Number of pins						
N	42					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

14.1 Flash devices

14.1.1 Flash configuration

Table 119. Flash option bytes

	Static option byte 0								Static option byte 1							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	WDG		Res	VD		Reserved		FMP_R	PKG1	RSTC	OSCTYPE		OSCRANGE			PLLOFF
	HALT	SW		1	0						1	0	2	1	0	
Default	1	1	1	0	0	1	1	1	See note 1	1	1	0	0	1	1	1

1. Depends on device type as defined in *Table 122: Package selection (OPT7) on page 181.*

The option bytes allow the hardware configuration of the microcontroller to be selected. They have no address in the memory map and can be accessed only in programming mode (for example using a standard ST7 programming tool). The default content of the Flash is fixed to FFh. To program directly the Flash devices using ICP, Flash devices are shipped to customers with the internal RC clock source. In masked ROM devices, the option bytes are fixed in hardware by the ROM code (see option list).

Table 120. Option byte 0 bit description

Bit	Name	Function
OPT7	WDG HALT	Watchdog reset on Halt This option bit determines if a reset is generated when entering Halt mode while the Watchdog is active. 0: No reset generation when entering Halt mode 1: Reset generation when entering Halt mode
OPT6	WDG SW	Hardware or software Watchdog This option bit selects the Watchdog type. 0: Hardware (Watchdog always enabled) 1: Software (Watchdog to be enabled by software)
OPT5	-	Reserved, must be kept at default value.
OPT4:3	VD[1:0]	Voltage detection These option bits enable the voltage detection block (LVD and AVD) with a selected threshold for the LVD and AVD. 00: Selected LVD = Highest threshold (V_{DD}~4V). 01: Selected LVD = Medium threshold (V_{DD}~3.5V). 10: Selected LVD = Lowest threshold (V_{DD}~3V). 11: LVD and AVD off **Caution:** If the medium or low thresholds are selected, the detection may occur outside the specified operating voltage range. Below 3.8V, device operation is not guaranteed. For details on the AVD and LVD threshold levels refer to *Section 12.4.1 on page 145*.
OPT2:1	-	Reserved, must be kept at default value

Table 121. Option byte 1 bit description (continued)

Bit	Name	Function
OPT0	PLL OFF	PLL activation This option bit activates the PLL which allows multiplication by two of the main input clock frequency. The PLL must not be used with the internal RC oscillator. The PLL is guaranteed only with an input frequency between 2 and 4 MHz. 0: PLL x2 enabled 1: PLL x2 disabled **Caution**: The PLL can be enabled only if the “OSCRANGE” (OPT3:1) bits are configured to “MP - 2~4 MHz”. Otherwise, the device functionality is not guaranteed.

Table 122. Package selection (OPT7)

Version	Selected package	PKG1
J	LQFP44/SDIP42	1
K	LQFP32/SDIP32	0

14.2 ROM devices

14.2.1 Transfer of customer code

Customer code is made up of the ROM/FASTROM contents and the list of the selected options (if any). The ROM/FASTROM contents are to be sent with the S19 hexadecimal file generated by the development tool. All unused bytes must be set to FFh. Complete the appended *ST72324Bxx MICROCONTROLLER OPTION LIST on page 182* to communicate the selected options to STMicroelectronics.

Refer to application note AN1635 for information on the counter listing returned by ST after code has been transferred.

Figure 93: ST72324Bxx ordering information scheme on page 178 serves as a guide for ordering. The STMicroelectronics sales organization will be pleased to provide detailed information on contractual points.

Caution: The readout protection binary value is inverted between ROM and Flash products. The option byte checksum differs between ROM and Flash.

Nested interrupt context

The symptom does not occur when the interrupts are handled normally, that is, when:

- The interrupt flag is cleared within its own interrupt routine
- The interrupt flag is cleared within any interrupt routine with higher or identical priority level
- The interrupt flag is cleared in any part of the code while this interrupt is disabled

If these conditions are not met, the symptom can be avoided by implementing the following sequence:

- PUSH CC
- SIM
- Reset interrupt flag
- POP CC

15.1.5 16-bit timer PWM mode

In PWM mode, the first PWM pulse is missed after writing the value FFFCh in the OC1R register (OC1HR, OC1LR). It leads to either full or no PWM during a period, depending on the OLVL1 and OLVL2 settings.

15.1.6 TIMD set simultaneously with OC interrupt

If the 16-bit timer is disabled at the same time the output compare event occurs then output compare flag gets locked and cannot be cleared before the timer is enabled again.

Impact on the application

If output compare interrupt is enabled, then the output compare flag cannot be cleared in the timer interrupt routine. Consequently the interrupt service routine is called repeatedly.

Workaround

Disable the timer interrupt before disabling the timer. Again while enabling, first enable the timer then the timer interrupts.

- Perform the following to disable the timer:
  - TACR1 or TBCR1 = 0x00h; // Disable the compare interrupt
  - TACSR I or TBCSR I = 0x40; // Disable the timer
- Perform the following to enable the timer again:
  - TACSR & or TBCSR & = ~0x40; // Enable the timer
  - TACR1 or TBCR1 = 0x40; // Enable the compare interrupt

15.1.7 SCI wrong break duration

Description

A single break character is sent by setting and resetting the SBK bit in the SCICR2 register. In some cases, the break character may have a longer duration than expected:

- 20 bits instead of 10 bits if M = 0
- 22 bits instead of 11 bits if M = 1

Table 125. Port A and F configuration

PLL	PA3	PF4	PF1	PF0	Clock disturbance
Off	0	1	0	Toggling	Maximum 2 clock cycles lost at each rising or falling edge of PF0
On	0	1	0	1	Maximum 1 clock cycle lost out of every 16

As a consequence, for cycle-accurate operations, these configurations are prohibited in either input or output mode.

Workaround

To avoid this from occurring, it is recommended to connect one of these pins to GND (PF4 or PF0) or V_{DD} (PA3 or PF1).

16 Revision history

Table 126. Document revision history

Date	Revision	Changes
05-May-2004	2.0	Merged ST72F324 Flash with ST72324B ROM datasheet. Vt POR max modified in *Section 12.4 on page 145* Added *Figure 79 on page 164* Modified V_{AREF} min in *"10-bit ADC characteristics" on page 168* Modified I INJ for PB0 in *Section 12.9 on page 158* Added *"Clearing active interrupts outside interrupt routine" on page 187* Modified "32K ROM DEVICES ONLY" on page 165
30-Mar-2005	3	Removed Clock Security System (CSS) throughout document Added notes on ST72F324B 8K/16K Flash devices in Table 27 Corrected MCO description in *Section 10.2 on page 69* Modified VtPOR in *Section 12.4 on page 145* Static current consumption modified in *Section 12.9 on page 158* Updated footnote and *Figure 78 on page 163* and *Figure 79 on page 164* Modified Soldering information in *Section 13.6* Updated *Section 14 on page 178* Added Table 27 Modified *Figure 8 on page 25* and note 4 in *"Flash program memory" on page 23* Added limitation on ICC entry mode with 39 pulses to *"Known limitations" on page 185* Added Section 16 on page 166 for ST72F324B 8K/16K Flash devices Modified "Internal Sales Types on box label" in Table 29 on page 157
12-Sep-2005	4	Removed notes related to ST72F324, refer to datasheet rev 3 for specifications on older devices. Note: This datasheet rev refers only to ST72F324B and ST72324B. Changed character transmission procedure in *Section on page 112* Updated Vt POR max in *Section 12.4 on page 145* Updated Current Consumption for in *Section 12.5 on page 146* Added oscillator diagram and table to *Section 12.6.3 on page 150* Increased Data retention max. parameter in *Section 12.7.2 on page 154* Updated ordering Section 14.3 on page 155 and Section 14.5 on page 157 Updated Development tools *Section 14.3 on page 183* Added "external interrupt missed" in *Section 15.1 on page 185*
06-Feb-2006	5	Added description of SICSR register at address 2Bh in *Table 3 on page 20* Changed description on port PF2 to add internal pull-up in *Section 9.5.1 on page 63* Highlighted note in SPI *"Master mode operation" on page 99* Changed *"Static latch-up" on page 157* Added note 5 on analog input static current consumption *"General characteristics" on page 158* Updated notes in *"Thermal characteristics" on page 177*

Table 126. Document revision history (continued)

Date	Revision	Changes
10-Oct-2007	6	Removed references to automotive versions (these are covered by separate ST72324B-Auto datasheet). Changed Flash endurance to 1 Kcycles at 55°C Replaced TQFP with LQFP in package outline and device summary on page *1* *Figure 1 on page 14*: Replaced 60 Kbytes with 32 Kbytes in program memory block Replaced TQFP with LQFP in *Figure 2 on page 15*, in *Figure 4 on page 16* and in *Table 2 on page 17* Changed note 3 in *Section 9.2.1 on page 58* Changed *Section 10.1.3 on page 65* Changed *Master mode operation on page 99* Added unit of measure to LVD supply current in *Section 12.5.3 on page 148* Replaced TQFP with LQFP in *Section 12.8.2 on page 156* Changed note 4 in *Section 12.9.1 on page 158* Changed *Figure 78 on page 163* Removed EMC protective circuitry in *Figure 79 on page 164* (device works correctly without these components) Changed titles of *Figure 89 on page 172* and *Figure 91 on page 174* Replaced TQFP with LQFP in *Section 13.3 on page 177* Changed *Section 13.6 on page 171* Replaced TQFP with LQFP in *Section 14.1 on page 179*, in *Table 122 on page 181*, in *Section Table 122. on page 182* and in *Section 14.3.5 on page 184*
17-Mar-2009	7	Removed soldering information section. In *Section 10.6.3: Functional description on page 129*, modified “Starting the conversion” paragraph: added “ or a write to any bit of the ADCCSR register”. Modified t_{RET} values in *Table 101: Dual voltage HDFlash memory on page 154* . *Section 13.2: Package mechanical data on page 172* modified (values in inches rounded to 4 decimal digits). Modified *Section 12.8.3: Absolute maximum ratings (electrical sensitivity) on page 157* (removed DLU and $V_{ESD\ (MM)}$). Added *Section 13.1: ECOPACK on page 172*. Modified *“Device configuration and ordering information” on page 178*.