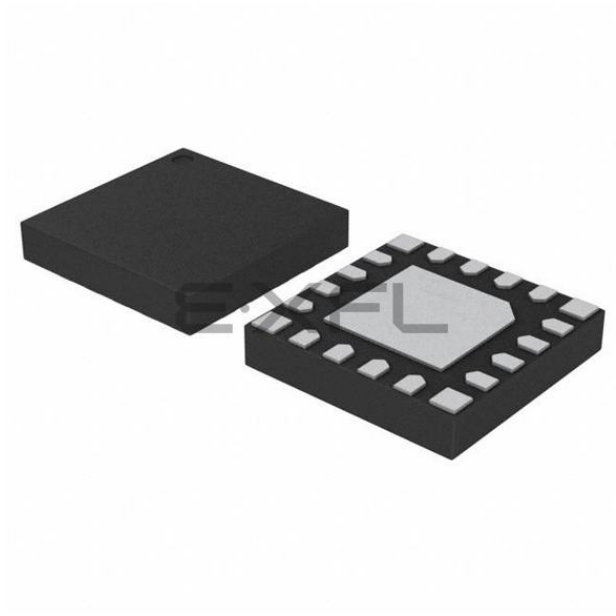
Silicon Labs - EFM8SB10F2G-A-QFN20R Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I²C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN Exposed Pad
Supplier Device Package	20-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8sb10f2g-a-qfn20r

3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 20 MHz low power oscillator divided by 8.

- Provides clock to core and peripherals.
- 20 MHz low power oscillator (LPOSC0), accurate to ±10% over supply and temperature corners.
- 24.5 MHz internal oscillator (HFOSC0), accurate to ±2% over supply and temperature corners.
- 16.4 kHz low-frequency oscillator (LFOSC0) or external RTC 32 kHz crystal.
- External RC, C, CMOS, and high-frequency crystal clock options (EXTCLK).
- Clock divider with eight settings for flexible clock scaling: Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.

3.5 Counters/Timers and PWM

Real Time Clock (RTC0)

The RTC is an ultra low power, 36 hour 32-bit independent time-keeping Real Time Clock with alarm. The RTC has a dedicated 32 kHz oscillator. No external resistor or loading capacitors are required, and a missing clock detector features alerts the system if the external crystal fails. The on-chip loading capacitors are programmable to 16 discrete levels allowing compatibility with a wide range of crystals.

The RTC module includes the following features:

- Up to 36 hours (32-bit) of independent time keeping.
- Support for internal 16.4 kHz low frequency oscillator (LFOSC0) or external 32 kHz crystal (crystal not available on CSP16 packages).
- Internal crystal loading capacitors with 16 levels.
- Operation in the lowest power mode and across the full supported voltage range.
- Alarm and oscillator failure events to wake from the lowest power mode or reset the device.
- Buffered clock output available for other system devices even in the lowest power mode.

Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base.
- Programmable clock divisor and clock source selection.
- Up to three independently-configurable channels
- 8, 9, 10, 11 and 16-bit PWM modes (edge-aligned operation).
- Frequency output mode.
- Capture on rising, falling or any edge.
- Compare function for arbitrary waveform generation.
- Software timer (internal compare) mode.
- Integrated watchdog timer.

3.7 Analog

Capacitive Sense (CS0)

The Capacitive Sense subsystem uses a capacitance-to-digital circuit to determine the capacitance on a port pin. The module can take measurements from different port pins using the module's analog multiplexer. The module can be configured to take measurements on one port pin, a group of port pins one-by-one using auto-scan, or the total capacitance on multiple channels together. A selectable gain circuit allows the designer to adjust the maximum allowable capacitance. An accumulator is also included, which can be configured to average multiple conversions on an input channel. Interrupts can be generated when the CS0 peripheral completes a conversion or when the measured value crosses a configurable threshold.

The Capacitive Sense module includes the following features:

- Measure multiple pins one-by-one using auto-scan or total capacitance on multiple channels together.
- Configurable input gain.
- Hardware auto-accumulate and average.
- Multiple internal start-of-conversion sources.
- Operational in Suspend when all other clocks are disabled.
- Interrupts available at the end of a conversion or when the measured value crosses a configurable threshold.

Programmable Current Reference (IREF0)

The programmable current reference (IREF0) module enables current source or sink with two output current settings: Low Power Mode and High Current Mode. The maximum current output in Low Power Mode is 63 µA (1 µA steps) and the maximum current output in High Current Mode is 504 µA (8 µA steps).

The IREF module includes the following features:

- Capable of sourcing or sinking current in programmable steps.
- Two operational modes: Low Power Mode and High Current Mode.
- Fine-tuning mode for higher output precision available in conjunction with the PCA0 module.

12-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 12-, 10-, and 8-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 10 external inputs.
- Single-ended 12-bit and 10-bit modes.
- Supports an output update rate of 75 ksps samples per second in 12-bit mode or 300 ksps samples per second in 10-bit mode.
- Operation in low power modes at lower conversion speeds.
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer sources.
- Output data window comparator allows automatic range checking.
- Support for burst mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Conversion complete and window compare interrupts supported.
- Flexible output data formatting.
- Includes an internal 1.65 V fast-settling reference and support for external reference.
- Integrated temperature sensor.

4.1.2 Power Consumption

Table 4.2. Power Consumption

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Digital Supply Current						
Normal Mode supply current - Full speed with code executing from flash [3, 4, 5]	I_{DD}	V_{DD} = 1.8–3.6 V, f_{SYSCLK} = 24.5 MHz	—	3.6	4.5	mA
		V_{DD} = 1.8–3.6 V, f_{SYSCLK} = 20 MHz	—	3.1	—	mA
		V_{DD} = 1.8–3.6 V, f_{SYSCLK} = 32.768 kHz	—	84	—	µA
Normal Mode supply current frequency sensitivity[1, 3, 5]	I_{DDFREQ}	V_{DD} = 1.8–3.6 V, T = 25 °C, f_{SYSCLK} < 14 MHz	—	174	—	µA/MHz
		V_{DD} = 1.8–3.6 V, T = 25 °C, f_{SYSCLK} > 14 MHz	—	88	—	µA/MHz
Idle Mode supply current - Core halted with peripherals running[4, 6]	I_{DD}	V_{DD} = 1.8–3.6 V, f_{SYSCLK} = 24.5 MHz	—	1.8	3.0	mA
		V_{DD} = 1.8–3.6 V, f_{SYSCLK} = 20 MHz	—	1.4	—	mA
		V_{DD} = 1.8–3.6 V, f_{SYSCLK} = 32.768 kHz	—	82	—	µA
Idle Mode Supply Current Frequency Sensitivity[1, 6]	I_{DDFREQ}	V_{DD} = 1.8–3.6 V, T = 25 °C	—	67	—	µA/MHz
Suspend Mode Supply Current	I_{DD}	V_{DD} = 1.8–3.6 V	—	77	—	µA
Sleep Mode Supply Current with RTC running from 32.768 kHz crystal	I_{DD}	1.8 V, T = 25 °C	—	0.60	—	µA
		3.6 V, T = 25 °C	—	0.80	—	µA
		1.8 V, T = 85 °C	—	0.80	—	µA
		3.6 V, T = 85 °C	—	1.00	—	µA
Sleep Mode Supply Current with RTC running from internal LFO	I_{DD}	1.8 V, T = 25 °C	—	0.30	—	µA
		3.6 V, T = 25 °C	—	0.50	—	µA
		1.8 V, T = 85 °C	—	0.50	—	µA
		3.6 V, T = 85 °C	—	0.80	—	µA
Sleep Mode Supply Current (RTC off)	I_{DD}	1.8 V, T = 25 °C	—	0.05	—	µA
		3.6 V, T = 25 °C	—	0.08	—	µA
		1.8 V, T = 85 °C	—	0.20	—	µA
		3.6 V, T = 85 °C	—	0.28	—	µA
V_{DD} Monitor Supply Current	I_{VMON}		—	7	—	µA
Oscillator Supply Current	I_{HFOSC0}	25 °C	—	300	—	µA

Parameter	Symbol	Conditions	Min	Typ	Max	Units
ADC0 Always-on Power Supply Current[7]	I_{ADC}	300 ksps, 10-bit conversions or 75 ksps, 12-bit conversions Normal bias settings V_{DD} = 3.0 V	—	740	—	µA
		150 ksps, 10-bit conversions or 37.5 ksps 12-bit conversions Low power bias settings V_{DD} = 3.0 V	—	400	—	µA
Comparator 0 (CMP0) Supply Current	I_{CMP}	CPMD = 11	—	0.4	—	µA
		CPMD = 10	—	2.6	—	µA
		CPMD = 01	—	8.8	—	µA
		CPMD = 00	—	23	—	µA
Internal Fast-Settling 1.65V ADC0 Reference, Always-on[8]	I_{VREFFS}	Normal Power Mode	—	260	—	µA
		Low Power Mode	—	140	—	µA
Temp sensor Supply Current	I_{TSENSE}		—	35	—	µA
Capacitive Sense Module (CS0) Supply Current	I_{CS0}	CS module bias current, 25 °C	—	50	60	µA
		CS module alone, maximum code output, 25 °C	—	90	125	µA
		Wake-on-CS threshold (suspend mode with regulator and CS module on)[9]	—	130	180	µA
Programmable Current Reference (IREF0) Supply Current[10]	I_{IREF0}	Current Source, Either Power Mode, Any Output Code	—	10	—	µA
		Low Power Mode, Current Sink IREF0DAT = 000001	—	1	—	µA
		Low Power Mode, Current Sink IREF0DAT = 111111	—	11	—	µA
		High Current Mode, Current Sink IREF0DAT = 000001	—	12	—	µA
		High Current Mode, Current Sink IREF0DAT = 111111	—	81	—	µA

Parameter	Symbol	Conditions	Min	Typ	Max	Units

Note:

1. Based on device characterization data; Not production tested.
2. SYSCLK must be at least 32 kHz to enable debugging.
3. Digital Supply Current depends upon the particular code being executed. The values in this table are obtained with the CPU executing an “sjmp $” loop, which is the compiled form of a while(1) loop in C. One iteration requires 3 CPU clock cycles, and the flash memory is read on each cycle. The supply current will vary slightly based on the physical location of the sjmp instruction and the number of flash address lines that toggle as a result. In the worst case, current can increase by up to 30% if the sjmp loop straddles a 64-byte flash address boundary (e.g., 0x007F to 0x0080). Real-world code with larger loops and longer linear sequences will have few transitions across the 64-byte address boundaries.
4. Includes supply current from regulator and oscillator source (24.5 MHz high-frequency oscillator, 20 MHz low-power oscillator, 1 MHz external oscillator, or 32.768 kHz RTC oscillator).
5. IDD can be estimated for frequencies < 14 MHz by simply multiplying the frequency of interest by the frequency sensitivity number for that range, then adding an offset of 84 µA. When using these numbers to estimate I_{DD} for > 14 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 3.0 V; F = 20 MHz, I_{DD} = 3.6 mA – (25 MHz – 20 MHz) x 0.088 mA/MHz = 3.16 mA assuming the same oscillator setting.
6. Idle IDD can be estimated by taking the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 3.0 V; F = 5 MHz, Idle I_{DD} = 1.75 mA – (25 MHz – 5 MHz) x 0.067 mA/MHz = 0.41 mA.
7. ADC0 always-on power excludes internal reference supply current.
8. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.
9. Includes only current from regulator, CS module, and MCU in suspend mode.
10. IREF0 supply current only. Does not include current sourced or sunk from IREF0 output pin.

4.1.3 Reset and Supply Monitor

Table 4.3. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Supply Monitor Threshold	V_{VDDM}	Reset Trigger	1.7	1.75	1.8	V
	V_{WARN}	Early Warning	1.8	1.85	1.9	V
VDD Supply Monitor Turn-On Time	t_{MON}		—	300	—	ns
Power-On Reset (POR) Monitor Threshold	V_{POR}	Rising Voltage on V_{DD}	—	1.75	—	V
		Falling Voltage on V_{DD}	0.75	1.0	1.3	V
V_{DD} Ramp Time	t_{RMP}	Time to V_{DD} ≥ 1.8 V	—	—	3	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	10	—	µs
Reset Delay from POR	t_{POR}	Relative to V_{DD} > V_{POR}	3	10	31	ms
RST Low Time to Generate Reset	t_{RSTL}		15	—	—	µs
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	F_{SYSCLK} > 1 MHz	100	650	1000	µs
Missing Clock Detector Trigger Frequency	F_{MCD}		—	7	10	kHz

4.1.9 ADC

Table 4.9. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}	12 Bit Mode		12		Bits
		10 Bit Mode		10		Bits
Throughput Rate	f_S	12 Bit Mode	—	—	75	ksps
		10 Bit Mode	—	—	300	ksps
Tracking Time	t_{TRK}	Initial Acquisition	1.5	—	—	us
		Subsequent Acquisitions (DC input, burst mode)	1.1	—	—	us
Power-On Time	t_{PWR}		1.5	—	—	µs
SAR Clock Frequency	f_{SAR}	High Speed Mode,	—	—	8.33	MHz
		Low Power Mode	—	—	4.4	MHz
Conversion Time	T_{CNV}	10-Bit Conversion	13	—	—	Clocks
Sample/Hold Capacitor	C_{SAR}	Gain = 1	—	16	—	pF
		Gain = 0.5	—	13	—	pF
Input Pin Capacitance	C_{IN}		—	20	—	pF
Input Mux Impedance	R_{MUX}		—	5	—	kΩ
Voltage Reference Range	V_{REF}		1	—	V_{DD}	V
Input Voltage Range[1]	V_{IN}	Gain = 1	0	—	V_{REF}	V
		Gain = 0.5	0	—	2 x V_{REF}	V
Power Supply Rejection Ratio	$PSRR_{ADC}$	Internal High Speed VREF	—	67	—	dB
		External VREF	—	74	—	dB
DC Performance						
Integral Nonlinearity	INL	12 Bit Mode	—	±1	±1.5	LSB
		10 Bit Mode	—	±0.5	±1	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode	—	±0.8	±1	LSB
		10 Bit Mode	—	±0.5	±1	LSB
Offset Error	E_{OFF}	12 Bit Mode, VREF = 1.65 V	–3	0	3	LSB
		10 Bit Mode, VREF = 1.65 V	–2	0	2	LSB
Offset Temperature Coefficient	TC_{OFF}		—	0.004	—	LSB/°C
Slope Error	E_M	12 Bit Mode	—	±0.02	±0.1	%
		10 Bit Mode	—	±0.06	±0.24	%
Dynamic Performance 10 kHz Sine Wave Input 1dB below full scale, Max throughput						
Signal-to-Noise	SNR	12 Bit Mode	62	65	—	dB
		10 Bit Mode	54	58	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	62	65	—	dB
		10 Bit Mode	54	58	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	12 Bit Mode	—	-76	—	dB
		10 Bit Mode	—	-73	—	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	82	—	dB
		10 Bit Mode	—	75	—	dB

Note:

1. Absolute input pin voltage is limited by the V_{DD} supply.
2. INL and DNL specifications for 12-bit mode do not include the first or last four ADC codes.
3. The maximum code in 12-bit mode is 0xFFFC. The Full Scale Error is referenced from the maximum code.

4.1.10 Voltage Reference

Table 4.10. Voltage Reference

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage	V_{REFFS}		1.62	1.65	1.68	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
External Reference						
Input Voltage	V_{EXTREF}		1	—	V_{DD}	V
Input Current	I_{EXTREF}	Sample Rate = 300 ksps; VREF = 3.0 V	—	5.25	—	µA

4.1.16 SMBus

Table 4.16. SMBus Peripheral Timing Performance (Master Mode)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Mode (100 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	70[2]	kHz
SMBus Operating Frequency	f_{SMB}		40[1]	—	70[2]	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		9.4	—	—	µs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		4.7	—	—	µs
Repeated START Condition Setup Time	$t_{SU:STA}$		9.4	—	—	µs
STOP Condition Setup Time	$t_{SU:STO}$		9.4	—	—	µs
Data Hold Time	$t_{HD:DAT}$		489[3]	—	—	ns
Data Setup Time	$t_{SU:DAT}$		448[3]	—	—	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		4.7	—	—	µs
Clock High Period	t_{HIGH}		9.4	—	50[4]	µs
Fast Mode (400 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	255[2]	kHz
SMBus Operating Frequency	f_{SMB}		40[1]	—	255[2]	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		2.6	—	—	µs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		1.3	—	—	µs
Repeated START Condition Setup Time	$t_{SU:STA}$		2.6	—	—	µs
STOP Condition Setup Time	$t_{SU:STO}$		2.6	—	—	µs
Data Hold Time	$t_{HD:DAT}$		489[3]	—	—	ns
Data Setup Time	$t_{SU:DAT}$		448[3]	—	—	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		1.3	—	—	µs
Clock High Period	t_{HIGH}		2.6	—	50[4]	µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. The minimum SMBus frequency is limited by the maximum Clock High Period requirement of the SMBus specification.
2. The maximum I2C and SMBus frequencies are limited by the minimum Clock Low Period requirements of their respective specifications. The maximum frequency cannot be achieved with all combinations of oscillators and dividers available, but the effective frequency must not exceed 256 kHz.
3. Data setup and hold timing at 25 MHz or lower with EXTHOLD set to 1.
4. SMBus has a maximum requirement of 50 µs for Clock High Period. Operating frequencies lower than 40 kHz will be longer than 50 µs. I2C can support periods longer than 50 µs.

Table 4.17. SMBus Peripheral Timing Formulas (Master Mode)

Parameter	Symbol	Clocks
SMBus Operating Frequency	f_{SMB}	f_{CSO} / 3
Bus Free Time Between STOP and START Conditions	t_{BUF}	2 / f_{CSO}
Hold Time After (Repeated) START Condition	$t_{HD:STA}$	1 / f_{CSO}
Repeated START Condition Setup Time	$t_{SU:STA}$	2 / f_{CSO}
STOP Condition Setup Time	$t_{SU:STO}$	2 / f_{CSO}
Clock Low Period	t_{LOW}	1 / f_{CSO}
Clock High Period	t_{HIGH}	2 / f_{CSO}

Note:

1. f_{CSO} is the SMBus peripheral clock source overflow frequency.

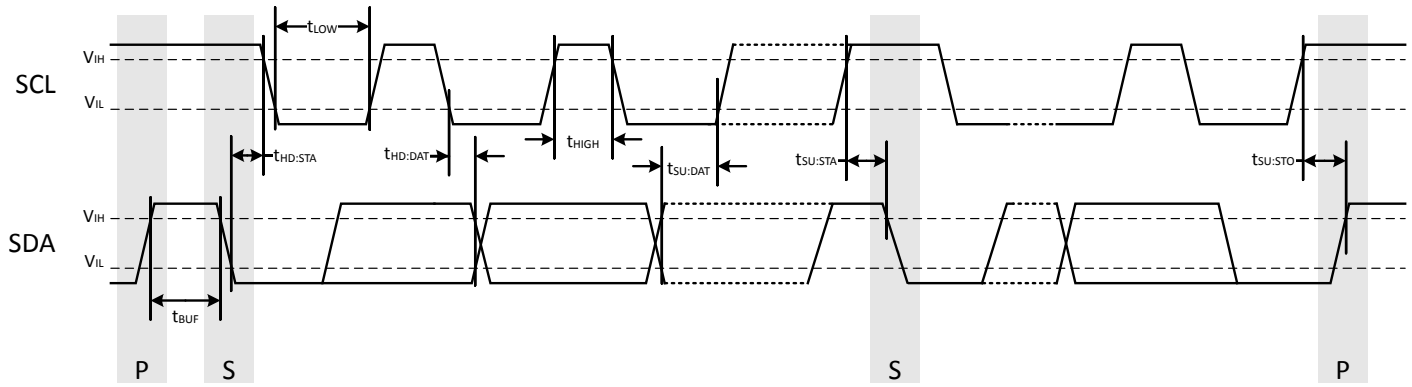

Figure 4.1. SMBus Peripheral Timing Diagram (Master Mode)

5. Typical Connection Diagrams

5.1 Power

Figure 5.1 Power Connection Diagram on page 31 shows a typical connection diagram for the power pins of the EFM8SB1 devices.

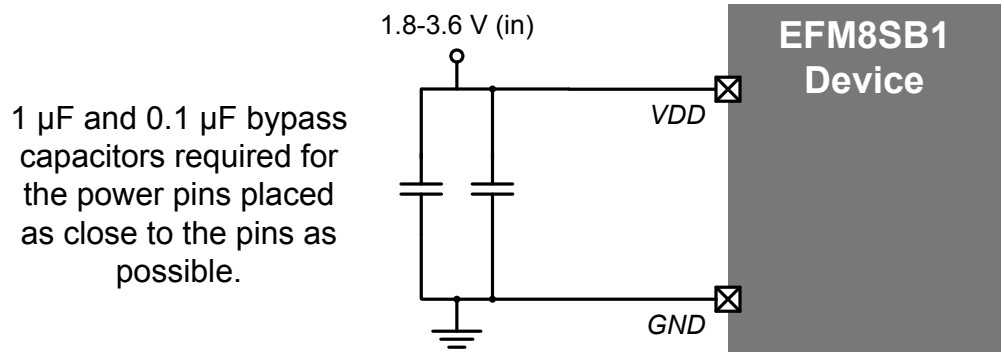

Figure 5.1. Power Connection Diagram

5.2 Debug

The diagram below shows a typical connection diagram for the debug connections pins. The pin sharing resistors are only required if the functionality on the C2D (a GPIO pin) and the C2CK (RSTb) is routed to external circuitry. For example, if the RSTb pin is connected to an external switch with debouncing filter or if the GPIO sharing with the C2D pin is connected to an external circuit, the pin sharing resistors and connections to the debug adapter must be placed on the hardware. Otherwise, these components and connections can be omitted.

For more information on debug connections, see the example schematics and information available in AN127: "Pin Sharing Techniques for the C2 Interface." Application notes can be found on the Silicon Labs website (http://www.silabs.com/8bit-appnotes) or in Simplicity Studio.

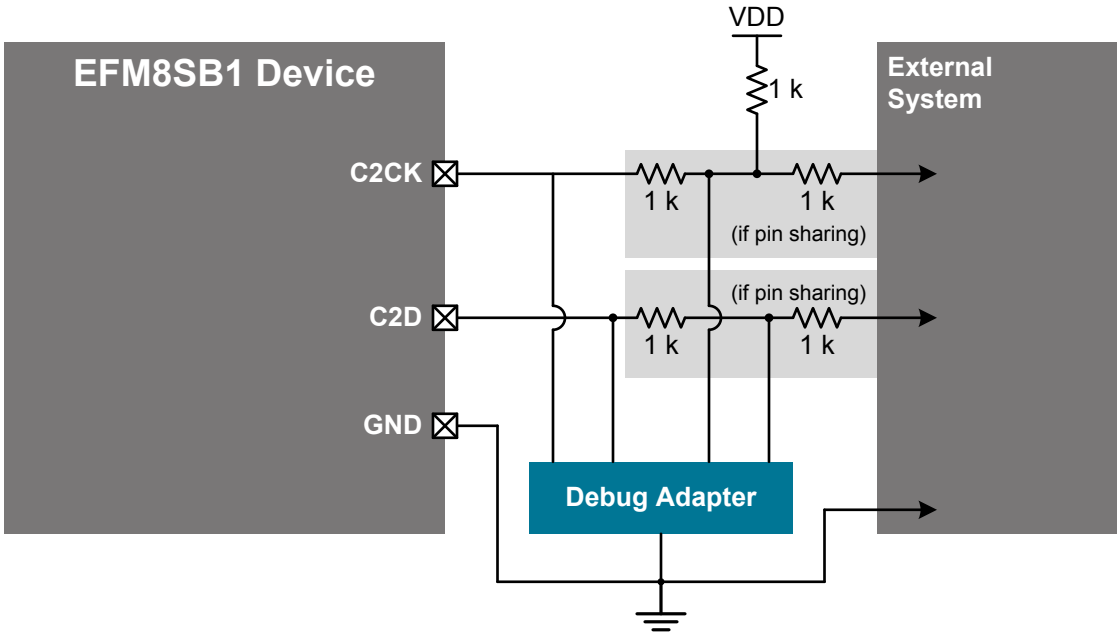

Figure 5.2. Debug Connection Diagram

6.2 EFM8SB1x-QFN24 Pin Definitions

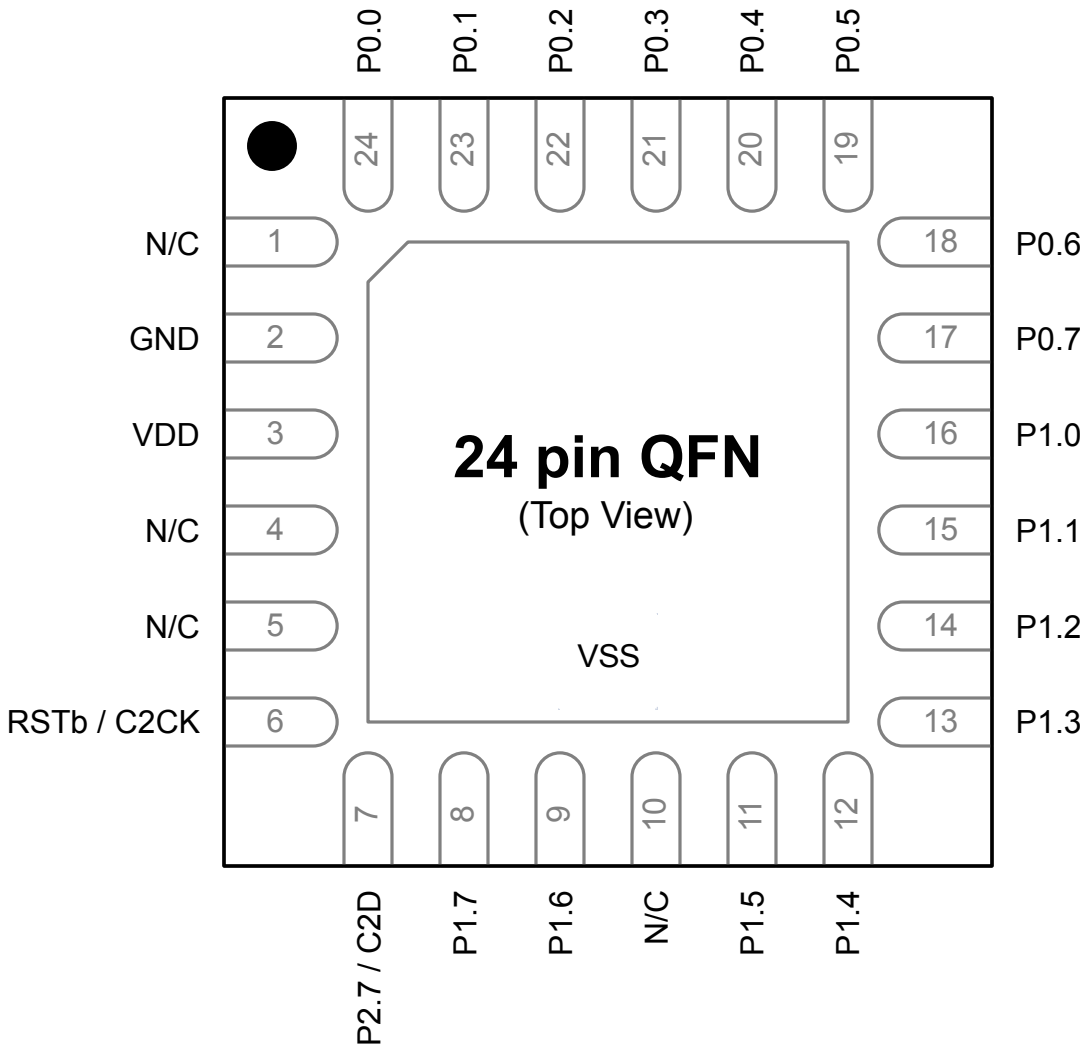

Figure 6.2. EFM8SB1x-QFN24 Pinout

Table 6.2. Pin Definitions for EFM8SB1x-QFN24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	N/C	No Connection			
2	GND	Ground			
3	VDD	Supply Power Input			
4	N/C	No Connection			
5	N/C	No Connection			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
6	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
7	P2.7 / C2D	Multifunction I/O / C2 Debug Data			
8	P1.7	Multifunction I/O	Yes	P1MAT.7	XTAL4
9	P1.6	Multifunction I/O	Yes	P1MAT.6	XTAL3
10	N/C	No Connection			
11	P1.5	Multifunction I/O	Yes	P1MAT.5	CS0.13
12	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CS0.12
13	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CS0.11
14	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CS0.10
15	P1.1	Multifunction I/O	Yes	P1MAT.1	CMP0N.4 CS0.9
16	P1.0	Multifunction I/O	Yes	P1MAT.0	CMP0P.4 CS0.8
17	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CS0.7 IREF0
18	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CS0.6
19	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CS0.5
20	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CS0.4
21	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK WAKEOUT INT0.3 INT1.3	ADC0.3 CS0.3 XTAL2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
23	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CS0.4
24	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK WAKEOUT INT0.3 INT1.3	ADC0.3 CS0.3 XTAL2

6.4 EFM8SB1x-CSP16 Pin Definitions

CSP devices can be handled and soldered using industry standard surface mount assembly techniques. However, because CSP devices are essentially a piece of silicon and are not encapsulated in plastic, they are susceptible to mechanical damage and may be sensitive to light. When CSP packages must be used in an environment exposed to light, it may be necessary to cover the top and sides with an opaque material.

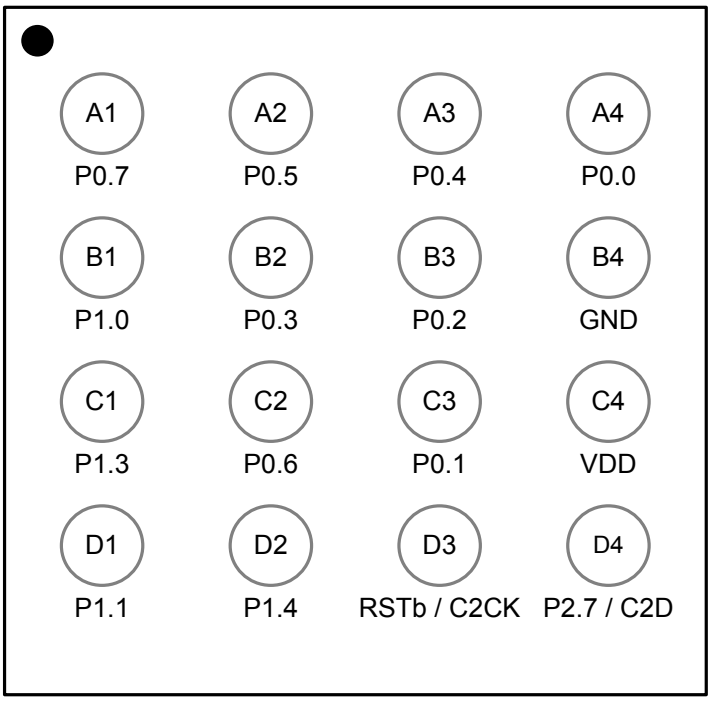

Figure 6.4. EFM8SB1x-CSP16 Pinout

Table 6.4. Pin Definitions for EFM8SB1x-CSP16

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
A1	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CS0.7 IREF0
A2	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CS0.5
A3	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CS0.4

7. CSP16 Package Specifications

7.1 CSP16 Package Dimensions

Note: CSP devices can be handled and soldered using industry standard surface mount assembly techniques. However, because CSP devices are essentially a piece of silicon and are not encapsulated in plastic, they are susceptible to mechanical damage and may be sensitive to light. When CSP packages must be used in an environment exposed to light, it may be necessary to cover the top and sides with an opaque material.

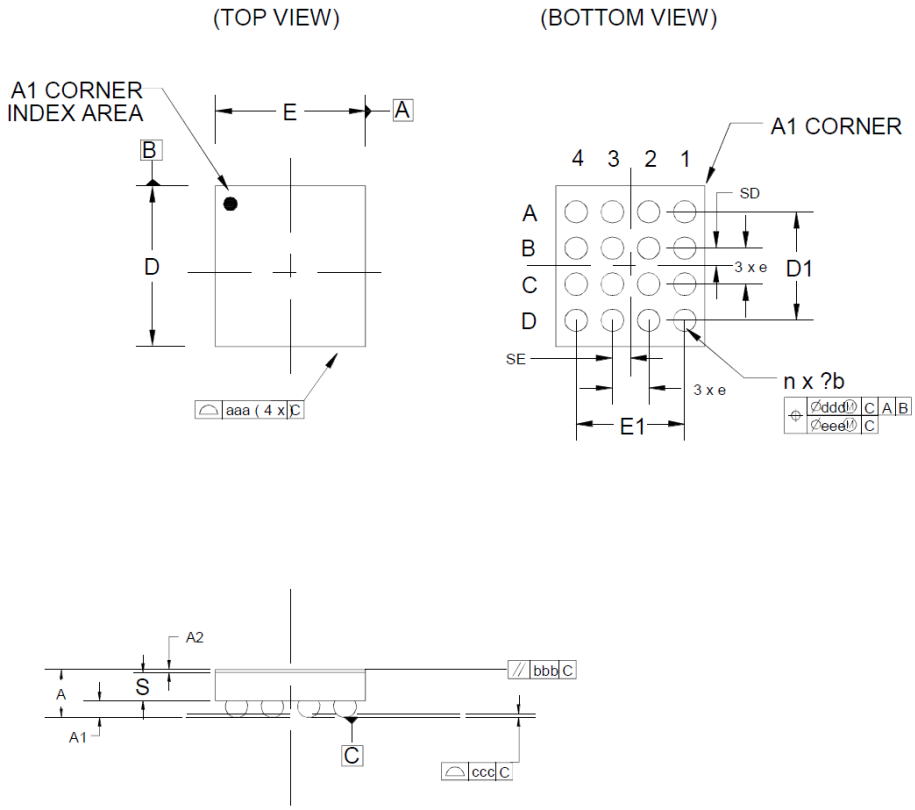

Figure 7.1. CSP16 Package Drawing

Table 7.1. CSP16 Package Dimensions

Dimension	Min	Typ	Max
A	0.491	0.55	0.609
A1	0.17	—	0.23
A2	0.036	0.040	0.044
b	0.23	—	0.29
S	0.3075	0.31	0.3125
D	1.781 BSC		
E	1.659 BSC		
e	0.40 BSC		
D1	1.20 BSC		

7.2 CSP16 PCB Land Pattern

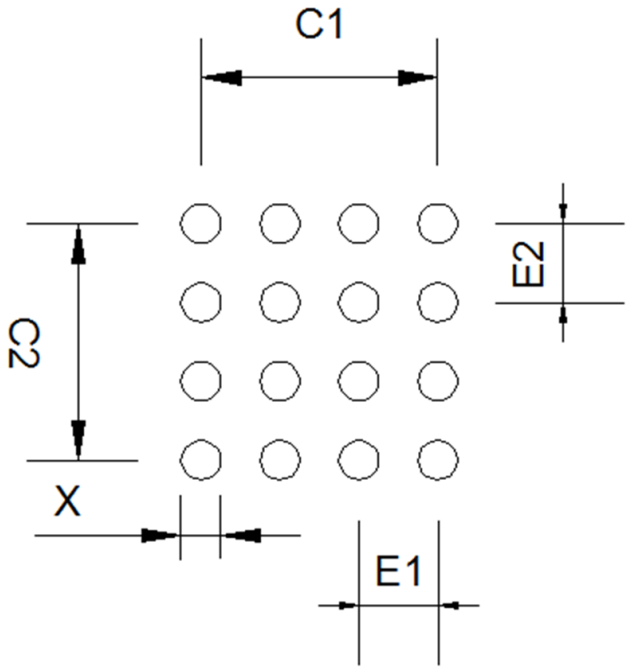

Figure 7.2. CSP16 PCB Land Pattern Drawing

Table 7.2. CSP16 PCB Land Pattern Dimensions

Dimension	Min	Max
X	0.20	
C1	1.20	
C2	1.20	
E1	0.40	
E2	0.40	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.075 mm (3 mils).
7. A stencil of square aperture (0.22 x 0.22 mm) is recommended.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. QFN24 Package Specifications

9.1 QFN24 Package Dimensions

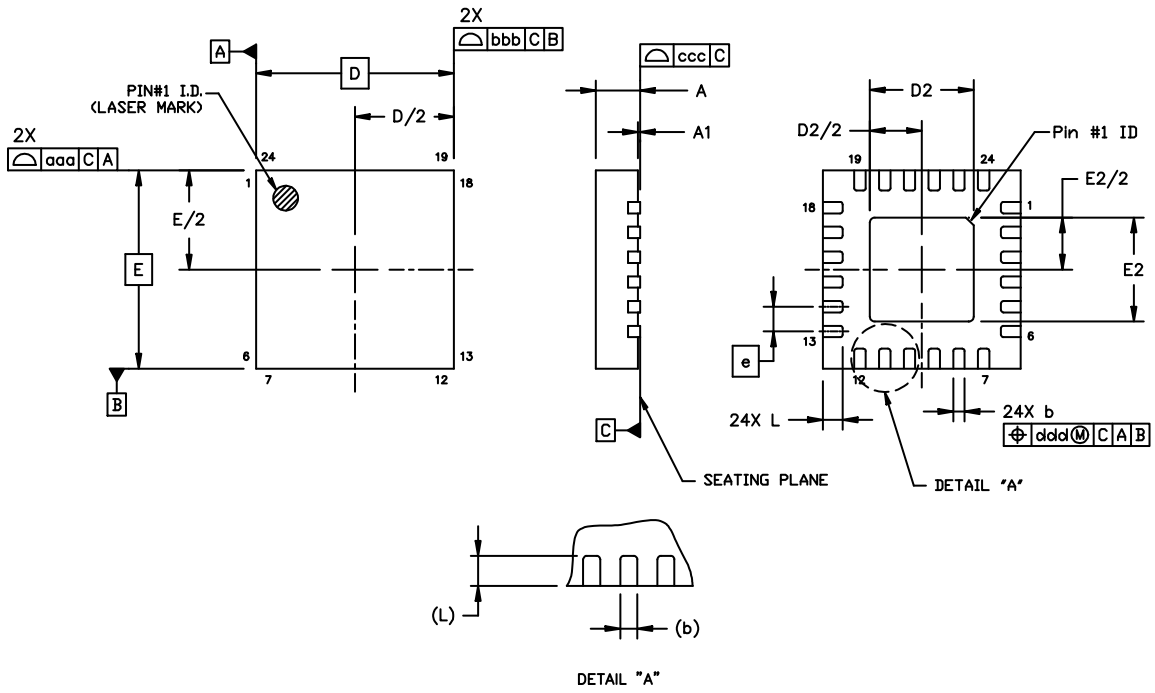

Figure 9.1. QFN24 Package Drawing

Table 9.1. QFN24 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
b	0.18	0.25	0.30
D		4.00 BSC	
D2	2.35	2.45	2.55
e		0.50 BSC	
E		4.00 BSC	
E2	2.35	2.45	2.55
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

10.2 QSOP24 PCB Land Pattern

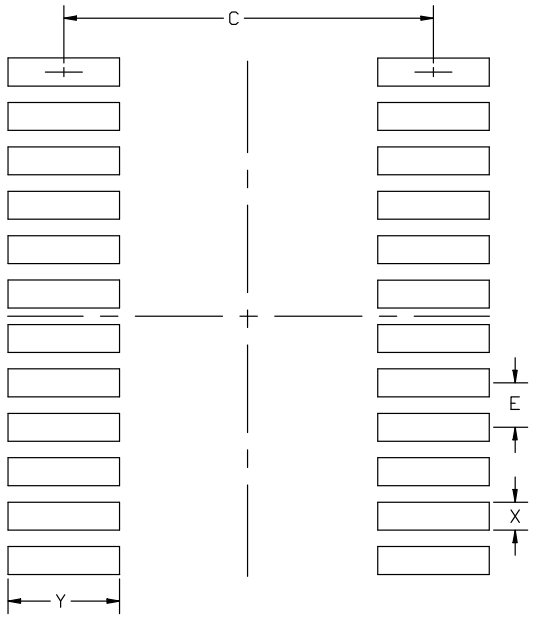

Figure 10.2. QSOP24 PCB Land Pattern Drawing

Table 10.2. QSOP24 PCB Land Pattern Dimensions

Dimension	Min	Max
C	5.20	5.30
E	0.635 BSC	
X	0.30	0.40
Y	1.50	1.60

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. Revision History

11.1 Revision 1.3

September 23, 2016

Added A-grade parts.

Added 5.2 Debug.

Added bootloader pinout information and a reference to *AN945: EFM8 Factory Bootloader User Guide* in 3.10 Bootloader.

Added specifications for 4.1.16 SMBus.

Added CRC Calculation Time to 4.1.4 Flash Memory.

Added a note linking to the Typical VOH and VOL Performance graphs in 4.1.15 Port I/O.

Added the t_{POR} and adjusted the V_{POR} falling specifications in 4.1.3 Reset and Supply Monitor.

Added a note to 3.1 Introduction referencing the Reference Manual.

Added a note to 3.2 Power to clarify that entering Sleep may disconnect the active debug session.

Specified that the UART has a 1-byte FIFO in 3.6 Communications and Other Digital Peripherals.

11.2 Revision 1.2

Added CSP16 package.

Updated the "C2D / P2.0" pin on the QSOP24 pinout diagram to "C2D / P2.7."

Added crystal oscillator drive current typical values to Table 4.7 Crystal Oscillator on page 18.

Corrected the number of capacitive sense channels for 24- and 20-pin packages in Table 4.14 Capacitive Sense (CS0) on page 24.

Corrected E dimension shown in Figure 8.2 QFN20 PCB Land Pattern Drawing on page 50.

Added more information to 3.10 Bootloader.

11.3 Revision 1.1

Initial release.

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