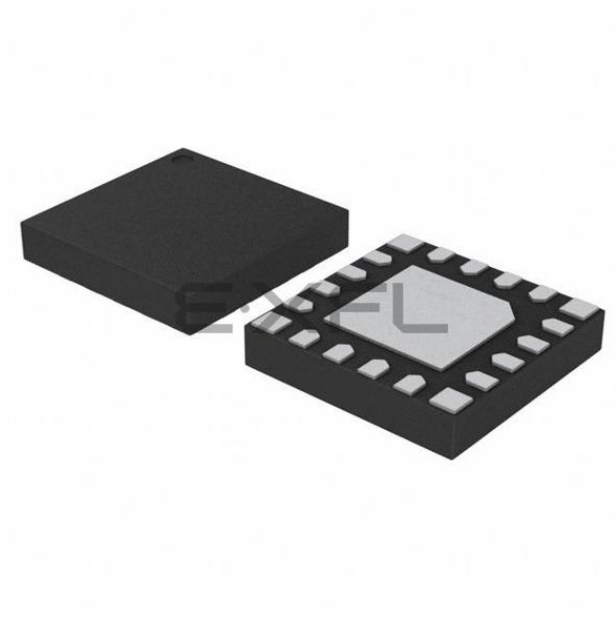
Silicon Labs - EFM8SB10F4G-A-QFN20 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I²C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN Exposed Pad
Supplier Device Package	20-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8sb10f4g-a-qfn20

3. System Overview

3.1 Introduction

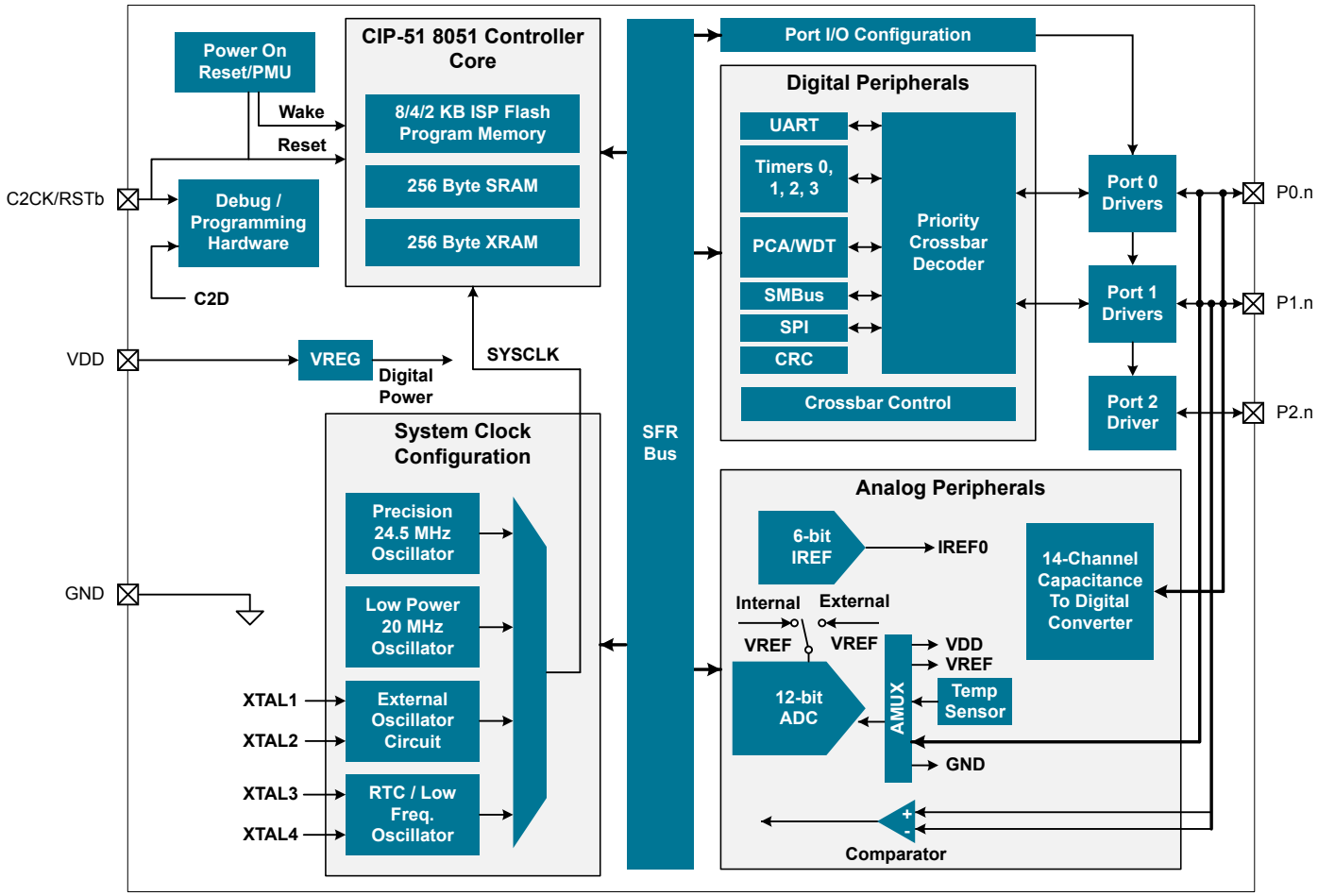

Figure 3.1. Detailed EFM8SB1 Block Diagram

This section describes the EFM8SB1 family at a high level. For more information on each module including register definitions, see the EFM8SB1 Reference Manual.

3.7 Analog

Capacitive Sense (CS0)

The Capacitive Sense subsystem uses a capacitance-to-digital circuit to determine the capacitance on a port pin. The module can take measurements from different port pins using the module's analog multiplexer. The module can be configured to take measurements on one port pin, a group of port pins one-by-one using auto-scan, or the total capacitance on multiple channels together. A selectable gain circuit allows the designer to adjust the maximum allowable capacitance. An accumulator is also included, which can be configured to average multiple conversions on an input channel. Interrupts can be generated when the CS0 peripheral completes a conversion or when the measured value crosses a configurable threshold.

The Capacitive Sense module includes the following features:

- Measure multiple pins one-by-one using auto-scan or total capacitance on multiple channels together.
- Configurable input gain.
- Hardware auto-accumulate and average.
- Multiple internal start-of-conversion sources.
- Operational in Suspend when all other clocks are disabled.
- Interrupts available at the end of a conversion or when the measured value crosses a configurable threshold.

Programmable Current Reference (IREF0)

The programmable current reference (IREF0) module enables current source or sink with two output current settings: Low Power Mode and High Current Mode. The maximum current output in Low Power Mode is 63 µA (1 µA steps) and the maximum current output in High Current Mode is 504 µA (8 µA steps).

The IREF module includes the following features:

- Capable of sourcing or sinking current in programmable steps.
- Two operational modes: Low Power Mode and High Current Mode.
- Fine-tuning mode for higher output precision available in conjunction with the PCA0 module.

12-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 12-, 10-, and 8-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 10 external inputs.
- Single-ended 12-bit and 10-bit modes.
- Supports an output update rate of 75 ksps samples per second in 12-bit mode or 300 ksps samples per second in 10-bit mode.
- Operation in low power modes at lower conversion speeds.
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer sources.
- Output data window comparator allows automatic range checking.
- Support for burst mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Conversion complete and window compare interrupts supported.
- Flexible output data formatting.
- Includes an internal 1.65 V fast-settling reference and support for external reference.
- Integrated temperature sensor.

4.1.2 Power Consumption

Table 4.2. Power Consumption

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Digital Supply Current						
Normal Mode supply current - Full speed with code executing from flash [3, 4, 5]	I_{DD}	V_{DD} = 1.8–3.6 V, f_{SYSCLK} = 24.5 MHz	—	3.6	4.5	mA
		V_{DD} = 1.8–3.6 V, f_{SYSCLK} = 20 MHz	—	3.1	—	mA
		V_{DD} = 1.8–3.6 V, f_{SYSCLK} = 32.768 kHz	—	84	—	µA
Normal Mode supply current frequency sensitivity[1, 3, 5]	I_{DDFREQ}	V_{DD} = 1.8–3.6 V, T = 25 °C, f_{SYSCLK} < 14 MHz	—	174	—	µA/MHz
		V_{DD} = 1.8–3.6 V, T = 25 °C, f_{SYSCLK} > 14 MHz	—	88	—	µA/MHz
Idle Mode supply current - Core halted with peripherals running[4, 6]	I_{DD}	V_{DD} = 1.8–3.6 V, f_{SYSCLK} = 24.5 MHz	—	1.8	3.0	mA
		V_{DD} = 1.8–3.6 V, f_{SYSCLK} = 20 MHz	—	1.4	—	mA
		V_{DD} = 1.8–3.6 V, f_{SYSCLK} = 32.768 kHz	—	82	—	µA
Idle Mode Supply Current Frequency Sensitivity[1, 6]	I_{DDFREQ}	V_{DD} = 1.8–3.6 V, T = 25 °C	—	67	—	µA/MHz
Suspend Mode Supply Current	I_{DD}	V_{DD} = 1.8–3.6 V	—	77	—	µA
Sleep Mode Supply Current with RTC running from 32.768 kHz crystal	I_{DD}	1.8 V, T = 25 °C	—	0.60	—	µA
		3.6 V, T = 25 °C	—	0.80	—	µA
		1.8 V, T = 85 °C	—	0.80	—	µA
		3.6 V, T = 85 °C	—	1.00	—	µA
Sleep Mode Supply Current with RTC running from internal LFO	I_{DD}	1.8 V, T = 25 °C	—	0.30	—	µA
		3.6 V, T = 25 °C	—	0.50	—	µA
		1.8 V, T = 85 °C	—	0.50	—	µA
		3.6 V, T = 85 °C	—	0.80	—	µA
Sleep Mode Supply Current (RTC off)	I_{DD}	1.8 V, T = 25 °C	—	0.05	—	µA
		3.6 V, T = 25 °C	—	0.08	—	µA
		1.8 V, T = 85 °C	—	0.20	—	µA
		3.6 V, T = 85 °C	—	0.28	—	µA
V_{DD} Monitor Supply Current	I_{VMON}		—	7	—	µA
Oscillator Supply Current	I_{HFOSC0}	25 °C	—	300	—	µA

Parameter	Symbol	Conditions	Min	Typ	Max	Units

Note:

1. Based on device characterization data; Not production tested.
2. SYSCLK must be at least 32 kHz to enable debugging.
3. Digital Supply Current depends upon the particular code being executed. The values in this table are obtained with the CPU executing an “sjmp $” loop, which is the compiled form of a while(1) loop in C. One iteration requires 3 CPU clock cycles, and the flash memory is read on each cycle. The supply current will vary slightly based on the physical location of the sjmp instruction and the number of flash address lines that toggle as a result. In the worst case, current can increase by up to 30% if the sjmp loop straddles a 64-byte flash address boundary (e.g., 0x007F to 0x0080). Real-world code with larger loops and longer linear sequences will have few transitions across the 64-byte address boundaries.
4. Includes supply current from regulator and oscillator source (24.5 MHz high-frequency oscillator, 20 MHz low-power oscillator, 1 MHz external oscillator, or 32.768 kHz RTC oscillator).
5. IDD can be estimated for frequencies < 14 MHz by simply multiplying the frequency of interest by the frequency sensitivity number for that range, then adding an offset of 84 µA. When using these numbers to estimate I_{DD} for > 14 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 3.0 V; F = 20 MHz, I_{DD} = 3.6 mA – (25 MHz – 20 MHz) x 0.088 mA/MHz = 3.16 mA assuming the same oscillator setting.
6. Idle IDD can be estimated by taking the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 3.0 V; F = 5 MHz, Idle I_{DD} = 1.75 mA – (25 MHz – 5 MHz) x 0.067 mA/MHz = 0.41 mA.
7. ADC0 always-on power excludes internal reference supply current.
8. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.
9. Includes only current from regulator, CS module, and MCU in suspend mode.
10. IREF0 supply current only. Does not include current sourced or sunk from IREF0 output pin.

4.1.3 Reset and Supply Monitor

Table 4.3. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Supply Monitor Threshold	V_{VDDM}	Reset Trigger	1.7	1.75	1.8	V
	V_{WARN}	Early Warning	1.8	1.85	1.9	V
VDD Supply Monitor Turn-On Time	t_{MON}		—	300	—	ns
Power-On Reset (POR) Monitor Threshold	V_{POR}	Rising Voltage on V_{DD}	—	1.75	—	V
		Falling Voltage on V_{DD}	0.75	1.0	1.3	V
V_{DD} Ramp Time	t_{RMP}	Time to V_{DD} ≥ 1.8 V	—	—	3	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	10	—	µs
Reset Delay from POR	t_{POR}	Relative to V_{DD} > V_{POR}	3	10	31	ms
RST Low Time to Generate Reset	t_{RSTL}		15	—	—	µs
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	F_{SYSCLK} > 1 MHz	100	650	1000	µs
Missing Clock Detector Trigger Frequency	F_{MCD}		—	7	10	kHz

4.1.9 ADC

Table 4.9. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}	12 Bit Mode		12		Bits
		10 Bit Mode		10		Bits
Throughput Rate	f_S	12 Bit Mode	—	—	75	ksps
		10 Bit Mode	—	—	300	ksps
Tracking Time	t_{TRK}	Initial Acquisition	1.5	—	—	us
		Subsequent Acquisitions (DC input, burst mode)	1.1	—	—	us
Power-On Time	t_{PWR}		1.5	—	—	µs
SAR Clock Frequency	f_{SAR}	High Speed Mode,	—	—	8.33	MHz
		Low Power Mode	—	—	4.4	MHz
Conversion Time	T_{CNV}	10-Bit Conversion	13	—	—	Clocks
Sample/Hold Capacitor	C_{SAR}	Gain = 1	—	16	—	pF
		Gain = 0.5	—	13	—	pF
Input Pin Capacitance	C_{IN}		—	20	—	pF
Input Mux Impedance	R_{MUX}		—	5	—	kΩ
Voltage Reference Range	V_{REF}		1	—	V_{DD}	V
Input Voltage Range[1]	V_{IN}	Gain = 1	0	—	V_{REF}	V
		Gain = 0.5	0	—	2 x V_{REF}	V
Power Supply Rejection Ratio	$PSRR_{ADC}$	Internal High Speed VREF	—	67	—	dB
		External VREF	—	74	—	dB
DC Performance						
Integral Nonlinearity	INL	12 Bit Mode	—	±1	±1.5	LSB
		10 Bit Mode	—	±0.5	±1	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode	—	±0.8	±1	LSB
		10 Bit Mode	—	±0.5	±1	LSB
Offset Error	E_{OFF}	12 Bit Mode, VREF = 1.65 V	–3	0	3	LSB
		10 Bit Mode, VREF = 1.65 V	–2	0	2	LSB
Offset Temperature Coefficient	TC_{OFF}		—	0.004	—	LSB/°C
Slope Error	E_M	12 Bit Mode	—	±0.02	±0.1	%
		10 Bit Mode	—	±0.06	±0.24	%
Dynamic Performance 10 kHz Sine Wave Input 1dB below full scale, Max throughput						
Signal-to-Noise	SNR	12 Bit Mode	62	65	—	dB
		10 Bit Mode	54	58	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	62	65	—	dB
		10 Bit Mode	54	58	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	12 Bit Mode	—	-76	—	dB
		10 Bit Mode	—	-73	—	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	82	—	dB
		10 Bit Mode	—	75	—	dB

Note:

1. Absolute input pin voltage is limited by the V_{DD} supply.
2. INL and DNL specifications for 12-bit mode do not include the first or last four ADC codes.
3. The maximum code in 12-bit mode is 0xFFFC. The Full Scale Error is referenced from the maximum code.

4.1.10 Voltage Reference

Table 4.10. Voltage Reference

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage	V_{REFFS}		1.62	1.65	1.68	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
External Reference						
Input Voltage	V_{EXTREF}		1	—	V_{DD}	V
Input Current	I_{EXTREF}	Sample Rate = 300 ksps; VREF = 3.0 V	—	5.25	—	µA

4.1.12 Comparators

Table 4.12. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	120	—	ns
		–100 mV Differential	—	110	—	ns
Response Time, CPMD = 11 (Lowest Power)	t_{RESP3}	+100 mV Differential	—	1.25	—	µs
		–100 mV Differential	—	3.2	—	µs
Positive Hysterisis Mode 0 (CPMD = 00)	HYS_{CP+}	CPHYP = 00	—	0.4	—	mV
		CPHYP = 01	—	8	—	mV
		CPHYP = 10	—	16	—	mV
		CPHYP = 11	—	32	—	mV
Negative Hysterisis Mode 0 (CPMD = 00)	HYS_{CP-}	CPHYN = 00	—	-0.4	—	mV
		CPHYN = 01	—	–8	—	mV
		CPHYN = 10	—	–16	—	mV
		CPHYN = 11	—	–32	—	mV
Positive Hysterisis Mode 1 (CPMD = 01)	HYS_{CP+}	CPHYP = 00	—	0.5	—	mV
		CPHYP = 01	—	6	—	mV
		CPHYP = 10	—	12	—	mV
		CPHYP = 11	—	24	—	mV
Negative Hysterisis Mode 1 (CPMD = 01)	HYS_{CP-}	CPHYN = 00	—	-0.5	—	mV
		CPHYN = 01	—	–6	—	mV
		CPHYN = 10	—	–12	—	mV
		CPHYN = 11	—	–24	—	mV
Positive Hysterisis Mode 2 (CPMD = 10)	HYS_{CP+}	CPHYP = 00	—	0.7	—	mV
		CPHYP = 01	—	4.5	—	mV
		CPHYP = 10	—	9	—	mV
		CPHYP = 11	—	18	—	mV
Negative Hysterisis Mode 2 (CPMD = 10)	HYS_{CP-}	CPHYN = 00	—	-0.6	—	mV
		CPHYN = 01	—	–4.5	—	mV
		CPHYN = 10	—	–9	—	mV
		CPHYN = 11	—	–18	—	mV
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CPHYP = 00	—	1.5	—	mV
		CPHYP = 01	—	4	—	mV
		CPHYP = 10	—	8	—	mV
		CPHYP = 11	—	16	—	mV

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Negative Hysteresis Mode 3 (CPMD = 11)	HYS_{CP-}	CPHYN = 00	—	-1.5	—	mV
		CPHYN = 01	—	–4	—	mV
		CPHYN = 10	—	–8	—	mV
		CPHYN = 11	—	–16	—	mV
Input Range (CP+ or CP–)	V_{IN}		-0.25	—	V_{DD}+0.25	V
Input Pin Capacitance	C_{CP}		—	12	—	pF
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	70	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
Input Offset Voltage	V_{OFF}	T_A = 25 °C	-10	0	10	mV
Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°C

4.1.13 Programmable Current Reference (IREF0)

Table 4.13. Programmable Current Reference (IREF0)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Performance						
Resolution	N_{bits}			6		bits
Output Compliance Range	V_{IOUT}	Low Power Mode, Source	0	—	V_{DD} – 0.4	V
		High Current Mode, Source	0	—	V_{DD} – 0.8	V
		Low Power Mode, Sink	0.3	—	V_{DD}	V
		High Current Mode, Sink	0.8	—	V_{DD}	V
Integral Nonlinearity	INL		—	<±0.2	±1.0	LSB
Differential Nonlinearity	DNL		—	<±0.2	±1.0	LSB
Offset Error	E_{OFF}		—	<±0.1	±0.5	LSB
Full Scale Error	E_{FS}	Low Power Mode, Source	—	—	±5	%
		High Current Mode, Source	—	—	±6	%
		Low Power Mode, Sink	—	—	±8	%
		High Current Mode, Sink	—	—	±8	%
Absolute Current Error	E_{ABS}	Low Power Mode Sourcing 20 µA	—	<±1	±3	%
Dynamic Performance						
Output Settling Time to 1/2 LSB	t_{SETTLE}		—	300	—	ns
Startup Time	t_{PWR}		—	1	—	µs

Note:
1. The PCA block may be used to improve IREF0 resolution by PWMing the two LSBs.

4.1.14 Capacitive Sense (CS0)

Table 4.14. Capacitive Sense (CS0)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Single Conversion Time[1]	t_{CNV}	12-bit Mode	20	25	40	µs
		13-bit Mode (default)	21	27	42.5	µs
		14-bit Mode	23	29	45	µs
		16-bit Mode	26	33	50	µs
Number of Channels	N_{CHAN}	24-pin Packages		14		Channels
		20-pin Packages		13		Channels
		16-pin Packages		12		Channels
Capacitance per Code	C_{LSB}	Default Configuration, 16-bit codes	—	1	—	fF
Maximum External Capacitive Load	C_{EXTMAX}	CS0CG = 111b (Default)	—	45	—	pF
		CS0CG = 000b	—	500	—	pF
Maximum External Series Impedance	R_{EXTMAX}	CS0CG = 111b (Default)	—	50	—	kΩ

Note:

1. Conversion time is specified with the default configuration.
2. RMS Noise is equivalent to one standard deviation. Peak-to-peak noise encompasses ±3.3 standard deviations. The RMS noise value is specified with the default configuration.

4.1.15 Port I/O

Table 4.15. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (High Drive)[1]	V_{OH}	I_{OH} = –3 mA	V_{DD} – 0.7	—	—	V
Output Low Voltage (High Drive)[1]	V_{OL}	I_{OL} = 8.5 mA	—	—	0.6	V
Output High Voltage (Low Drive)[1]	V_{OH}	I_{OH} = –1 mA	V_{DD} – 0.7	—	—	V
Output Low Voltage (Low Drive)[1]	V_{OL}	I_{OL} = 1.4 mA	—	—	0.6	V
Input High Voltage	V_{IH}	V_{DD} = 2.0 to 3.6 V	V_{DD} – 0.6	—	—	V
		V_{DD} = 1.8 to 2.0 V	0.7 x V_{DD}	—	—	V
Input Low Voltage	V_{IL}	V_{DD} = 2.0 to 3.6 V	—	—	0.6	V
		V_{DD} = 1.8 to 2.0 V	—	—	0.3 x V_{DD}	V
Weak Pull-Up Current	I_{PU}	V_{DD} = 1.8 V V_{IN} = 0 V	—	–4	—	µA
		V_{DD} = 3.6 V V_{IN} = 0 V	–35	–20	—	µA
Input Leakage	I_{LK}	Weak pullup disabled or pin in analog mode	–1	—	1	µA

Note:
1. See Figure 4.3 Typical V_{OH} Curves on page 29 and Figure 4.4 Typical V_{OL} Curves on page 30 for more information.

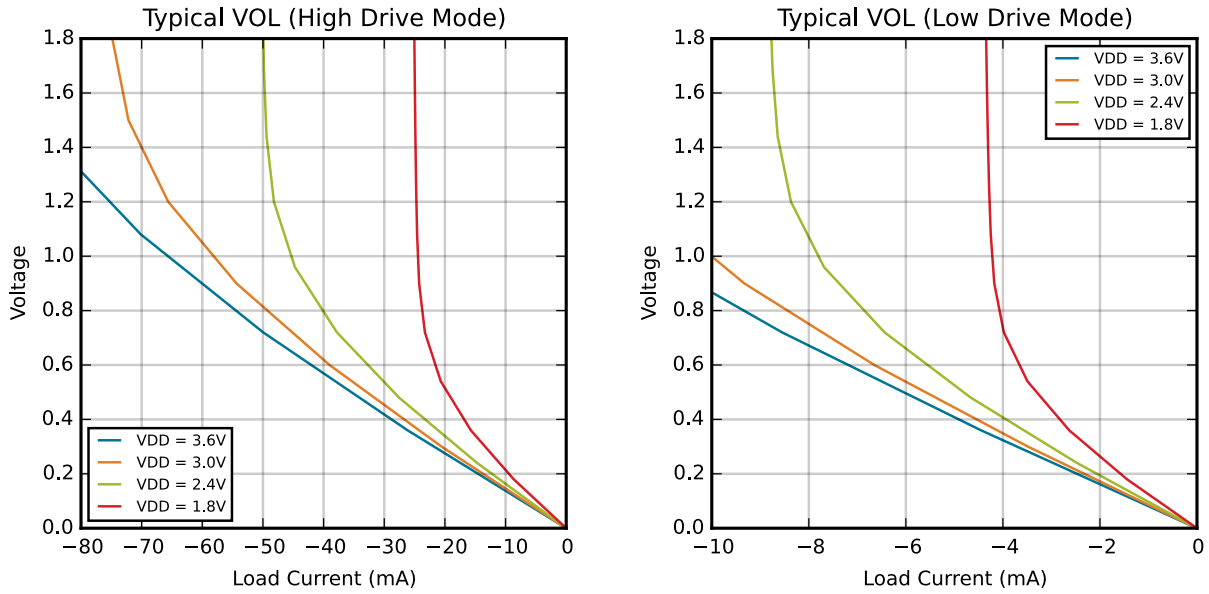

Figure 4.4. Typical V_{OL} Curves

5. Typical Connection Diagrams

5.1 Power

Figure 5.1 Power Connection Diagram on page 31 shows a typical connection diagram for the power pins of the EFM8SB1 devices.

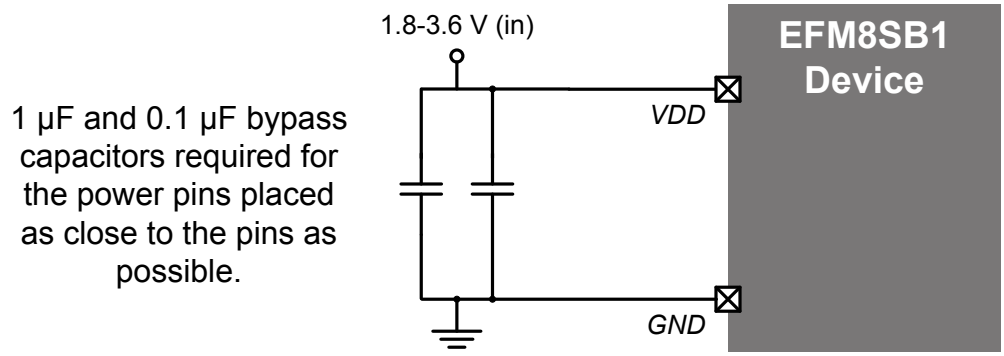

Figure 5.1. Power Connection Diagram

5.2 Debug

The diagram below shows a typical connection diagram for the debug connections pins. The pin sharing resistors are only required if the functionality on the C2D (a GPIO pin) and the C2CK (RSTb) is routed to external circuitry. For example, if the RSTb pin is connected to an external switch with debouncing filter or if the GPIO sharing with the C2D pin is connected to an external circuit, the pin sharing resistors and connections to the debug adapter must be placed on the hardware. Otherwise, these components and connections can be omitted.

For more information on debug connections, see the example schematics and information available in AN127: "Pin Sharing Techniques for the C2 Interface." Application notes can be found on the Silicon Labs website (http://www.silabs.com/8bit-appnotes) or in Simplicity Studio.

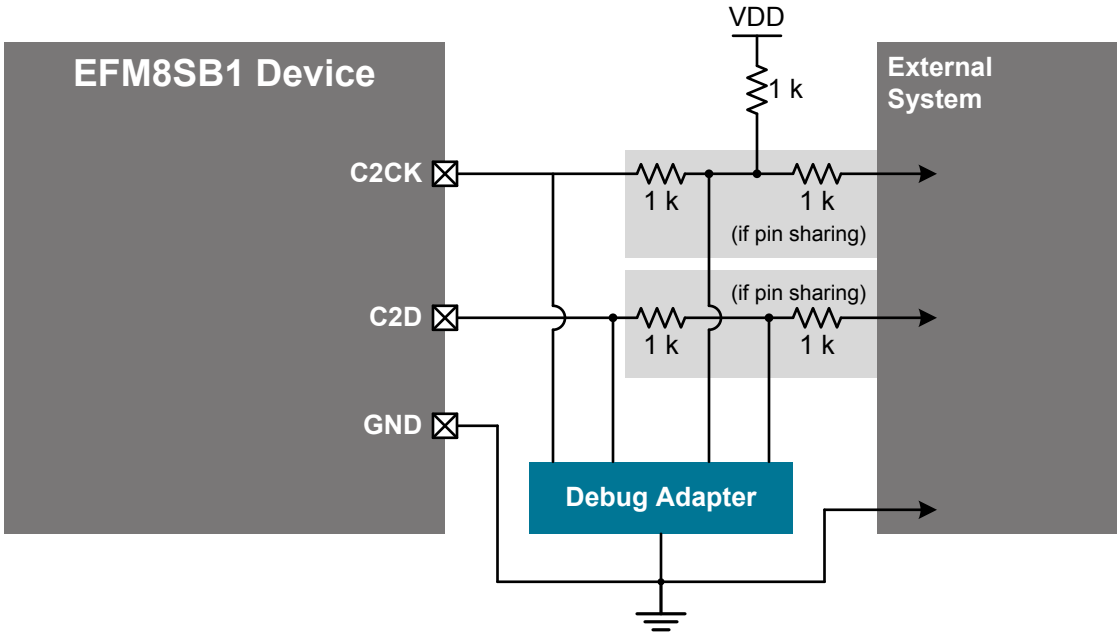

Figure 5.2. Debug Connection Diagram

6.2 EFM8SB1x-QFN24 Pin Definitions

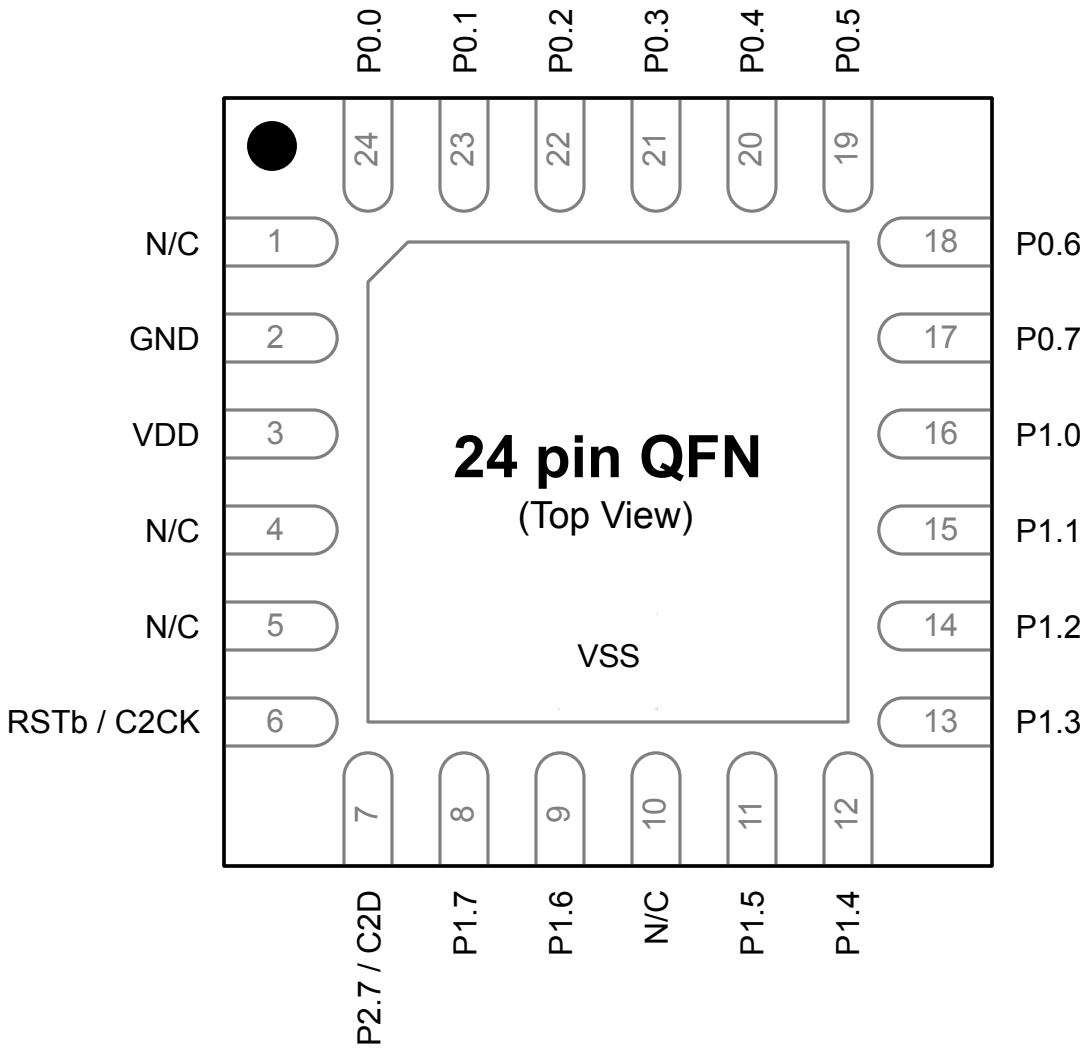

Figure 6.2. EFM8SB1x-QFN24 Pinout

Table 6.2. Pin Definitions for EFM8SB1x-QFN24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	N/C	No Connection			
2	GND	Ground			
3	VDD	Supply Power Input			
4	N/C	No Connection			
5	N/C	No Connection			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
6	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
7	P2.7 / C2D	Multifunction I/O / C2 Debug Data			
8	P1.7	Multifunction I/O	Yes	P1MAT.7	XTAL4
9	P1.6	Multifunction I/O	Yes	P1MAT.6	XTAL3
10	N/C	No Connection			
11	P1.5	Multifunction I/O	Yes	P1MAT.5	CS0.13
12	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CS0.12
13	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CS0.11
14	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CS0.10
15	P1.1	Multifunction I/O	Yes	P1MAT.1	CMP0N.4 CS0.9
16	P1.0	Multifunction I/O	Yes	P1MAT.0	CMP0P.4 CS0.8
17	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CS0.7 IREF0
18	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CS0.6
19	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CS0.5
20	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CS0.4
21	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK WAKEOUT INT0.3 INT1.3	ADC0.3 CS0.3 XTAL2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
3	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	CS0.0 VREF
4	N/C	No Connection			
5	GND	Ground			
6	VDD	Supply Power Input			
7	N/C	No Connection			
8	N/C	No Connection			
9	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
10	P2.7 / C2D	Multifunction I/O / C2 Debug Data			
11	P1.7	Multifunction I/O	Yes	P1MAT.7	XTAL4
12	P1.6	Multifunction I/O	Yes	P1MAT.6	XTAL3
13	N/C	No Connection			
14	P1.5	Multifunction I/O	Yes	P1MAT.5	CS0.13
15	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CS0.12
16	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CS0.11
17	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CS0.10
18	P1.1	Multifunction I/O	Yes	P1MAT.1	CMP0N.4 CS0.9
19	P1.0	Multifunction I/O	Yes	P1MAT.0	CMP0P.4 CS0.8
20	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CS0.7 IREF0
21	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CS0.6
22	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CS0.5

Dimension	Min	Typ	Max
E1		1.20 BSC	
SD		0.2	
SE		0.2	
n		16	
aaa		0.03	
bbb		0.06	
ccc		0.05	
ddd		0.015	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Primary datum “C” and seating plane are defined by the spherical crowns of the solder balls.
4. Dimension “b” is measured at the maximum solder bump diameter, parallel to primary datum “C”.
5. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Dimension	Min	Typ	Max
L1	0.00	—	0.10
aaa	—	0.10	—
bbb	—	0.10	—
ddd	—	0.05	—
eee	—	—	0.08

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing is based upon JEDEC Solid State Product Outline MO-248 but includes custom features which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2 QFN20 PCB Land Pattern

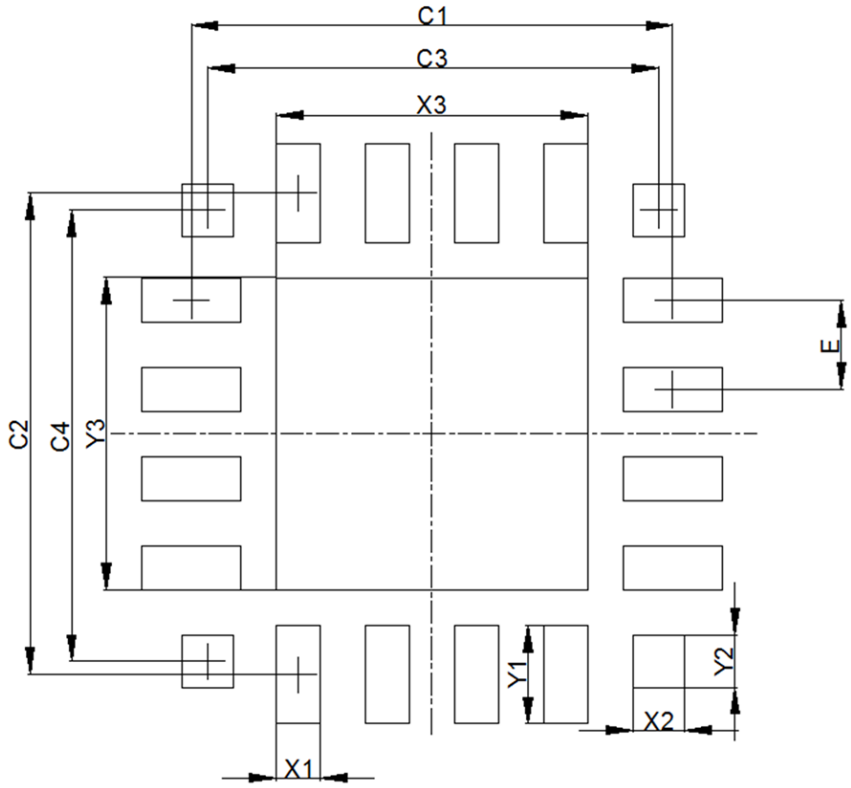

Figure 8.2. QFN20 PCB Land Pattern Drawing

Table 8.2. QFN20 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	2.70	
C2	2.70	
C3	2.53	
C4	2.53	
E	0.50 REF	
X1	0.20	0.30
X2	0.24	.034
X3	1.70	1.80
Y1	0.50	0.60
Y2	0.24	0.34
Y3	1.70	1.80

Dimension	Min	Typ	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.