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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN Exposed Pad
Supplier Device Package	20-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8sb10f8g-a-qfn20r

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC0 Channels	Capacitive Touch Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8SB10F2G-A-QFN20	2	256	16	9	13	Yes	-40 to +85 C	QFN20
EFM8SB10F8A-A-QFN24	8	512	17	10	14	Yes	-40 to +85 C	QFN24
EFM8SB10F8A-A-QFN20	8	512	16	9	13	Yes	-40 to +85 C	QFN20

The A-grade (i.e. EFM8SB10F8A-A-QFN20) devices receive full automotive quality production status, including AEC-Q100 qualification, registration with International Material Data System (IMDS), and Part Production Approval Process (PPAP) documentation. PPAP documentation is available at www.silabs.com with a registered and NDA approved user account.

3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 20 MHz low power oscillator divided by 8.

- Provides clock to core and peripherals.
- 20 MHz low power oscillator (LPOSC0), accurate to $\pm 10\%$ over supply and temperature corners.
- 24.5 MHz internal oscillator (HFOSC0), accurate to $\pm 2\%$ over supply and temperature corners.
- 16.4 kHz low-frequency oscillator (LFOSC0) or external RTC 32 kHz crystal.
- External RC, C, CMOS, and high-frequency crystal clock options (EXTCLK).
- Clock divider with eight settings for flexible clock scaling: Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.

3.5 Counters/Timers and PWM

Real Time Clock (RTC0)

The RTC is an ultra low power, 36 hour 32-bit independent time-keeping Real Time Clock with alarm. The RTC has a dedicated 32 kHz oscillator. No external resistor or loading capacitors are required, and a missing clock detector features alerts the system if the external crystal fails. The on-chip loading capacitors are programmable to 16 discrete levels allowing compatibility with a wide range of crystals.

The RTC module includes the following features:

- Up to 36 hours (32-bit) of independent time keeping.
- Support for internal 16.4 kHz low frequency oscillator (LFOSC0) or external 32 kHz crystal (crystal not available on CSP16 packages).
- Internal crystal loading capacitors with 16 levels.
- Operation in the lowest power mode and across the full supported voltage range.
- Alarm and oscillator failure events to wake from the lowest power mode or reset the device.
- Buffered clock output available for other system devices even in the lowest power mode.

Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base.
- Programmable clock divisor and clock source selection.
- Up to three independently-configurable channels
- 8, 9, 10, 11 and 16-bit PWM modes (edge-aligned operation).
- Frequency output mode.
- Capture on rising, falling or any edge.
- Compare function for arbitrary waveform generation.
- Software timer (internal compare) mode.
- Integrated watchdog timer.

Timers (Timer 0, Timer 1, Timer 2, and Timer 3)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2 and Timer 3 are 16-bit timers including the following features:

- Clock sources include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8.
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- Comparator 0 or RTC0 capture (Timer 2)
- RTC0 or EXTCLK/8 capture (Timer 3)

Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) integrated within the PCA0 peripheral. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software. The state of the RSTb pin is unaffected by this reset.

The Watchdog Timer integrated in the PCA0 peripheral has the following features:

- Programmable timeout interval
- Runs from the selected PCA clock source
- Automatically enabled after any system reset

3.6 Communications and Other Digital Peripherals

Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions.
- Baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive).
- 8- or 9-bit data.
- Automatic start and stop generation.
- Single-byte FIFO on transmit and receive.

Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

The SPI module includes the following features:

- Supports 3- or 4-wire operation in master or slave modes.
- Supports external clock frequencies up to $\text{SYSCLK} / 2$ in master mode and $\text{SYSCLK} / 10$ in slave mode.
- Support for four clock phase and polarity options.
- 8-bit dedicated clock rate generator.
- Support for multiple masters on the same data lines.

System Management Bus / I2C (SMB0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I²C serial bus.

The SMBus module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to inhibit all slave states.
- Programmable data setup/hold times.

16-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the 16-bit result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for CCITT-16 polynomial
- Byte-level bit reversal
- Automatic CRC of flash contents on one or more 256-byte blocks
- Initial seed selection of 0x0000 or 0xFFFF

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in [Table 4.1 Recommended Operating Conditions on page 13](#), unless stated otherwise.

4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V _{DD}		1.8	2.4	3.6	V
Minimum RAM Data Retention Voltage on VDD ¹	V _{RAM}	Not in Sleep Mode	—	1.4	—	V
		Sleep Mode	—	0.3	0.5	V
System Clock Frequency	f _{SYSCLK}		0	—	25	MHz
Operating Ambient Temperature	T _A		−40	—	85	°C
Note: 1. All voltages with respect to GND.						

4.1.2 Power Consumption

Table 4.2. Power Consumption

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Digital Supply Current						
Normal Mode supply current - Full speed with code executing from flash ^{3, 4, 5}	I _{DD}	V _{DD} = 1.8–3.6 V, f _{SYSCLOCK} = 24.5 MHz	—	3.6	4.5	mA
		V _{DD} = 1.8–3.6 V, f _{SYSCLOCK} = 20 MHz	—	3.1	—	mA
		V _{DD} = 1.8–3.6 V, f _{SYSCLOCK} = 32.768 kHz	—	84	—	μA
Normal Mode supply current frequency sensitivity ^{1, 3, 5}	I _{DDFREQ}	V _{DD} = 1.8–3.6 V, T = 25 °C, f _{SYSCLOCK} < 14 MHz	—	174	—	μA/MHz
		V _{DD} = 1.8–3.6 V, T = 25 °C, f _{SYSCLOCK} > 14 MHz	—	88	—	μA/MHz
Idle Mode supply current - Core halted with peripherals running ^{4, 6}	I _{DD}	V _{DD} = 1.8–3.6 V, f _{SYSCLOCK} = 24.5 MHz	—	1.8	3.0	mA
		V _{DD} = 1.8–3.6 V, f _{SYSCLOCK} = 20 MHz	—	1.4	—	mA
		V _{DD} = 1.8–3.6 V, f _{SYSCLOCK} = 32.768 kHz	—	82	—	μA
Idle Mode Supply Current Frequency Sensitivity ^{1, 6}	I _{DDFREQ}	V _{DD} = 1.8–3.6 V, T = 25 °C	—	67	—	μA/MHz
Suspend Mode Supply Current	I _{DD}	V _{DD} = 1.8–3.6 V	—	77	—	μA
Sleep Mode Supply Current with RTC running from 32.768 kHz crystal	I _{DD}	1.8 V, T = 25 °C	—	0.60	—	μA
		3.6 V, T = 25 °C	—	0.80	—	μA
		1.8 V, T = 85 °C	—	0.80	—	μA
		3.6 V, T = 85 °C	—	1.00	—	μA
Sleep Mode Supply Current with RTC running from internal LFO	I _{DD}	1.8 V, T = 25 °C	—	0.30	—	μA
		3.6 V, T = 25 °C	—	0.50	—	μA
		1.8 V, T = 85 °C	—	0.50	—	μA
		3.6 V, T = 85 °C	—	0.80	—	μA
Sleep Mode Supply Current (RTC off)	I _{DD}	1.8 V, T = 25 °C	—	0.05	—	μA
		3.6 V, T = 25 °C	—	0.08	—	μA
		1.8 V, T = 85 °C	—	0.20	—	μA
		3.6 V, T = 85 °C	—	0.28	—	μA
V _{DD} Monitor Supply Current	I _{VMON}		—	7	—	μA
Oscillator Supply Current	I _{HFOSC0}	25 °C	—	300	—	μA

Parameter	Symbol	Conditions	Min	Typ	Max	Units
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Note:

1. Based on device characterization data; Not production tested.
2. SYSCLK must be at least 32 kHz to enable debugging.
3. Digital Supply Current depends upon the particular code being executed. The values in this table are obtained with the CPU executing an “sjmp \$” loop, which is the compiled form of a while(1) loop in C. One iteration requires 3 CPU clock cycles, and the flash memory is read on each cycle. The supply current will vary slightly based on the physical location of the sjmp instruction and the number of flash address lines that toggle as a result. In the worst case, current can increase by up to 30% if the sjmp loop straddles a 64-byte flash address boundary (e.g., 0x007F to 0x0080). Real-world code with larger loops and longer linear sequences will have few transitions across the 64-byte address boundaries.
4. Includes supply current from regulator and oscillator source (24.5 MHz high-frequency oscillator, 20 MHz low-power oscillator, 1 MHz external oscillator, or 32.768 kHz RTC oscillator).
5. IDD can be estimated for frequencies < 14 MHz by simply multiplying the frequency of interest by the frequency sensitivity number for that range, then adding an offset of 84 μ A. When using these numbers to estimate IDD for > 14 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: $V_{DD} = 3.0$ V; $F = 20$ MHz, $I_{DD} = 3.6$ mA – (25 MHz – 20 MHz) \times 0.088 mA/MHz = 3.16 mA assuming the same oscillator setting.
6. Idle IDD can be estimated by taking the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: $V_{DD} = 3.0$ V; $F = 5$ MHz, Idle $I_{DD} = 1.75$ mA – (25 MHz – 5 MHz) \times 0.067 mA/MHz = 0.41 mA.
7. ADC0 always-on power excludes internal reference supply current.
8. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.
9. Includes only current from regulator, CS module, and MCU in suspend mode.
10. IREF0 supply current only. Does not include current sourced or sunk from IREF0 output pin.

4.1.3 Reset and Supply Monitor

Table 4.3. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Supply Monitor Threshold	V _{VDDM}	Reset Trigger	1.7	1.75	1.8	V
	V _{WARN}	Early Warning	1.8	1.85	1.9	V
VDD Supply Monitor Turn-On Time	t _{MON}		—	300	—	ns
Power-On Reset (POR) Monitor Threshold	V _{POR}	Rising Voltage on V _{DD}	—	1.75	—	V
		Falling Voltage on V _{DD}	0.75	1.0	1.3	V
V _{DD} Ramp Time	t _{RMP}	Time to V _{DD} \geq 1.8 V	—	—	3	ms
Reset Delay from non-POR source	t _{RST}	Time between release of reset source and code execution	—	10	—	μ s
Reset Delay from POR	t _{POR}	Relative to V _{DD} > V _{POR}	3	10	31	ms
RST Low Time to Generate Reset	t _{RSTL}		15	—	—	μ s
Missing Clock Detector Response Time (final rising edge to reset)	t _{MCD}	F _{SYSCLK} > 1 MHz	100	650	1000	μ s
Missing Clock Detector Trigger Frequency	F _{MCD}		—	7	10	kHz

4.1.4 Flash Memory

Table 4.4. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Write Time ¹	t_{WRITE}	One Byte	57	64	71	μs
Erase Time ¹	t_{ERASE}	One Page	28	32	36	ms
Endurance (Write/Erase Cycles)	N_{WE}		20 k	100 k	—	Cycles
CRC Calculation Time	t_{CRC}	One 256-Byte Block SYSCLK = 24.5 MHz	—	21.5	—	μs
Note: 1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles. 2. Data Retention Information is published in the Quarterly Quality and Reliability Report.						

4.1.5 Power Management Timing

Table 4.5. Power Management Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Idle Mode Wake-up Time	t_{IDLEWK}		2	—	3	SYSCLKs
Suspend Mode Wake-up Time	$t_{\text{SUS-}}t_{\text{PENDWK}}$	CLKDIV = 0x00 Low Power or Precision Osc.	—	400	—	ns
Sleep Mode Wake-up Time	t_{SLEEPWK}		—	2	—	μs

4.1.6 Internal Oscillators

Table 4.6. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Frequency Oscillator 0 (24.5 MHz)						
Oscillator Frequency	f_{HFOSC0}	Full Temperature and Supply Range	24	24.5	25	MHz
Low Power Oscillator (20 MHz)						
Oscillator Frequency	f_{LPOSC}	Full Temperature and Supply Range	18	20	22	MHz
Low Frequency Oscillator (16.4 kHz internal RTC oscillator)						
Oscillator Frequency	f_{LFOSC}	Full Temperature and Supply Range	13.1	16.4	19.7	kHz

4.1.12 Comparators

Table 4.12. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	120	—	ns
		–100 mV Differential	—	110	—	ns
Response Time, CPMD = 11 (Low- est Power)	t_{RESP3}	+100 mV Differential	—	1.25	—	μ s
		–100 mV Differential	—	3.2	—	μ s
Positive Hysteresis Mode 0 (CPMD = 00)	HYS_{CP+}	CPHYP = 00	—	0.4	—	mV
		CPHYP = 01	—	8	—	mV
		CPHYP = 10	—	16	—	mV
		CPHYP = 11	—	32	—	mV
Negative Hysteresis Mode 0 (CPMD = 00)	HYS_{CP-}	CPHYN = 00	—	–0.4	—	mV
		CPHYN = 01	—	–8	—	mV
		CPHYN = 10	—	–16	—	mV
		CPHYN = 11	—	–32	—	mV
Positive Hysteresis Mode 1 (CPMD = 01)	HYS_{CP+}	CPHYP = 00	—	0.5	—	mV
		CPHYP = 01	—	6	—	mV
		CPHYP = 10	—	12	—	mV
		CPHYP = 11	—	24	—	mV
Negative Hysteresis Mode 1 (CPMD = 01)	HYS_{CP-}	CPHYN = 00	—	–0.5	—	mV
		CPHYN = 01	—	–6	—	mV
		CPHYN = 10	—	–12	—	mV
		CPHYN = 11	—	–24	—	mV
Positive Hysteresis Mode 2 (CPMD = 10)	HYS_{CP+}	CPHYP = 00	—	0.7	—	mV
		CPHYP = 01	—	4.5	—	mV
		CPHYP = 10	—	9	—	mV
		CPHYP = 11	—	18	—	mV
Negative Hysteresis Mode 2 (CPMD = 10)	HYS_{CP-}	CPHYN = 00	—	–0.6	—	mV
		CPHYN = 01	—	–4.5	—	mV
		CPHYN = 10	—	–9	—	mV
		CPHYN = 11	—	–18	—	mV
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CPHYP = 00	—	1.5	—	mV
		CPHYP = 01	—	4	—	mV
		CPHYP = 10	—	8	—	mV
		CPHYP = 11	—	16	—	mV

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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Note:

1. The minimum SMBus frequency is limited by the maximum Clock High Period requirement of the SMBus specification.
2. The maximum I2C and SMBus frequencies are limited by the minimum Clock Low Period requirements of their respective specifications. The maximum frequency cannot be achieved with all combinations of oscillators and dividers available, but the effective frequency must not exceed 256 kHz.
3. Data setup and hold timing at 25 MHz or lower with EXTHOLD set to 1.
4. SMBus has a maximum requirement of 50 μ s for Clock High Period. Operating frequencies lower than 40 kHz will be longer than 50 μ s. I2C can support periods longer than 50 μ s.

Table 4.17. SMBus Peripheral Timing Formulas (Master Mode)

Parameter	Symbol	Clocks
SMBus Operating Frequency	f_{SMB}	$f_{CSO} / 3$
Bus Free Time Between STOP and START Conditions	t_{BUF}	$2 / f_{CSO}$
Hold Time After (Repeated) START Condition	$t_{HD:STA}$	$1 / f_{CSO}$
Repeated START Condition Setup Time	$t_{SU:STA}$	$2 / f_{CSO}$
STOP Condition Setup Time	$t_{SU:STO}$	$2 / f_{CSO}$
Clock Low Period	t_{LOW}	$1 / f_{CSO}$
Clock High Period	t_{HIGH}	$2 / f_{CSO}$

Note:

1. f_{CSO} is the SMBus peripheral clock source overflow frequency.

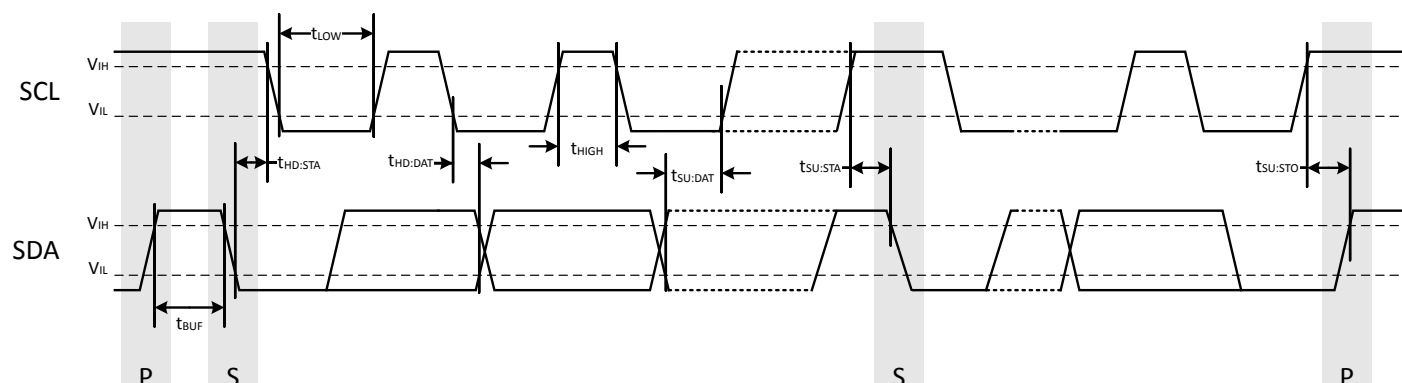


Figure 4.1. SMBus Peripheral Timing Diagram (Master Mode)

4.2 Thermal Conditions

Table 4.18. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance*	θ_{JA}	QFN-24 Packages	—	35	—	°C/W
		QFN-20 Packages	—	60	—	°C/W
		QSOP-24 Packages	—	65	—	°C/W
Note: 1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.						

4.3 Absolute Maximum Ratings

Stresses above those listed in [Table 4.19 Absolute Maximum Ratings on page 28](#) may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

Table 4.19. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		−55	125	°C
Storage Temperature	T_{STG}		−65	150	°C
Voltage on V_{DD}	V_{DD}		GND−0.3	4.0	V
Voltage on I/O pins or RSTb	V_{IN}		GND−0.3	$V_{DD} + 0.3$	V
Total Current Sunk into Supply Pin	I_{VDD}		—	400	mA
Total Current Sourced out of Ground Pin	I_{GND}		400	—	mA
Current Sourced or Sunk by Any I/O Pin or RSTb	I_{IO}		−100	100	mA
Maximum Total Current through all Port Pins	I_{IOTOT}		—	200	mA
Operating Junction Temperature	T_J		−40	105	°C
Exposure to maximum rating conditions for extended periods may affect device reliability.					

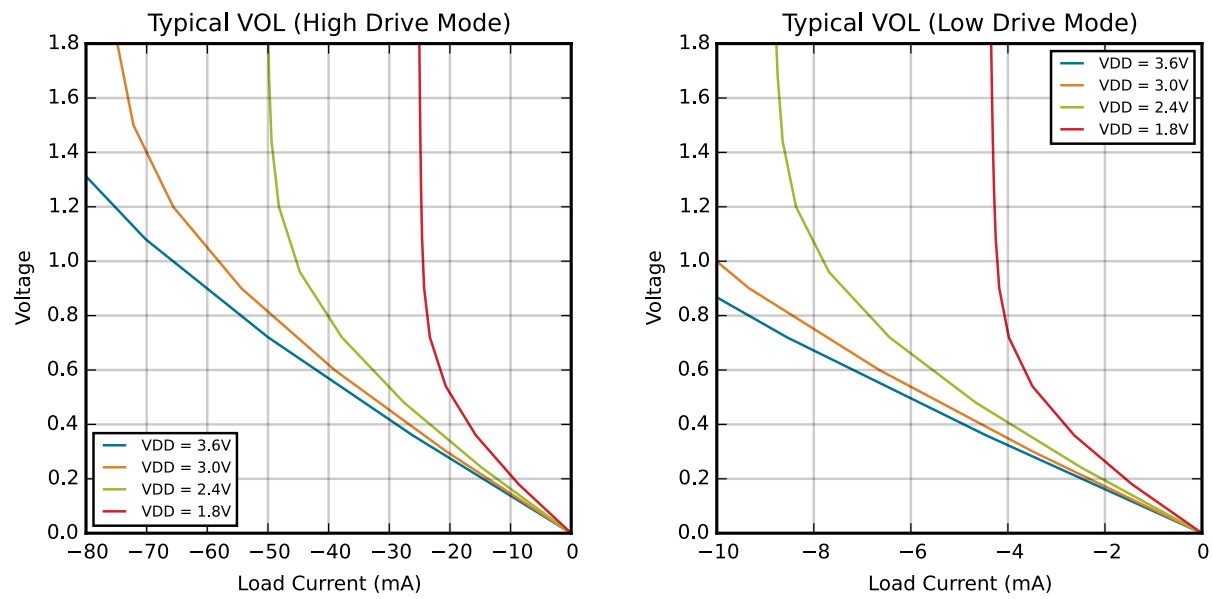


Figure 4.4. Typical V_{OL} Curves

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
3	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	CS0.0 VREF
4	N/C	No Connection			
5	GND	Ground			
6	VDD	Supply Power Input			
7	N/C	No Connection			
8	N/C	No Connection			
9	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
10	P2.7 / C2D	Multifunction I/O / C2 Debug Data			
11	P1.7	Multifunction I/O	Yes	P1MAT.7	XTAL4
12	P1.6	Multifunction I/O	Yes	P1MAT.6	XTAL3
13	N/C	No Connection			
14	P1.5	Multifunction I/O	Yes	P1MAT.5	CS0.13
15	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CS0.12
16	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CS0.11
17	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CS0.10
18	P1.1	Multifunction I/O	Yes	P1MAT.1	CMP0N.4 CS0.9
19	P1.0	Multifunction I/O	Yes	P1MAT.0	CMP0P.4 CS0.8
20	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CS0.7 IREF0
21	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CS0.6
22	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CS0.5

8. QFN20 Package Specifications

8.1 QFN20 Package Dimensions

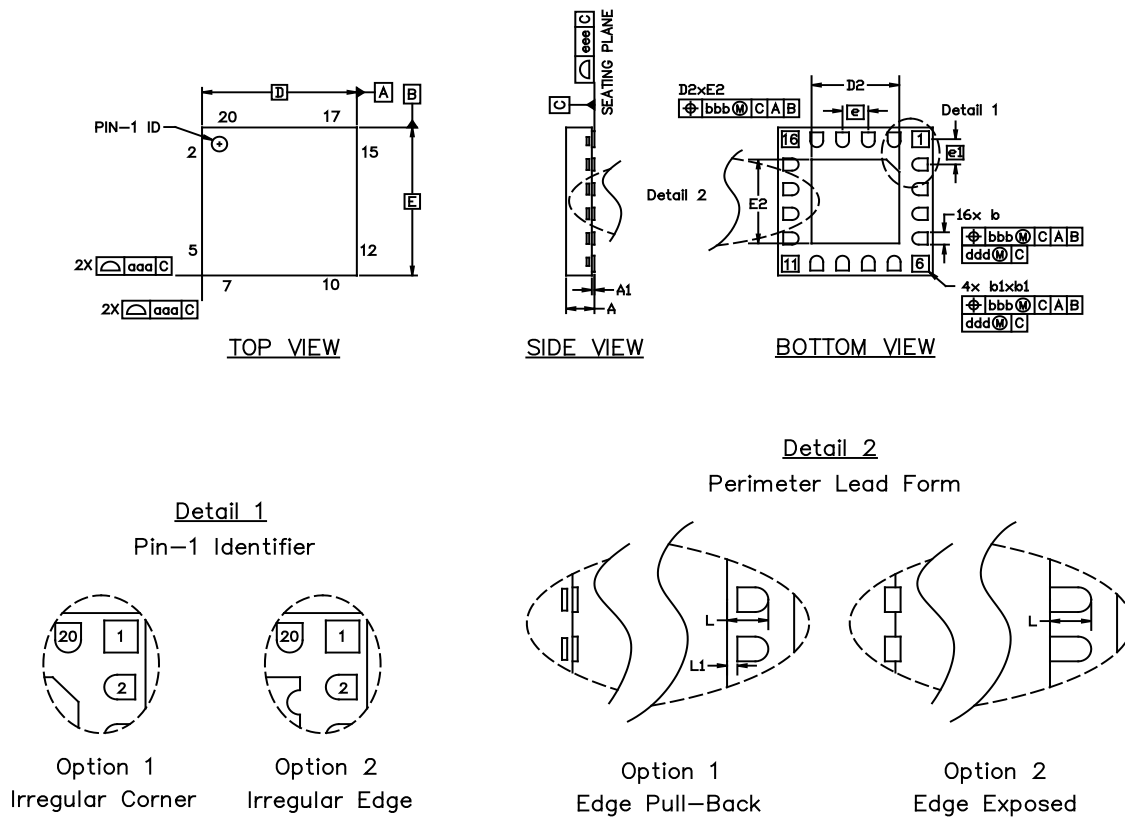


Figure 8.1. QFN20 Package Drawing

Table 8.1. QFN20 Package Dimensions

Dimension	Min	Typ	Max
A	0.50	0.55	0.60
A1	0.00	—	0.05
b	0.20	0.25	0.30
b1	0.275	0.325	0.375
D	3.00 BSC		
D2	1.6	1.70	1.80
e	0.50 BSC		
e1	0.513 BSC		
E	3.00 BSC		
E2	1.60	1.70	1.80
L	0.35	0.40	0.45

9. QFN24 Package Specifications

9.1 QFN24 Package Dimensions

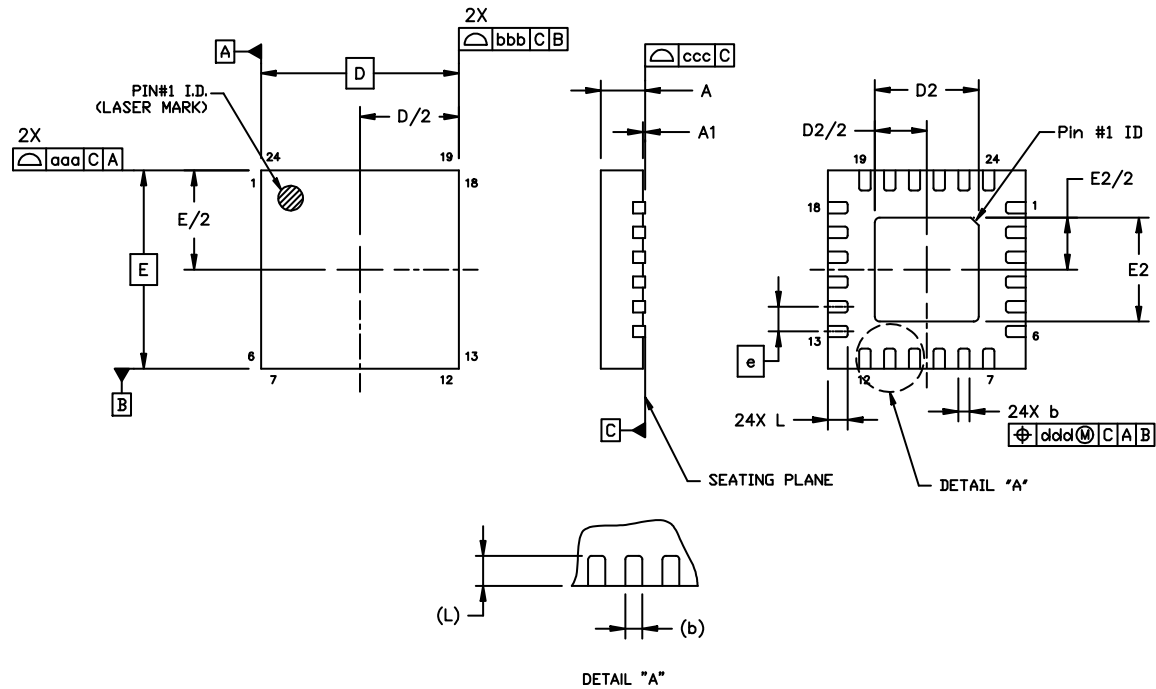


Figure 9.1. QFN24 Package Drawing

Table 9.1. QFN24 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
b	0.18	0.25	0.30
D	4.00 BSC		
D2	2.35	2.45	2.55
e	0.50 BSC		
E	4.00 BSC		
E2	2.35	2.45	2.55
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Dimension	Min	Typ	Max
Note: <ol style="list-style-type: none">1. All dimensions shown are in millimeters (mm) unless otherwise noted.2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.3. This drawing conforms to JEDEC Solid State Outline MO-220.4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.			

11. Revision History

11.1 Revision 1.3

September 23, 2016

Added A-grade parts.

Added [5.2 Debug](#).

Added bootloader pinout information and a reference to *AN945: EFM8 Factory Bootloader User Guide* in [3.10 Bootloader](#).

Added specifications for [4.1.16 SMBus](#).

Added CRC Calculation Time to [4.1.4 Flash Memory](#).

Added a note linking to the Typical VOH and VOL Performance graphs in [4.1.15 Port I/O](#).

Added the t_{POR} and adjusted the V_{POR} falling specifications in [4.1.3 Reset and Supply Monitor](#).

Added a note to [3.1 Introduction](#) referencing the Reference Manual.

Added a note to [3.2 Power](#) to clarify that entering Sleep may disconnect the active debug session.

Specified that the UART has a 1-byte FIFO in [3.6 Communications and Other Digital Peripherals](#).

11.2 Revision 1.2

Added CSP16 package.

Updated the "C2D / P2.0" pin on the QSOP24 pinout diagram to "C2D / P2.7."

Added crystal oscillator drive current typical values to [Table 4.7 Crystal Oscillator on page 18](#).

Corrected the number of capacitive sense channels for 24- and 20-pin packages in [Table 4.14 Capacitive Sense \(CS0\) on page 24](#).

Corrected E dimension shown in [Figure 8.2 QFN20 PCB Land Pattern Drawing on page 50](#).

Added more information to [3.10 Bootloader](#).

11.3 Revision 1.1

Initial release.

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