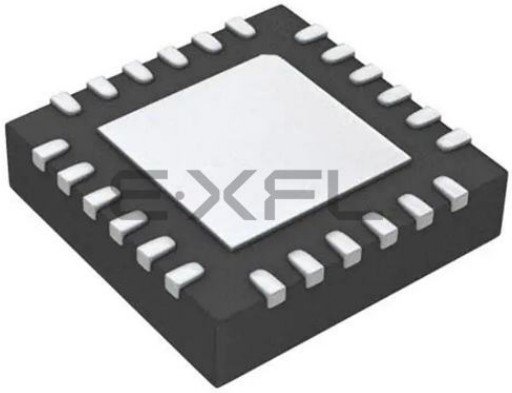

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I²C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8sb10f8g-a-qfn24r

1. Feature List

The EFM8SB1 highlighted features are listed below.

- Core:
  - Pipelined CIP-51 Core
  - Fully compatible with standard 8051 instruction set
  - 70% of instructions execute in 1-2 clock cycles
  - 25 MHz maximum operating frequency
- Memory:
  - Up to 8 kB flash memory, in-system re-programmable from firmware.
  - Up to 512 bytes RAM (including 256 bytes standard 8051 RAM and 256 bytes on-chip XRAM)
- Power:
  - Internal LDO regulator for CPU core voltage
  - Power-on reset circuit and brownout detectors
- I/O: Up to 17 total multifunction I/O pins:
  - Flexible peripheral crossbar for peripheral routing
  - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- Clock Sources:
  - Internal 20 MHz low power oscillator with ±10% accuracy
  - Internal 24.5 MHz precision oscillator with ±2% accuracy
  - Internal 16.4 kHz low-frequency oscillator or RTC 32 kHz crystal (RTC crystal not available on CSP16 packages)
  - External crystal, RC, C, and CMOS clock options
- Timers/Counters and PWM:
  - 32-bit Real Time Clock (RTC)
  - 3-channel Programmable Counter Array (PCA) supporting PWM, capture/compare, and frequency output modes with watchdog timer function
  - 4 x 16-bit general-purpose timers
- Communications and Digital Peripherals:
  - UART
  - SPI™ Master / Slave
  - SMBus™ / I2C™ Master / Slave
  - 16-bit CRC unit, supporting automatic CRC of flash at 256-byte boundaries
- Analog:
  - Capacitive Sense (CS0)
  - Programmable current reference (IREF0)
  - 12-Bit Analog-to-Digital Converter (ADC0)
  - 1 x Low-current analog comparator
- On-Chip, Non-Intrusive Debugging
  - Full memory and register inspection
  - Four hardware breakpoints, single-stepping
- Pre-loaded UART bootloader
- Temperature range -40 to 85 ºC
- Single power supply 1.8 to 3.6 V
- QSOP24, QFN24, QFN20, and CSP16 packages

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8SB1 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing non-volatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Each device is specified for 1.8 to 3.6 V operation. Devices are AEC-Q100 qualified (Grade 3) and are available in 16-pin CSP, 20-pin QFN, 24-pin QFN, or 24-pin QSOP packages. All package options are lead-free and RoHS compliant.

Note: CSP devices can be handled and soldered using industry standard surface mount assembly techniques. However, because CSP devices are essentially a piece of silicon and are not encapsulated in plastic, they are susceptible to mechanical damage and may be sensitive to light. When CSP packages must be used in an environment exposed to light, it may be necessary to cover the top and sides with an opaque material.

Timers (Timer 0, Timer 1, Timer 2, and Timer 3)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2 and Timer 3 are 16-bit timers including the following features:

- Clock sources include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8.
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- Comparator 0 or RTC0 capture (Timer 2)
- RTC0 or EXTCLK/8 capture (Timer 3)

Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) integrated within the PCA0 peripheral. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software. The state of the RSTb pin is unaffected by this reset.

The Watchdog Timer integrated in the PCA0 peripheral has the following features:

- Programmable timeout interval
- Runs from the selected PCA clock source
- Automatically enabled after any system reset

3.6 Communications and Other Digital Peripherals

Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions.
- Baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive).
- 8- or 9-bit data.
- Automatic start and stop generation.
- Single-byte FIFO on transmit and receive.

Low Current Comparator (CMP0)

An analog comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator module includes the following features:

- Input options in addition to the pins:
  - Capacitive Sense Comparator output.
  - VDD.
  - VDD divided by 2.
  - Internal connection to LDO output.
  - Direct connection to GND.
- Synchronous and asynchronous outputs can be routed to pins via crossbar.
- Programmable hysteresis between 0 and ±20 mV.
- Programmable response time.
- Interrupts generated on rising, falling, or both edges.

3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. The Port I/O latches are reset to 1 in open-drain mode. Weak pullups are enabled during and after the reset. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- Watchdog timer reset
- Missing clock detector reset
- Flash error reset
- RTC0 alarm or oscillator failure

3.9 Debugging

The EFM8SB1 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

3.10 Bootloader

All devices come pre-programmed with a UART bootloader. This bootloader resides in the last page of flash and can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

More information about the bootloader protocol and usage can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website (www.silabs.com/8bit-appnotes) or within Simplicity Studio by using the [**Application Notes**] tile.

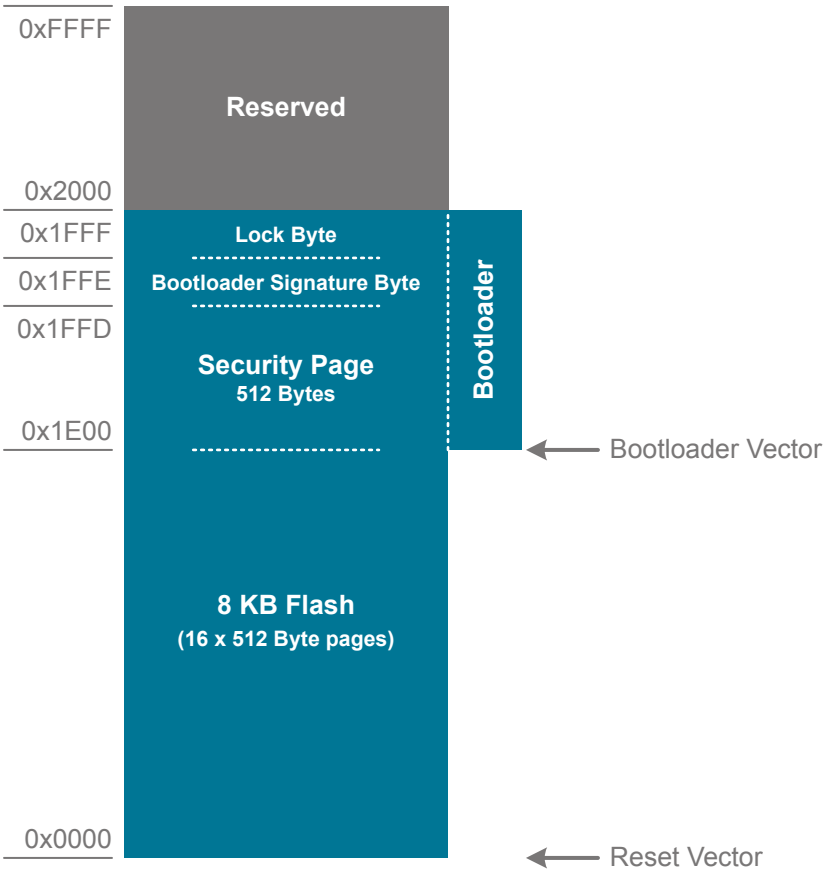

Figure 3.2. Flash Memory Map with Bootloader—8 kB Devices

Table 3.2. Summary of Pins for Bootloader Communication

Bootloader	Pins for Bootload Communication
UART	TX – P0.4
	RX – P0.5

Table 3.3. Summary of Pins for Bootload Mode Entry

Device Package	Pin for Bootload Mode Entry
QFN20	P2.7 / C2D
QFN24	P2.7 / C2D
QSOP24	P2.7 / C2D
CSP16	P2.7 / C2D

4.1.9 ADC

Table 4.9. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}	12 Bit Mode		12		Bits
		10 Bit Mode		10		Bits
Throughput Rate	f_S	12 Bit Mode	—	—	75	ksps
		10 Bit Mode	—	—	300	ksps
Tracking Time	t_{TRK}	Initial Acquisition	1.5	—	—	us
		Subsequent Acquisitions (DC input, burst mode)	1.1	—	—	us
Power-On Time	t_{PWR}		1.5	—	—	µs
SAR Clock Frequency	f_{SAR}	High Speed Mode,	—	—	8.33	MHz
		Low Power Mode	—	—	4.4	MHz
Conversion Time	T_{CNV}	10-Bit Conversion	13	—	—	Clocks
Sample/Hold Capacitor	C_{SAR}	Gain = 1	—	16	—	pF
		Gain = 0.5	—	13	—	pF
Input Pin Capacitance	C_{IN}		—	20	—	pF
Input Mux Impedance	R_{MUX}		—	5	—	kΩ
Voltage Reference Range	V_{REF}		1	—	V_{DD}	V
Input Voltage Range[1]	V_{IN}	Gain = 1	0	—	V_{REF}	V
		Gain = 0.5	0	—	2 x V_{REF}	V
Power Supply Rejection Ratio	$PSRR_{ADC}$	Internal High Speed VREF	—	67	—	dB
		External VREF	—	74	—	dB
DC Performance						
Integral Nonlinearity	INL	12 Bit Mode	—	±1	±1.5	LSB
		10 Bit Mode	—	±0.5	±1	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode	—	±0.8	±1	LSB
		10 Bit Mode	—	±0.5	±1	LSB
Offset Error	E_{OFF}	12 Bit Mode, VREF = 1.65 V	–3	0	3	LSB
		10 Bit Mode, VREF = 1.65 V	–2	0	2	LSB
Offset Temperature Coefficient	TC_{OFF}		—	0.004	—	LSB/°C
Slope Error	E_M	12 Bit Mode	—	±0.02	±0.1	%
		10 Bit Mode	—	±0.06	±0.24	%
Dynamic Performance 10 kHz Sine Wave Input 1dB below full scale, Max throughput						
Signal-to-Noise	SNR	12 Bit Mode	62	65	—	dB
		10 Bit Mode	54	58	—	dB

4.1.12 Comparators

Table 4.12. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	120	—	ns
		–100 mV Differential	—	110	—	ns
Response Time, CPMD = 11 (Lowest Power)	t_{RESP3}	+100 mV Differential	—	1.25	—	µs
		–100 mV Differential	—	3.2	—	µs
Positive Hysterisis Mode 0 (CPMD = 00)	HYS_{CP+}	CPHYP = 00	—	0.4	—	mV
		CPHYP = 01	—	8	—	mV
		CPHYP = 10	—	16	—	mV
		CPHYP = 11	—	32	—	mV
Negative Hysterisis Mode 0 (CPMD = 00)	HYS_{CP-}	CPHYN = 00	—	-0.4	—	mV
		CPHYN = 01	—	–8	—	mV
		CPHYN = 10	—	–16	—	mV
		CPHYN = 11	—	–32	—	mV
Positive Hysterisis Mode 1 (CPMD = 01)	HYS_{CP+}	CPHYP = 00	—	0.5	—	mV
		CPHYP = 01	—	6	—	mV
		CPHYP = 10	—	12	—	mV
		CPHYP = 11	—	24	—	mV
Negative Hysterisis Mode 1 (CPMD = 01)	HYS_{CP-}	CPHYN = 00	—	-0.5	—	mV
		CPHYN = 01	—	–6	—	mV
		CPHYN = 10	—	–12	—	mV
		CPHYN = 11	—	–24	—	mV
Positive Hysterisis Mode 2 (CPMD = 10)	HYS_{CP+}	CPHYP = 00	—	0.7	—	mV
		CPHYP = 01	—	4.5	—	mV
		CPHYP = 10	—	9	—	mV
		CPHYP = 11	—	18	—	mV
Negative Hysterisis Mode 2 (CPMD = 10)	HYS_{CP-}	CPHYN = 00	—	-0.6	—	mV
		CPHYN = 01	—	–4.5	—	mV
		CPHYN = 10	—	–9	—	mV
		CPHYN = 11	—	–18	—	mV
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CPHYP = 00	—	1.5	—	mV
		CPHYP = 01	—	4	—	mV
		CPHYP = 10	—	8	—	mV
		CPHYP = 11	—	16	—	mV

4.1.15 Port I/O

Table 4.15. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (High Drive)[1]	V_{OH}	I_{OH} = –3 mA	V_{DD} – 0.7	—	—	V
Output Low Voltage (High Drive)[1]	V_{OL}	I_{OL} = 8.5 mA	—	—	0.6	V
Output High Voltage (Low Drive)[1]	V_{OH}	I_{OH} = –1 mA	V_{DD} – 0.7	—	—	V
Output Low Voltage (Low Drive)[1]	V_{OL}	I_{OL} = 1.4 mA	—	—	0.6	V
Input High Voltage	V_{IH}	V_{DD} = 2.0 to 3.6 V	V_{DD} – 0.6	—	—	V
		V_{DD} = 1.8 to 2.0 V	0.7 x V_{DD}	—	—	V
Input Low Voltage	V_{IL}	V_{DD} = 2.0 to 3.6 V	—	—	0.6	V
		V_{DD} = 1.8 to 2.0 V	—	—	0.3 x V_{DD}	V
Weak Pull-Up Current	I_{PU}	V_{DD} = 1.8 V V_{IN} = 0 V	—	–4	—	µA
		V_{DD} = 3.6 V V_{IN} = 0 V	–35	–20	—	µA
Input Leakage	I_{LK}	Weak pullup disabled or pin in analog mode	–1	—	1	µA

Note:
1. See Figure 4.3 Typical V_{OH} Curves on page 29 and Figure 4.4 Typical V_{OL} Curves on page 30 for more information.

4.4 Typical Performance Curves

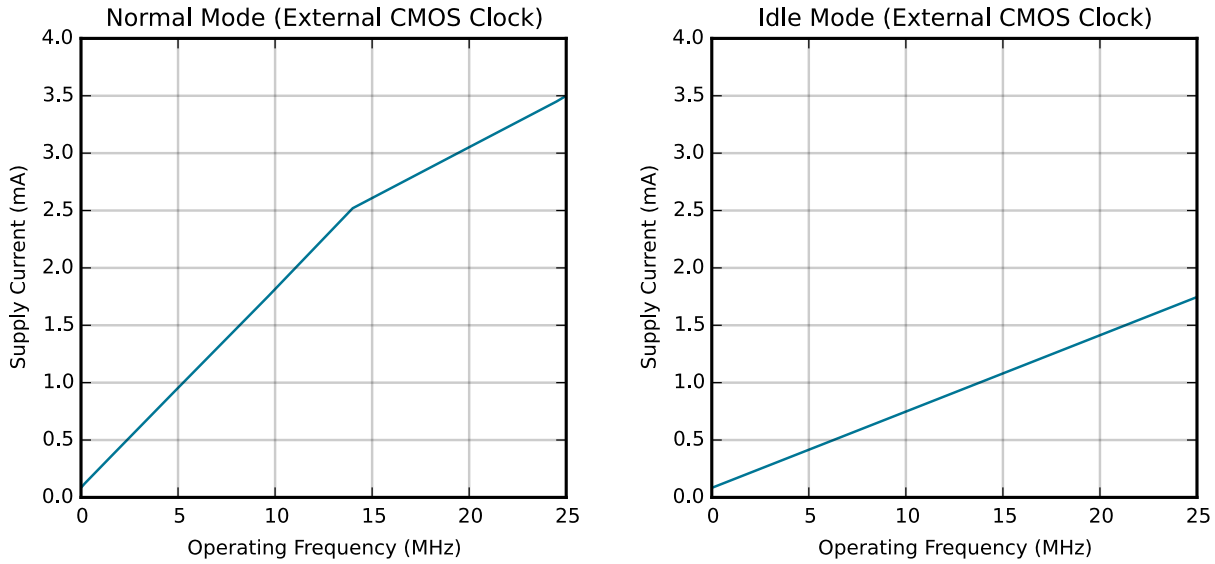

Figure 4.2. Typical Operating Supply Current (full supply voltage range)

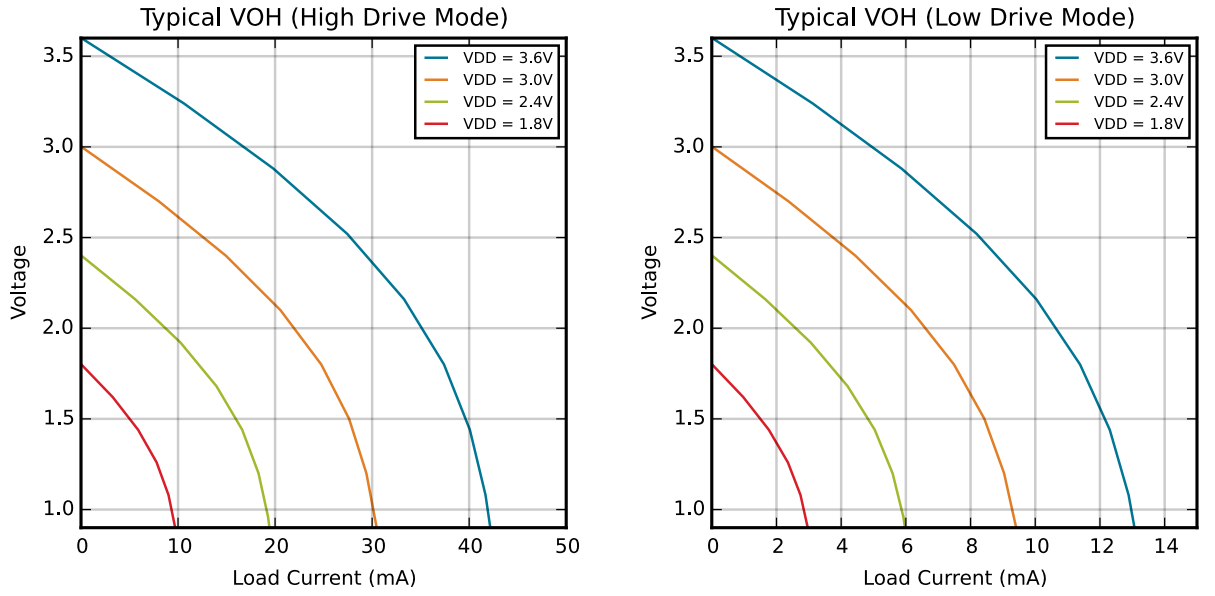

Figure 4.3. Typical V_{OH} Curves

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application note, "AN203: 8-bit MCU Printed Circuit Board Design Notes", contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/8bit-appnotes).

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
22	P0.2	Multifunction I/O	Yes	P0MAT.2 RTCOUT INT0.2 INT1.2	ADC0.2 CS0.2 XTAL1
23	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CS0.1 AGND
24	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	CS0.0 VREF
Center	GND	Ground			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
3	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	CS0.0 VREF
4	N/C	No Connection			
5	GND	Ground			
6	VDD	Supply Power Input			
7	N/C	No Connection			
8	N/C	No Connection			
9	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
10	P2.7 / C2D	Multifunction I/O / C2 Debug Data			
11	P1.7	Multifunction I/O	Yes	P1MAT.7	XTAL4
12	P1.6	Multifunction I/O	Yes	P1MAT.6	XTAL3
13	N/C	No Connection			
14	P1.5	Multifunction I/O	Yes	P1MAT.5	CS0.13
15	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CS0.12
16	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CS0.11
17	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CS0.10
18	P1.1	Multifunction I/O	Yes	P1MAT.1	CMP0N.4 CS0.9
19	P1.0	Multifunction I/O	Yes	P1MAT.0	CMP0P.4 CS0.8
20	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CS0.7 IREF0
21	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CS0.6
22	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CS0.5

Dimension	Min	Typ	Max
E1		1.20 BSC	
SD		0.2	
SE		0.2	
n		16	
aaa		0.03	
bbb		0.06	
ccc		0.05	
ddd		0.015	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Primary datum “C” and seating plane are defined by the spherical crowns of the solder balls.
4. Dimension “b” is measured at the maximum solder bump diameter, parallel to primary datum “C”.
5. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7.3 CSP16 Package Marking

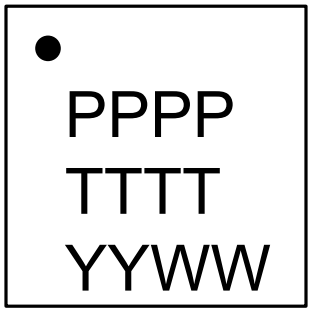

Figure 7.3. CSP16 Package Marking

The package marking consists of:

- PPPP – The part number designation.
- TTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

8. QFN20 Package Specifications

8.1 QFN20 Package Dimensions

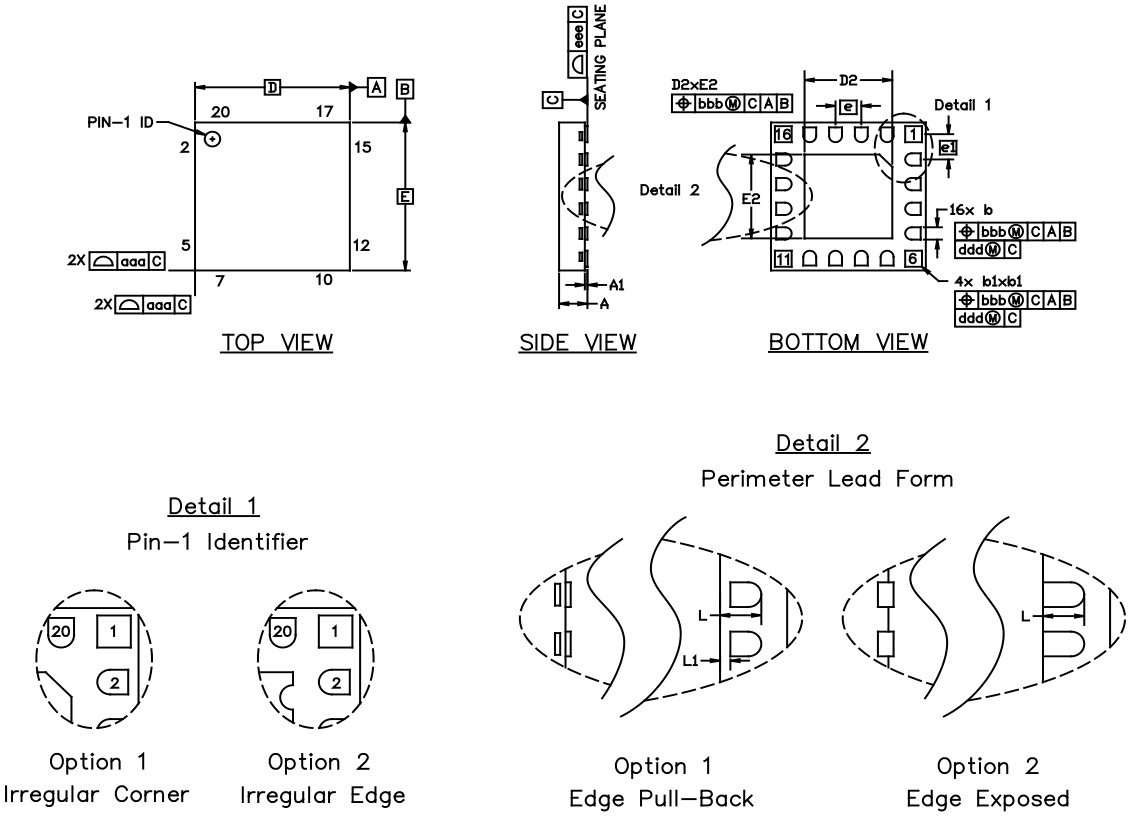

Figure 8.1. QFN20 Package Drawing

Table 8.1. QFN20 Package Dimensions

Dimension	Min	Typ	Max
A	0.50	0.55	0.60
A1	0.00	—	0.05
b	0.20	0.25	0.30
b1	0.275	0.325	0.375
D		3.00 BSC	
D2	1.6	1.70	1.80
e		0.50 BSC	
e1		0.513 BSC	
E		3.00 BSC	
E2	1.60	1.70	1.80
L	0.35	0.40	0.45

9. QFN24 Package Specifications

9.1 QFN24 Package Dimensions

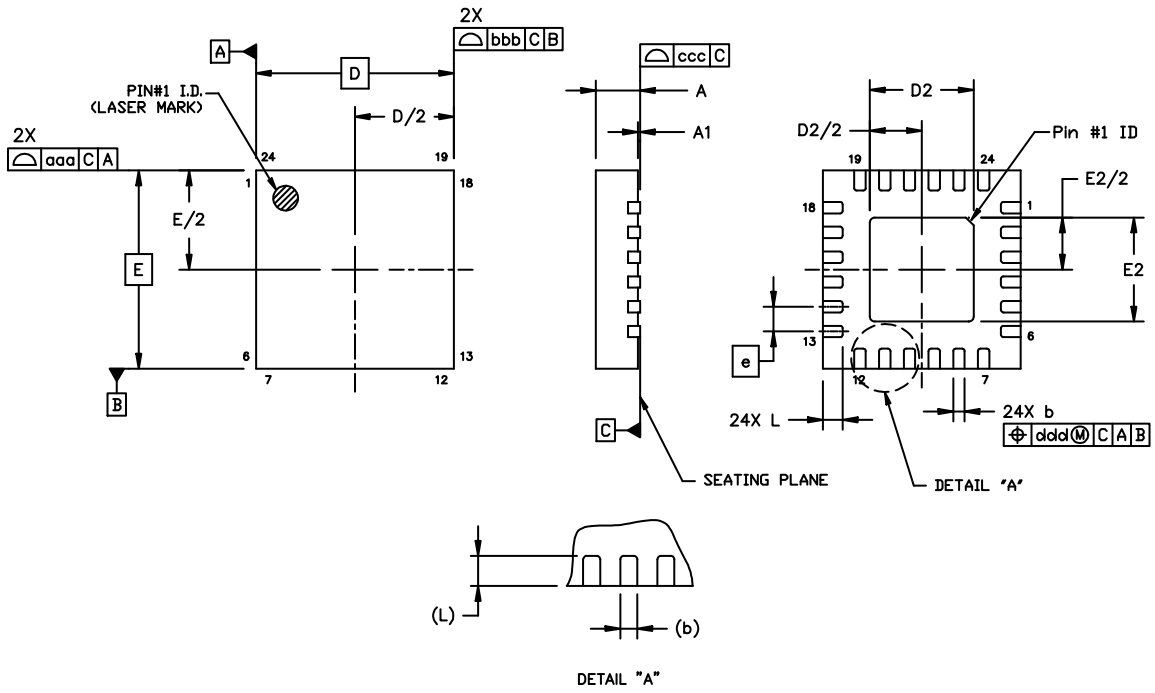

Figure 9.1. QFN24 Package Drawing

Table 9.1. QFN24 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
b	0.18	0.25	0.30
D		4.00 BSC	
D2	2.35	2.45	2.55
e		0.50 BSC	
E		4.00 BSC	
E2	2.35	2.45	2.55
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

9.2 QFN24 PCB Land Pattern

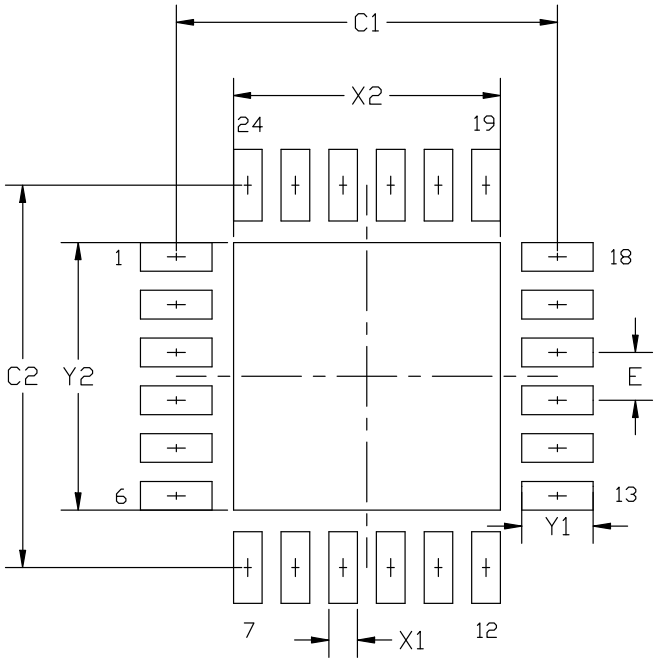

Figure 9.2. QFN24 PCB Land Pattern Drawing

Table 9.2. QFN24 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	3.90	4.00
C2	3.90	4.00
E	0.50 BSC	
X1	0.20	0.30
X2	2.70	2.80
Y1	0.65	0.75
Y2	2.70	2.80

Dimension	Min	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2 x 2 array of 1.10 mm x 1.10 mm openings on 1.30 mm pitch should be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.3 QFN24 Package Marking

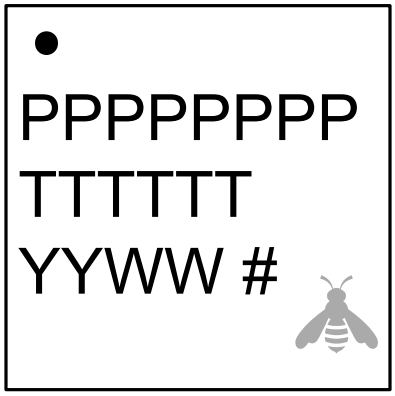

Figure 9.3. QFN24 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

10. QSOP24 Package Specifications

10.1 QSOP24 Package Dimensions

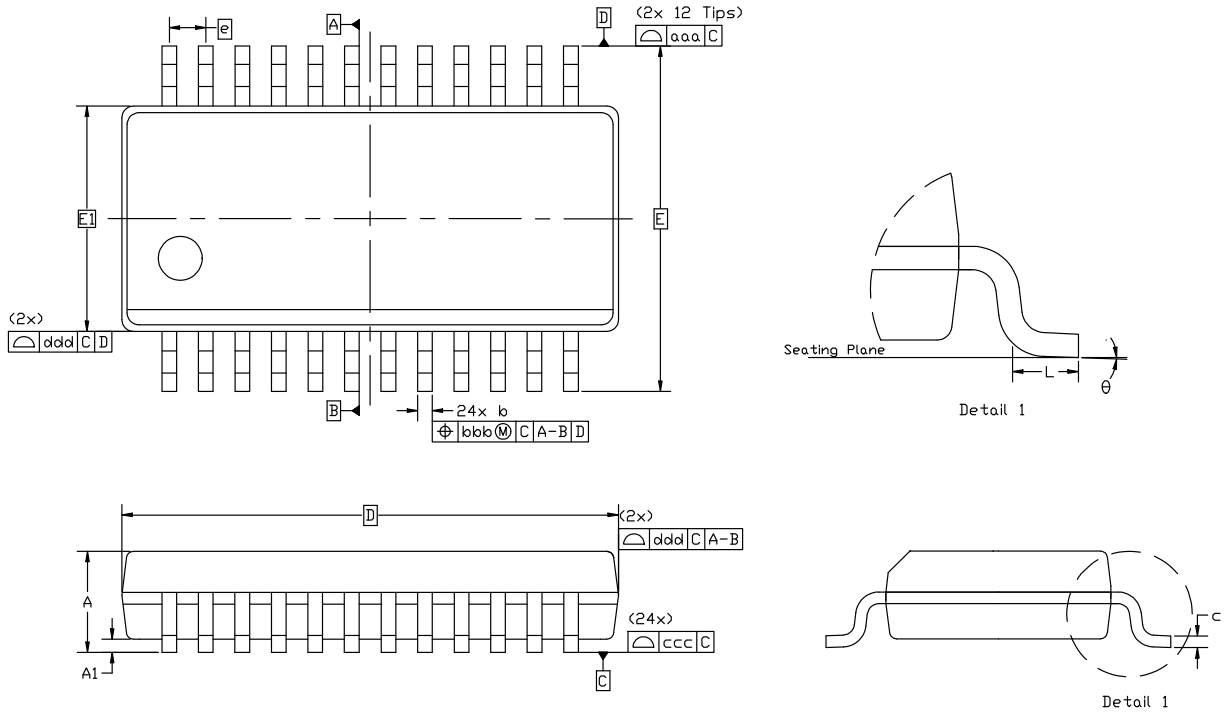

Figure 10.1. QSOP24 Package Drawing

Table 10.1. QSOP24 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.75
A1	0.10	—	0.25
b	0.20	—	0.30
c	0.10	—	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	0.635 BSC		
L	0.40	—	1.27
theta	0°	—	8°

10.2 QSOP24 PCB Land Pattern

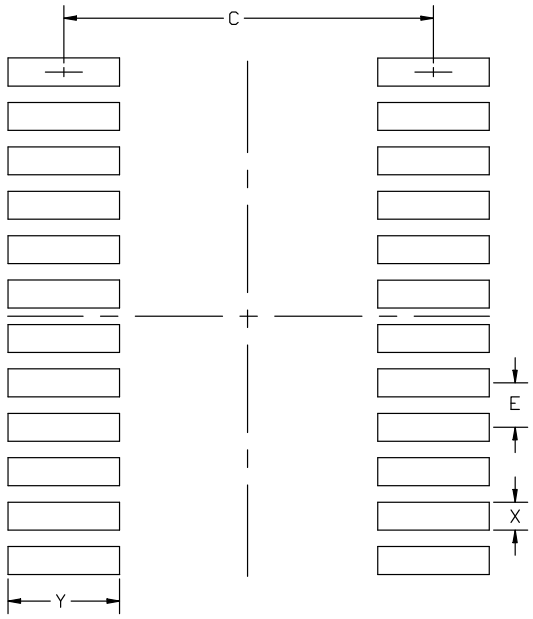

Figure 10.2. QSOP24 PCB Land Pattern Drawing

Table 10.2. QSOP24 PCB Land Pattern Dimensions

Dimension	Min	Max
C	5.20	5.30
E	0.635 BSC	
X	0.30	0.40
Y	1.50	1.60

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.