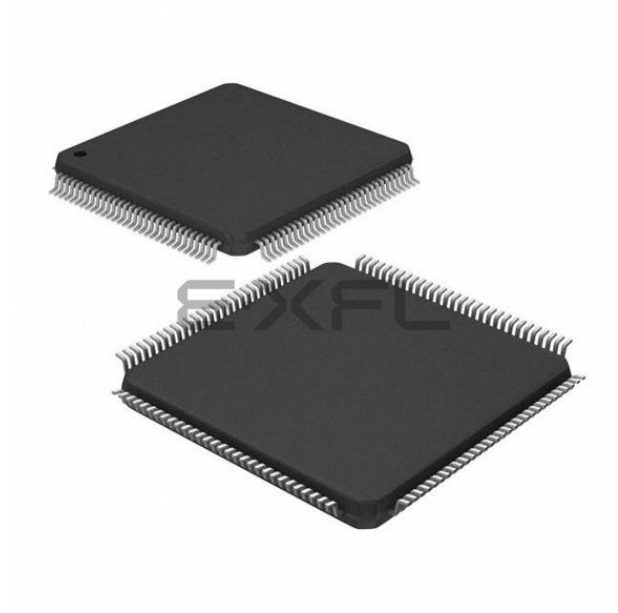

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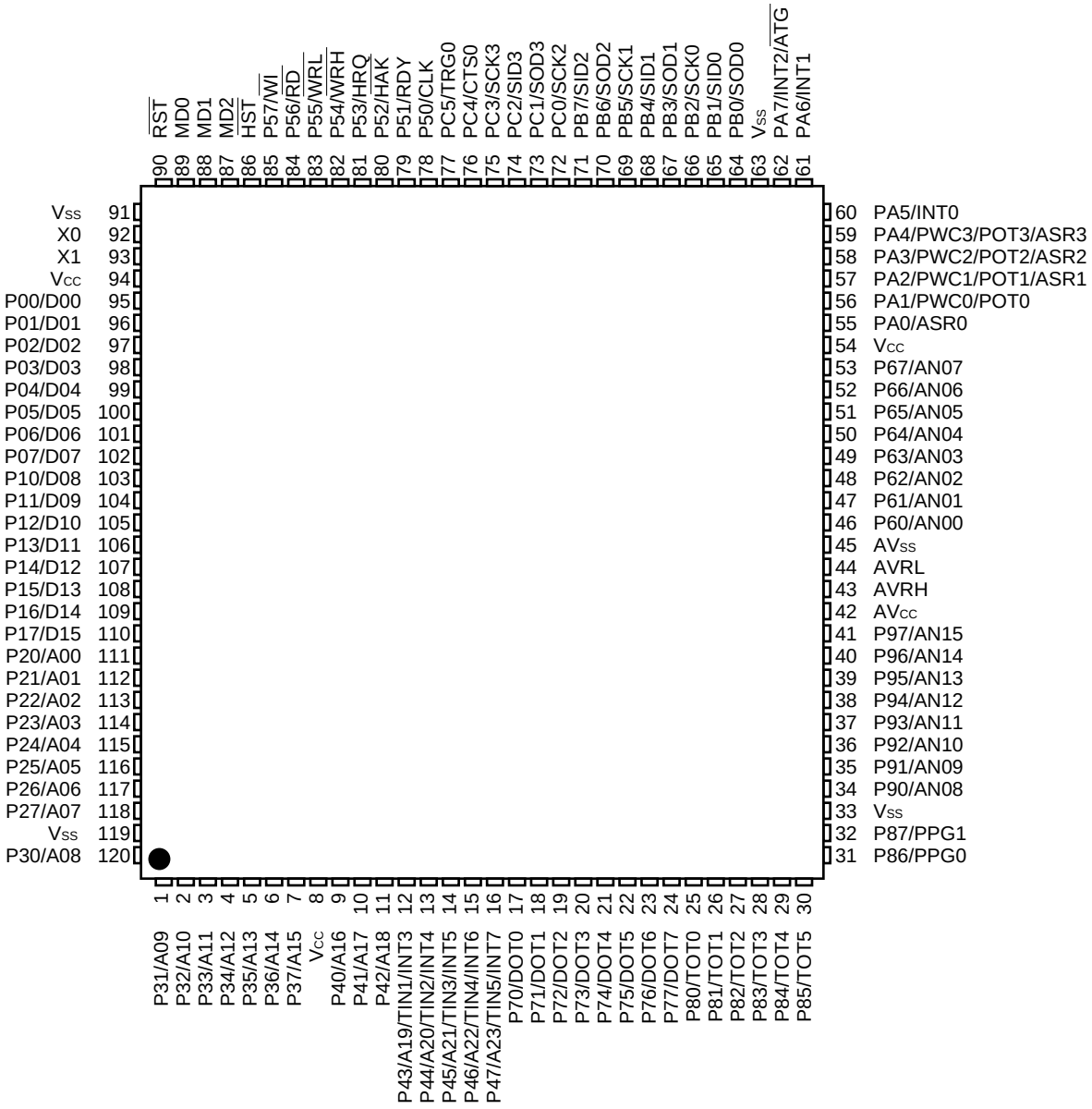
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16F
Core Size	16-Bit
Speed	16MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	102
Program Memory Size	64KB (64K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-BQFP
Supplier Device Package	120-QFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90223pf-gt-372

■ PIN ASSIGNMENT

(Top view)



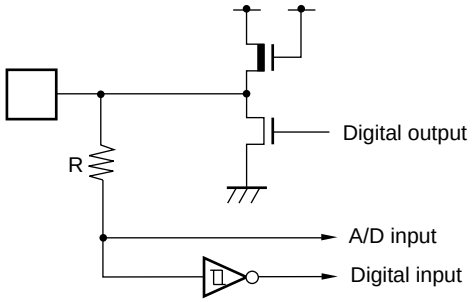
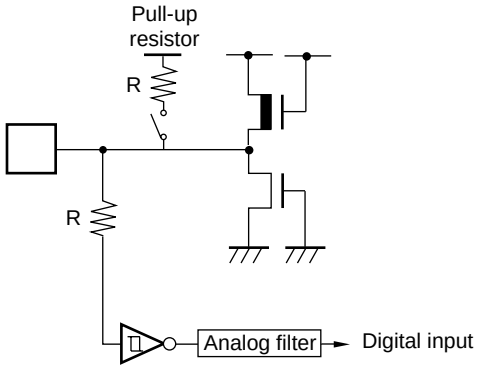
(FPT-120P-M03)
(FPT-120C-C02)

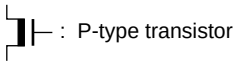
Pin no. QFP*	Pin name	Circuit type	Function
62	INT2	B	DTP/External interrupt request input pin When DTP/external interrupts are enabled, these inputs may be used suddenly at any time; therefore, it is necessary to stop output by other functions on these pins, except when using them for output deliberately. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode.
	$\overline{ATG}$		10-bit A/D converter external trigger input pin When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode.
64	PB0	C	General-purpose I/O port This function is valid when the UART0 (ch.0) serial data output specification is “disabled”.
	SOD0		UART0 (ch.0) serial data output This function is valid when the UART0 (ch.0) serial data output specification is “enabled”.
65	PB1	C	General-purpose I/O port This function is always valid.
	SID0		UART0 (ch.0) serial data input pin During UART0 (ch.0) input operations, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately.
66	PB2	C	General-purpose output port This function is valid when the UART0 (ch.0) clock output specification is “disabled”.
	SCK0		UART0 (ch.0) clock output pin The clock output function is valid when the UART0 (ch.0) clock output specification is “enabled”. UART0 (ch.0) external clock input pin. This function is valid when the port is in input mode and the UART0 (ch.0) specification is external clock mode.
67	PB3	C	General-purpose I/O port This function is valid when the UART0 (ch.1) serial data output specification is “disabled”.
	SOD1		UART0 (ch.1) serial data output pin This function is valid when the UART0 (ch.1) serial data output specification is “enabled”.
68	PB4	C	General-purpose I/O port This function is always valid.
	SID1		UART0 (ch.1) serial data input pin During UART0 (ch.1) input operations, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately.

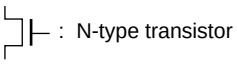
* : FPT-120P-M03, FPT-120C-C02

(Continued)

(Continued)

Type	Circuit	Remarks
F		• N-channel open-drain output • CMOS-level hysteresis input with A/D control and with standby control
G		• CMOS-level hysteresis input with no standby control and with pull-up resistor • With input analog filter (40 ns Typ.) MB90223, MB90224: $\overline{\text{RST}}$ pin can be set to with or without a pull-up resistor by a mask option. MB90P224A: With pull-up resistor MB90W224A: With pull-up resistor MB90P224B: With no pull-up resistor MB90W224B: With no pull-up resistor

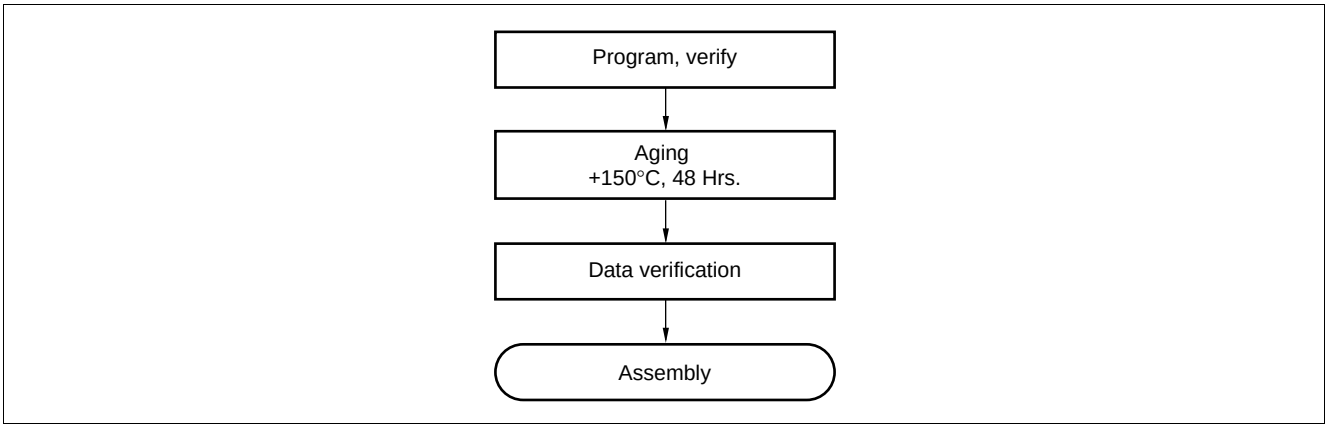




Note: The pull-up and pull-down resistors are always connected, regardless of the state.

5. Recommended Screening Conditions

High temperature aging is recommended as the pre-assembly screening procedure.



6. Programming Yeild

MB90P224A/P224B cannot be write-tested for all bits due to their nature. Therefore the write yield cannot always be guaranteed to be 100%.

7. Pin Assignments in EPROM Mode

(1) Pins Compatible with MBM27C1000

MBM27C1000		MB90P224A/P224B/ MB90W224A/W224B	
Pin no.	Pin name	Pin no.	Pin name
1	V_{PP}	87	MD2 (V_{PP})
2	OE	83	P55
3	A15	7	P37
4	A12	4	P34
5	A07	118	P27
6	A06	117	P26
7	A05	116	P25
8	A04	115	P24
9	A03	114	P23
10	A02	113	P22
11	A01	112	P21
12	A00	111	P20
13	D00	95	P00
14	D01	96	P01
15	D02	97	P02
16	GND	33, 63, 91,119	V_{SS}

MBM27C1000		MB90P224A/P224B/ MB90W224A/W224B	
Pin no.	Pin name	Pin no.	Pin name
32	V_{CC}	8, 54, 94	V_{CC}
31	PGM	84	P56
30	N.C.	—	—
29	A14	6	P36
28	A13	5	P35
27	A08	120	P30
26	A09	1	P31
25	A11	3	P33
24	A16	9	P40
23	A10	2	P32
22	CE	82	P54
21	D07	102	P07
20	D06	101	P06
19	D05	100	P05
18	D04	99	P04
17	D03	98	P03

Address	Register	Register name	Access	Resouce name	Initial value
000062H	OCU0 control register 01	CCR01	R/W	OCU (Output Compare Unit)	1 1 1 1 0 0 0 0
000063H					– – – – 0 0 0 0
000064H	(Reserved area)*1				
000065H					
000066H					
000067H					
000068H	OCU0 control register 10	CCR10	R/W	OCU (Output Compare Unit)	– – – – 0 0 0 0
000069H					0 0 0 0 0 0 0 0
00006AH	OCU0 control register 11	CCR11	R/W		– – – – 0 0 0 0
00006BH					0 0 0 0 0 0 0 0
00006CH	(Reserved area)*1				
00006DH					
00006EH					
00006FH					
000070H	Free-run timer control register	TCCR	R/W	24-bit timer counter	1 1 0 0 0 0 0 0
000071H					– – 1 1 1 1 1 1
000072H	Free-run timer lower-order data register	TCRL	R		0 0 0 0 0 0 0 0
000073H					0 0 0 0 0 0 0 0
000074H	Free-run timer upper-order data register	TCRH			0 0 0 0 0 0 0 0
000075H					0 0 0 0 0 0 0 0
000076H	(Reserved area)*1				
000077H					
000078H					
000079H					
00007AH	PWC divider ratio control register 0	DIVR0	R/W	PWC timer 0	– – – – – – 0 0
00007BH	Reserved area*1				
00007CH	PWC divider ratio control register 1	DIVR1	R/W	PWC timer 1	– – – – – – 0 0
00007DH	Reserved area*1				
00007EH	PWC divider ratio control register 2	DIVR2	R/W	PWC timer 2	– – – – – – 0 0
00007FH	Reserved area*1				
000080H	PWC divider ratio control register 3	DIVR3	R/W	PWC timer 3	– – – – – – 0 0
000081H to 8DH	(Reserved area)*1				

(Continued)

Address	Register	Register name	Access	Resouce name	Initial value
00008E$_H$	WI control register	WICR	R/W	Write-inhibit RAM	– – – X – – – –
00008F$_H$	(Reserved area)[*1]				
000090$_H$ to 9E$_H$					
00009F$_H$	Delay interrupt source generation /release register	DIRR	R/W	Delay interrupt generation module	– – – – – – – 0
0000A0$_H$	Standby control register	STBYC	R/W	Low power consumption	0 0 0 1 * * * *
0000A3$_H$	Address mid-order control register	MACR	W	External pin	# # # # # # # #
0000A4$_H$	Address higher-order control register	HACR	W	External pin	# # # # # # # #
0000A5$_H$	External pin control register	EPCR	W	External pin	# # 0 – 0 # 0 0
0000A8$_H$	Watchdog timer control register	WDTC	R/W	Watchdog timer	X X X X X X X X
0000A9$_H$	Timebase timer control register	TBTC	R/W	Timebase timer	– – – 0 0 0 0 0
0000B0$_H$	Interrupt control register 00	ICR00	R/W	Interrupt controller	0 0 0 0 0 1 1 1
0000B1$_H$	Interrupt control register 01	ICR01	R/W		0 0 0 0 0 1 1 1
0000B2$_H$	Interrupt control register 02	ICR02	R/W		0 0 0 0 0 1 1 1
0000B3$_H$	Interrupt control register 03	ICR03	R/W		0 0 0 0 0 1 1 1
0000B4$_H$	Interrupt control register 04	ICR04	R/W		0 0 0 0 0 1 1 1
0000B5$_H$	Interrupt control register 05	ICR05	R/W		0 0 0 0 0 1 1 1
0000B6$_H$	Interrupt control register 06	ICR06	R/W		0 0 0 0 0 1 1 1
0000B7$_H$	Interrupt control register 07	ICR07	R/W		0 0 0 0 0 1 1 1
0000B8$_H$	Interrupt control register 08	ICR08	R/W		0 0 0 0 0 1 1 1
0000B9$_H$	Interrupt control register 09	ICR09	R/W		0 0 0 0 0 1 1 1
0000BA$_H$	Interrupt control register 10	ICR10	R/W		0 0 0 0 0 1 1 1
0000BB$_H$	Interrupt control register 11	ICR11	R/W		0 0 0 0 0 1 1 1
0000BC$_H$	Interrupt control register 12	ICR12	R/W		0 0 0 0 0 1 1 1
0000BD$_H$	Interrupt control register 13	ICR13	R/W		0 0 0 0 0 1 1 1
0000BE$_H$	Interrupt control register 14	ICR14	R/W		0 0 0 0 0 1 1 1
0000BF$_H$	Interrupt control register 15	ICR15	R/W		0 0 0 0 0 1 1 1
0000C0$_H$ to FF$_H$	(External area)[*2]				
001F00$_H$	PWC data buffer register 0	PWCR0	R/W	PWC timer 0	0 0 0 0 0 0 0 0
001F01$_H$					0 0 0 0 0 0 0 0

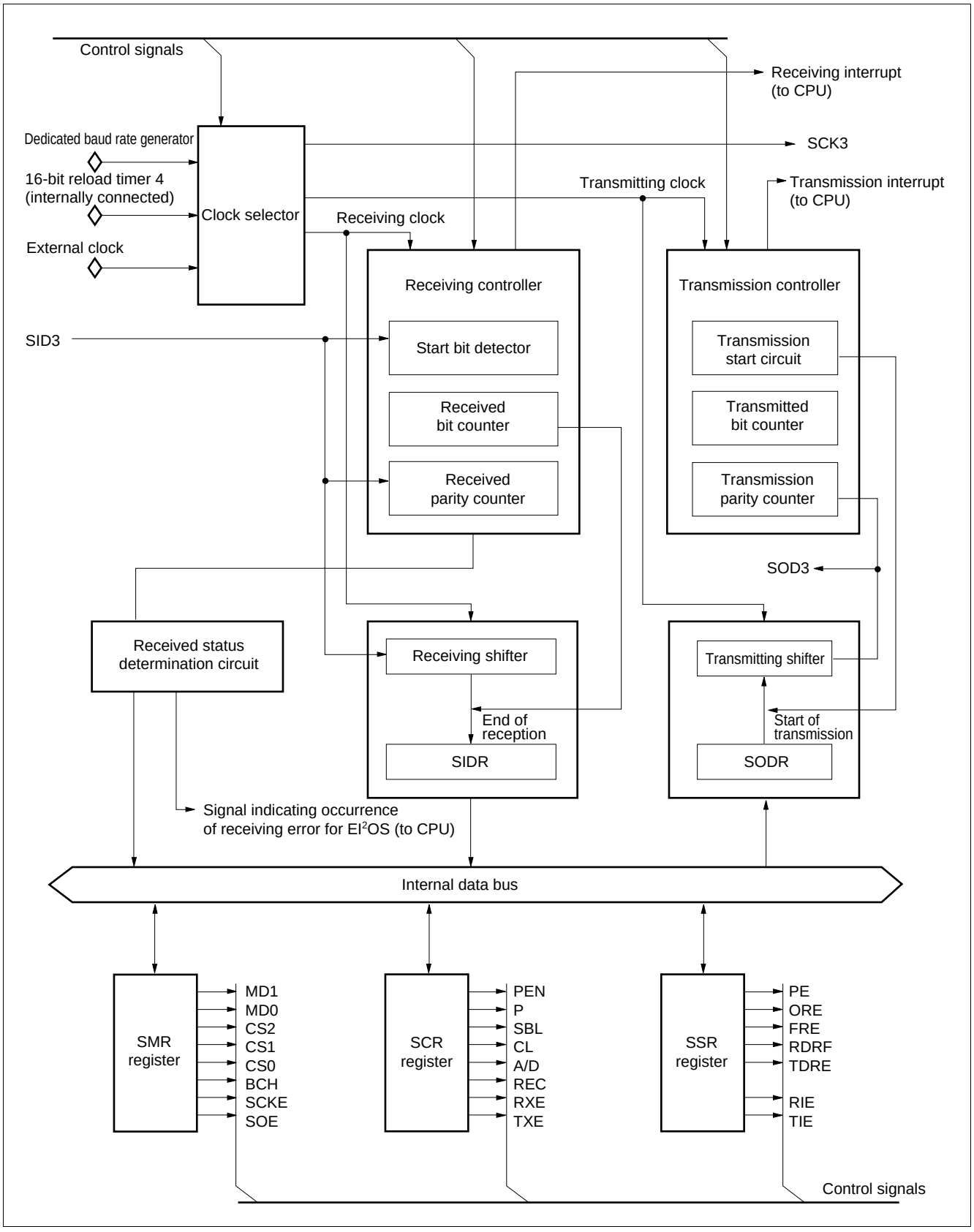
(Continued)

(Continued)

Address	Register	Register name	Access	Resouce name	Initial value
001F48H	PPG cycle setting register 0	PCSR0	W	16-bit PPG timer 0	XXXXXXXX
001F49H					XXXXXXXX
001F4AH	PPG duty setting register 0	PDUT0	W		XXXXXXXX
001F4BH					XXXXXXXX
001F4CH	PPG cycle setting register 1	PCSR1	W	16-bit PPG timer 1	XXXXXXXX
001F4DH					XXXXXXXX
001F4EH	PPG duty setting register 1	PDUT1	W		XXXXXXXX
001F4FH					XXXXXXXX
001F50H	ICU lower-order data register 0	ICRL0	R	Input capture 0	XXXXXXXX
001F51H					XXXXXXXX
001F52H	ICU higher-order data register 0	ICRH0	R		XXXXXXXX
001F53H					00000000
001F54H	ICU lower-order data register 1	ICRL1	R	Input capture 1	XXXXXXXX
001F55H					XXXXXXXX
001F56H	ICU higher-order data register 1	ICRH1	R		XXXXXXXX
001F57H					00000000
001F58H	ICU lower-order data register 2	ICRL2	R	Input capture 2	XXXXXXXX
001F59H					XXXXXXXX
001F5AH	ICU higher-order data register 2	ICRH2	R		XXXXXXXX
001F5BH					00000000
001F5CH	ICU lower-order data register 3	ICRL3	R	Input capture 3	XXXXXXXX
001F5DH					XXXXXXXX
001F5EH	ICU higher-order data register 3	ICRH3	R		XXXXXXXX
001F5FH					00000000
001F60H to 1FFFH	(Reserved area)*1				

Initial value
0: The initial value of this bit is “0”.
1: The initial value of this bit is “1”.
X: The initial value of this bit is undefined.
–: This bit is not used. The initial value is undefined.
*: The initial value of this bit varies with the reset source.
#: The initial value of this bit varies with the operation mode.
*1: Access prohibited
*2: Only this area is open to external access in the area below address 0000FFH (inclusive). All addresses which are not described in the table are reserved areas, and accesses to these areas are handled in the same manner as for internal areas. The access signal for the external bus is not generated.
*3: When an external bus is enable mode, never access to resisters which are not used as general ports in areas address 000000H to 000005H or 000010H to 000015H.

(2) Block Diagram



5. 10-bit A/D Converter

The 10-bit A/D converter converts analog input voltage into a digital value. The features of this module are described below:

- Conversion time: 6.125 µs/channel (min.) (with machine clock running at 16 MHz)
- Uses RC-type sequential comparison and conversion method with built-in sample and hold circuit
- 10-bit resolution
- Analog input can be selected by software from among 16 channels
  Single-conversion mode: Selects and converts one channel.
  Scan conversion mode: Converts several consecutive channels (up to 16 can be programmed).
  One-shot mode: Converts the specified channel once and terminates.
  Continuous conversion mode: Repeatedly converts the specified channel.
  Stop conversion mode: Pauses after converting one channel and waits until the next startup (permits synchronization of start of conversion).
- When A/D conversion is completed, an "A/D conversion complete" interrupt request can be issued to the CPU. Because the generation of this interrupt can be used to start up the EI^{2}OS and transfer the A/D conversion results to memory, this function is suitable for continuous processing.
- Startup triggers can be selected from among software, an external trigger (falling edge), and a timer (rising edge).

(1) Register Configuration

- **A/D Channel Setting Register (ADCH)**

This register specfies the A/D converter conversion channel.

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
ADCH	000032$_H$	ANS3	ANS2	ANS1	ANS0	ANE3	ANE2	ANE1	ANE0	00000000$_B$
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

- **A/D Mode Register (ADMD)**

This register specfies the A/D converter operation mode and the startup source.

Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
ADMD	000033$_H$	—	—	—	Reserved	MOD1	MOD0	STS1	STS0	- - - X0000$_B$
		(—)	(—)	(—)	(W)	(R/W)	(R/W)	(R/W)	(R/W)	

Note: Program "0" to bit 12 when write. Read value is indeterminated.

- **A/D Control Status Register (ADCS)**

This register is the A/D converter control and status register.

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
ADCS	000034$_H$	BUSY	INT	INTE	PAUS	—	—	STRT	Reserved	0000 - - 00$_B$
		(R/W)	(R/W)	(R/W)	(R/W)	(—)	(—)	(W)	(R/W)	

- **A/D Data Register (ADCD)**

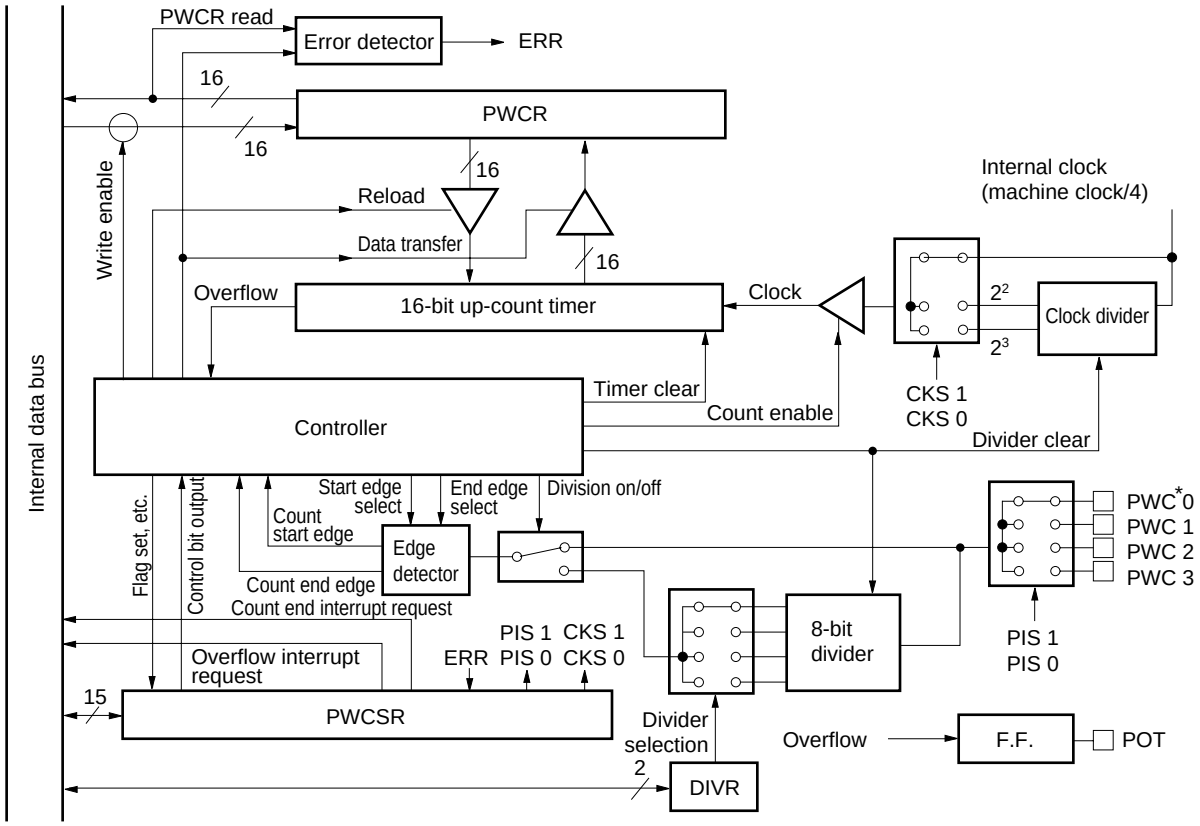
This register stores the A/D converter conversion data.

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
ADCD	000036$_H$	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX$_B$
		(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

- **PWC Division Ratio Control Register 0 to 3 (DIVR0 to DIVR3)**

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
DIVR0	00007A H	—	—	—	—	—	—	MOD1	MOD0	------ 00B
DIVR1	00007C H									
DIVR2	00007E H									
DIVR3	000080 H	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	(R/W)	

(2) Block Diagram



*: In the MB90220 series, only the module input PWC 0 of each channel is connected to the respective external pins.

Channel	POT pin
PWC ch. 0	PA 1/PWC 0/POT 0
PWC ch. 1	PA 2/PWC 1/POT 1/ASR 1
PWC ch. 2	PA 3/PWC 2/POT 2/ASR 2
PWC ch. 3	PA 4/PWC 3POT 3/ASR 3

8. 24-bit Timer Counter

The 24-bit timer counter consists of a 24-bit up-counter, an 8-bit output buffer register, and a control register. The count value output by this timer counter is used to generate the base time used for input capture and output compare.

The interrupt functions provided are timer overflow interrupts and timer intermediate bit interrupts. The intermediate bit interrupt permits four time settings.

The 24-bit timer counter value is cleared to all zeroes by a reset.

(1) Register Configuration

- **Free-run Timer Control Register (TCCR)**

Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
TCCR	000071H	—	—	Reserved	Reserved	Reserved	Reserved	Reserved	PR0	- - 111111B
		(—)	(—)	(W)	(W)	(R/W)	(R/W)	(R/W)	(R/W)	

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
TCCR	000070H	CLR2	CLR	IVF	IVFE	TIM	TIME	TIS1	TIS0	11000000B
		(W)	(W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

- **Free-run Timer Low-order Data Register (TCRL)**

Register name	Address	bit15	bit0	Initial value	Access
TCRL	000072H 000073H	TCRL		00000000B	R

- **Free-run Timer High-order Data Register (TCRH)**

Register name	Address	bit15	bit8	bit7	bit0	Initial value	Access
TCRH	000074H 000075H	—		TCRH		00000000B	R

(Continued)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Analog power supply voltage	I_A	AV_{CC}	f_C = 16 MHz*9	—	3	7	mA	
	I_{AH}		—	—	—	5*6	µA	At stop mode
Input capacitance	C_{IN}	*7	—	—	10	—	pF	

*1: Hysteresis input pins
$\overline{RST}$, $\overline{HST}$, P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P80 to P87, P90 to P97, PA0 to PA7, PB0 to PB7, PC0 to PC5

*2: Ouput pins
P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P77, P80 to P87, PA0 to PA7, PB0 to PB7, PC0 to PC5

*3: Output pins
P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA7, PB0 to PB7, PC0 to PC5

*4: A list of availabilities of pull-up/pull-down resistors

Pin name	MB90223/224	MB90P224A/W224A	MB90P224B/W224B
$\overline{RST}$	Availability of pull-up resistors is optionally defined.	Pull-up resistors available	Unavailable
MD1	Pull-up resistors available	Unavailable	Unavailable
MD0, MD2	Pull-up resistors available	Unavailable	Unavailable

*5: V_{CC} = +5.0 V, V_{SS} = 0.0 V, T_A = +25°C, F_C = 16 MHz

*6: The current value applies to the CPU stop mode with A/D converter inactive (V_{CC} = AV_{CC} = AVRH = +5.5 V).

*7: Other than V_{CC}, V_{SS}, AV_{CC} and AV_{SS}

*8: Measurement condition of power supply current; external clock pin and output pin are open.
Measurement condition of V_{CC}; see the table above mentioned.

*9: F_C = 12 MHz for MB90223

(4) Power on Supply Specifications (Power-on Reset)

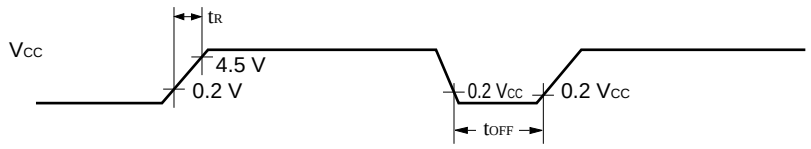
Single-chip mode MB90223/224/P224B/W224B: (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +105°C)
MB90P224A/W224A : (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)
External bus mode : (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply rising time	t_R	V_{CC}	—	—	—	30	ms	*
Power supply cut-off time	t_{OFF}	V_{CC}	—	1	—	—	ms	

* : Before power supply rising, it is required to be V_{CC} < 0.2 V.

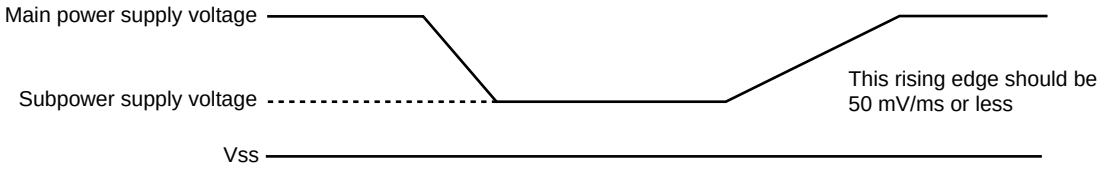
Notes:
- Power-on reset assumes the above values.
- Whether the power-on reset is required or not, turn the power on according to these characteristics and trigger the power-on reset.
- There are internal registers (STBYC, etc.) which is initialized only by the power-on reset in the device.

• Power-on Reset



Note: Note on changing power supply
Even if above characteristics are not insufficient, abrupt changes in power supply voltage may cause a power-on reset. Therefore, at the time of a momentary changes such as when power is turned on, rise the power smoothly as shown below.

• Changing Power Supply



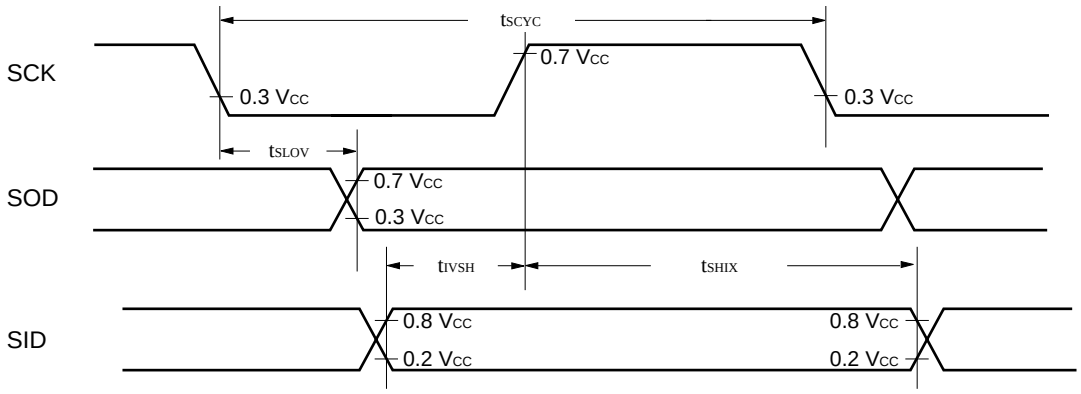
(9) UART Timing

Single-chip mode MB90223/224/P224B/W224B: (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +105°C)
MB90P224A/W224A : (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)
External bus mode : (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +70°C)

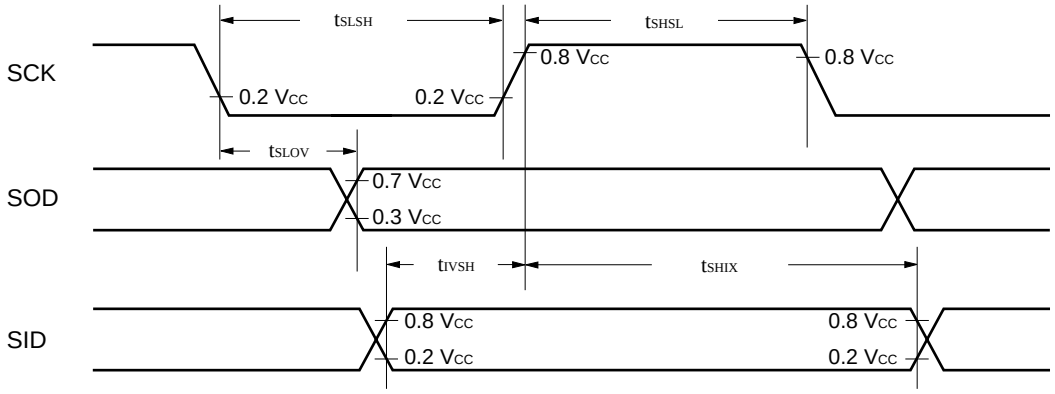
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	—	Load condition: 80 pF	8 t_{CYC}	—	ns	Internal clock operation output pin
SCLK ↓ → SOUT delay time	t_{SLOV}	—		–80	80	ns	
Valid SIN → SCLK ↑	t_{IVSH}	—		100	—	ns	
SCLK ↑ → Valid SIN hold time	t_{SHIX}	—		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	—	Load condition: 80 pF	4 t_{CYC}	—	ns	External clock operation output pin
Serial clock “L” pulse width	t_{SLSH}	—		4 t_{CYC}	—	ns	
SCLK ↓ → SOUT delay time	t_{SLOV}	—		—	150	ns	
Valid SIN → SCLK ↑	t_{IVSH}	—		60	—	ns	
SCLK ↑ → valid SIN hold time	t_{SHIX}	—		60	—	ns	

Notes: • These AC characteristics assume in CLK synchronization mode.
• “t_{CYC}” is the machine cycle (unit: ns).

- **Internal Shift Clock Mode**

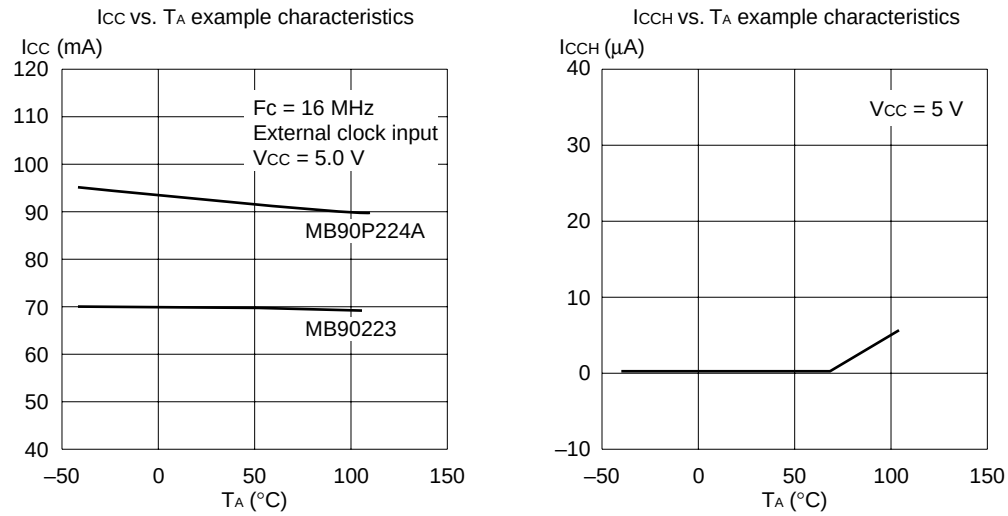


- **External Shift Clock Input Mode**



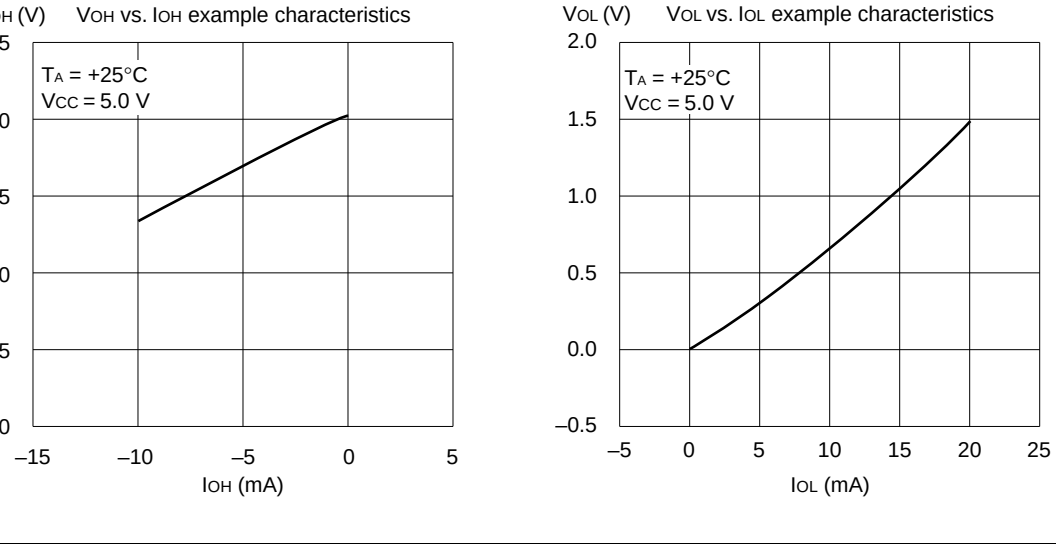
■ EXAMPLE CHARACTERISTICS

(1) Power Supply Current



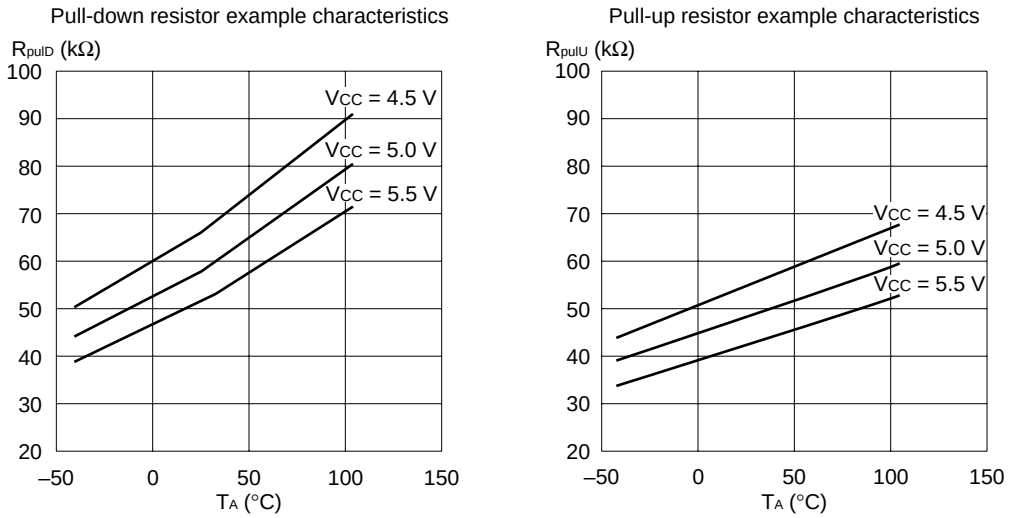
Note: These are not assured value of characteristics but example characteristics.

(2) Output Voltage



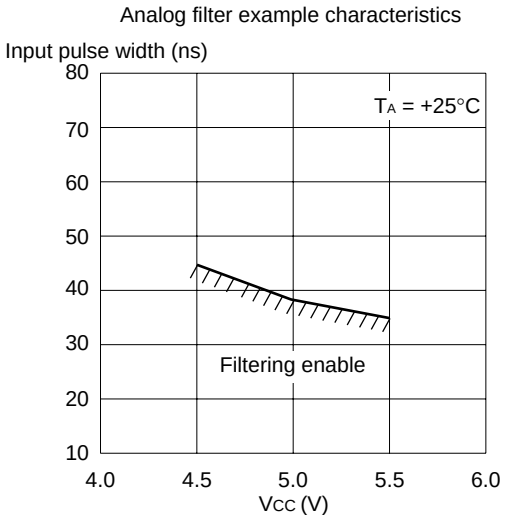
Note: These are not assured value of characteristics but example characteristics.

(3) Pull-up/Pull-down Resistor



Note: These are not assured value of characteristics but example characteristics.

(4) Analog Filter



Note: These are not assured value of characteristics but example characteristics.

Table 10 Increment and Decrement Instructions (Byte/Word/Long Word) [12 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
INC ear	2	2	0	byte (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	*
INC eam	2+	3+ (a)	2× (b)	byte (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DEC ear	2	2	0	byte (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	*
DEC eam	2+	3+ (a)	2× (b)	byte (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*
INCW ear	2	2	0	word (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	*
INCW eam	2+	3+ (a)	2× (c)	word (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DECW ear	2	2	0	word (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	*
DECW eam	2+	3+ (a)	2× (c)	word (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*
INCL ear	2	4	0	long (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	*
INCL eam	2+	5+ (a)	2× (d)	long (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DECL ear	2	4	0	long (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	*
DECL eam	2+	5+ (a)	2× (d)	long (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*

For an explanation of “(a)”, “(b)”, “(c)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 11 Compare Instructions (Byte/Word/Long Word) [11 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
CMP A	1	2	0	byte (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
CMP A, ear	2	2	0	byte (A) – (ear)	–	–	–	–	–	*	*	*	*	–
CMP A, eam	2+	2+ (a)	(b)	byte (A) – (eam)	–	–	–	–	–	*	*	*	*	–
CMP A, #imm8	2	2	0	byte (A) – imm8	–	–	–	–	–	*	*	*	*	–
CMPW A	1	2	0	word (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
CMPW A, ear	2	2	0	word (A) – (ear)	–	–	–	–	–	*	*	*	*	–
CMPW A, eam	2+	2+ (a)	(c)	word (A) – (eam)	–	–	–	–	–	*	*	*	*	–
CMPW A, #imm16	3	2	0	word (A) – imm16	–	–	–	–	–	*	*	*	*	–
CMPL A, ear	2	3	0	long (A) – (ear)	–	–	–	–	–	*	*	*	*	–
CMPL A, eam	2+	4+ (a)	(d)	long (A) – (eam)	–	–	–	–	–	*	*	*	*	–
CMPL A, #imm32	5	3	0	long (A) – imm32	–	–	–	–	–	*	*	*	*	–

For an explanation of “(a)”, “(b)”, “(c)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 15 Logical 2 Instructions (Long Word) [6 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
ANDL A, ear	2	5	0	long (A) ← (A) and (ear)	–	–	–	–	–	*	*	R	–	–
ANDL A, eam	2+	6+ (a)	(d)	long (A) ← (A) and (eam)	–	–	–	–	–	*	*	R	–	–
ORL A, ear	2	5	0	long (A) ← (A) or (ear)	–	–	–	–	–	*	*	R	–	–
ORL A, eam	2+	6+ (a)	(d)	long (A) ← (A) or (eam)	–	–	–	–	–	*	*	R	–	–
XORL A, ear	2	5	0	long (A) ← (A) xor (ear)	–	–	–	–	–	*	*	R	–	–
XORL A, eam	2+	6+ (a)	(d)	long (A) ← (A) xor (eam)	–	–	–	–	–	*	*	R	–	–

For an explanation of “(a)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 16 Sign Inversion Instructions (Byte/Word) [6 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
NEG A	1	2	0	byte (A) ← 0 – (A)	X	–	–	–	–	*	*	*	*	–
NEG ear	2	2	0	byte (ear) ← 0 – (ear)	–	–	–	–	–	*	*	*	*	*
NEG eam	2+	3+ (a)	2× (b)	byte (eam) ← 0 – (eam)	–	–	–	–	–	*	*	*	*	*
NEGW A	1	2	0	word (A) ← 0 – (A)	–	–	–	–	–	*	*	*	*	–
NEGW ear	2	2	0	word (ear) ← 0 – (ear)	–	–	–	–	–	*	*	*	*	*
NEGW eam	2+	3+ (a)	2× (c)	word (eam) ← 0 – (eam)	–	–	–	–	–	*	*	*	*	*

For an explanation of “(a)”, “(b)” and “(c)” and refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 17 Absolute Value Instructions (Byte/Word/Long Word) [3 Insturctions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
ABS A	2	2	0	byte (A) ← absolute value (A)	Z	–	–	–	–	*	*	*	–	–
ABSW A	2	2	0	word (A) ← absolute value (A)	–	–	–	–	–	*	*	*	–	–
ABSL A	2	4	0	long (A) ← absolute value (A)	–	–	–	–	–	*	*	*	–	–

Table 18 Normalize Instructions (Long Word) [1 Instruction]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
NRML A, R0	2	*	0	long (A) ← Shifts to the position at which “1” was set first byte (R0) ← current shift count	–	–	–	–	*	–	–	–	–	–

* : 5 when the contents of the accumulator are all zeroes, 5 + (R0) in all other cases.

Table 22 Other Control Instructions (Byte/Word/Long Word) [36 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
PUSHW A	1	3	(c)	word (SP) ← (SP) –2, ((SP)) ← (A)	–	–	–	–	–	–	–	–	–	–
PUSHW AH	1	3	(c)	word (SP) ← (SP) –2, ((SP)) ← (AH)	–	–	–	–	–	–	–	–	–	–
PUSHW PS	1	3	(c)	word (SP) ← (SP) –2, ((SP)) ← (PS)	–	–	–	–	–	–	–	–	–	–
PUSHW rlst	2	*3	*4	(SP) ← (SP) –2n, ((SP)) ← (rlst)	–	–	–	–	–	–	–	–	–	–
POPW A	1	3	(c)	word (A) ← ((SP)), (SP) ← (SP) +2	–	*	–	–	–	–	–	–	–	–
POPW AH	1	3	(c)	word (AH) ← ((SP)), (SP) ← (SP) +2	–	–	–	–	–	–	–	–	–	–
POPW PS	1	3	(c)	word (PS) ← ((SP)), (SP) ← (SP) +2	–	–	*	*	*	*	*	*	*	–
POPW rlst	2	*2	*4	(rlst) ← ((SP)) , (SP) ← (SP)	–	–	–	–	–	–	–	–	–	–
JCTX @A	1	9	6× (c)	Context switch instruction	–	–	*	*	*	*	*	*	*	–
AND CCR, #imm8	2	3	0	byte (CCR) ← (CCR) and imm8	–	–	*	*	*	*	*	*	*	–
OR CCR, #imm8	2	3	0	byte (CCR) ← (CCR) or imm8	–	–	*	*	*	*	*	*	*	–
MOV RP, #imm8	2	2	0	byte (RP) ←imm8	–	–	–	–	–	–	–	–	–	–
MOV ILM, #imm8	2	2	0	byte (ILM) ←imm8	–	–	–	–	–	–	–	–	–	–
MOVEA RWi, ear	2	3	0	word (RWi) ←ear	–	–	–	–	–	–	–	–	–	–
MOVEA RWi, eam	2+	2+ (a)	0	word (RWi) ←eam	–	–	–	–	–	–	–	–	–	–
MOVEA A, ear	2	2	0	word(A) ←ear	–	*	–	–	–	–	–	–	–	–
MOVEA A, eam	2+	1+ (a)	0	word (A) ←eam	–	*	–	–	–	–	–	–	–	–
ADDSP #imm8	2	3	0	word (SP) ← ext (imm8)	–	–	–	–	–	–	–	–	–	–
ADDSP #imm16	3	3	0	word (SP) ← imm16	–	–	–	–	–	–	–	–	–	–
MOV A, brgl	2	*1	0	byte (A) ← (brgl)	Z	*	–	–	–	*	*	–	–	–
MOV brg2, A	2	1	0	byte (brg2) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV brg2, #imm8	3	2	0	byte (brg2) ← imm8	–	–	–	–	–	*	*	–	–	–
NOP	1	1	0	No operation	–	–	–	–	–	–	–	–		–
ADB	1	1	0	Prefix code for AD space access	–	–	–	–	–	–	–	–	–	–
DTB	1	1	0	Prefix code for DT space access	–	–	–	–	–	–	–	–	–	–
PCB	1	1	0	Prefix code for PC space access	–	–	–	–	–	–	–	–	–	–
SPB	1	1	0	Prefix code for SP space access	–	–	–	–	–	–	–	–	–	–
NCC	1	1	0	Prefix code for no flag change	–	–	–	–	–	–	–	–	–	–
CMR	1	1	0	Prefix code for the common register bank	–	–	–	–	–	–	–	–	–	–
MOVW SPCU, #imm16	4	2	0	word (SPCU) ← (imm16)	–	–	–	–	–	–	–	–	–	–
MOVW SPCL, #imm16	4	2	0	word (SPCL) ← (imm16)	–	–	–	–	–	–	–	–	–	–
SETSPC	2	2	0	Stack check ooperation enable	–	–	–	–	–	–	–	–	–	–
CLRSPC	2	2	0	Stack check ooperation disable	–	–	–	–	–	–	–	–	–	–
BTSCN A	2	*5	0	byte (A)← position of "1" bit in word (A)	Z	–	–	–	–	–	*	–	–	–
BTSCNS A	2	*6	0	byte (A)← position of "1" bit in word (A) ×2	Z	–	–	–	–	–	*	–	–	–
BTSCND A	2	*7	0	byte (A)← position of "1" bit in word (A) ×4	Z	–	–	–	–	–	*	–	–	–

For an explanation of "(a)" and "(c)", refer to Tables 4 and 5.

*1: PCB, ADB, SSB, USB, and SPB: 1 cycle
DTB: 2 cycles
DPR: 3 cycles
*2: 3 + 4 × (pop count)
*3: 3 + 4 × (push count)
*4: Pop count × (c), or push count × (c)
*5: 3 when AL is 0, 5 when AL is not 0.
*6: 4 when AL is 0, 6 when AL is not 0.
*7: 5 when AL is 0, 7 when AL is not 0.