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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16F
Core Size	16-Bit
Speed	16MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	102
Program Memory Size	64KB (64K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-BQFP
Supplier Device Package	120-QFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90223pf-gt-374

Pin no. QFP*	Pin name	Circuit type	Function
84	P56	C	General-purpose I/O port This function is valid in single-chip mode. This function is valid in modes where the external bus is valid.
	$\overline{RD}$		Read strobe output pin for the data bus This function is valid in modes where the external bus is enabled.
85	P57	B	General-purpose I/O port This function is always valid. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode.
	$\overline{WI}$		RAM write disable request input During this operation, the input may be used suddenly at any time; therefore, it is necessary to stop output by other fuctions on this pin, except when using it for output deliberately.
46 to 53	P60 to P67	F	Open-drain I/O ports This function is valid when the analog input enable register specification is “port”.
	AN00 to AN07		10-bit A/D converter analog input pins This function is valid when the analog input enable register specification is “analog input”.
17 to 24	P70 to P77	C	General-purpose I/O ports This function is valid when the output specification for DOT0 to DOT7 is “disabled”.
	DOT0 to DOT7		This function is valid when OCU (output compare unit) output is enabled.
25 to 30	P80 to P85	C	General-purpose I/O ports This function is valid when the output specification for TOT0 to TOT5 is “disabled”.
	TOT0 to TOT5		16-bit reload timer output pins (TOT0 to TOT5)
31, 32	P86, P87	C	General-purpose I/O ports This function is valid when the PPG0, and PPG1 output specification is “disabled”.
	PPG0, PPG1		16-bit PPG timer output pins This function is valid when the PPG control/status register specification is “PPG output pins”.
34 to 41	P90 to P97	F	Open-drain I/O ports This function is valid when the analog input enable register specification is “port”.
	AN08 to AN15		10-bit A/D converter analog input pins This function is valid when the analog input enable register specification is “analog input”.

* : FPT-120P-M03, FPT-120C-C02

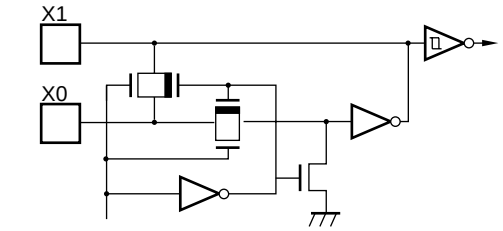
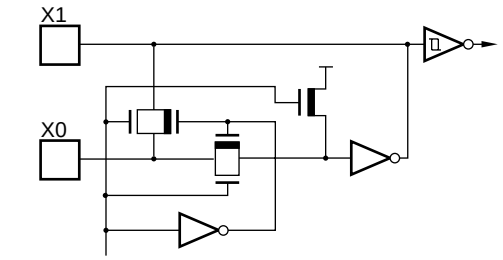
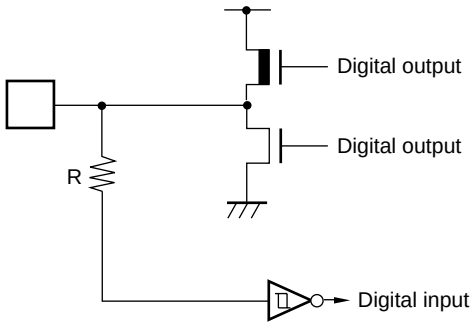
(Continued)

Pin no. QFP*	Pin name	Circuit type	Function
62	INT2	B	DTP/External interrupt request input pin When DTP/external interrupts are enabled, these inputs may be used suddenly at any time; therefore, it is necessary to stop output by other functions on these pins, except when using them for output deliberately. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode.
	$\overline{ATG}$		10-bit A/D converter external trigger input pin When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode.
64	PB0	C	General-purpose I/O port This function is valid when the UART0 (ch.0) serial data output specification is “disabled”.
	SOD0		UART0 (ch.0) serial data output This function is valid when the UART0 (ch.0) serial data output specification is “enabled”.
65	PB1	C	General-purpose I/O port This function is always valid.
	SID0		UART0 (ch.0) serial data input pin During UART0 (ch.0) input operations, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately.
66	PB2	C	General-purpose output port This function is valid when the UART0 (ch.0) clock output specification is “disabled”.
	SCK0		UART0 (ch.0) clock output pin The clock output function is valid when the UART0 (ch.0) clock output specification is “enabled”. UART0 (ch.0) external clock input pin. This function is valid when the port is in input mode and the UART0 (ch.0) specification is external clock mode.
67	PB3	C	General-purpose I/O port This function is valid when the UART0 (ch.1) serial data output specification is “disabled”.
	SOD1		UART0 (ch.1) serial data output pin This function is valid when the UART0 (ch.1) serial data output specification is “enabled”.
68	PB4	C	General-purpose I/O port This function is always valid.
	SID1		UART0 (ch.1) serial data input pin During UART0 (ch.1) input operations, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately.

* : FPT-120P-M03, FPT-120C-C02

(Continued)

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Oscillation feedback resistor: Approx. 1 MΩ MB90223 MB90224 MB90P224B MB90W224B
		• Oscillation feedback resistor: Approx. 1 MΩ MB90P224A MB90W224A
B		• CMOS-level output • CMOS-level hysteresis input with no standby control

Note: The pull-up and pull-down resistors are always connected, regardless of the state.

(Continued)

■ PROGRAMMING FOR MB90P224A/P224B/W224A/W224B

In EPROM mode, the MB90P224A/P224B/W224A/W224B functions equivalent to the MBM27C1000. This allows the EPROM to be programmed with a general-purpose EPROM programmer by using the dedicated socket adapter (do not use the electronic signature mode).

1. Program Mode

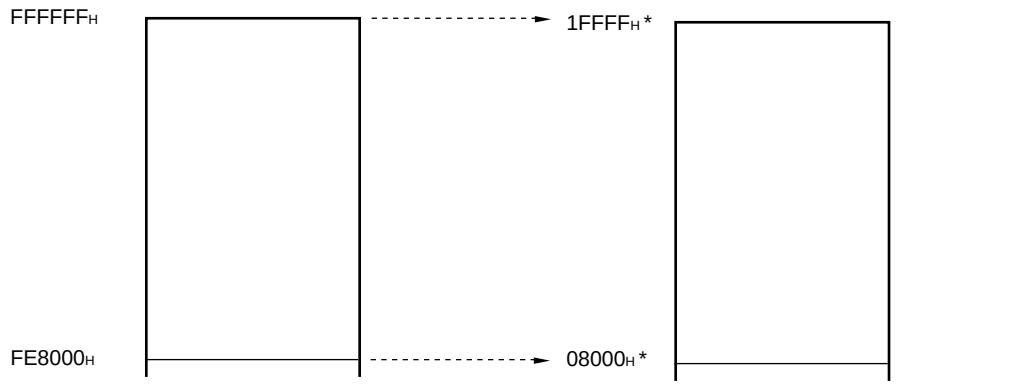
When shipped from Fujitsu, and after each erasure, all bits (96 K × 8 bits) in the MB90P224A/P224B/W224A/W224B are in the "1" state. Data is written to the ROM by selectively programming "0's" into the desired bit locations. Bits cannot be set to "1" electrically.

2. Programming Procedure

(1) Set the EPROM programmer to MBM27C1000.

(2) Load program data into the EPROM programmer at 08000_H to $1FFFF_H$.

Note that ROM addresses $FE8000_H$ to $FFFFFF_H$ in the operation mode in the MB90P224A/P224B/W224A/W224B series assign to 08000_H to $1FFFF_H$ in the EPROM mode (on the EPROM programmer).



* : Be sure to set the programming, the start address and the stop address on the EPROM programmer to 08000_H/$1FFFF_H$.

(3) Mount the MB90P224A/P224B/W224A/W224B on the adapter socket, then fit the adapter socket onto the EPROM programmer. When mounting the device and the adapter socket, pay attention to their mounting orientations.

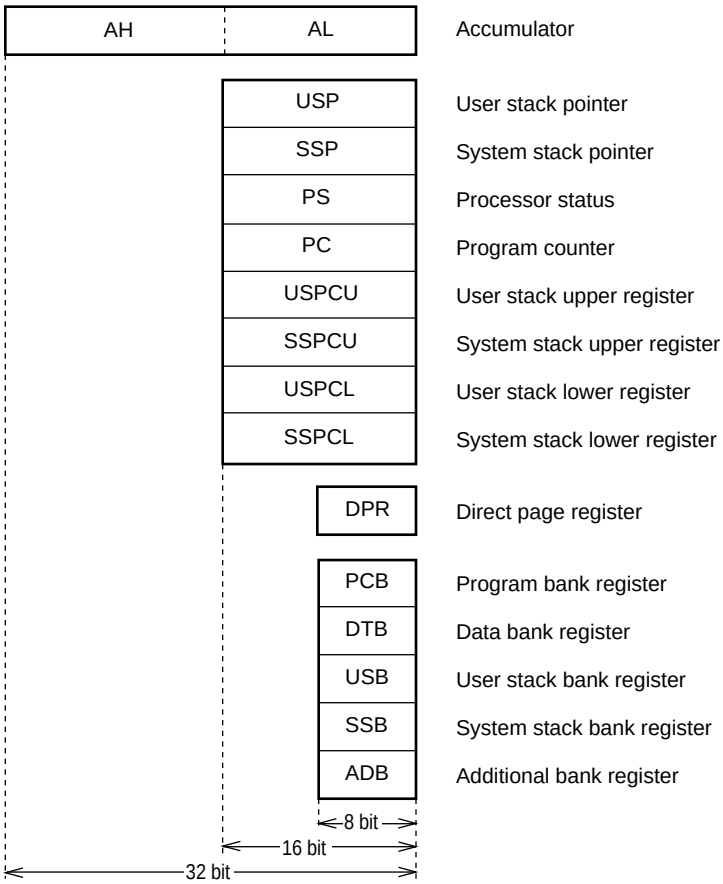
(4) Start programming the program data to the device.

(5) If programming has not successfully resulted, connect a capacitor of approx. 0.1 μF between V_{CC} and GND, between V_{PP} and GND.

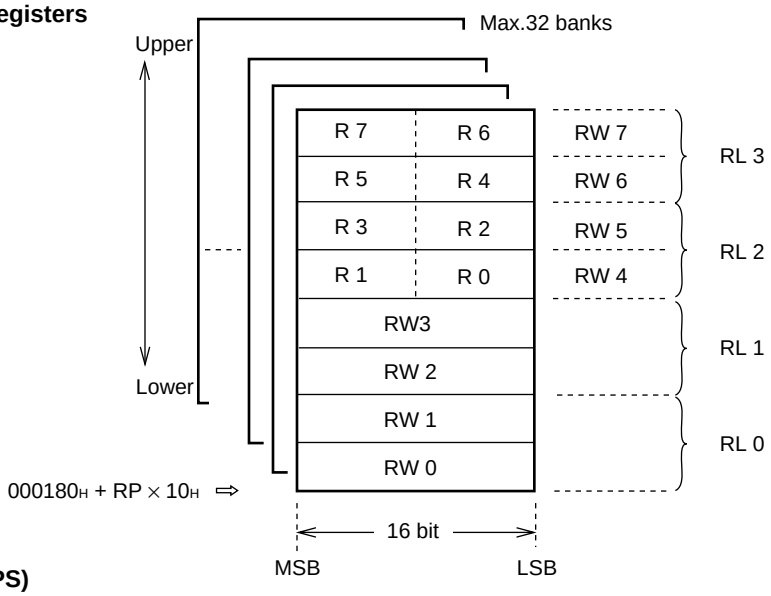
Note: The mask ROM products (MB90223, MB90224) does not support EPROM mode. Data cannot, therefore, be read by the EPROM programmer.

■ PROGRAMMING MODEL

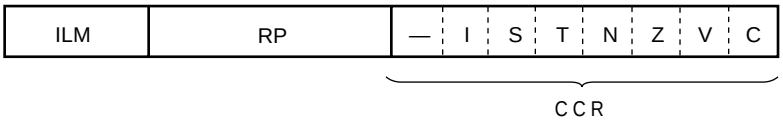
Dedicated Registers



General-purpose Registers



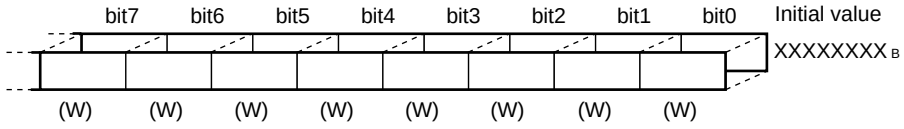
Processor Status (PS)



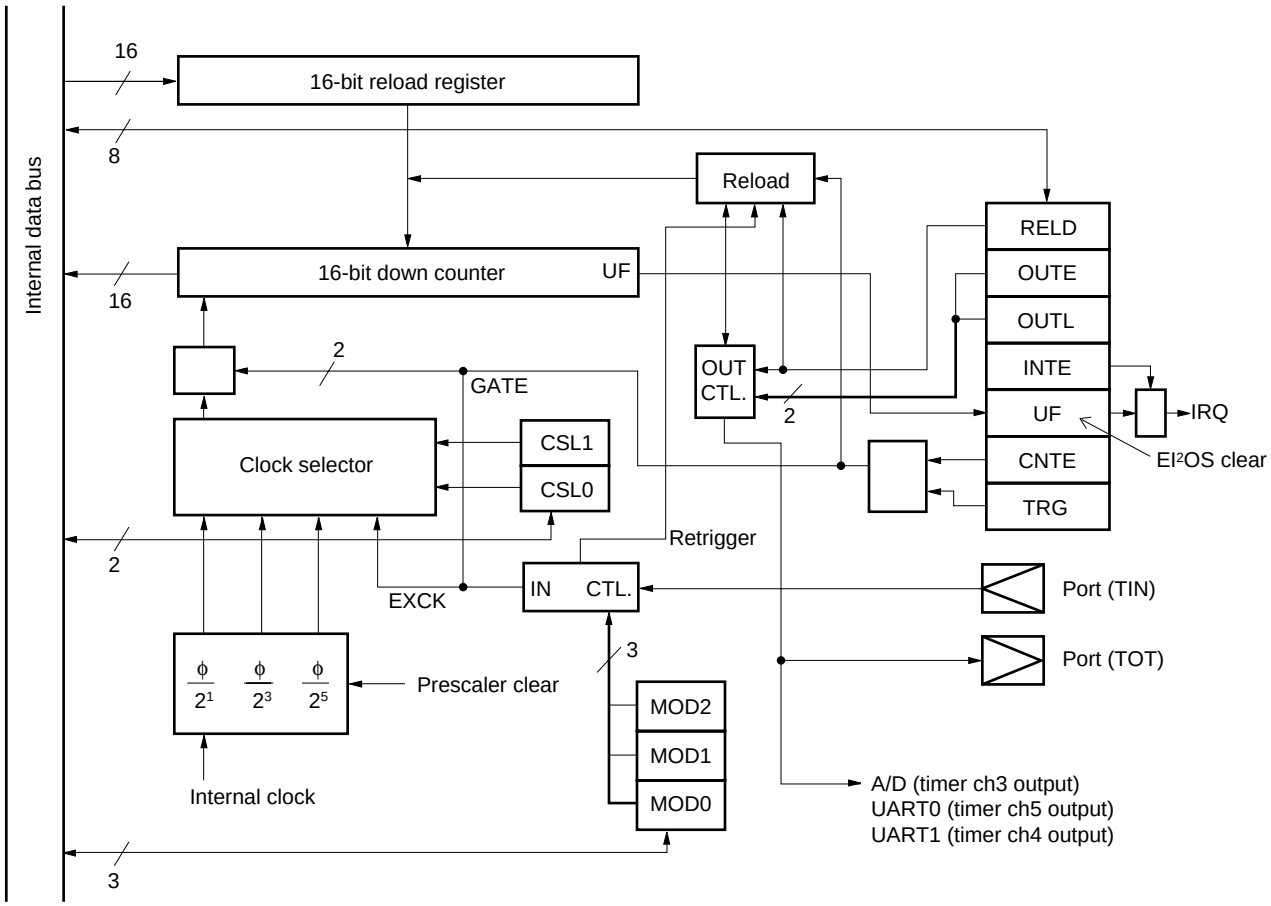
Address	Register	Register name	Access	Resouce name	Initial value
001F02H	PWC data buffer register 1	PWCR1	R/W	PWC timer 1	0 0 0 0 0 0 0 0
001F03H					0 0 0 0 0 0 0 0
001F04H	PWC data buffer register 2	PWCR2	R/W	PWC timer 2	0 0 0 0 0 0 0 0
001F05H					0 0 0 0 0 0 0 0
001F06H	PWC data buffer register 3	PWCR3	R/W	PWC timer 3	0 0 0 0 0 0 0 0
001F07H					0 0 0 0 0 0 0 0
001F08H to 1F0FH	(Reserved area)*1				
001F10H	OCU compare lower-order data register 00	CPR00L	R/W	Output compare 00	0 0 0 0 0 0 0 0
001F11H					0 0 0 0 0 0 0 0
001F12H	OCU compare higher-order data register 00	CPR00			0 0 0 0 0 0 0 0
001F13H					0 0 0 0 0 0 0 0
001F14H	OCU compare lower-order data register 01	CPR01L	R/W	Output compare 01	0 0 0 0 0 0 0 0
001F15H					0 0 0 0 0 0 0 0
001F16H	OCU compare higher-order data register 01	CPR01			0 0 0 0 0 0 0 0
001F17H					0 0 0 0 0 0 0 0
001F18H	OCU compare lower-order data register 02	CPR02L	R/W	Output compare 02	0 0 0 0 0 0 0 0
001F19H					0 0 0 0 0 0 0 0
001F1AH	OCU compare higher-order data register 02	CPR02			0 0 0 0 0 0 0 0
001F1BH					0 0 0 0 0 0 0 0
001F1CH	OCU compare lower-order data register 03	CPR03L	R/W	Output compare 03	0 0 0 0 0 0 0 0
001F1DH					0 0 0 0 0 0 0 0
001F1EH	OCU compare higher-order data register 03	CPR03			0 0 0 0 0 0 0 0
001F1FH					0 0 0 0 0 0 0 0
001F20H	OCU compare lower-order data register 04	CPR04L	R/W	Output compare 10	0 0 0 0 0 0 0 0
001F21H					0 0 0 0 0 0 0 0
001F22H	OCU compare higher-order data register 04	CPR04			0 0 0 0 0 0 0 0
001F23H					0 0 0 0 0 0 0 0
001F24H	OCU compare lower-order data register 05	CPR05L	R/W	Output compare 11	0 0 0 0 0 0 0 0
001F25H					0 0 0 0 0 0 0 0
001F26H	OCU compare higher-order data register 05	CPR05			0 0 0 0 0 0 0 0
001F27H					0 0 0 0 0 0 0 0

(Continued)

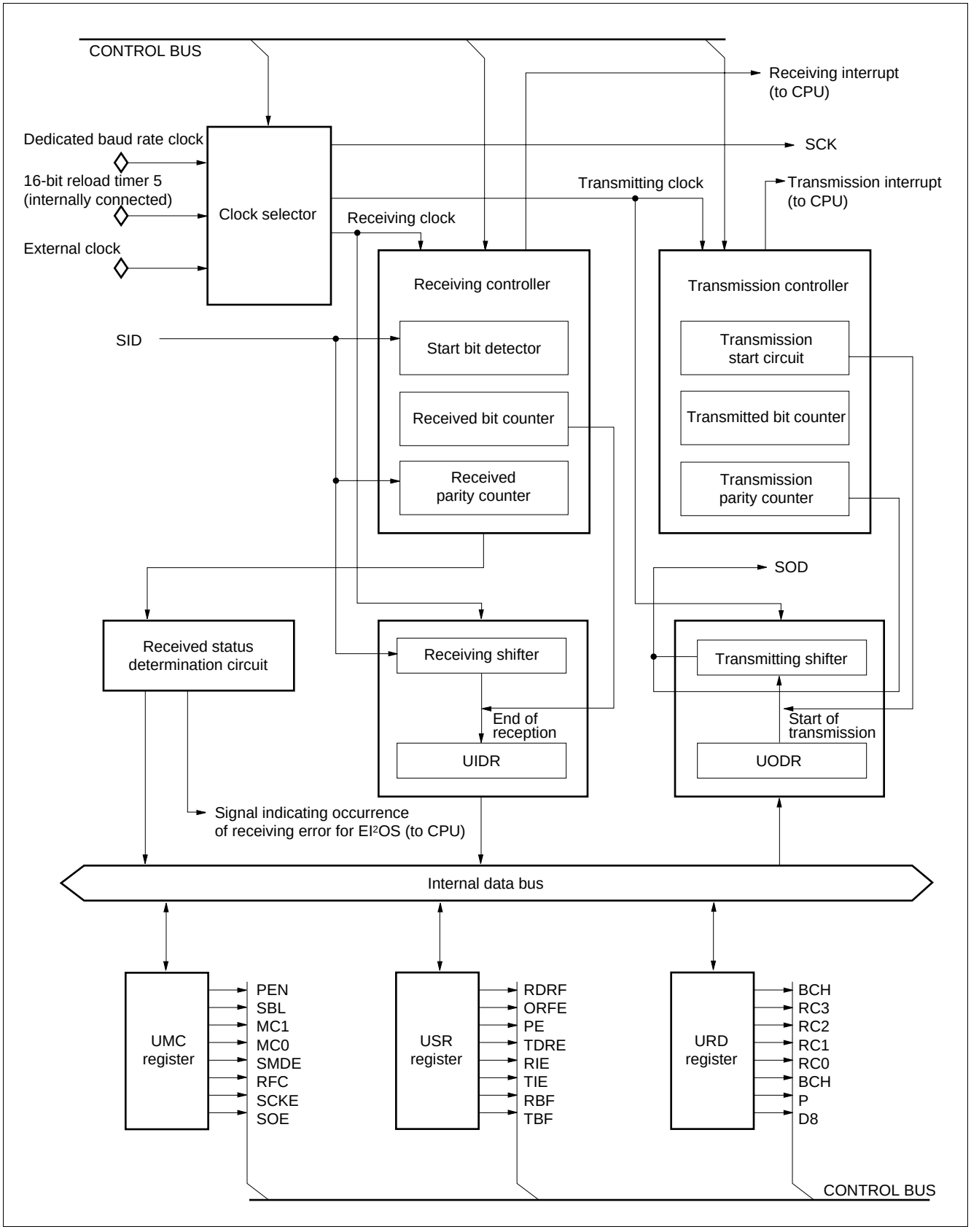
Register name	Address
TMRLR0	001F32 H
TMRLR1	001F36 H
TMRLR2	001F3A H
TMRLR3	001F3E H
TMRLR4	001F42 H
TMRLR5	001F46 H



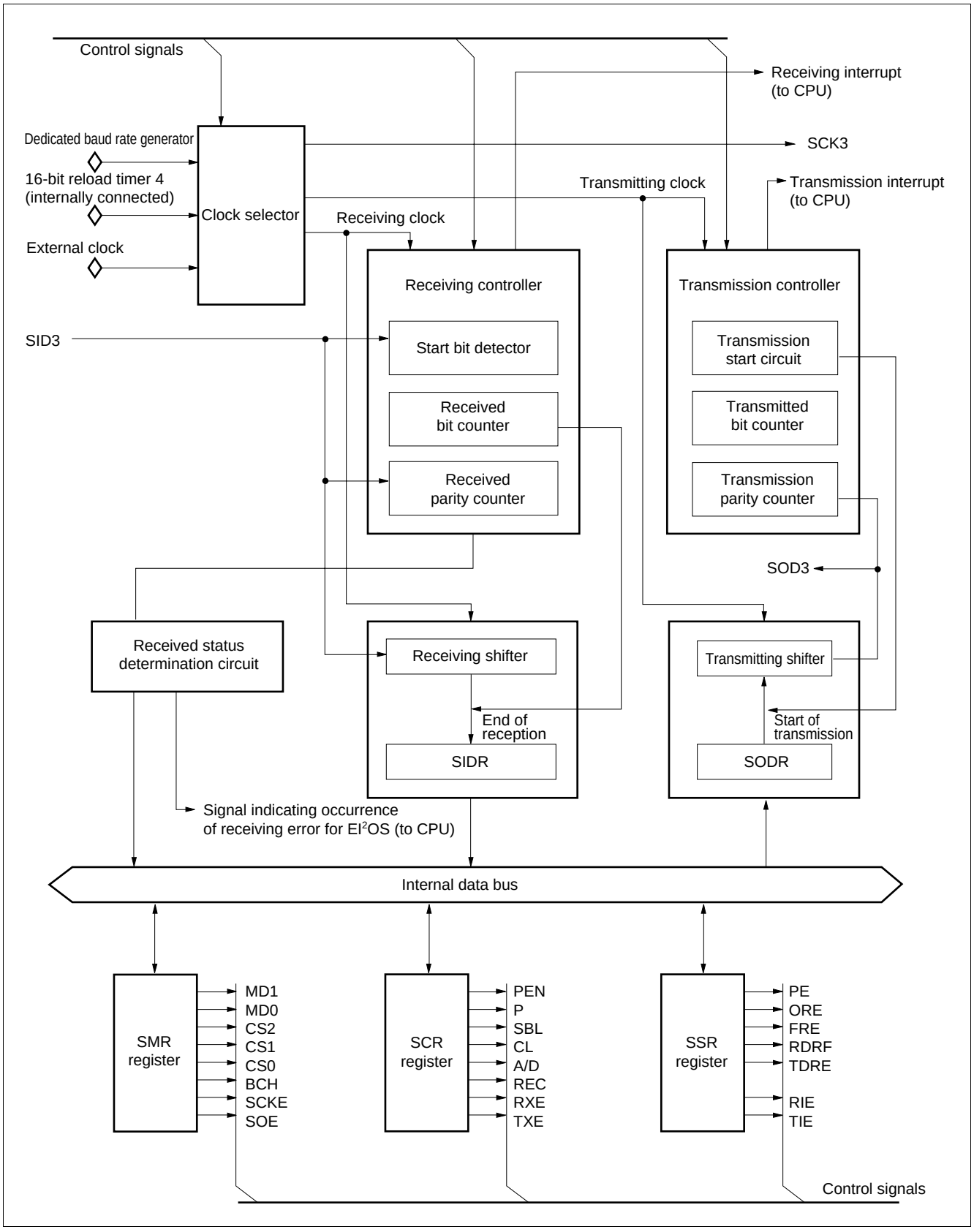
(2) Block Diagram



(2) Block Diagram



(2) Block Diagram



5. 10-bit A/D Converter

The 10-bit A/D converter converts analog input voltage into a digital value. The features of this module are described below:

- Conversion time: 6.125 µs/channel (min.) (with machine clock running at 16 MHz)
- Uses RC-type sequential comparison and conversion method with built-in sample and hold circuit
- 10-bit resolution
- Analog input can be selected by software from among 16 channels
  Single-conversion mode: Selects and converts one channel.
  Scan conversion mode: Converts several consecutive channels (up to 16 can be programmed).
  One-shot mode: Converts the specified channel once and terminates.
  Continuous conversion mode: Repeatedly converts the specified channel.
  Stop conversion mode: Pauses after converting one channel and waits until the next startup (permits synchronization of start of conversion).
- When A/D conversion is completed, an "A/D conversion complete" interrupt request can be issued to the CPU. Because the generation of this interrupt can be used to start up the EI^{2}OS and transfer the A/D conversion results to memory, this function is suitable for continuous processing.
- Startup triggers can be selected from among software, an external trigger (falling edge), and a timer (rising edge).

(1) Register Configuration

- **A/D Channel Setting Register (ADCH)**

This register specfies the A/D converter conversion channel.

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
ADCH	000032$_H$	ANS3	ANS2	ANS1	ANS0	ANE3	ANE2	ANE1	ANE0	00000000$_B$
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

- **A/D Mode Register (ADMD)**

This register specfies the A/D converter operation mode and the startup source.

Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
ADMD	000033$_H$	—	—	—	Reserved	MOD1	MOD0	STS1	STS0	- - - X0000$_B$
		(—)	(—)	(—)	(W)	(R/W)	(R/W)	(R/W)	(R/W)	

Note: Program "0" to bit 12 when write. Read value is indeterminated.

- **A/D Control Status Register (ADCS)**

This register is the A/D converter control and status register.

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
ADCS	000034$_H$	BUSY	INT	INTE	PAUS	—	—	STRT	Reserved	0000 - - 00$_B$
		(R/W)	(R/W)	(R/W)	(R/W)	(—)	(—)	(W)	(R/W)	

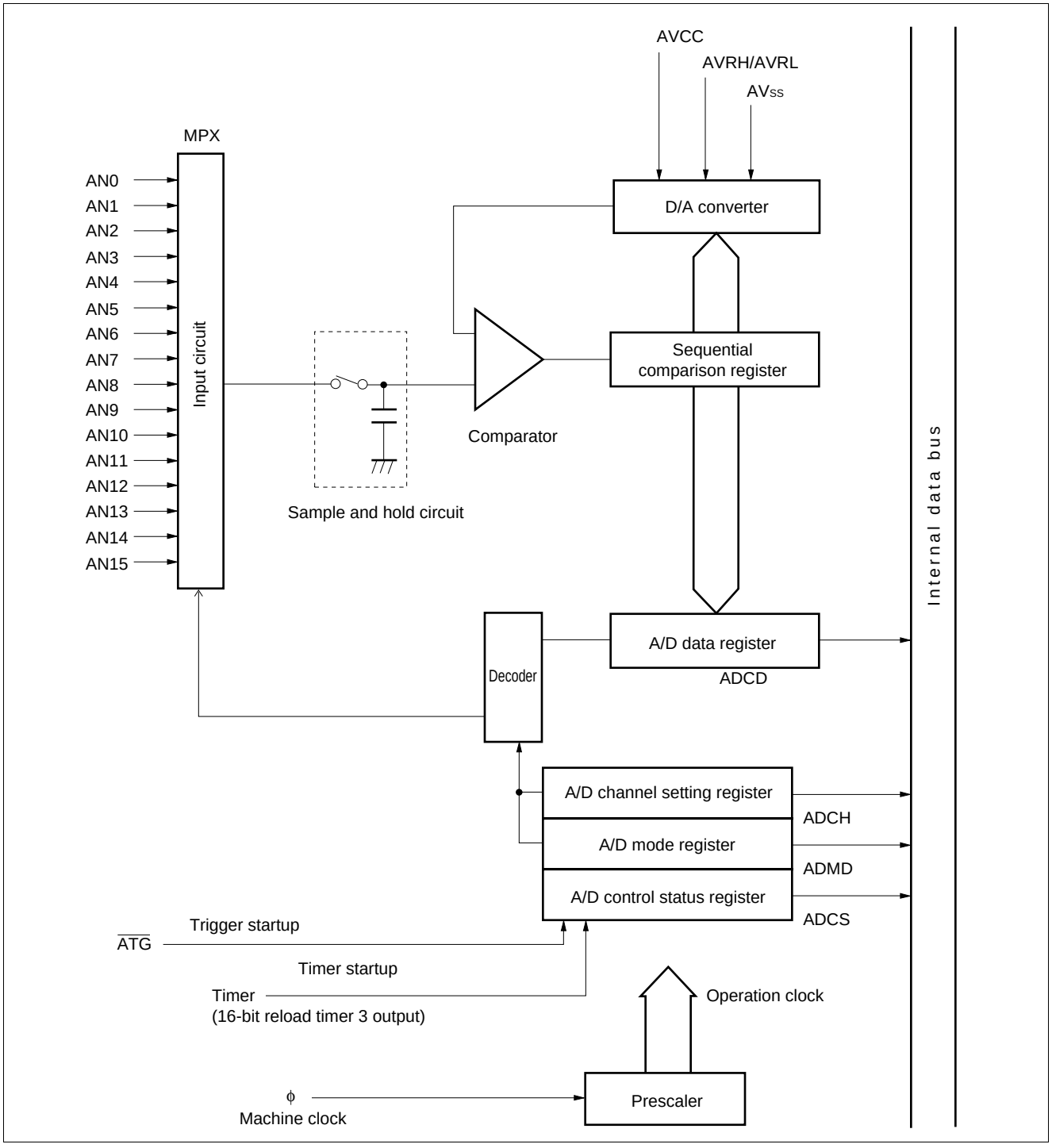
- **A/D Data Register (ADCD)**

This register stores the A/D converter conversion data.

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
ADCD	000036$_H$	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX$_B$
		(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
ADCD	000037H	—	—	—	—	—	—	D9	D8	000000XXB
		(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

(2) Block Diagram



6. PWC (Pulse Width Count) Timer

The PWC (pulse width count) timer is a 16-bit multifunction up-count timer with an input-signal pulse-width count function and a reload timer function. The hardware configuration of this module is a 16-bit up-count timer, an input pulse divider with divide ratio control register, four count input pins, and a 16-bit control register. Using these components, the PWC timer provides the following features:

- Timer functions: An interrupt request can be generated at set time intervals.
  Pulse signals synchronized with the timer cycle can be output.
  The reference internal clock can be selected from among three internal clocks.
- Pulse-width count functions: The time between arbitrary pulse input events can be counted.
  The reference internal clock can be selected from among three internal clocks.
  Various count modes:
  "H" pulse width (↑ to ↓)/"L" pulse width (↓ to ↑)
  Rising-edge cycle (↑ to ↑/Falling-edge cycle (↓ to ↓)
  Count between edges (↑ or ↓ to ↓ or ↑)
  Cycle count can be performed by 2^{2n} division (n = 1, 2, 3, 4) of the input pulse, with an 8 bit input divider.
  An interrupt request can be generated once counting has been performed.
  The number of times counting is to be performed (once or subsequently) can be selected.

The MB90220 series has four channels for this module.

(1) Register Configuration

- **PWC Control Status Register 0 to 3 (PWCSR0 to PWCSR3)**

Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
PWCSR0	000051H	STRT	STOP	EDIR	EDIE	OVIR	OVIE	ERR	POUT	00000000B
PWCSR1	000053H									
PWCSR2	000055H									
PWCSR3	000057H	(R/W)	(R/W)	(R)	(R/W)	(R/W)	(R/W)	(R)	(R/W)	

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
PWCSR0	000050H	CKS1	CKS0	PIS1	PIS0	S/C	MOD1	MOD1	MOD0	00000000B
PWCSR1	000052H									
PWCSR2	000054H									
PWCSR3	000056H	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

- **PWC Data Buffer Register 0 to 3 (PWCR0 to PWCR3)**

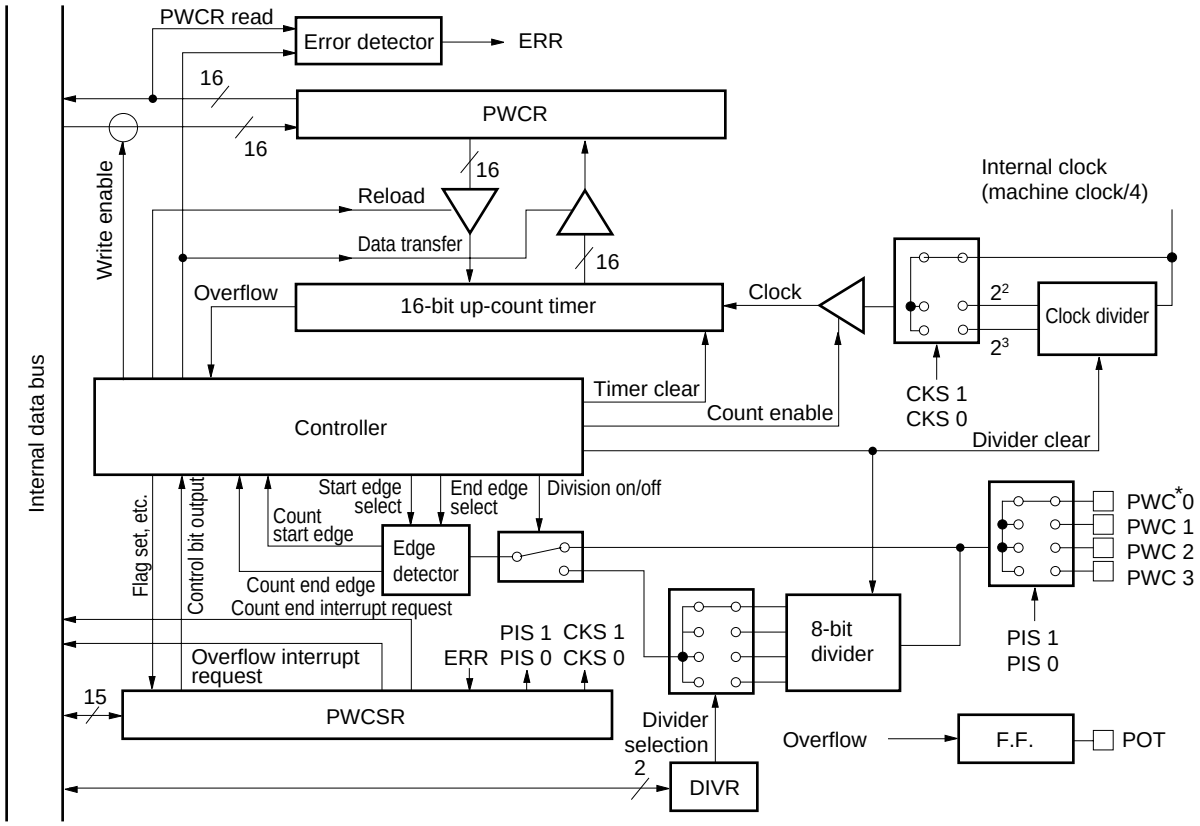
Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
PWCR0	001F01H									00000000B
PWCR1	001F03H									
PWCR2	001F05H									
PWCR3	001F07H	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
PWCR0	001F00H									00000000B
PWCR1	001F02H									
PWCR2	001F04H									
PWCR3	001F06H	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

- **PWC Division Ratio Control Register 0 to 3 (DIVR0 to DIVR3)**

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
DIVR0	00007A H	—	—	—	—	—	—	MOD1	MOD0	------ 00B
DIVR1	00007C H									
DIVR2	00007E H									
DIVR3	000080 H	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	(R/W)	

(2) Block Diagram



*: In the MB90220 series, only the module input PWC 0 of each channel is connected to the respective external pins.

Channel	POT pin
PWC ch. 0	PA 1/PWC 0/POT 0
PWC ch. 1	PA 2/PWC 1/POT 1/ASR 1
PWC ch. 2	PA 3/PWC 2/POT 2/ASR 2
PWC ch. 3	PA 4/PWC 3POT 3/ASR 3

7. DTP/External Interrupts

DTP (Data Transfer Peripheral) is located between external peripherals and the F²MC-16F CPU. It receives a DMA request or an interrupt request generated by the external peripherals and reports it to the F²MC-16F CPU to activate the extended intelligent I/O service or interrupt handler. The user can select two request levels of “H” and “L” for extended intelligent I/O service or, and four request levels of “H,” “L,” rising edge and falling edge for external interrupt requests. In MB90220, only parts corresponding to INT2 to INT0 are usable as external interrupt/DTP request.

Parts corresponding to INT7 to INT3 cannot be used as external interrupt/DTP request, but only for edge detection at external terminals.

Note: INT7 to INT3 are not usable as DTP/external interrupts.

(1) Register Configuration

- **DTP/Interrupt Enable Register (ENIR)**

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
ENIR	00003A$_H$	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	00000000$_B$
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

- **DTP/Interrupt Source Register (EIRR)**

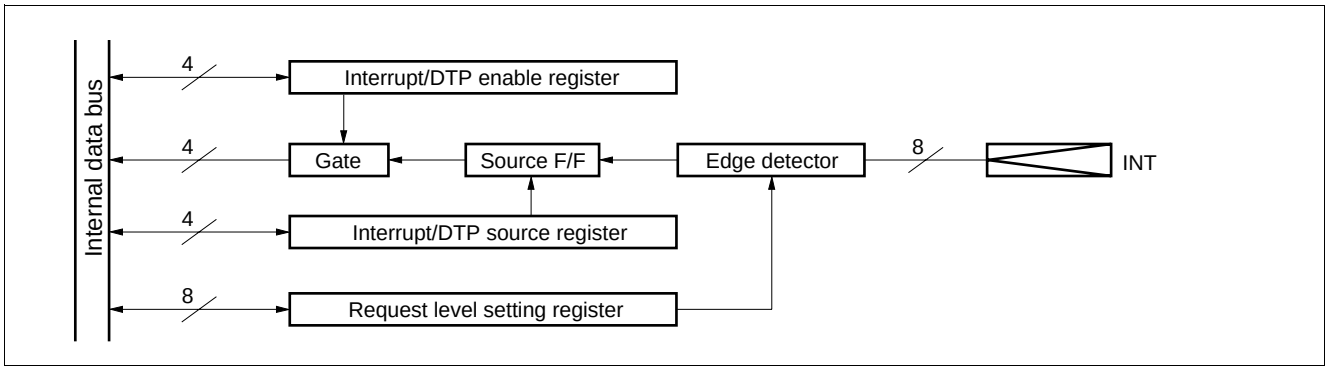
Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
EIRR	00003B$_H$	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	00000000$_B$
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

- **Request Level Setting Register (ELVR)**

Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
ELVR	00003D$_H$	LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4	00000000$_B$
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
ELVR	00003C$_H$	LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0	00000000$_B$
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

(2) Block Diagram



13. Delay Interruupt Generation Module

The delayed interrupt generation module is used to generate an interrupt task switching. Using this module allows an interrupt request to the F²MC-16F CPU to generated or cancel by software.

(1) Register Configuration

- **Delay Interrupt Source Generation/Cancel Register (DIRR)**

Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
DIRR	00009F H	—	—	—	—	—	—	—	R0	Initial value 0
		(—)	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	

(2) Block Diagram

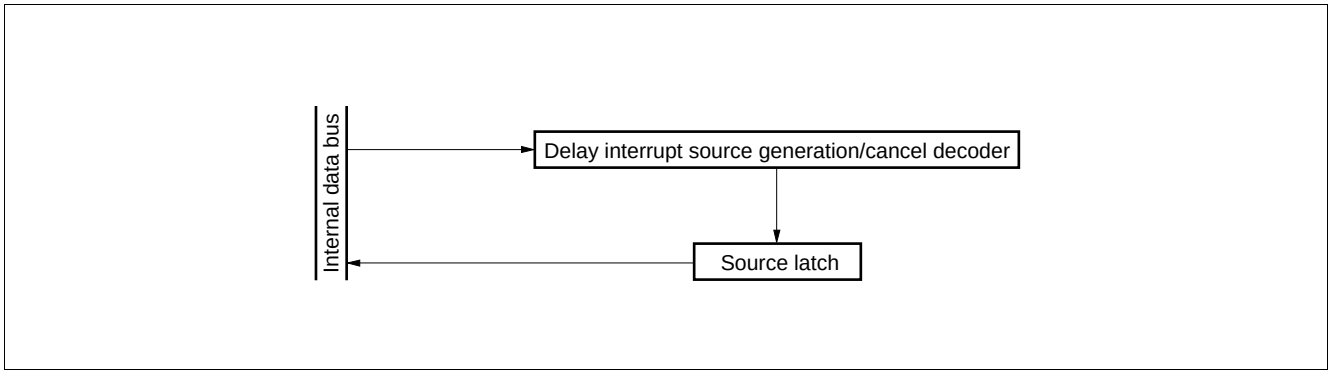


Table 2 Explanation of Symbols in Table of Instructions

Symbol	Explanation
A	32-bit accumulator The number of bits used varies according to the instruction. Byte: Low order 8 bits of AL Word: 16 bits of AL Long: 32 bits of AL, AH
AH	High-order 16 bits of A
AL	Low-order 16 bits of A
SP	Stack pointer (USP or SSP)
PC	Program counter
SPCU	Stack pointer upper limit register
SPCL	Stack pointer lower limit register
PCB	Program bank register
DTB	Data bank register
ADB	Additional data bank register
SSB	System stack bank register
USB	User stack bank register
SPB	Current stack bank register (SSB or USB)
DPR	Direct page register
brg1	DTB, ADB, SSB, USB, DPR, PCB, SPB
brg2	DTB, ADB, SSB, USB, DPR, SPB
Ri	R0, R1, R2, R3, R4, R5, R6, R7
RWi	RW0, RW1, RW2, RW3, RW4, RW5, RW6, RW7
RWj	RW0, RW1, RW2, RW3
RLi	RL0, RL1, RL2, RL3
dir addr16 addr24 addr24 0 to 15 addr24 16 to 23	Compact direct addressing Direct addressing Physical direct addressing Bits 0 to 15 of addr24 Bits 16 to 23 of addr24
io	I/O area (000000_H to $0000FF_H$)

(Continued)

Table 4 Number of Execution Cycles for Each Form of Addressing

Code	Operand	(a)*
		Number of execution cycles for each from of addressing
00 to 07	Ri RWi RLi	Listed in Table of Instructions
08 to 0B	@RWj	1
0C to 0F	@RWj +	4
10 to 17	@RWi + disp8	1
18 to 1B	@RWj + disp16	1
1C 1D 1E 1F	@RW0 + RW7 @RW1 + RW7 @PC + dip16 @addr16	2 2 2 1

* : “(a)” is used in the “cycles” (number of cycles) column and column B (correction value) in the Table of Instructions.

Table 5 Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles

Operand	(b)*		(c)*		(d)*	
	byte		word		long	
Internal register	+	0	+	0	+	0
Internal RAM even address	+	0	+	0	+	0
Internal RAM odd address	+	0	+	1	+	2
Even address not in internal RAM	+	1	+	1	+	2
Odd address not in internal RAM	+	1	+	3	+	6
External data bus (8 bits)	+	1	+	3	+	6

* : “(b)”, “(c)”, and “(d)” are used in the “cycles” (number of cycles) column and column B (correction value) in the Table of Instructions.

Table 8 Transfer Instructions (Long Word) [11 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVL A, ear	2	1	0	long (A) ← (ear)	–	–	–	–	–	*	*	–	–	–
MOVL A, eam	2+	3+ (a)	(d)	long (A) ← (eam)	–	–	–	–	–	*	*	–	–	–
MOVL A, # imm32	5	3	0	long (A) ← imm32	–	–	–	–	–	*	*	–	–	–
MOVL A, @SP + disp8	3	4	(d)	long (A) ← ((SP) +disp8)	–	–	–	–	–	*	*	–	–	–
MOVPL A, addr24	5	4	(d)	long (A) ← (addr24)	–	–	–	–	–	*	*	–	–	–
MOVPL A, @A	2	3	(d)	long (A) ← ((A))	–	–	–	–	–	*	*	–	–	–
MOVPL @A, RLi	2	5	(d)	long ((A)) ← (RLi)	–	–	–	–	–	*	*	–	–	–
MOVL @SP + disp8, A	3	4	(d)	long ((SP) + disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVPL addr24, A	5	4	(d)	long (addr24) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVL ear, A	2	2	0	long (ear) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVL eam, A	2+	3+ (a)	(d)	long (eam) ← (A)	–	–	–	–	–	*	*	–	–	–

For an explanation of “(a)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 10 Increment and Decrement Instructions (Byte/Word/Long Word) [12 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
INC ear	2	2	0	byte (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	*
INC eam	2+	3+ (a)	2× (b)	byte (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DEC ear	2	2	0	byte (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	*
DEC eam	2+	3+ (a)	2× (b)	byte (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*
INCW ear	2	2	0	word (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	*
INCW eam	2+	3+ (a)	2× (c)	word (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DECW ear	2	2	0	word (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	*
DECW eam	2+	3+ (a)	2× (c)	word (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*
INCL ear	2	4	0	long (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	*
INCL eam	2+	5+ (a)	2× (d)	long (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DECL ear	2	4	0	long (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	*
DECL eam	2+	5+ (a)	2× (d)	long (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*

For an explanation of “(a)”, “(b)”, “(c)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

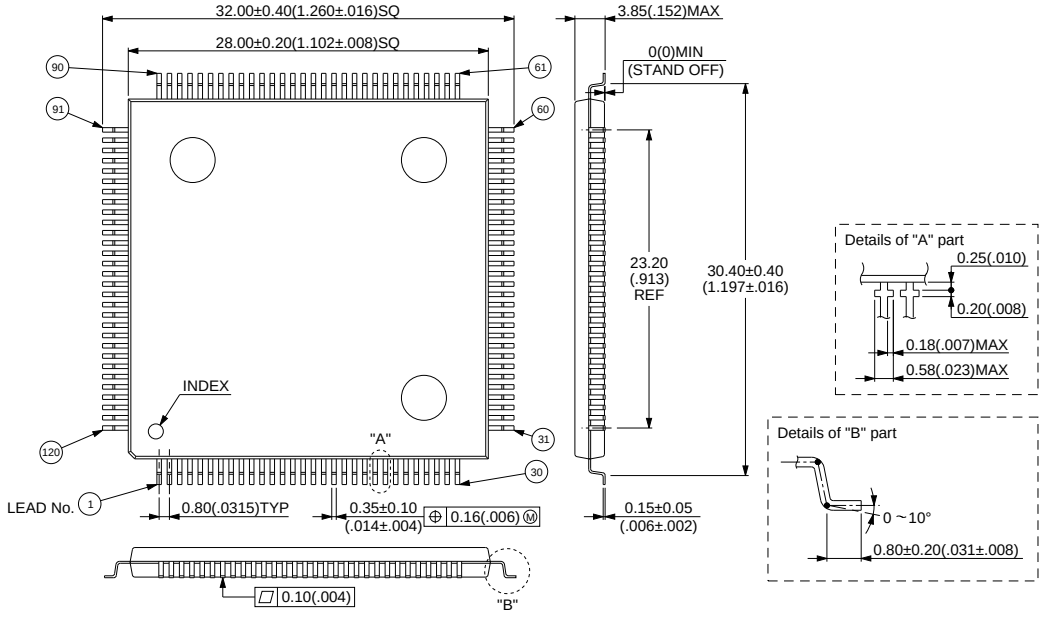
Table 11 Compare Instructions (Byte/Word/Long Word) [11 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
CMP A	1	2	0	byte (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
CMP A, ear	2	2	0	byte (A) – (ear)	–	–	–	–	–	*	*	*	*	–
CMP A, eam	2+	2+ (a)	(b)	byte (A) – (eam)	–	–	–	–	–	*	*	*	*	–
CMP A, #imm8	2	2	0	byte (A) – imm8	–	–	–	–	–	*	*	*	*	–
CMPW A	1	2	0	word (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
CMPW A, ear	2	2	0	word (A) – (ear)	–	–	–	–	–	*	*	*	*	–
CMPW A, eam	2+	2+ (a)	(c)	word (A) – (eam)	–	–	–	–	–	*	*	*	*	–
CMPW A, #imm16	3	2	0	word (A) – imm16	–	–	–	–	–	*	*	*	*	–
CMPL A, ear	2	3	0	long (A) – (ear)	–	–	–	–	–	*	*	*	*	–
CMPL A, eam	2+	4+ (a)	(d)	long (A) – (eam)	–	–	–	–	–	*	*	*	*	–
CMPL A, #imm32	5	3	0	long (A) – imm32	–	–	–	–	–	*	*	*	*	–

For an explanation of “(a)”, “(b)”, “(c)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

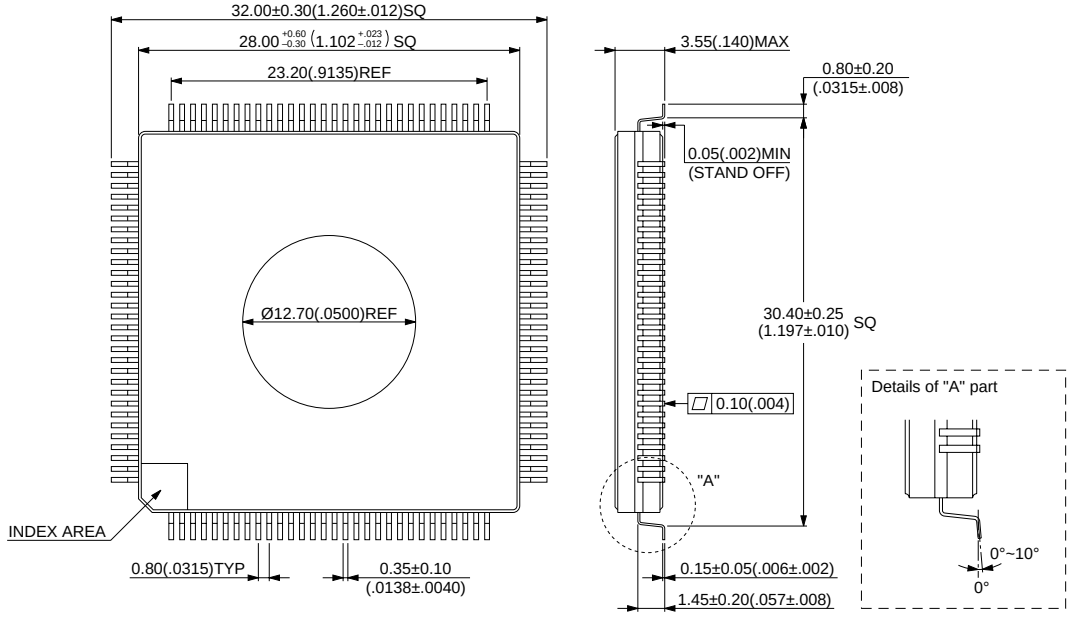
■ PACKAGE DIMENSIONS

120-pin Plastic QFP
(FPT-120P-M03)



Dimensions in mm (inches)

120-pin Ceramic QFP
(FPT-120C-C02)



Dimensions in mm (inches)

Note: See to the latest version of Package Data Book for official package dimensions.