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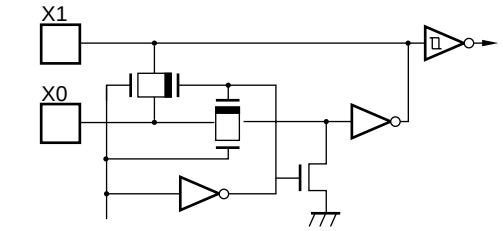
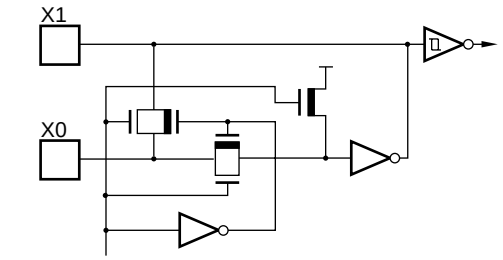
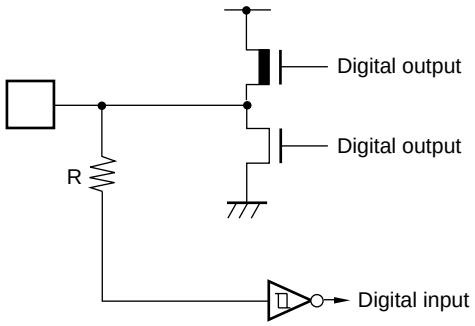
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

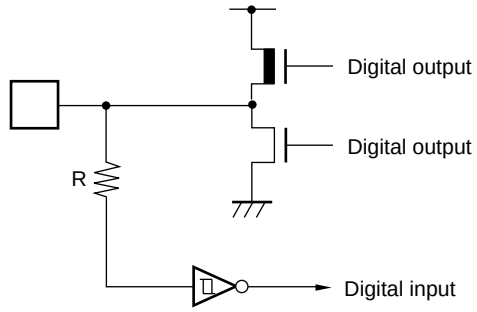
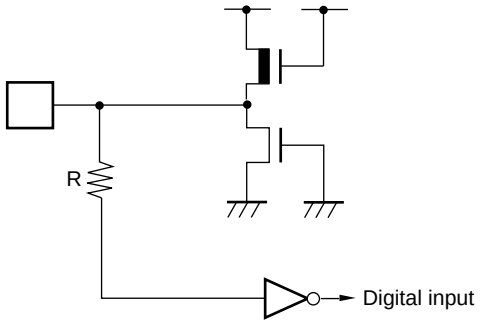
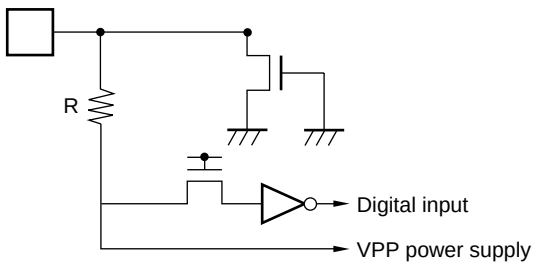
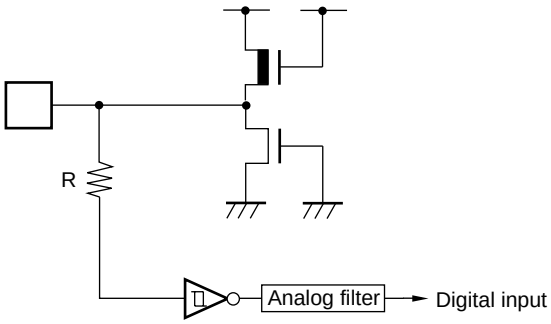
Details	
Product Status	Active
Core Processor	F²MC-16F
Core Size	16-Bit
Speed	16MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	102
Program Memory Size	96KB (96K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	4.5K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-BQFP
Supplier Device Package	120-QFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90224pf-gt-370

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Oscillation feedback resistor: Approx. 1 MΩ MB90223 MB90224 MB90P224B MB90W224B
		• Oscillation feedback resistor: Approx. 1 MΩ MB90P224A MB90W224A
B		• CMOS-level output • CMOS-level hysteresis input with no standby control

Note: The pull-up and pull-down resistors are always connected, regardless of the state.

(Continued)

Type	Circuit	Remarks
C		• CMOS-level output • CMOS-level hysteresis input with standby control
D		• CMOS-level input with no standby control Mask ROM products only: MD2: with pull-down resistor MD1: with pull-up resistor MD0: with pull-down resistor
		• CMOS-level input with no standby control MD2 of OTPROM products/EPROM products only
E		• CMOS-level hysteresis input with no standby control • With input analog filter (40 ns Typ.)

Note: The pull-up and pull-down resistors are always connected, regardless of the state.

(Continued)

Address	Register	Register name	Access	Resouce name	Initial value
000023H	Rate and data register 0	URD0	R/W	UART0 (ch.0)	0 0 0 0 0 0 0 X
000024H	Mode control register 1	UMC1	R/W	UART0 (ch.1)	0 0 0 0 0 1 0 0
000025H	Status register 1	USR1	R/W		0 0 0 1 0 0 0 0
000026H	Input data register 1 /output data register 1	UIDR1 /UODR1	R/W		X X X X X X X X
000027H	Rate and data register 1	URD1	R/W		0 0 0 0 0 0 0 X
000028H	Mode control register 2	UMC2	R/W	UART0 (ch.2)	0 0 0 0 0 1 0 0
000029H	Status register 2	USR2	R/W		0 0 0 1 0 0 0 0
00002AH	Input data register 2 /output data register 2	UIDR2 /UODR2	R/W		X X X X X X X X
00002BH	Rate and data register 2	URD2	R/W		0 0 0 0 0 0 0 X
00002CH	UART CTS control register	UCCR	R/W	UART0 (ch.0)	– – – 0 0 0 – –
00002DH	(Reserved area)*1				
00002EH	Mode register	SMR	R/W	UART1	0 0 0 0 0 0 0 0
00002FH	Control register	SCR	R/W		0 0 0 0 0 1 0 0
000030H	Input data register /output data register	SIDR /SODR	R/W		X X X X X X X X
000031H	Status register	SSR	R/W		0 0 0 0 1 – 0 0
000032H	A/D channel setting register	ADCH	R/W	10-bit A/D converter	0 0 0 0 0 0 0 0
000033H	A/D mode register	ADMD	R/W		– – – X 0 0 0 0
000034H	A/D control status register	ADCS	R/W		0 0 0 0 – – 0 0
000035H	(Reserved area)*1				
000036H	A/D data register	ADCD	R	10-bit A/D converter	X X X X X X X X
000037H					0 0 0 0 0 0 X X
000038H	(Reserved area)*1				
000039H					
00003AH	DTP/interrupt enable register	ENIR	R/W	DTP/external interrupt	0 0 0 0 0 0 0 0
00003BH	DTP/interrupt source register	EIRR	R/W		0 0 0 0 0 0 0 0
00003CH	Request level setting register	ELVR	R/W		0 0 0 0 0 0 0 0
00003DH					0 0 0 0 0 0 0 0
00003EH to 3FH	(Reserved area)*1				
000040H	Timer control status register 0	TMCSR0	R/W	16-bit reload timer 0	0 0 0 0 0 0 0 0
000041H					– – – – 0 0 0 0

(Continued)

Address	Register	Register name	Access	Resouce name	Initial value
000042H	Timer control status register 1	TMCSR1	R/W	16-bit reload timer 1	0 0 0 0 0 0 0 0
000043H					– – – – 0 0 0 0
000044H	Timer control status register 2	TMCSR2	R/W	16-bit reload timer 2	0 0 0 0 0 0 0 0
000045H					– – – – 0 0 0 0
000046H	Timer control status register 3	TMCSR3	R/W	16-bit reload timer 3	0 0 0 0 0 0 0 0
000047H					– – – – 0 0 0 0
000048H	Timer control status register 4	TMCSR4	R/W	16-bit reload timer 4	0 0 0 0 0 0 0 0
000049H					– – – – 0 0 0 0
00004AH	Timer control status register 5	TMCSR5	R/W	16-bit reload timer 5	0 0 0 0 0 0 0 0
00004BH					– – – – 0 0 0 0
00004CH	PPG control status register 0	PCNT0	R/W	16-bit PPG timer 0	0 0 0 0 0 0 0 0
00004DH					0 0 0 0 0 0 0 0
00004EH	PPG control status register 1	PCNT1	R/W	16-bit PPG timer 1	0 0 0 0 0 0 0 0
00004FH					0 0 0 0 0 0 0 0
000050H	PWC control status register 0	PWCSR0	R/W	PWC timer 0	0 0 0 0 0 0 0 0
000051H					0 0 0 0 0 0 0 0
000052H	PWC control status register 1	PWCSR1	R/W	PWC timer 1	0 0 0 0 0 0 0 0
000053H					0 0 0 0 0 0 0 0
000054H	PWC control status register 2	PWCSR2	R/W	PWC timer 2	0 0 0 0 0 0 0 0
000055H					0 0 0 0 0 0 0 0
000056H	PWC control status register 3	PWCSR3	R/W	PWC timer 3	0 0 0 0 0 0 0 0
000057H					0 0 0 0 0 0 0 0
000058H	ICU control register 0	ICC0	R/W	ICU (Input Capture Unit)	0 0 0 0 0 0 0 0
000059H	(Reserved area)*1				
00005AH	Input capture control register 1	ICC1	R/W	ICU (Input Capture Unit)	0 0 0 0 0 0 0 0
00005BH	(Reserved area)*1				
00005CH					
00005DH					
00005EH					
00005FH					
000060H	OCU control register 00	CCR00	R/W	OCU (Output Compare Unit)	1 1 1 1 0 0 0 0
000061H					– – – – 0 0 0 0

(Continued)

Address	Register	Register name	Access	Resouce name	Initial value
001F02H	PWC data buffer register 1	PWCR1	R/W	PWC timer 1	0 0 0 0 0 0 0 0
001F03H					0 0 0 0 0 0 0 0
001F04H	PWC data buffer register 2	PWCR2	R/W	PWC timer 2	0 0 0 0 0 0 0 0
001F05H					0 0 0 0 0 0 0 0
001F06H	PWC data buffer register 3	PWCR3	R/W	PWC timer 3	0 0 0 0 0 0 0 0
001F07H					0 0 0 0 0 0 0 0
001F08H to 1F0FH	(Reserved area)*1				
001F10H	OCU compare lower-order data register 00	CPR00L	R/W	Output compare 00	0 0 0 0 0 0 0 0
001F11H					0 0 0 0 0 0 0 0
001F12H	OCU compare higher-order data register 00	CPR00			0 0 0 0 0 0 0 0
001F13H					0 0 0 0 0 0 0 0
001F14H	OCU compare lower-order data register 01	CPR01L	R/W	Output compare 01	0 0 0 0 0 0 0 0
001F15H					0 0 0 0 0 0 0 0
001F16H	OCU compare higher-order data register 01	CPR01			0 0 0 0 0 0 0 0
001F17H					0 0 0 0 0 0 0 0
001F18H	OCU compare lower-order data register 02	CPR02L	R/W	Output compare 02	0 0 0 0 0 0 0 0
001F19H					0 0 0 0 0 0 0 0
001F1AH	OCU compare higher-order data register 02	CPR02			0 0 0 0 0 0 0 0
001F1BH					0 0 0 0 0 0 0 0
001F1CH	OCU compare lower-order data register 03	CPR03L	R/W	Output compare 03	0 0 0 0 0 0 0 0
001F1DH					0 0 0 0 0 0 0 0
001F1EH	OCU compare higher-order data register 03	CPR03			0 0 0 0 0 0 0 0
001F1FH					0 0 0 0 0 0 0 0
001F20H	OCU compare lower-order data register 04	CPR04L	R/W	Output compare 10	0 0 0 0 0 0 0 0
001F21H					0 0 0 0 0 0 0 0
001F22H	OCU compare higher-order data register 04	CPR04			0 0 0 0 0 0 0 0
001F23H					0 0 0 0 0 0 0 0
001F24H	OCU compare lower-order data register 05	CPR05L	R/W	Output compare 11	0 0 0 0 0 0 0 0
001F25H					0 0 0 0 0 0 0 0
001F26H	OCU compare higher-order data register 05	CPR05			0 0 0 0 0 0 0 0
001F27H					0 0 0 0 0 0 0 0

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Interrupt source	EI²OS support	Interrupt vector			Interrupt control register	
		No.		Address	ICR	Address
UART0 (ch.0) reception completed	◎	#39	27H	FFFF60H	ICR14	0000BEH
Delay interrupt generation module	×	#42	2AH	FFFF54H	ICR15	0000BFH
Stack fault	×	#255	FFH	FFFC00H	—	—

◎: EI²OS is supported (with stop request).
□: EI²OS is supported (without stop request).
○: EI²OS is supported; however, since two interrupt sources are allocated to a single ICR, in case EI²OS is used for one of the two, EI²OS and ordinary interrupt are not both available for the other (with stop request).
△: EI²OS is supported; however, since two interrupt sources are allocated to a single ICR, in case EI²OS is used for one of the two, EI²OS and ordinary interrupt are not both available for the other (without stop request).
×: EI²OS is not supported.

Note: Since the interrupt sources having interrupt vector Nos. 15 to 18, 20, and 25 to 28 are OR'ed, respectively, select them by means of the interrupt enable bits of each resource.

If EI²OS is used with the above-mentioned interrupt sources OR'ed with the interrupt vector Nos. 15 to 18, 20, and 25 to 28, be sure to activate one of the interrupt sources.

Also in this case, a request flag in the same series as the one interrupt source is likely to be cleared automatically by EI²OS.

Assume for example that an interrupt for compare 4 of the interrupt vector No. 25 is activated at this time by ICR07, so that the compare 6 is disabled. If EI²OS is activated at this time by ICR07, so that the compare 6 interrupt takes place during generation of or simultaneously with the compare 4 interrupt, not only the interrupt flag for the compare 4 but also that for the compare 6 will be automatically cleared after EI²OS is automatically transferred due to the compare 4 interrupt.

■ PERIPHERAL RESOURCES

1. Parallel Ports

The MB90220 series has 86 I/O pins and 16 open-drain I/O pins.

(1) Register Configuration

- **Port 0 to C Data Register (PDR0 to PDRC)**

Register name	Address
PDR1	000001H
PDR3	000003H
PDR5	000005H
PDR7	000007H
PDR9	000009H
PDRB	00000BH

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
	PD x 7	PD x 6	PD x 5	PD x 4	PD x 3	PD x 2	PD x 1	PD x 0	XXXXXXXXB
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(PDR9 only: 11111111)
PDR7 only: (R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

Register name	Address
PDR0	000000H
PDR2	000002H
PDR4	000004H
PDR6	000006H
PDR8	000008H
PDRA	00000AH
PDRC	00000CH

	bit7	bit6	bit5	bit 4	bit3	bit2	bit1	bit0	Initial value
	PD x 7	PD x 6	PD x 5	PD x 4	PD x 3	PD x 2	PD x 1	PD x 0	XXXXXXXXB
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(PDR6 only: 11111111)

Note: There are no register bits for bits 7 and 6 of port C.

- **Port 0 to C Data Register (PDR0 to PDRC)**

Register name	Address
DDR1	000011H
DDR3	000013H
DDR5	000015H
DDR7	000017H
DDRB	00001BH

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
	DD x 7	DD x 6	DD x 5	DD x 4	DD x 3	DD x 2	DD x 1	DD x 0	00000000B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(PDR7 only: 11111111)

Register name	Address
DDR0	000010H
DDR2	000012H
DDR4	000014H
DDR8	000018H
DDRA	00001AH
DDRC	00001CH

	bit7	bit6	bit5	bit 4	bit3	bit2	bit1	bit0	Initial value
	DD x 7	DD x 6	DD x 5	DD x 4	DD x 3	DD x 2	DD x 1	DD x 0	00000000B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Note: There are no register bits for bits 7 and 6 of port C.

- **Port 6, 9 Analog Input Enable Register (ADER0, ADER1)**

Register name	Address
ADER0	000016H

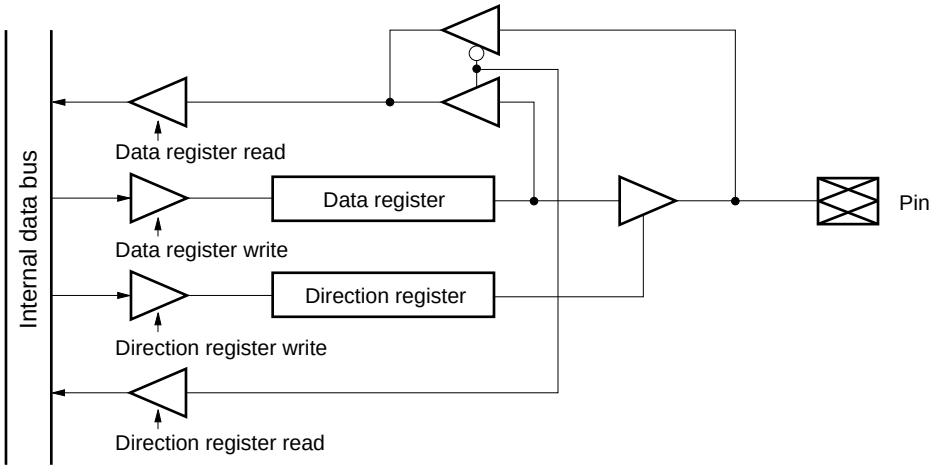
	bit7	bit6	bit5	bit 4	bit3	bit2	bit1	bit0	Initial value
	AE07	AE06	AE05	AE04	AE03	AE02	AE01	AE00	11111111B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Register name	Address
ADER1	000019H

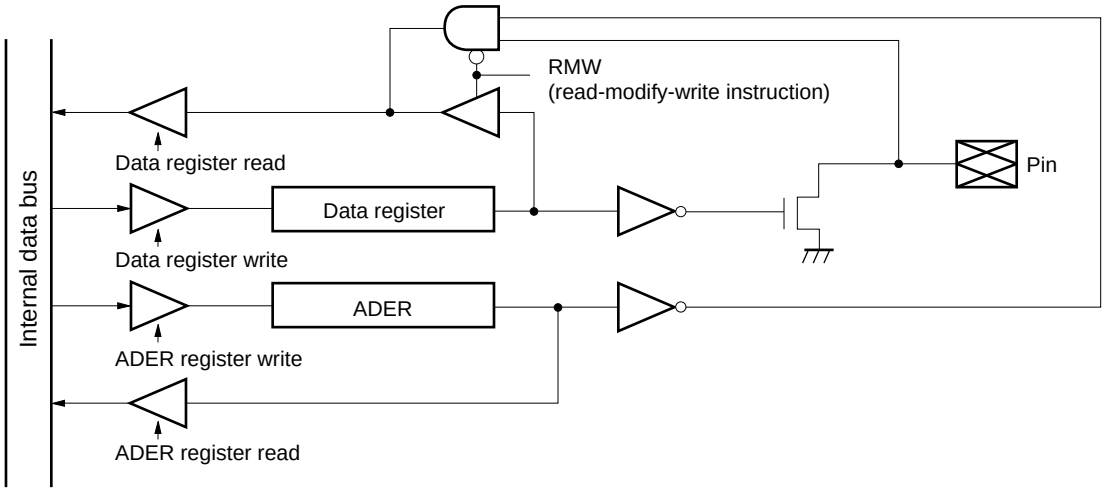
	bit7	bit6	bit5	bit 4	bit3	bit2	bit1	bit0	Initial value
	AE15	AE14	AE13	AE12	AE11	AE10	AE09	AE08	11111111B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

(2) Block Diagram

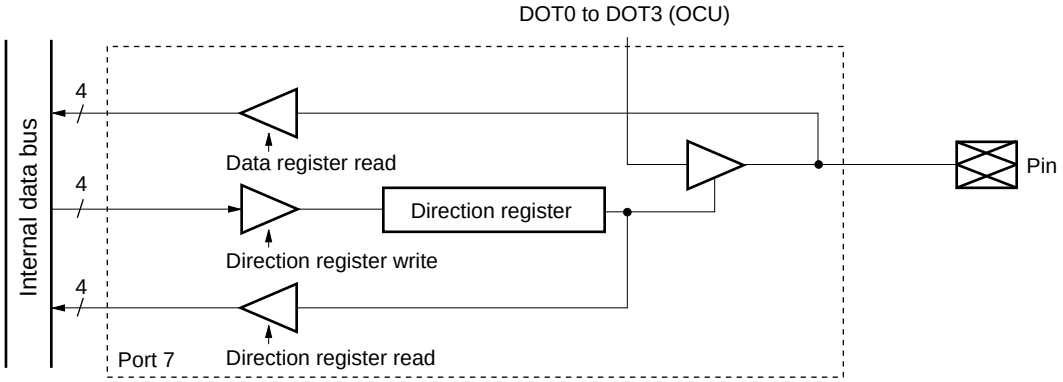
- **I/O Port (Port 0 to 5, 8, and A to C)**



- **I/O Ports with an Open-drain output (Port 6, and 9)**

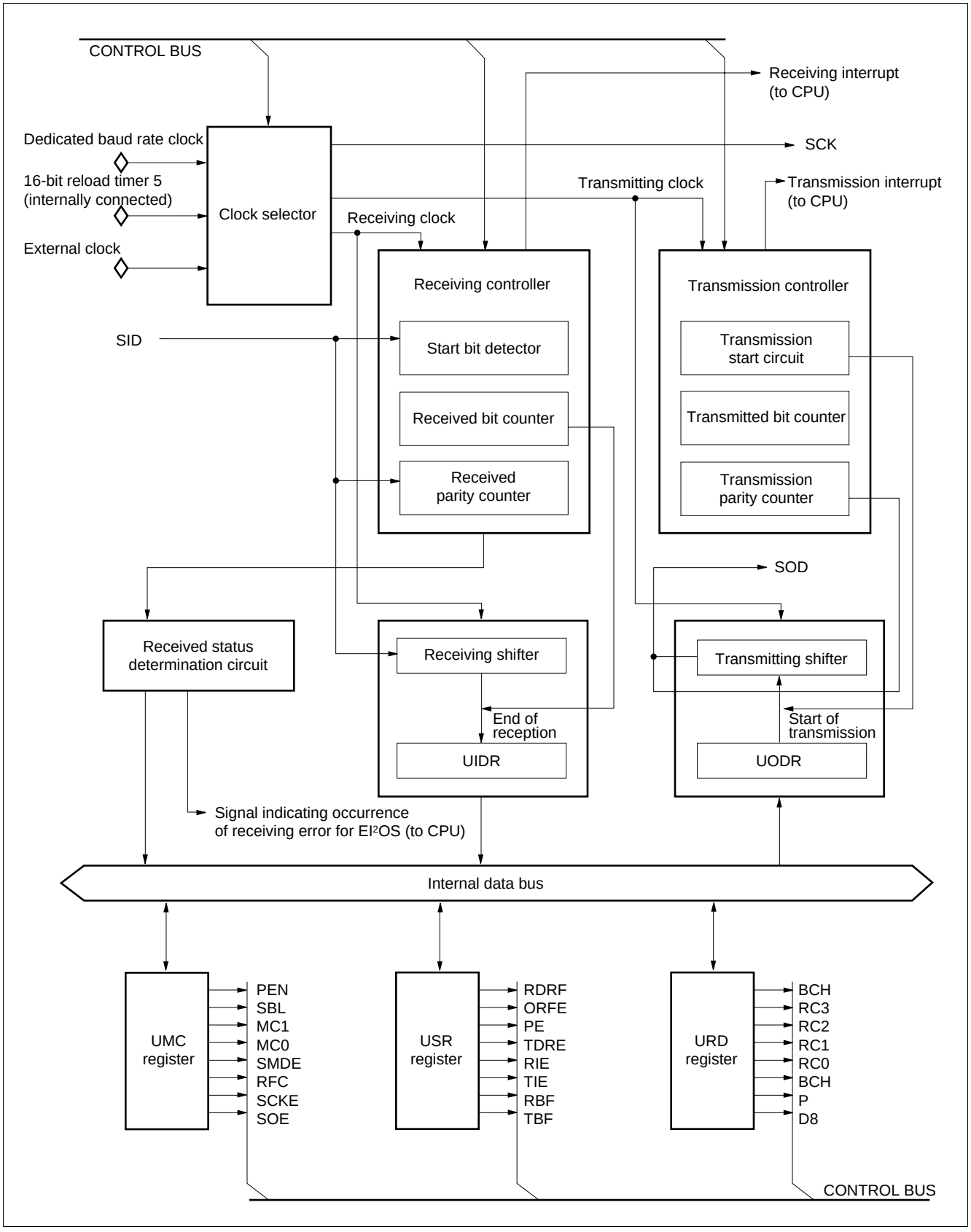


- **I/O Port (Port 7)**



Note: Port 7 is input port. This pin also usable as I/O port for OCU internal function.

(2) Block Diagram



6. PWC (Pulse Width Count) Timer

The PWC (pulse width count) timer is a 16-bit multifunction up-count timer with an input-signal pulse-width count function and a reload timer function. The hardware configuration of this module is a 16-bit up-count timer, an input pulse divider with divide ratio control register, four count input pins, and a 16-bit control register. Using these components, the PWC timer provides the following features:

- Timer functions: An interrupt request can be generated at set time intervals.
  Pulse signals synchronized with the timer cycle can be output.
  The reference internal clock can be selected from among three internal clocks.
- Pulse-width count functions: The time between arbitrary pulse input events can be counted.
  The reference internal clock can be selected from among three internal clocks.
  Various count modes:
  "H" pulse width (↑ to ↓)/"L" pulse width (↓ to ↑)
  Rising-edge cycle (↑ to ↑/Falling-edge cycle (↓ to ↓)
  Count between edges (↑ or ↓ to ↓ or ↑)
  Cycle count can be performed by 2^{2n} division (n = 1, 2, 3, 4) of the input pulse, with an 8 bit input divider.
  An interrupt request can be generated once counting has been performed.
  The number of times counting is to be performed (once or subsequently) can be selected.

The MB90220 series has four channels for this module.

(1) Register Configuration

- **PWC Control Status Register 0 to 3 (PWCSR0 to PWCSR3)**

Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
PWCSR0	000051H	STRT	STOP	EDIR	EDIE	OVIR	OVIE	ERR	POUT	00000000B
PWCSR1	000053H									
PWCSR2	000055H									
PWCSR3	000057H	(R/W)	(R/W)	(R)	(R/W)	(R/W)	(R/W)	(R)	(R/W)	

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
PWCSR0	000050H	CKS1	CKS0	PIS1	PIS0	S/C	MOD1	MOD1	MOD0	00000000B
PWCSR1	000052H									
PWCSR2	000054H									
PWCSR3	000056H	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

- **PWC Data Buffer Register 0 to 3 (PWCR0 to PWCR3)**

Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
PWCR0	001F01H									00000000B
PWCR1	001F03H									
PWCR2	001F05H									
PWCR3	001F07H	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
PWCR0	001F00H									00000000B
PWCR1	001F02H									
PWCR2	001F04H									
PWCR3	001F06H	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

12. Watchdog Timer and Timebase Timer Functions

The watchdog timer consists of a 2-bit watchdog counter using carry from an 18-bit timebase timer as the clock source, a control register, and a watchdog reset control section. The timebase timer consists of an 18-bit timer and an interval interrupt control circuit.

(1) Register Configuration

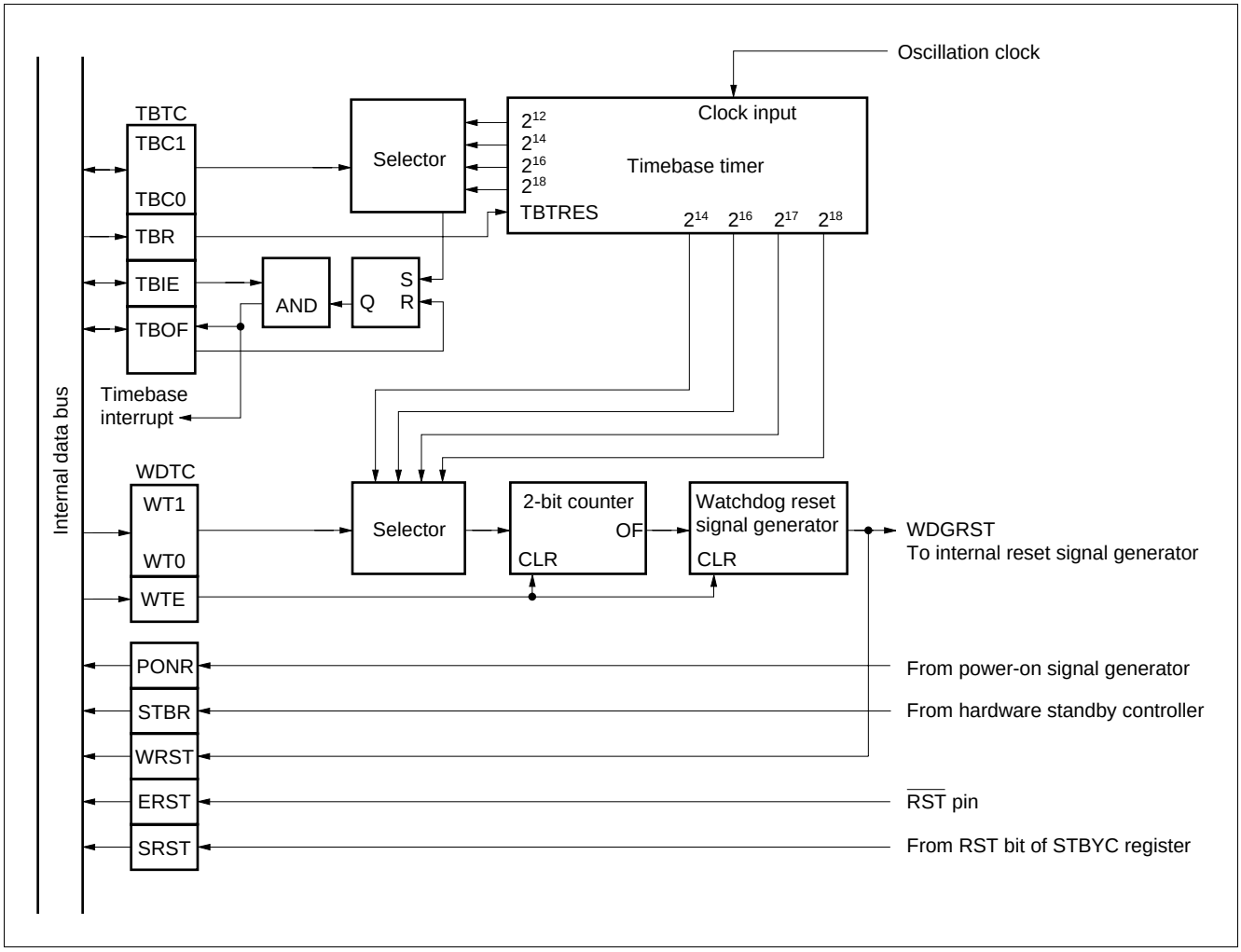
- **Watchdog Timer Control Register (WDTC)**

Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
WDTC	0000A8H	PONR	STBR	WRST	ERST	SRST	WTE	WT1	WT0	XXXXXXXX
		(R)	(R)	(R)	(R)	(R)	(W)	(W)	(W)	

- **Timebase Timer Control Register (TBTC)**

Register name	Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
TBTC	0000A9H	—	—	—	TBIE	TBOF	TBR	TBC1	TBC0	- - - XXXXX
		(—)	(—)	(—)	(R/W)	(R/W)	(R)	(R/W)	(R/W)	

(2) Block Diagram



■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min.	Max.		
Power supply voltage	V_{CC}	V_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	
Program voltage	V_{PP}	V_{PP}	V_{SS} – 0.3	13.0	V	MB90P224A/P224B MB90W224A/W224B
Analog power supply voltage	AV_{CC}	AV_{CC}	V_{SS} – 0.3	V_{CC} + 0.3	V	Power supply voltage for A/D converter
	AVRH AVRL	AVRH AVRL	V_{SS} – 0.3	AV_{CC}	V	Reference voltage for A/D converter
Input voltage	V_I*1	—	V_{SS} – 0.3	V_{CC} + 0.3	V	
Output voltage	V_O	*2	V_{SS} – 0.3	V_{CC} + 0.3	V	
“L” level output current	I_{OL}	*3	—	20	mA	Rush current
“L” level total output current	ΣI_{OL}	*3	—	50	mA	Total output current
“H” level output current	I_{OH}	*2	—	–10	mA	Rush current
“H” level total output current	ΣI_{OH}	*2	—	–48	mA	Total output current
Power consumption	P_D	—	—	650	mW	
Operating temperature	T_A	—	–40	+105	°C	MB90223/224/P224B /W224B
			–40	+85	°C	MB90P224A/W224A
Storage temperature	Tstg	—	–55	+150	°C	

*1: V_1 must not exceed V_{CC} + 0.3 V.

*2: Output pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P77, P80 to P87, PA0 to PA7, PB0 to PB7, PC0 to PC5

*3: Output pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA7, PB0 to PB7, PC0 to PC5

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

(Continued)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Analog power supply voltage	I_A	AV_{CC}	f_C = 16 MHz*9	—	3	7	mA	
	I_{AH}		—	—	—	5*6	µA	At stop mode
Input capacitance	C_{IN}	*7	—	—	10	—	pF	

*1: Hysteresis input pins
$\overline{RST}$, $\overline{HST}$, P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P80 to P87, P90 to P97, PA0 to PA7, PB0 to PB7, PC0 to PC5

*2: Ouput pins
P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P77, P80 to P87, PA0 to PA7, PB0 to PB7, PC0 to PC5

*3: Output pins
P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA7, PB0 to PB7, PC0 to PC5

*4: A list of availabilities of pull-up/pull-down resistors

Pin name	MB90223/224	MB90P224A/W224A	MB90P224B/W224B
$\overline{RST}$	Availability of pull-up resistors is optionally defined.	Pull-up resistors available	Unavailable
MD1	Pull-up resistors available	Unavailable	Unavailable
MD0, MD2	Pull-up resistors available	Unavailable	Unavailable

*5: V_{CC} = +5.0 V, V_{SS} = 0.0 V, T_A = +25°C, F_C = 16 MHz

*6: The current value applies to the CPU stop mode with A/D converter inactive (V_{CC} = AV_{CC} = AVRH = +5.5 V).

*7: Other than V_{CC}, V_{SS}, AV_{CC} and AV_{SS}

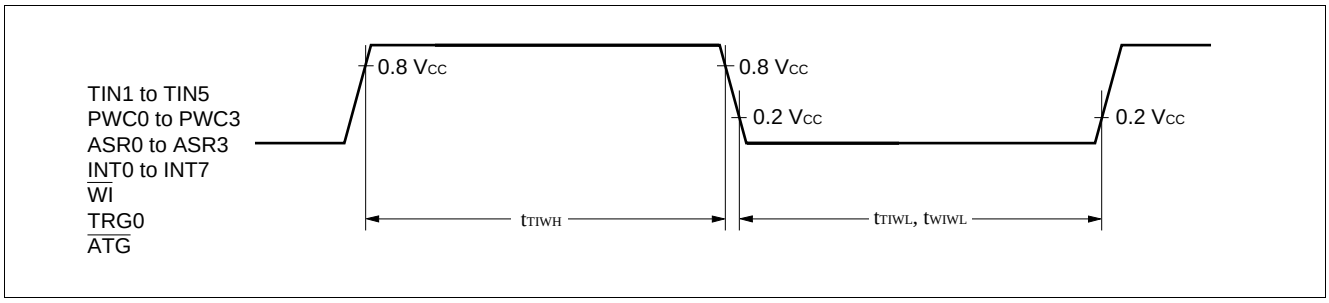
*8: Measurement condition of power supply current; external clock pin and output pin are open.
Measurement condition of V_{CC}; see the table above mentioned.

*9: F_C = 12 MHz for MB90223

(10) Resourse Input Timing

Single-chip mode MB90223/224/P224B/W224B: (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +105°C)
MB90P224A/W224A : (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)
External bus mode : (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +70°C)

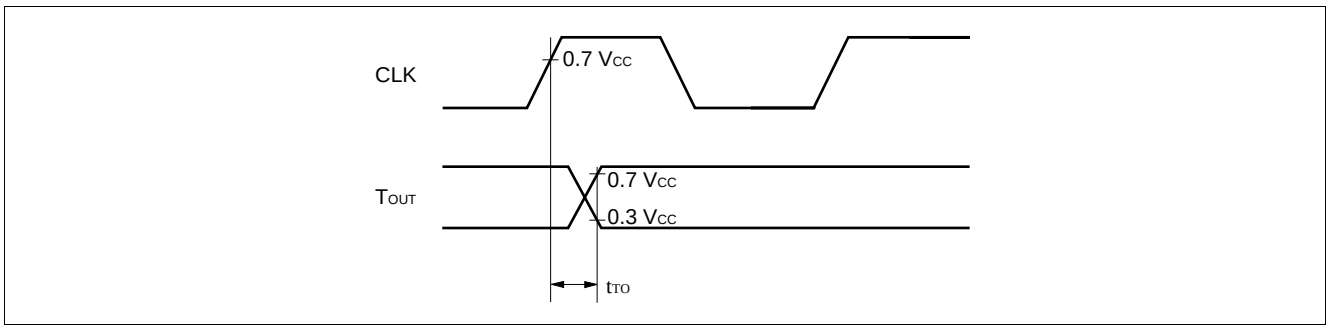
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Input pulse width	t_{TIWH} t_{TIWL}	TIN1 to TIN5	Load condition: 80 pF	4 t_{CYC}	—	—	ns	External event count input mode
				2 t_{CYC}	—	—	ns	Trigger input/gate input mode
		PWC0 to PWC3		2 t_{CYC}	—	—	ns	
		ASR0 to ASR3		2 t_{CYC}	—	—	ns	
		INT0 to INT7		3 t_{CYC}	—	—	ns	
		TRG0		2 t_{CYC}	—	—	ns	
		$\overline{ATG}$		2 t_{CYC}	—	—	ns	
	t_{WIWL}	$\overline{WI}$		4 t_{CYC}	—	—	ns	



(11) Resourse Output Timing

Single-chip mode MB90223/224/P224B/W224B: (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +105°C)
MB90P224A/W224A : (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)
External bus mode : (V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
CLK ↑ → T_{OUT} transition time	t_{TO}	TOT0 to TOT5 PPG0 to PPG1 POT0 to POT3 DOT0 to DOT7	Load condition: 80 pF	—	—	30	ns	



5. A/D Converter Electrical Characteristics

Single-chip mode MB90223/224/P224B/W224B
: (AV_{CC} = V_{CC} = +4.5 V to +5.5 V, AV_{SS} =V_{SS} = 0.0 V, T_A = –40°C to +105°C, +4.5 V ≤ AVRH – AVRL)
MB90P224A/W224A
: (AV_{CC} = V_{CC} = +4.5 V to +5.5 V, AV_{SS} = V_{SS} =0.0 V, T_A = –40°C to +85°C, +4.5 V ≤ AVRH – AVRL)
External bus mode : (AV_{CC} = V_{CC} = +4.5 V to +5.5 V, AV_{SS} = V_{SS} =0.0 V, T_A = –40°C to +70°C, +4.5 V ≤ AVRH – AVRL)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Resolution	n	—	—	—	—	10	bit	
Total error	—	—	—	—	—	±3.0	LSB	
Linearity error	—	—	—	—	—	±2.0	LSB	
Differential linearity error	—	—	—	—	—	±1.5	LSB	
Zero transition voltage	V_{0T}	AN00 to AN15	—	AVRL – 1.5	AVRL + 0.5	AVRL + 2.5	LSB	
Full-scale transition voltage	V_{FST}		—	AVRH – 3.5	AVRH – 1.5	AVRH + 0.5	LSB	
Conversion time*1	T_{CONV}	—	t_{CYC} = 62.5 ns	6.125	—	—	µs	98 machine cycles
Sampling period	T_{SAMP}	—		3.75	—	—	µs	60 machine cycles
Analog port input current	I_{AIN}	AN00 to AN15	—	—	—	±0.1	µA	
Analog input voltage	V_{AIN}		—	AVRL	—	AVRH	V	
Analog reference voltage	—	AVRH	—	AVRL	—	AV_{CC}	V	
		AVRL	—	AV_{SS}	—	AVRH	V	
Reference voltage supply current	I_R	AVRH	—	—	200	500	µA	
	I_{RH}		—	—	—	5*2	µA	
Variation between channels	—	AN00 to AN15	—	—	—	4	LSB	

*1: These standards in this table are for MB90224/P224A/P224B/W224A/W224B.
MB90223: Minimum conversion time is 8.17 µs and minimum sampling time is 5 µs at t_{CYC} = 83.4 ns.
*2: The current value applies to the CPU stop mode with the A/D converter inactive (V_{CC} = AV_{CC} = AVRH = +5.5 V).
Notes: (1) The error becomes larger as | AVRH – AVRL | becomes smaller.
(2) Use the output impedance of the external circuit for analog input under the following conditions:
External circuit output impedance < approx. 10 kΩ (Sampling time approx. 3.75 µs, t_{CYC} = 62.5 ns)
(3) Precision values are standard values applicable to sleep mode.
(4) If V_{CC}/AV_{CC} or V_{SS}/AV_{SS} is caused by a noise to drop to below the analog input volgtage, the analog input current is likely to increase. In such cases, a bypass capacitor or the like should be provided in the external circuit to suppress the noise.

■ INSTRUCTION SET (412 INSTRUCTIONS)

Table 1 Explanation of Items in Table of Instructions

Item	Explanation
Mnemonic	Upper-case letters and symbols: Represented as they appear in assembler Lower-case letters: Replaced when described in assembler. Numbers after lower-case letters: Indicate the bit width within the instruction.
#	Indicates the number of bytes.
~	Indicates the number of cycles. See Table 4 for details about meanings of letters in items.
B	Indicates the correction value for calculating the number of actual cycles during execution of instruction. The number of actual cycles during execution of instruction is summed with the value in the “cycles” column.
Operation	Indicates operation of instruction.
LH	Indicates special operations involving the bits 15 through 08 of the accumulator. Z: Transfers “0”. X: Extends before transferring. —: Transfers nothing.
AH	Indicates special operations involving the high-order 16 bits in the accumulator. *: Transfers from AL to AH. —: No transfer. Z: Transfers 00_H to AH. X: Transfers 00_H or FF_H to AH by extending AL.
I	Indicates the status of each of the following flags: I (interrupt enable), S (stack), T (sticky bit), N (negative), Z (zero), V (overflow), and C (carry). *: Changes due to execution of instruction. —: No change. S: Set by execution of instruction. R: Reset by execution of instruction.
S	
T	
N	
Z	
V	
C	
RMW	Indicates whether the instruction is a read-modify-write instruction (a single instruction that reads data from memory, etc., processes the data, and then writes the result to memory.). *: Instruction is a read-modify-write instruction —: Instruction is not a read-modify-write instruction Note: Cannot be used for addresses that have different meanings depending on whether they are read or written.

(Continued)

Symbol	Explanation
#imm4 #imm8 #imm16 #imm32 ext (imm8)	4-bit immediate data 8-bit immediate data 16-bit immediate data 32-bit immediate data 16-bit data signed and extended from 8-bit immediate data
disp8 disp16	8-bit displacement 16-bit displacement
bp	Bit offset value
vct4 vct8	Vector number (0 to 15) Vector number (0 to 255)
( )b	Bit address
rel ear eam	Branch specification relative to PC Effective addressing (codes 00 to 07) Effective addressing (codes 08 to 1F)
rlst	Register list

(Continued)

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
XCH A, ear	2	3	0	byte (A) ↔ (ear)	Z	–	–	–	–	–	–	–	–	–
XCH A, eam	2+	3+ (a)	2× (b)	byte (A) ↔ (eam)	Z	–	–	–	–	–	–	–	–	–
XCH Ri, ear	2	4	0	byte (Ri) ↔ (ear)	–	–	–	–	–	–	–	–	–	–
XCH Ri, eam	2+	5+ (a)	2× (b)	byte (Ri) ↔ (eam)	–	–	–	–	–	–	–	–	–	–

For an explanation of “(a)” and “(b)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 7 Transfer Instructions (Word) [40 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVW A, dir	2	2	(c)	word (A) ← (dir)	–	*	–	–	–	*	*	–	–	–
MOVW A, addr16	3	2	(c)	word (A) ← (addr16)	–	*	–	–	–	*	*	–	–	–
MOVW A, SP	1	2	0	word (A) ← (SP)	–	*	–	–	–	*	*	–	–	–
MOVW A, RWi	1	1	0	word (A) ← (RWi)	–	*	–	–	–	*	*	–	–	–
MOVW A, ear	2	1	0	word (A) ← (ear)	–	*	–	–	–	*	*	–	–	–
MOVW A, eam	2+	2+ (a)	(c)	word (A) ← (eam)	–	*	–	–	–	*	*	–	–	–
MOVW A, io	2	2	(c)	word (A) ← (io)	–	*	–	–	–	*	*	–	–	–
MOVW A, @A	2	2	(c)	word (A) ← ((A))	–	–	–	–	–	*	*	–	–	–
MOVW A, #imm16	3	2	0	word (A) ← imm16	–	*	–	–	–	*	*	–	–	–
MOVW A, @RWi+disp8	2	3	(c)	word (A) ← ((RWi) +disp8)	–	*	–	–	–	*	*	–	–	–
MOVW A, @RLi+disp8	3	6	(c)	word (A) ← ((RLi) +disp8)	–	*	–	–	–	*	*	–	–	–
MOVW A, @SP+disp8	3	3	(c)	word (A) ← ((SP) +disp8	–	*	–	–	–	*	*	–	–	–
MOVPW A, addr24	5	3	(c)	word (A) ← (addr24)	–	*	–	–	–	*	*	–	–	–
MOVPW A, @A	2	2	(c)	word (A) ← ((A))	–	–	–	–	–	*	*	–	–	–
MOVW dir, A	2	2	(c)	word (dir) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW addr16, A	3	2	(c)	word (addr16) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW SP, # imm16	4	2	0	word (SP) ← imm16	–	–	–	–	–	*	*	–	–	–
MOVW SP, A	1	2	0	word (SP) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, A	1	1	0	word (RWi) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW ear, A	2	2	0	word (ear) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW eam, A	2+	2+ (a)	(c)	word (eam) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW io, A	2	2	(c)	word (io) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW @RWi+disp8, A	2	3	(c)	word ((RWi) +disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW @RLi+disp8, A	3	6	(c)	word ((RLi) +disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW @SP+disp8, A	3	3	(c)	word ((SP) +disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVPW addr24, A	5	3	(c)	word (addr24) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVPW @A, RWi	2	3	(c)	word ((A)) ← (RWi)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, ear	2	2	0	word (RWi) ← (ear)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, eam	2+	3+ (a)	(c)	word (RWi) ← (eam)	–	–	–	–	–	*	*	–	–	–
MOVW ear, RWi	2	3	0	word (ear) ← (RWi)	–	–	–	–	–	*	*	–	–	–
MOVW eam, RWi	2+	3+ (a)	(c)	word (eam) ← (RWi)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, #imm16	3	2	0	word (RWi) ← imm16	–	–	–	–	–	*	*	–	–	–
MOVW io, #imm16	4	3	(c)	word (io) ← imm16	–	–	–	–	–	–	–	–	–	–
MOVW ear, #imm16	4	2	0	word (ear) ← imm16	–	–	–	–	–	*	*	–	–	–
MOVW eam, #imm16	4+	2+ (a)	(c)	word (eam) ← imm16	–	–	–	–	–	–	–	–	–	–
MOVW @AL, AH	2	2	(c)	word ((A)) ← (AH)	–	–	–	–	–	*	*	–	–	–
XCHW A, ear	2	3	0	word (A) ↔ (ear)	–	–	–	–	–	–	–	–	–	–
XCHW A, eam	2+	3+ (a)	2× (c)	word (A) ↔ (eam)	–	–	–	–	–	–	–	–	–	–
XCHW RWi, ear	2	4	0	word (RWi) ↔ (ear)	–	–	–	–	–	–	–	–	–	–
XCHW RWi, eam	2+	5+ (a)	2× (c)	word (RWi) ↔ (eam)	–	–	–	–	–	–	–	–	–	–

Note: For an explanation of “(a)” and “(c)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 9 Addition and Subtraction Instructions (Byte/Word/Long Word) [42 Instructions]

Mnemonic	#	cycles	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
ADD A, #imm8	2	2	0	byte (A) ← (A) +imm8	Z	–	–	–	–	*	*	*	*	–
ADD A, dir	2	3	(b)	byte (A) ← (A) +(dir)	Z	–	–	–	–	*	*	*	*	–
ADD A, ear	2	2	0	byte (A) ← (A) +(ear)	Z	–	–	–	–	*	*	*	*	–
ADD A, eam	2+	3+ (a)	(b)	byte (A) ← (A) +(eam)	Z	–	–	–	–	*	*	*	*	–
ADD ear, A	2	2	0	byte (ear) ← (ear) + (A)	–	–	–	–	–	*	*	*	*	*
ADD eam, A	2+	3+ (a)	2× (b)	byte (eam) ← (eam) + (A)	Z	–	–	–	–	*	*	*	*	*
ADDC A	1	2	0	byte (A) ← (AH) + (AL) + (C)	Z	–	–	–	–	*	*	*	*	–
ADDC A, ear	2	2	0	byte (A) ← (A) + (ear) + (C)	Z	–	–	–	–	*	*	*	*	–
ADDC A, eam	2+	3+ (a)	(b)	byte (A) ← (A) + (eam) + (C)	Z	–	–	–	–	*	*	*	*	–
ADDDC A	1	3	0	byte (A) ← (AH) + (AL) + (C) (Decimal)	Z	–	–	–	–	*	*	*	*	–
SUB A, #imm8	2	2	0	byte (A) ← (A) –imm8	Z	–	–	–	–	*	*	*	*	–
SUB A, dir	2	3	(b)	byte (A) ← (A) – (dir)	Z	–	–	–	–	*	*	*	*	–
SUB A, ear	2	2	0	byte (A) ← (A) – (ear)	Z	–	–	–	–	*	*	*	*	–
SUB A, eam	2+	3+ (a)	(b)	byte (A) ← (A) – (eam)	Z	–	–	–	–	*	*	*	*	–
SUB ear, A	2	2	0	byte (ear) ← (ear) – (A)	–	–	–	–	–	*	*	*	*	*
SUB eam, A	2+	3+ (a)	2× (b)	byte (eam) ← (eam) – (A)	–	–	–	–	–	*	*	*	*	*
SUBC A	1	2	0	byte (A) ← (AH) – (AL) – (C)	Z	–	–	–	–	*	*	*	*	–
SUBC A, ear	2	2	0	byte (A) ← (A) – (ear) – (C)	Z	–	–	–	–	*	*	*	*	–
SUBC A, eam	2+	3+ (a)	(b)	byte (A) ← (A) – (eam) – (C)	Z	–	–	–	–	*	*	*	*	–
SUBDC A	1	3	0	byte (A) ← (AH) – (AL) – (C) (Decimal)	Z	–	–	–	–	*	*	*	*	–
ADDW A	1	2	0	word (A) ← (AH) + (AL)	–	–	–	–	–	*	*	*	*	–
ADDW A, ear	2	2	0	word (A) ← (A) +(ear)	–	–	–	–	–	*	*	*	*	–
ADDW A, eam	2+	3+ (a)	(c)	word (A) ← (A) +(eam)	–	–	–	–	–	*	*	*	*	–
ADDW A, #imm16	3	2	0	word (A) ← (A) +imm16	–	–	–	–	–	*	*	*	*	–
ADDW ear, A	2	2	0	word (ear) ← (ear) + (A)	–	–	–	–	–	*	*	*	*	*
ADDW eam, A	2+	3+ (a)	2× (c)	word (eam) ← (eam) + (A)	–	–	–	–	–	*	*	*	*	*
ADDCW A, ear	2	2	0	word (A) ← (A) + (ear) + (C)	–	–	–	–	–	*	*	*	*	–
ADDCW A, eam	2+	3+ (a)	(c)	word (A) ← (A) + (eam) + (C)	–	–	–	–	–	*	*	*	*	–
SUBW A	1	2	0	word (A) ← (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
SUBW A, ear	2	2	0	word (A) ← (A) – (ear)	–	–	–	–	–	*	*	*	*	–
SUBW A, eam	2+	3+ (a)	(c)	word (A) ← (A) – (eam)	–	–	–	–	–	*	*	*	*	–
SUBW A, #imm16	3	2	0	word (A) ← (A) –imm16	–	–	–	–	–	*	*	*	*	–
SUBW ear, A	2	2	0	word (ear) ← (ear) – (A)	–	–	–	–	–	*	*	*	*	*
SUBW eam, A	2+	3+ (a)	2× (c)	word (eam) ← (eam) – (A)	–	–	–	–	–	*	*	*	*	*
SUBCW A, ear	2	2	0	word (A) ← (A) – (ear) – (C)	–	–	–	–	–	*	*	*	*	–
SUBCW A, eam	2+	3+ (a)	(c)	word (A) ← (A) – (eam) – (C)	–	–	–	–	–	*	*	*	*	–
ADDL A, ear	2	5	0	long (A) ← (A) + (ear)	–	–	–	–	–	*	*	*	*	–
ADDL A, eam	2+	6+ (a)	(d)	long (A) ← (A) + (eam)	–	–	–	–	–	*	*	*	*	–
ADDL A, #imm32	5	4	0	long (A) ← (A) +imm32	–	–	–	–	–	*	*	*	*	–
SUBL A, ear	2	5	0	long (A) ← (A) – (ear)	–	–	–	–	–	*	*	*	*	–
SUBL A, eam	2+	6+ (a)	(d)	long (A) ← (A) – (eam)	–	–	–	–	–	*	*	*	*	–
SUBL A, #imm32	5	4	0	long (A) ← (A) –imm32	–	–	–	–	–	*	*	*	*	–

For an explanation of “(a)”, “(b)”, “(c)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”