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Details

Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I ² C), SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f334-gmr

C8051F330/1/2/3/4/5

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory (kB)	RAM (bytes)	Calibrated Internal 24.5 MHz Oscillator	Internal 80 kHz Oscillator	SMBus/I ² C	Enhanced SPI	UART	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	10-bit 200kps ADC	10-bit Current Output DAC	Internal Voltage Reference	Temperature Sensor	Analog Comparator	Lead-free (RoHS Compliant)	Package
C8051F330-GM	25	8	768	✓	✓	✓	✓	✓	4	✓	17	✓	✓	✓	✓	✓	✓	QFN-20
C8051F331-GM	25	8	768	✓	✓	✓	✓	✓	4	✓	17	—	—	—	—	✓	✓	QFN-20
C8051F332-GM	25	4	768	✓	✓	✓	✓	✓	4	✓	17	✓	—	✓	✓	✓	✓	QFN-20
C8051F333-GM	25	4	768	✓	✓	✓	✓	✓	4	✓	17	—	—	—	—	✓	✓	QFN-20
C8051F334-GM	25	2	768	✓	✓	✓	✓	✓	4	✓	17	✓	—	✓	✓	✓	✓	QFN-20
C8051F335-GM	25	2	768	✓	✓	✓	✓	✓	4	✓	17	—	—	—	—	✓	✓	QFN-20

C8051F330/1/2/3/4/5

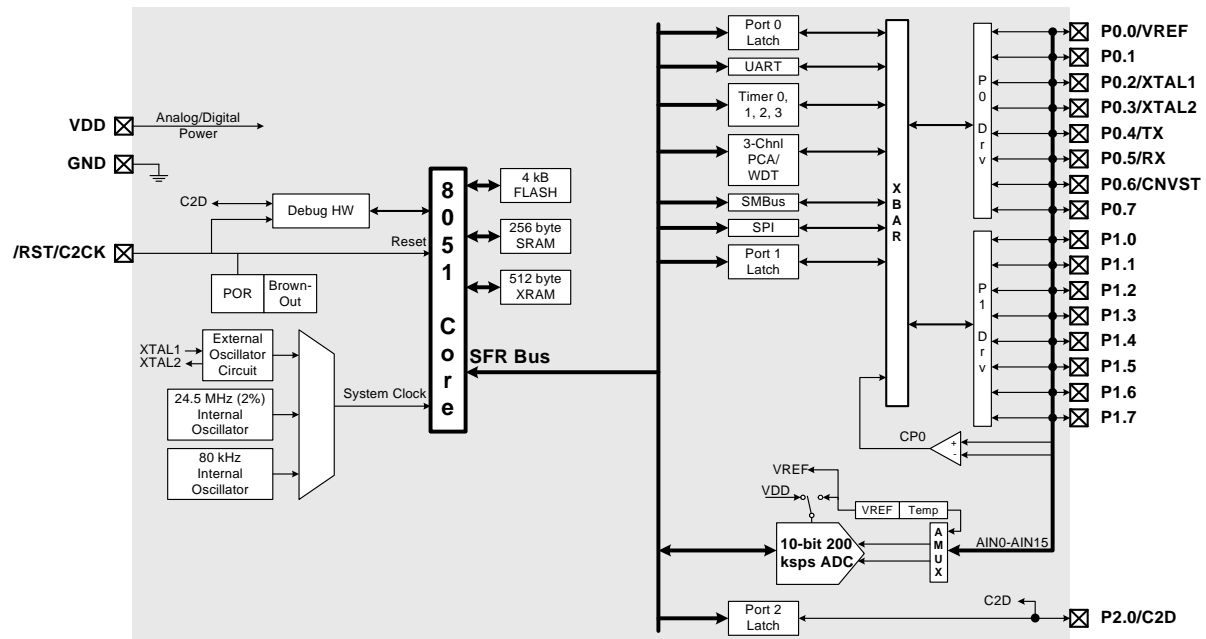


Figure 1.3. C8051F332 Block Diagram

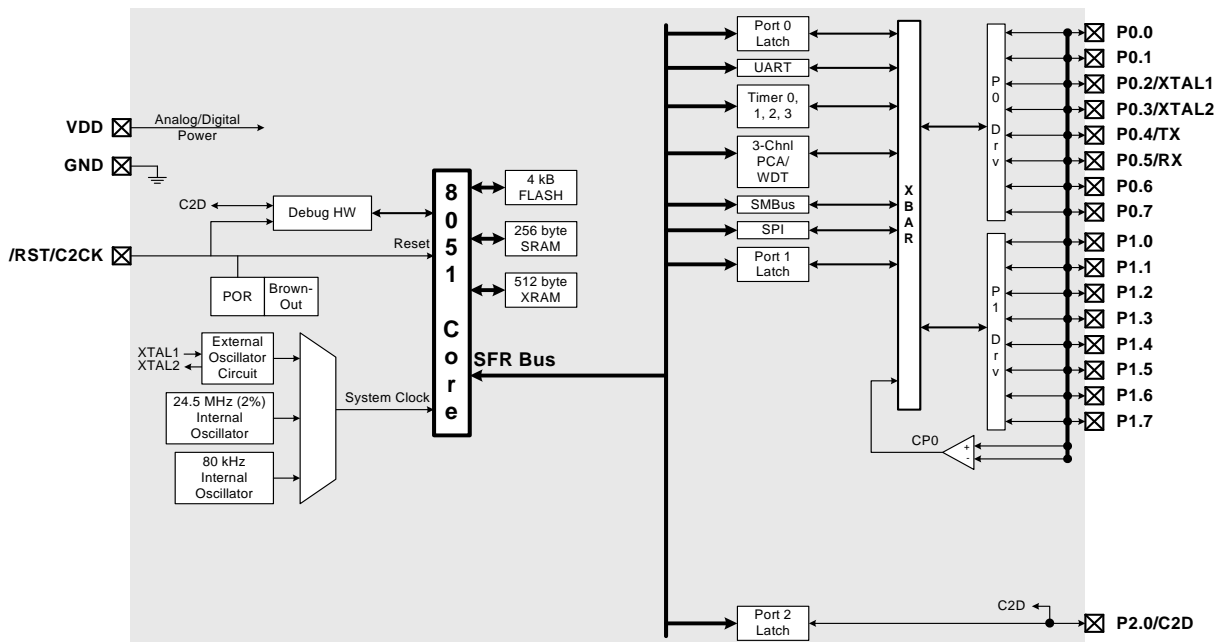


Figure 1.4. C8051F333 Block Diagram

C8051F330/1/2/3/4/5

1.4. Programmable Digital I/O and Crossbar

C8051F330/1/2/3/4/5 devices include 17 I/O pins (two byte-wide Ports and one 1-bit-wide Port). The C8051F330/1/2/3/4/5 Ports behave like typical 8051 Ports with a few enhancements. Each Port pin may be configured as an analog input or a digital I/O pin. Pins selected as digital I/Os may additionally be configured for push-pull or open-drain output. The “weak pullups” that are fixed on typical 8051 devices may be globally disabled, providing power savings capabilities.

The Digital Crossbar allows mapping of internal digital system resources to Port I/O pins. (See Figure 1.11.) On-chip counter/timers, serial buses, HW interrupts, comparator output, and other digital signals in the controller can be configured to appear on the Port I/O pins specified in the Crossbar Control registers. This allows the user to select the exact mix of general purpose Port I/O and digital resources needed for the particular application.

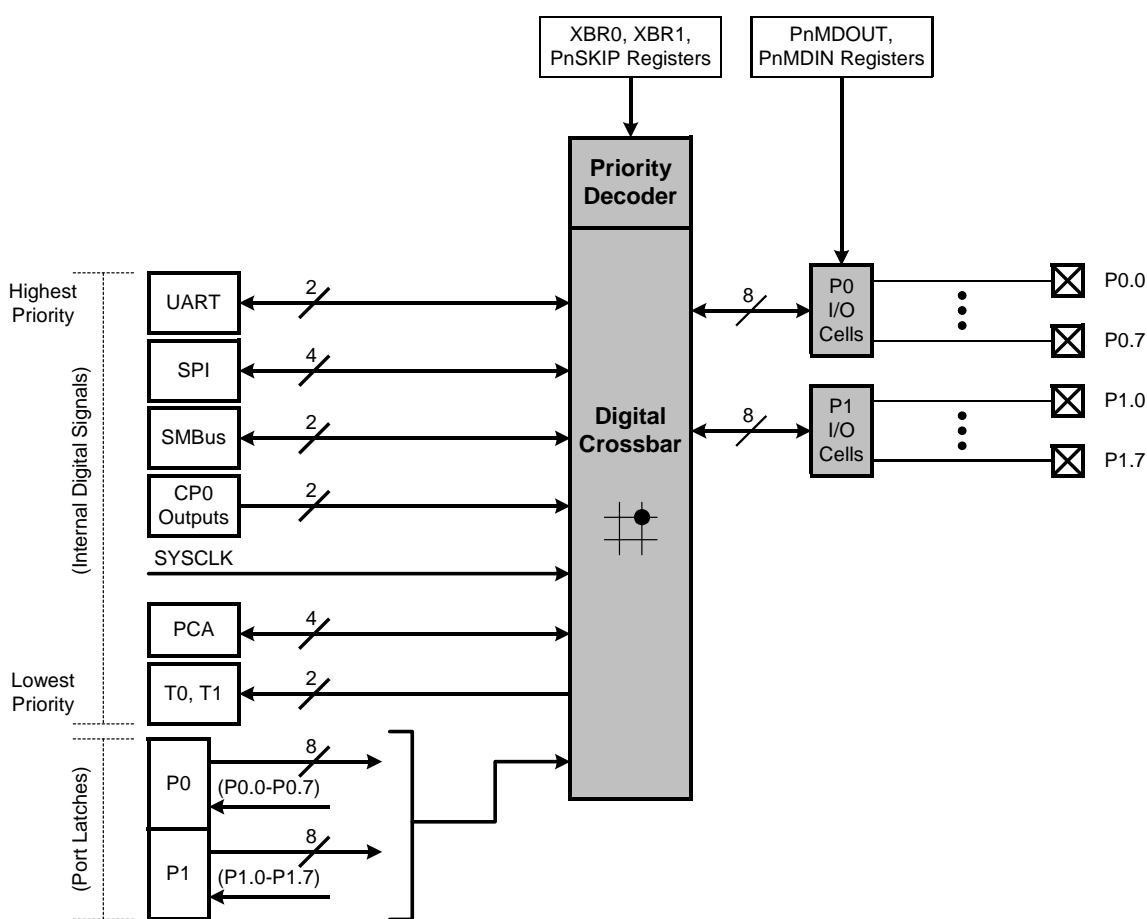


Figure 1.11. Digital Crossbar Diagram

1.5. Serial Ports

The C8051F330/1/2/3/4/5 Family includes an SMBus/I²C interface, a full-duplex UART with enhanced baud rate configuration, and an Enhanced SPI interface. Each of the serial buses is fully implemented in hardware and makes extensive use of the CIP-51's interrupts, thus requiring very little CPU intervention.

1.9. 10-bit Current Output DAC

The C8051F330 device includes a 10-bit current-mode Digital-to-Analog Converter (IDA0). The maximum current output of the IDA0 can be adjusted for three different current settings; 0.5 mA, 1 mA, and 2 mA. IDA0 features a flexible output update mechanism which allows for seamless full-scale changes and supports jitter-free updates for waveform generation. Three update modes are provided, allowing IDA0 output updates on a write to IDA0H, on a Timer overflow, or on an external pin edge.

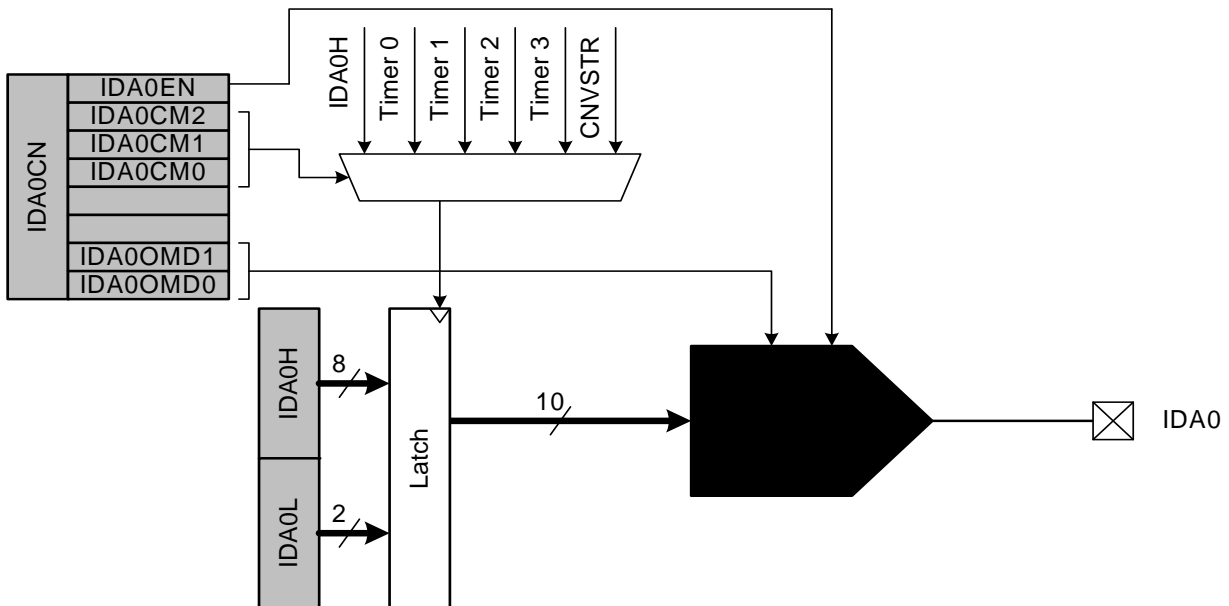


Figure 1.16. IDA0 Functional Block Diagram

C8051F330/1/2/3/4/5

3. Global Electrical Characteristics

Table 3.1. Global Electrical Characteristics

–40 to +85 °C, 25 MHz system clock unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Digital Supply Voltage		V_{RST}^1	3.0	3.6	V
Digital Supply RAM Data Retention Voltage		—	1.5	—	V
SYSCLK (System Clock) (Note 2)		0	—	25	MHz
T_{SYSH} (SYSCLK High Time)		18	—	—	ns
T_{SYSL} (SYSCLK Low Time)		18	—	—	ns
Specified Operating Temperature Range		–40	—	+85	°C
Digital Supply Current—CPU Active (Normal Mode, fetching instructions from Flash)					
I_{DD} (Note 3)	$V_{DD} = 3.6$ V, $F = 25$ MHz	—	10.7	11.7	mA
	$V_{DD} = 3.0$ V, $F = 25$ MHz	—	7.8	8.3	mA
	$V_{DD} = 3.0$ V, $F = 1$ MHz	—	0.38	—	mA
	$V_{DD} = 3.0$ V, $F = 80$ kHz	—	31	—	μA
I_{DD} Supply Sensitivity (Note 3)	$F = 25$ MHz	—	65	—	%/V
	$F = 1$ MHz	—	61	—	%/V
I_{DD} Frequency Sensitivity (Note 3, Note 4)	$V_{DD} = 3.0$ V, $F \leq 15$ MHz, $T = 25$ °C	—	0.38	—	mA/MHz
	$V_{DD} = 3.0$ V, $F > 15$ MHz, $T = 25$ °C	—	0.21	—	mA/MHz
	$V_{DD} = 3.6$ V, $F \leq 15$ MHz, $T = 25$ °C	—	0.53	—	mA/MHz
	$V_{DD} = 3.6$ V, $F > 15$ MHz, $T = 25$ °C	—	0.27	—	mA/MHz

Table 3.1. Global Electrical Characteristics

–40 to +85 °C, 25 MHz system clock unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Digital Supply Current—CPU Inactive (Idle Mode, not fetching instructions from Flash)					
I _{DD} (Note 3)	V _{DD} = 3.6 V, F = 25 MHz	—	4.8	5.2	mA
	V _{DD} = 3.0 V, F = 25 MHz	—	3.8	4.1	mA
	V _{DD} = 3.0 V, F = 1 MHz	—	0.20	—	mA
	V _{DD} = 3.0 V, F = 80 kHz	—	16	—	μA
I _{DD} Supply Sensitivity (Note 3)	F = 25 MHz	—	43	—	%/V
	F = 1 MHz	—	55	—	%/V
I _{DD} Frequency Sensitivity (Note 3, Note 5)	V _{DD} = 3.0 V, F ≤ 1 MHz, T = 25 °C	—	0.20	—	mA/MHz
	V _{DD} = 3.0 V, F > 1 MHz, T = 25 °C	—	0.15	—	mA/MHz
	V _{DD} = 3.6 V, F ≤ 1 MHz, T = 25 °C	—	0.24	—	mA/MHz
	V _{DD} = 3.6 V, F > 1 MHz, T = 25 °C	—	0.19	—	mA/MHz
Digital Supply Current (Stop Mode, shutdown)	Oscillator not running, V _{DD} Monitor Disabled	—	< 0.1	—	μA
Notes: <ol style="list-style-type: none"> Given in Table 10.1 on page 102. SYSCLK must be at least 32 kHz to enable debugging. Based on device characterization data; Not production tested. ID_{DD} can be estimated for frequencies ≤ 15 MHz by simply multiplying the frequency of interest by the frequency sensitivity number for that range. When using these numbers to estimate I_{DD} for >15 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 3.0 V; F = 20 MHz, I_{DD} = 7.8 mA - (25 MHz - 20 MHz) * 0.21 mA/MHz = 6.75 mA. Idle ID_{DD} can be estimated for frequencies ≤ 1 MHz by simply multiplying the frequency of interest by the frequency sensitivity number for that range. When using these numbers to estimate Idle I_{DD} for >1 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 3.0 V; F = 5 MHz, Idle I_{DD} = 4.8 mA - (25 MHz - 5 MHz) * 0.15 mA/MHz = 1.8 mA. 					

Other electrical characteristics tables are found in the data sheet section corresponding to the associated peripherals. For more information on electrical characteristics for a specific peripheral, refer to the page indicated in Table 3.2.

SFR Definition 5.6. ADC0CN: ADC0 Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
AD0EN	AD0TM	AD0INT	AD0BUSY	AD0WINT	AD0CM2	AD0CM1	AD0CM0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xE8
						(bit addressable)		
Bit7:	AD0EN: ADC0 Enable Bit. 0: ADC0 Disabled. ADC0 is in low-power shutdown. 1: ADC0 Enabled. ADC0 is active and ready for data conversions.							
Bit6:	AD0TM: ADC0 Track Mode Bit. 0: Normal Track Mode: When ADC0 is enabled, tracking is continuous unless a conversion is in progress. 1: Low-power Track Mode: Tracking Defined by AD0CM2–0 bits (see below).							
Bit5:	AD0INT: ADC0 Conversion Complete Interrupt Flag. 0: ADC0 has not completed a data conversion since the last time AD0INT was cleared. 1: ADC0 has completed a data conversion.							
Bit4:	AD0BUSY: ADC0 Busy Bit. Read: 0: ADC0 conversion is complete or a conversion is not currently in progress. AD0INT is set to logic 1 on the falling edge of AD0BUSY. 1: ADC0 conversion is in progress. Write: 0: No Effect. 1: Initiates ADC0 Conversion if AD0CM2–0 = 000b							
Bit3:	AD0WINT: ADC0 Window Compare Interrupt Flag. 0: ADC0 Window Comparison Data match has not occurred since this flag was last cleared. 1: ADC0 Window Comparison Data match has occurred.							
Bits2–0:	AD0CM2–0: ADC0 Start of Conversion Mode Select. When AD0TM = 0: 000: ADC0 conversion initiated on every write of '1' to AD0BUSY. 001: ADC0 conversion initiated on overflow of Timer 0. 010: ADC0 conversion initiated on overflow of Timer 2. 011: ADC0 conversion initiated on overflow of Timer 1. 100: ADC0 conversion initiated on rising edge of external CNVSTR. 101: ADC0 conversion initiated on overflow of Timer 3. 11x: Reserved. When AD0TM = 1: 000: Tracking initiated on write of '1' to AD0BUSY and lasts 3 SAR clocks, followed by conversion. 001: Tracking initiated on overflow of Timer 0 and lasts 3 SAR clocks, followed by conversion. 010: Tracking initiated on overflow of Timer 2 and lasts 3 SAR clocks, followed by conversion. 011: Tracking initiated on overflow of Timer 1 and lasts 3 SAR clocks, followed by conversion. 100: ADC0 tracks only when CNVSTR input is logic low; conversion starts on rising CNVSTR edge. 101: Tracking initiated on overflow of Timer 3 and lasts 3 SAR clocks, followed by conversion. 11x: Reserved.							

6. 10-Bit Current Mode DAC (IDA0, C8051F330 only)

The C8051F330 device includes a 10-bit current-mode Digital-to-Analog Converter (IDAC). The maximum current output of the IDAC can be adjusted for three different current settings; 0.5 mA, 1 mA, and 2 mA. The IDAC is enabled or disabled with the IDA0EN bit in the IDA0 Control Register (see SFR Definition 6.1). When IDA0EN is set to '0', the IDAC port pin (P0.1) behaves as a normal GPIO pin. When IDA0EN is set to '1', the digital output drivers and weak pullup for the IDAC pin are automatically disabled, and the pin is connected to the IDAC output. An internal bandgap bias generator is used to generate a reference current for the IDAC whenever it is enabled. When using the IDAC, bit 1 in the P0SKIP register should be set to '1', to force the Crossbar to skip the IDAC pin.

6.1. IDA0 Output Scheduling

IDA0 features a flexible output update mechanism which allows for seamless full-scale changes and supports jitter-free updates for waveform generation. Three update modes are provided, allowing IDAC output updates on a write to IDA0H, on a Timer overflow, or on an external pin edge.

6.1.1. Update Output On-Demand

In its default mode (IDA0CN.[6:4] = '111') the IDA0 output is updated “on-demand” on a write to the high-byte of the IDA0 data register (IDA0H). It is important to note that writes to IDA0L are held in this mode, and have no effect on the IDA0 output until a write to IDA0H takes place. If writing a full 10-bit word to the IDAC data registers, the 10-bit data word is written to the low byte (IDA0L) and high byte (IDA0H) data registers. Data is latched into IDA0 after a write to the IDA0H register, **so the write sequence should be IDA0L followed by IDA0H** if the full 10-bit resolution is required. The IDAC can be used in 8-bit mode by initializing IDA0L to the desired value (typically 0x00), and writing data to only IDA0H (see **Section 6.2** for information on the format of the 10-bit IDAC data word within the 16-bit SFR space).

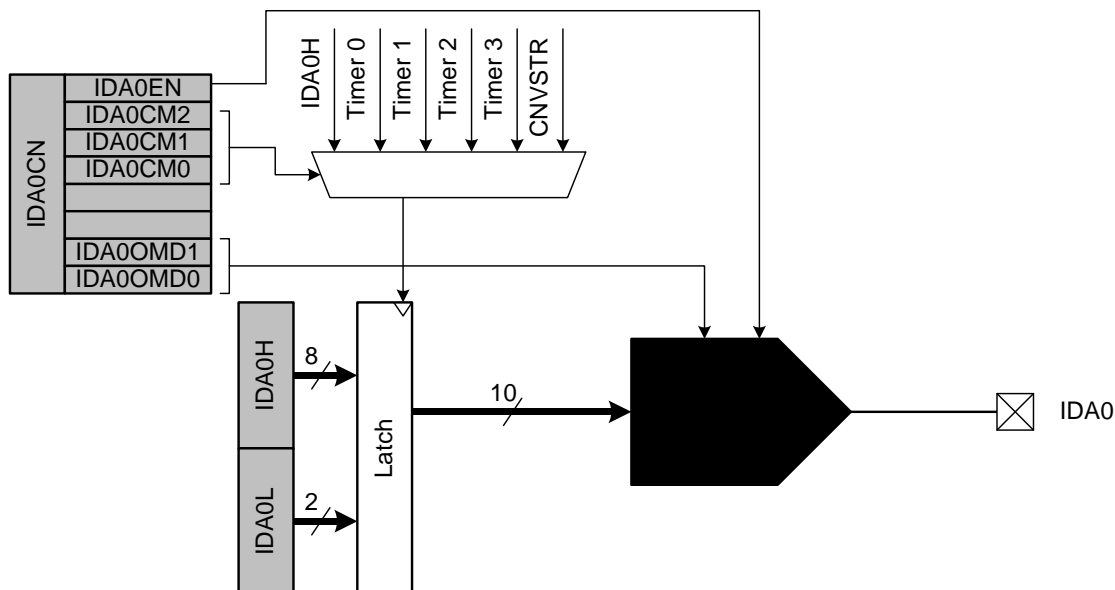


Figure 6.1. IDA0 Functional Block Diagram

9.2.2. Data Memory

The CIP-51 includes 256 bytes of internal RAM mapped into the data memory space from 0x00 through 0xFF. The lower 128 bytes of data memory are used for general purpose registers and scratch pad memory. Either direct or indirect addressing may be used to access the lower 128 bytes of data memory. Locations 0x00 through 0x1F are addressable as four banks of general purpose registers, each bank consisting of eight byte-wide registers. The next 16 bytes, locations 0x20 through 0x2F, may either be addressed as bytes or as 128 bit locations accessible with the direct addressing mode.

The upper 128 bytes of data memory are accessible only by indirect addressing. This region occupies the same address space as the Special Function Registers (SFR) but is physically separate from the SFR space. The addressing mode used by an instruction when accessing locations above 0x7F determines whether the CPU accesses the upper 128 bytes of data memory space or the SFRs. Instructions that use direct addressing will access the SFR space. Instructions using indirect addressing above 0x7F access the upper 128 bytes of data memory. Figure 9.2 illustrates the data memory organization of the CIP-51.

9.2.3. General Purpose Registers

The lower 32 bytes of data memory, locations 0x00 through 0x1F, may be addressed as four banks of general-purpose registers. Each bank consists of eight byte-wide registers designated R0 through R7. Only one of these banks may be enabled at a time. Two bits in the program status word, RS0 (PSW.3) and RS1 (PSW.4), select the active register bank (see description of the PSW in SFR Definition 9.4). This allows fast context switching when entering subroutines and interrupt service routines. Indirect addressing modes use registers R0 and R1 as index registers.

9.2.4. Bit Addressable Locations

In addition to direct access to data memory organized as bytes, the sixteen data memory locations at 0x20 through 0x2F are also accessible as 128 individually addressable bits. Each bit has a bit address from 0x00 to 0x7F. Bit 0 of the byte at 0x20 has bit address 0x00 while bit7 of the byte at 0x20 has bit address 0x07. Bit 7 of the byte at 0x2F has bit address 0x7F. A bit access is distinguished from a full byte access by the type of instruction used (bit source or destination operands as opposed to a byte source or destination).

The MCS-51™ assembly language allows an alternate notation for bit addressing of the form XX.B where XX is the byte address and B is the bit position within the byte. For example, the instruction:

```
MOV     C, 22.3h
```

moves the Boolean value at 0x13 (bit 3 of the byte at location 0x22) into the Carry flag.

9.2.5. Stack

A programmer's stack can be located anywhere in the 256-byte data memory. The stack area is designated using the Stack Pointer (SP, 0x81) SFR. The SP will point to the last location used. The next value pushed on the stack is placed at SP+1 and then SP is incremented. A reset initializes the stack pointer to location 0x07. Therefore, the first value pushed on the stack is placed at location 0x08, which is also the first register (R0) of register bank 1. Thus, if more than one register bank is to be used, the SP should be initialized to a location in the data memory not being used for data storage. The stack depth can extend up to 256 bytes.

Table 9.3. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Description	Page
OSCXCN	0xB1	External Oscillator Control	117
P0	0x80	Port 0 Latch	130
P0MDIN	0xF1	Port 0 Input Mode Configuration	130
P0MDOUT	0xA4	Port 0 Output Mode Configuration	131
P0SKIP	0xD4	Port 0 Skip	131
P1	0x90	Port 1 Latch	131
P1MDIN	0xF2	Port 1 Input Mode Configuration	132
P1MDOUT	0xA5	Port 1 Output Mode Configuration	132
P1SKIP	0xD5	Port 1 Skip	132
P2	0xA0	Port 2 Latch	133
P2MDOUT	0xA6	Port 2 Output Mode Configuration	133
PCA0CN	0xD8	PCA Control	205
PCA0CPH0	0xFC	PCA Capture 0 High	208
PCA0CPH1	0xEA	PCA Capture 1 High	208
PCA0CPH2	0xEC	PCA Capture 2 High	208
PCA0CPL0	0xFB	PCA Capture 0 Low	208
PCA0CPL1	0xE9	PCA Capture 1 Low	208
PCA0CPL2	0xEB	PCA Capture 2 Low	208
PCA0CPM0	0xDA	PCA Module 0 Mode Register	207
PCA0CPM1	0xDB	PCA Module 1 Mode Register	207
PCA0CPM2	0xDC	PCA Module 2 Mode Register	207
PCA0H	0xFA	PCA Counter High	208
PCA0L	0xF9	PCA Counter Low	208
PCA0MD	0xD9	PCA Mode	206
PCON	0x87	Power Control	95
PSCTL	0x8F	Program Store R/W Control	108
PSW	0xD0	Program Status Word	84
REF0CN	0xD1	Voltage Reference Control	62
RSTSRC	0xEF	Reset Source Configuration/Status	101
SBUF0	0x99	UART0 Data Buffer	159
SCON0	0x98	UART0 Control	158
SMB0CF	0xC1	SMBus Configuration	142
SMB0CN	0xC0	SMBus Control	144
SMB0DAT	0xC2	SMBus Data	146

SFR Definition 9.9. EIE1: Extended Interrupt Enable 1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
ET3	Reserved	ECP0	EPCA0	EADC0	EWADC0	Reserved	ESMB0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xE6

Bit7: ET3: Enable Timer 3 Interrupt.
This bit sets the masking of the Timer 3 interrupt.
0: Disable Timer 3 interrupts.
1: Enable interrupt requests generated by the TF3L or TF3H flags.

Bit6: RESERVED. Read = 0. Must Write 0.

Bit5: ECP0: Enable Comparator0 (CP0) Interrupt.
This bit sets the masking of the CP0 interrupt.
0: Disable CP0 interrupts.
1: Enable interrupt requests generated by the CP0RIF or CP0FIF flags.

Bit4: EPCA0: Enable Programmable Counter Array (PCA0) Interrupt.
This bit sets the masking of the PCA0 interrupts.
0: Disable all PCA0 interrupts.
1: Enable interrupt requests generated by PCA0.

Bit3: EADC0: Enable ADC0 Conversion Complete Interrupt.
This bit sets the masking of the ADC0 Conversion Complete interrupt.
0: Disable ADC0 Conversion Complete interrupt.
1: Enable interrupt requests generated by the AD0INT flag.

Bit2: EWADC0: Enable Window Comparison ADC0 Interrupt.
This bit sets the masking of ADC0 Window Comparison interrupt.
0: Disable ADC0 Window Comparison interrupt.
1: Enable interrupt requests generated by ADC0 Window Compare flag (AD0WINT).

Bit1: RESERVED. Read = 0. Must Write 0.

Bit0: ESMB0: Enable SMBus (SMB0) Interrupt.
This bit sets the masking of the SMB0 interrupt.
0: Disable all SMB0 interrupts.
1: Enable interrupt requests generated by SMB0.

SFR Definition 9.11. IT01CF: INT0/INT1 Configuration

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
IN1PL	IN1SL2	IN1SL1	IN1SL0	IN0PL	IN0SL2	IN0SL1	IN0SL0	00000001
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xE4

***Note:** Refer to SFR Definition 18.1 for INT0/1 edge- or level-sensitive interrupt selection.

Bit7: IN1PL: /INT1 Polarity
 0: /INT1 input is active low.
 1: /INT1 input is active high.

Bits6–4: IN1SL2–0: /INT1 Port Pin Selection Bits

These bits select which Port pin is assigned to /INT1. Note that this pin assignment is independent of the Crossbar; /INT1 will monitor the assigned Port pin without disturbing the peripheral that has been assigned the Port pin via the Crossbar. The Crossbar will not assign the Port pin to a peripheral if it is configured to skip the selected pin (accomplished by setting to '1' the corresponding bit in register P0SKIP).

IN1SL2–0	/INT1 Port Pin
000	P0.0
001	P0.1
010	P0.2
011	P0.3
100	P0.4
101	P0.5
110	P0.6
111	P0.7

Bit3: IN0PL: /INT0 Polarity
 0: /INT0 interrupt is active low.
 1: /INT0 interrupt is active high.

Bits2–0: IN0SL2–0: /INT0 Port Pin Selection Bits

These bits select which Port pin is assigned to /INT0. Note that this pin assignment is independent of the Crossbar; /INT0 will monitor the assigned Port pin without disturbing the peripheral that has been assigned the Port pin via the Crossbar. The Crossbar will not assign the Port pin to a peripheral if it is configured to skip the selected pin (accomplished by setting to '1' the corresponding bit in register P0SKIP).

IN0SL2–0	/INT0 Port Pin
000	P0.0
001	P0.1
010	P0.2
011	P0.3
100	P0.4
101	P0.5
110	P0.6
111	P0.7

The capacitors shown in the external crystal configuration provide the load capacitance required by the crystal for correct oscillation. These capacitors are "in series" as seen by the crystal and "in parallel" with the stray capacitance of the XTAL1 and XTAL2 pins.

Note: The desired load capacitance depends upon the crystal and the manufacturer. Please refer to the crystal data sheet when completing these calculations.

For example, a tuning-fork crystal of 32.768 kHz with a recommended load capacitance of 12.5 pF should use the configuration shown in Figure 13.1, Option 1. The total value of the capacitors and the stray capacitance of the XTAL pins should equal 25 pF. With a stray capacitance of 3 pF per pin, the 22 pF capacitors yield an equivalent capacitance of 12.5 pF across the crystal, as shown in Figure 13.2.

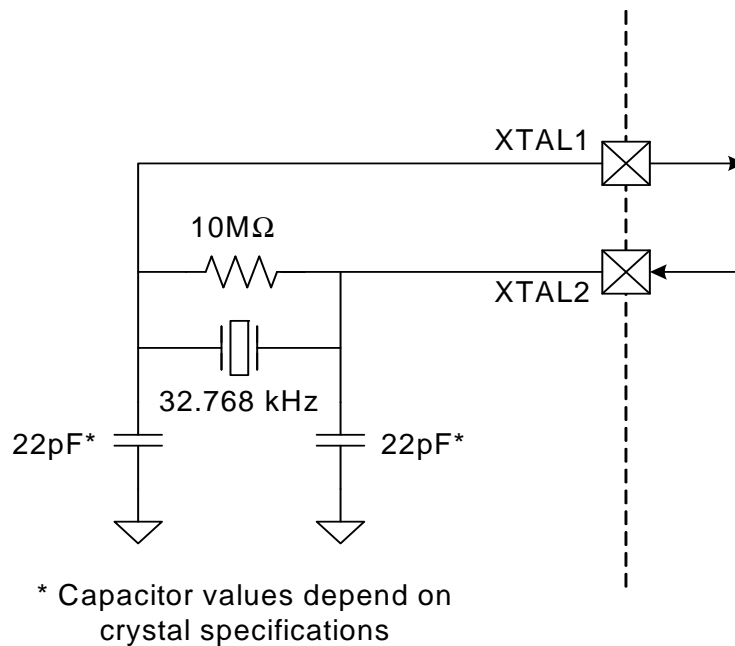


Figure 13.2. External 32.768 kHz Quartz Crystal Oscillator Connection Diagram

13.3.2. External RC Example

If an RC network is used as an external oscillator source for the MCU, the circuit should be configured as shown in Figure 13.1, Option 2. The capacitor should be no greater than 100 pF; however for very small capacitors, the total capacitance may be dominated by parasitic capacitance in the PCB layout. To determine the required External Oscillator Frequency Control value (XFCN) in the OSCXCN Register, first select the RC network value to produce the desired frequency of oscillation. If the frequency desired is 100 kHz, let $R = 246 \text{ k}\Omega$ and $C = 50 \text{ pF}$:

$$f = 1.23(10^3) / RC = 1.23(10^3) / [246 \times 50] = 0.1 \text{ MHz} = 100 \text{ kHz}$$

Referring to the table in SFR Definition 13.4, the required XFCN setting is 010b.

13.3.3. External Capacitor Example

If a capacitor is used as an external oscillator for the MCU, the circuit should be configured as shown in Figure 13.1, Option 3. The capacitor should be no greater than 100 pF; however for very small capacitors, the total capacitance may be dominated by parasitic capacitance in the PCB layout. To determine the required External Oscillator Frequency Control value (XFCN) in the OSCXCN Register, select the capacitor to be used and find the frequency of oscillation from the equations below. Assume $V_{DD} = 3.0 \text{ V}$ and $f = 150 \text{ kHz}$:

$$f = KF / (C \times V_{DD})$$
$$0.150 \text{ MHz} = KF / (C \times 3.0)$$

Since the frequency of roughly 150 kHz is desired, select the K Factor from the table in SFR Definition 13.4 (OSCXCN) as $KF = 22$:

$$0.150 \text{ MHz} = 22 / (C \times 3.0)$$
$$C \times 3.0 = 22 / 0.150 \text{ MHz}$$
$$C = 146.6 / 3.0 \text{ pF} = 48.8 \text{ pF}$$

Therefore, the XFCN value to use in this example is 011b and $C = 50 \text{ pF}$.

SFR Definition 15.1. SMB0CF: SMBus Clock/Configuration

R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	Reset Value
ENSMB	INH	BUSY	EXTHOLD	SMBTOE	SMBFTE	SMBCS1	SMBCS0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xC1

- Bit7:** ENSMB: SMBus Enable.
This bit enables/disables the SMBus interface. When enabled, the interface constantly monitors the SDA and SCL pins.
0: SMBus interface disabled.
1: SMBus interface enabled.
- Bit6:** INH: SMBus Slave Inhibit.
When this bit is set to logic 1, the SMBus does not generate an interrupt when slave events occur. This effectively removes the SMBus slave from the bus. Master Mode interrupts are not affected.
0: SMBus Slave Mode enabled.
1: SMBus Slave Mode inhibited.
- Bit5:** BUSY: SMBus Busy Indicator.
This bit is set to logic 1 by hardware when a transfer is in progress. It is cleared to logic 0 when a STOP or free-timeout is sensed.
- Bit4:** EXTHOLD: SMBus Setup and Hold Time Extension Enable.
This bit controls the SDA setup and hold times according to .
0: SDA Extended Setup and Hold Times disabled.
1: SDA Extended Setup and Hold Times enabled.
- Bit3:** SMBTOE: SMBus SCL Timeout Detection Enable.
This bit enables SCL low timeout detection. If set to logic 1, the SMBus forces Timer 3 to reload while SCL is high and allows Timer 3 to count when SCL goes low. If Timer 3 is configured to Split Mode, only the High Byte of the timer is held in reload while SCL is high. Timer 3 should be programmed to generate interrupts at 25 ms, and the Timer 3 interrupt service routine should reset SMBus communication.
- Bit2:** SMBFTE: SMBus Free Timeout Detection Enable.
When this bit is set to logic 1, the bus will be considered free if SCL and SDA remain high for more than 10 SMBus clock source periods.
- Bits1–0:** SMBCS1–SMBCS0: SMBus Clock Source Selection.
These two bits select the SMBus clock source, which is used to generate the SMBus bit rate. The selected device should be configured according to Equation 15.1.

SMBCS1	SMBCS0	SMBus Clock Source
0	0	Timer 0 Overflow
0	1	Timer 1 Overflow
1	0	Timer 2 High Byte Overflow
1	1	Timer 2 Low Byte Overflow

16.1. Enhanced Baud Rate Generation

The UART0 baud rate is generated by Timer 1 in 8-bit auto-reload mode. The TX clock is generated by TL1; the RX clock is generated by a copy of TL1 (shown as RX Timer in Figure 16.2), which is not user-accessible. Both TX and RX Timer overflows are divided by two to generate the TX and RX baud rates. The RX Timer runs when Timer 1 is enabled, and uses the same reload value (TH1). However, an RX Timer reload is forced when a START condition is detected on the RX pin. This allows a receive to begin any time a START is detected, independent of the TX Timer state.

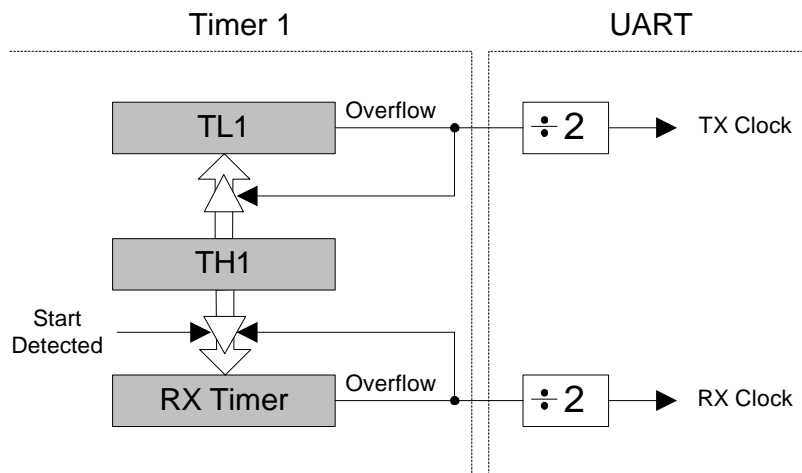


Figure 16.2. UART0 Baud Rate Logic

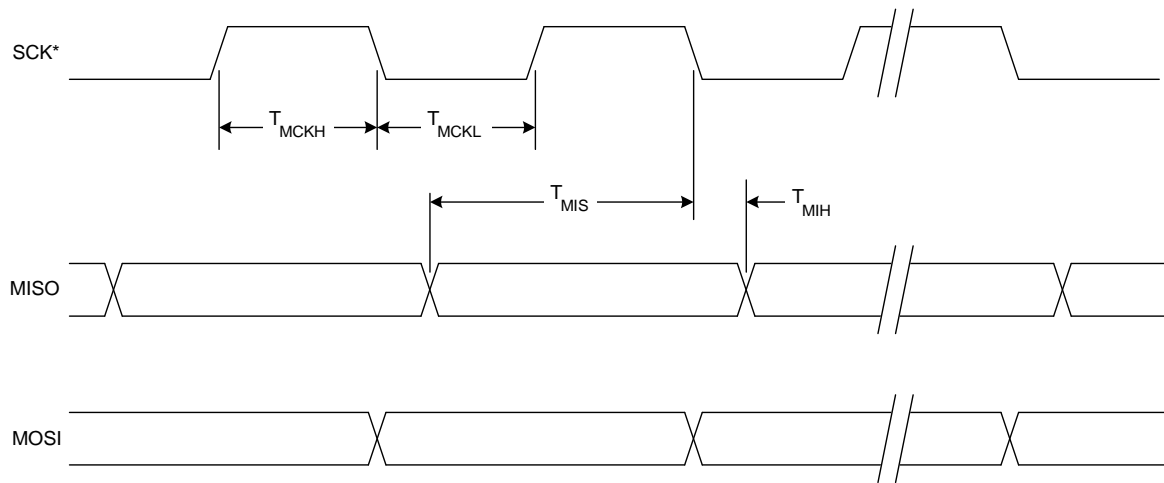
Timer 1 should be configured for Mode 2, 8-bit auto-reload (see **Section “18.1.3. Mode 2: 8-bit Counter/Timer with Auto-Reload” on page 179**). The Timer 1 reload value should be set so that overflows will occur at two times the desired UART baud rate frequency. Note that Timer 1 may be clocked by one of six sources: SYSCLK, SYSCLK / 4, SYSCLK / 12, SYSCLK / 48, the external oscillator clock / 8, or an external input T1. For any given Timer 1 clock source, the UART0 baud rate is determined by Equation 16.1-A and Equation 16.1-B.

$$\text{A) } \text{UartBaudRate} = \frac{1}{2} \times \text{T1_Overflow_Rate}$$

$$\text{B) } \text{T1_Overflow_Rate} = \frac{T1_{CLK}}{256 - TH1}$$

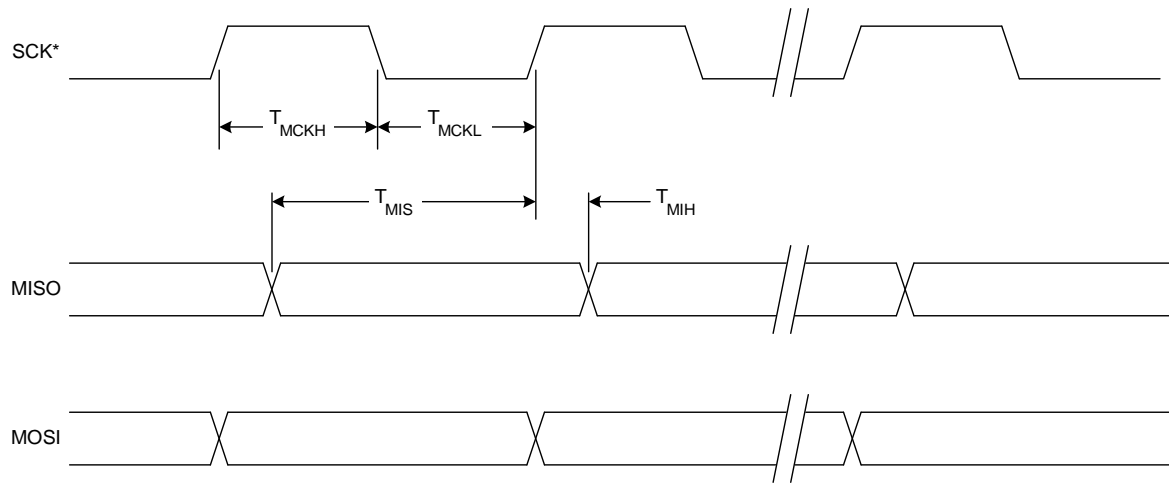
Equation 16.1. UART0 Baud Rate

Where $T1_{CLK}$ is the frequency of the clock supplied to Timer 1, and $T1H$ is the high byte of Timer 1 (reload value). Timer 1 clock frequency is selected as described in **Section “18. Timers” on page 177**. A quick reference for typical baud rates and system clock frequencies is given in Table 16.1 through Table 16.6. Note that the internal oscillator may still generate the system clock when the external oscillator is driving Timer 1.



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 17.8. SPI Master Timing (CKPHA = 0)



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 17.9. SPI Master Timing (CKPHA = 1)

SFR Definition 18.1. TCON: Timer Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
						(bit addressable)		0x88
Bit7:	<p>TF1: Timer 1 Overflow Flag. Set by hardware when Timer 1 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine. 0: No Timer 1 overflow detected. 1: Timer 1 has overflowed.</p>							
Bit6:	<p>TR1: Timer 1 Run Control. 0: Timer 1 disabled. 1: Timer 1 enabled.</p>							
Bit5:	<p>TF0: Timer 0 Overflow Flag. Set by hardware when Timer 0 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine. 0: No Timer 0 overflow detected. 1: Timer 0 has overflowed.</p>							
Bit4:	<p>TR0: Timer 0 Run Control. 0: Timer 0 disabled. 1: Timer 0 enabled.</p>							
Bit3:	<p>IE1: External Interrupt 1. This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 1 service routine if IT1 = 1. When IT1 = 0, this flag is set to '1' when /INT1 is active as defined by bit IN1PL in register IT01CF (see SFR Definition 9.11).</p>							
Bit2:	<p>IT1: Interrupt 1 Type Select. This bit selects whether the configured /INT1 interrupt will be edge or level sensitive. /INT1 is configured active low or high by the IN1PL bit in the IT01CF register (see SFR Definition 9.11). 0: /INT1 is level triggered. 1: /INT1 is edge triggered.</p>							
Bit1:	<p>IE0: External Interrupt 0. This flag is set by hardware when an edge/level of type defined by IT0 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 0 service routine if IT0 = 1. When IT0 = 0, this flag is set to '1' when /INT0 is active as defined by bit IN0PL in register IT01CF (see SFR Definition 9.11).</p>							
Bit0:	<p>IT0: Interrupt 0 Type Select. This bit selects whether the configured /INT0 interrupt will be edge or level sensitive. /INT0 is configured active low or high by the IN0PL bit in register IT01CF (see SFR Definition 9.11). 0: /INT0 is level triggered. 1: /INT0 is edge triggered.</p>							

SFR Definition 18.13. TMR3CN: Timer 3 Control

R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	Reset Value
TF3H	TF3L	TF3LEN	TF3CEN	T3SPLIT	TR3	—	T3XCLK	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x91
Bit7:	<p>TF3H: Timer 3 High Byte Overflow Flag. Set by hardware when the Timer 3 high byte overflows from 0xFF to 0x00. In 16 bit mode, this will occur when Timer 3 overflows from 0xFFFF to 0x0000. When the Timer 3 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 3 interrupt service routine. TF3H is not automatically cleared by hardware and must be cleared by software.</p>							
Bit6:	<p>TF3L: Timer 3 Low Byte Overflow Flag. Set by hardware when the Timer 3 low byte overflows from 0xFF to 0x00. When this bit is set, an interrupt will be generated if TF3LEN is set and Timer 3 interrupts are enabled. TF3L will set when the low byte overflows regardless of the Timer 3 mode. This bit is not automatically cleared by hardware.</p>							
Bit5:	<p>TF3LEN: Timer 3 Low Byte Interrupt Enable. This bit enables/disables Timer 3 Low Byte interrupts. If TF3LEN is set and Timer 3 interrupts are enabled, an interrupt will be generated when the low byte of Timer 3 overflows. 0: Timer 3 Low Byte interrupts disabled. 1: Timer 3 Low Byte interrupts enabled.</p>							
Bit4:	<p>TF3CEN: Timer 3 Low-Frequency Oscillator Capture Enable. This bit enables/disables Timer 3 Low-Frequency Oscillator Capture Mode. If TF3CEN is set and Timer 3 interrupts are enabled, an interrupt will be generated on a rising edge of the low-frequency oscillator output, and the current 16-bit timer value in TMR3H:TMR3L will be copied to TMR3RLH:TMR3RLL. See Section “13. Oscillators” on page 113 for more details. 0: Timer 3 Low-Frequency Oscillator Capture disabled. 1: Timer 3 Low-Frequency Oscillator Capture enabled.</p>							
Bit3:	<p>T3SPLIT: Timer 3 Split Mode Enable. When this bit is set, Timer 3 operates as two 8-bit timers with auto-reload. 0: Timer 3 operates in 16-bit auto-reload mode. 1: Timer 3 operates as two 8-bit auto-reload timers.</p>							
Bit2:	<p>TR3: Timer 3 Run Control. This bit enables/disables Timer 3. In 8-bit mode, this bit enables/disables TMR3H only; TMR3L is always enabled in this mode. 0: Timer 3 disabled. 1: Timer 3 enabled.</p>							
Bit1:	<p>UNUSED. Read = 0b. Write = don't care.</p>							
Bit0:	<p>T3XCLK: Timer 3 External Clock Select. This bit selects the external clock source for Timer 3. If Timer 3 is in 8-bit mode, this bit selects the external oscillator clock source for both timer bytes. However, the Timer 3 Clock Select bits (T3MH and T3ML in register CKCON) may still be used to select between the external clock and the system clock for either timer. 0: Timer 3 external clock selection is the system clock divided by 12. 1: Timer 3 external clock selection is the external clock divided by 8. Note that the external oscillator source divided by 8 is synchronized with the system clock.</p>							

20.2. C2 Pin Sharing

The C2 protocol allows the C2 pins to be shared with user functions so that in-system debugging and Flash programming may be performed. This is possible because C2 communication is typically performed when the device is in the halt state, where all on-chip peripherals and user software are stalled. In this halted state, the C2 interface can safely 'borrow' the C2CK ($\overline{\text{RST}}$) and C2D (P2.0) pins. In most applications, external resistors are required to isolate C2 interface traffic from the user application. A typical isolation configuration is shown in Figure 20.1.

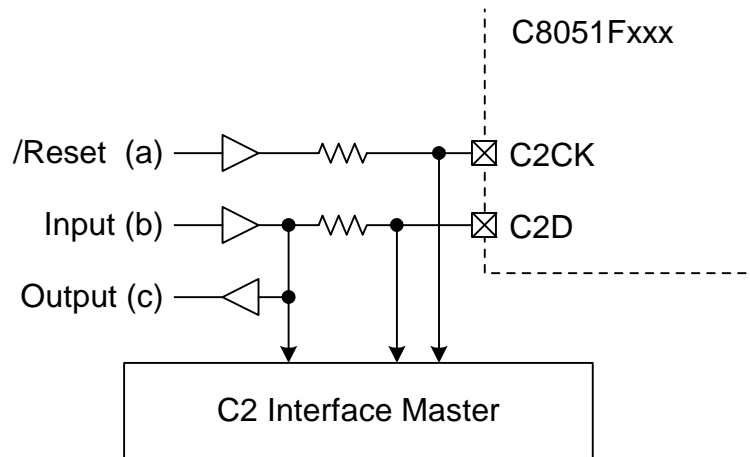


Figure 20.1. Typical C2 Pin Sharing

The configuration in Figure 20.1 assumes the following:

1. The user input (b) cannot change state while the target device is halted.
2. The $\overline{\text{RST}}$ pin on the target device is used as an input only.

Additional resistors may be necessary depending on the specific application.