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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XA
Core Size	16-Bit
Speed	30MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	DMA, WDT
Number of I/O	33
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/pxah40kfbe-557

DESCRIPTION

The powerful 16-bit XA CPU core and rich feature set make the XA-H3 and XA-H4 devices ideal for high-performance real-time applications such as industrial control and networking. By supporting of up to 32 MB of external memory, these devices provide a low-cost solution to embedded applications of any complexity. Features like DMA, memory controller and four advanced USARTs help solve I/O intensive tasks with a minimum of CPU load.

The XA-H3 feature set is a subset of the XA-H4 (see Table 1). The XA-H3/H4 devices are members of the Philips XA (eXtended Architecture) family of high performance 16-bit microcontrollers.

The XA-H3 and XA-H4 are designed to significantly minimize the need for external components.

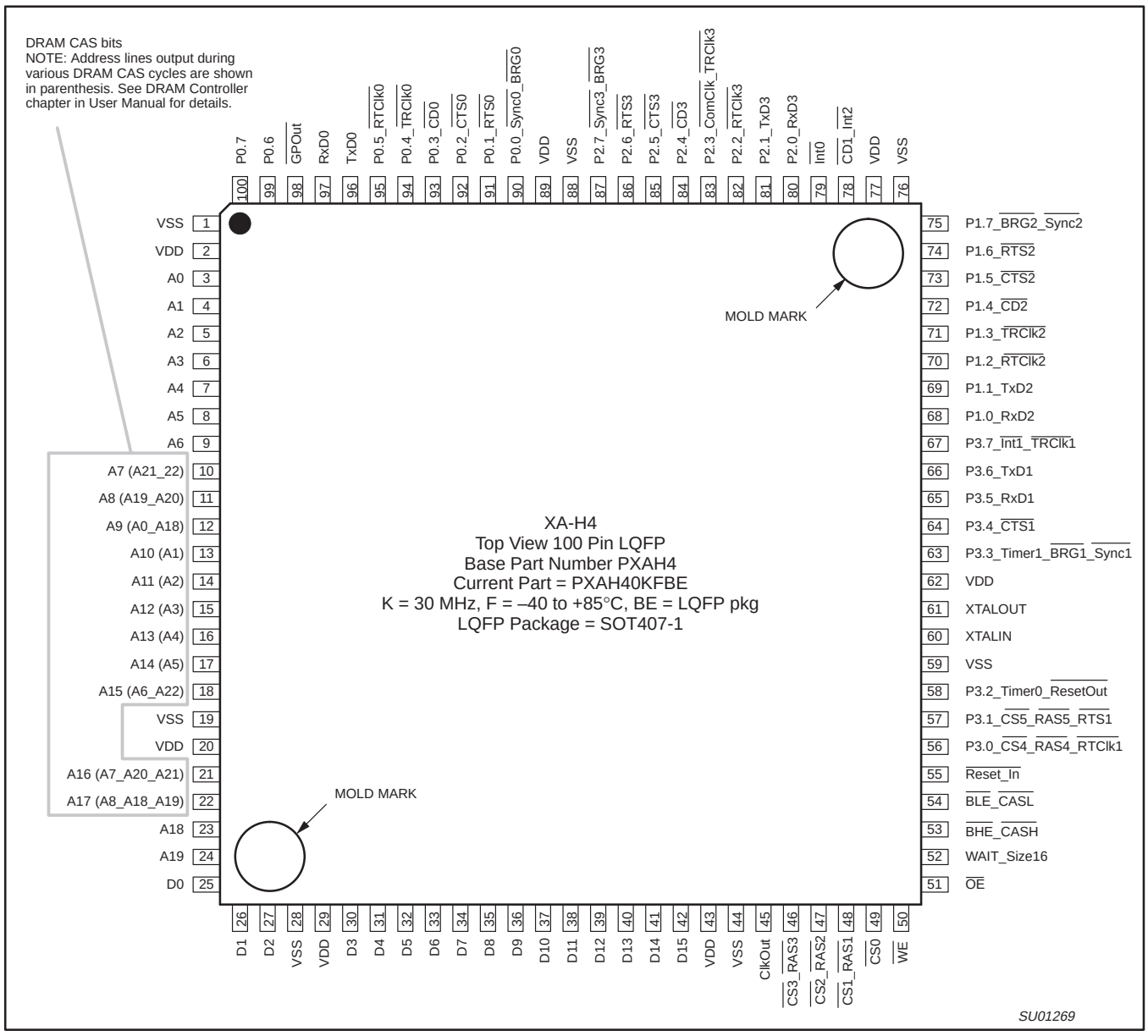
FEATURES

- Large Memory Support
- De-multiplexed Address/Data Bus
- Six Programmable Chip Selects
  - Support for Unified Memory – allows easy user modification of all code
  - External ISP Flash support for easy code download
- Dynamic Bus Sizing – each of 6 Chip Selects can be programmed for 8-bit or 16-bit bus.
- Dynamic Bus Timing – each of 6 chip selects has individual programmable bus timing.
- 32 Programmable General Purpose I/O Pins
- Four USARTs with 230.4 kbps capability
- Eight DMA Channels

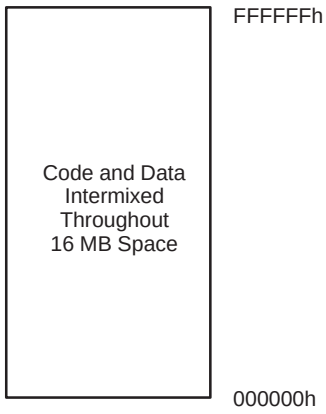
ADDITIONAL XA-H4 FEATURES (NOT AVAILABLE ON XA-H3)

- Complete DRAM controller supports up to four banks of 8 MB each
- Memory controller supports 16 MB in Unified Mode
- Memory controller supports 32 MB in Harvard Mode
- Serial ports are USARTs
  - Synchronous capability up to 1 Mbps, and include HDLC/SDLC support
  - Four Match Characters are supported on each USART in Async Mode
  - Hardware Autobaud on all four USARTs in Async Mode
  - USARTs are improved 85C30 style

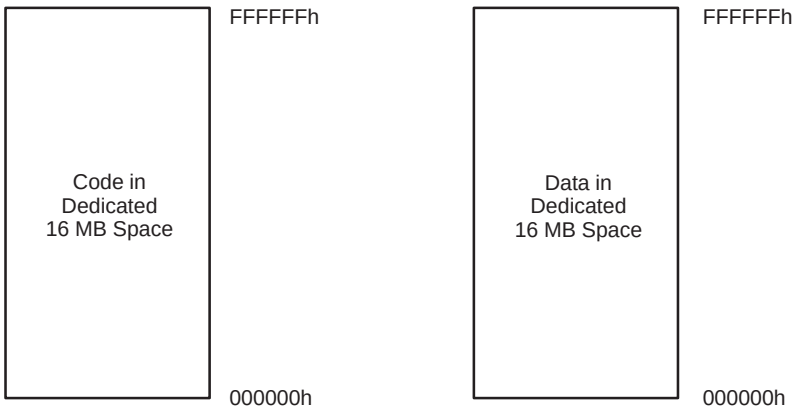
PIN CONFIGURATION



XA-H4 MEMORY MAPS



Unified Memory
(also known as von Neuman architecture)



Harvard Architecture

SU01272

PIN DESCRIPTIONS

Mnemonic	Lqfp Pin No.	Type	Name and Function	See Note
V_{SS}	1, 19, 28, 44, 59, 76, 88	I	**Ground:** 0 V reference.	
V_{DD}	2, 20, 29, 43, 62, 77, 89	I	**Power Supply:** This is the power supply voltage for normal, idle, and power down operation.	
$\overline{\text{ResetIn}}$	55	I	**Reset:** A low on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor to begin execution at the address contained in the reset vector.	
WAIT/ Size16	52	I	**Wait/Size16:** During Reset, this input determines bus size for boot device ("1" = 16-bit boot device; "0" = 8-bit.) During normal operation this is the Wait input ("1" = Wait; "0" = Proceed.)	
XTALIn	60	I	**Crystal 1:** Input to the inverting amplifier used in the oscillator circuit and input to the internal clock generator circuits.	
XTALOut	61	I	**Crystal 2:** Output from the oscillator amplifier.	
$\overline{\text{CS0}}$	49	O	**Chip Select 0:** This output provides the active low chip select to the boot device (usually ROM or Flash.) It cannot be connected to DRAM. From reset, it is enabled and mapped to an address range based at 000000h. It can be remapped by software to a higher base in the address map (see the "Memory Interface" chapter in the *XA-H4 User Manual*.)	
$\overline{\text{CS1}}$_$\overline{\text{RAS1}}$	48	O	**Chip Select 1** or **$\overline{\text{RAS}}$1:** Chip Selects and $\overline{\text{RAS}}$ 1 through 5 come out of reset disabled. They can be programmed to function as normal chip selects, or as $\overline{\text{RAS}}$ strobes to DRAM. CS1 can be "swapped" with CS0 (see the SWAP operation and control bit in the "Memory Controller" chapter of the *XA-H4 User Manual*.) CS1 is usually mapped to be based at 000000h after the swap, but is capable of being based anywhere in the 16 MB space.	
$\overline{\text{CS2}}$_$\overline{\text{RAS2}}$	47	O	**Chip Select 2** or **$\overline{\text{RAS}}$2:** Active low Chip Selects CS1 through CS5 come out of reset disabled. They can be programmed to function as normal chip selects, or as $\overline{\text{RAS}}$ strobes to DRAM. CS2 through CS5 are not used with the "SWAP" operation (see the "Memory Controller" chapter in the *XA-H4 User Manual*.) They are mappable to any region of the 16 MB address space.	
$\overline{\text{CS3}}$_$\overline{\text{RAS3}}$	46	O	**CS3 or $\overline{\text{RAS}}$3:** See Chip Select 2 for description.	
See Pins 56, 57 for 2 additional Chip Selects				
$\overline{\text{WE}}$	50	O	**Write Enable:** Goes active low during all bus write cycles only.	
$\overline{\text{OE}}$	51	O	**Output Enable:** Goes active low during all bus read cycles only.	
$\overline{\text{BLE}}$_$\overline{\text{CASL}}$	54	O	**Byte Low Enable** or **$\overline{\text{CAS}}$_Low_Byte:** Goes active low during all bus cycles that access D7 – D0, read or write, Generic or DRAM. Functions as $\overline{\text{CAS}}$ during DRAM cycles.	
$\overline{\text{BHE}}$_$\overline{\text{CASH}}$	53	O	**Byte High Enable** or **$\overline{\text{CAS}}$_High_Byte:** Goes active low during all bus cycles that access data bus lines D15 – D8, read or write, Generic or DRAM. Functions as $\overline{\text{CAS}}$ during DRAM cycles.	
ClkOut	45	O	**Clock Output:** This pin outputs a buffered version of the internal CPU clock. The clock output may be used in conjunction with the external bus to synchronize WAIT state generators, etc. The clock output may be disabled by software. **WARNING:** The capacitive loading on this output must not exceed 40 pf.	
A19 – A0	24 – 21, 18 – 3	O	**Address[19:0]:** These address lines output A19 – A0 during (SRAM, etc.) bus cycles. DRAMS (H4 only) are connected only to pins 22, 21, 18 – 10 (pins A17 to A7; see user manual "MIF Chapter" for connecting various DRAM sizes); the appropriate address values are multiplexed onto these 11 pins for $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ during DRAM bus cycles.	
D15 – D0	42 – 30, 27 – 25	I/O	**Data[15:0]:** Bi-directional data bus, D15 – D0.	
P0.0	90	I/O	**P0.0_Sync0_$\overline{\text{BRG0}}$:** Port 0 Bit 0, or USART0 $\overline{\text{Sync}}$ input or output, or USART0 $\overline{\text{BRG}}$ output, or USART0 **$\overline{\text{TxClk}}$** output.	1
P0.1	91	I/O	**P0.1_$\overline{\text{RTS0}}$:** Port 0 Bit 1, or USART0 **$\overline{\text{RTS}}$** (Request To Send) output.	1
P0.2	92	I/O	**P0.2_$\overline{\text{CTS0}}$:** Port 0 Bit 2, or USART0 $\overline{\text{CTS}}$ (Clear To Send) input.	1
P0.3	93	I/O	**P0.3_$\overline{\text{CD0}}$:** Port 0 Bit 3, or USART0 Carrier Detect input.	1
P0.4	94	I/O	**P0.4_$\overline{\text{TRClk0}}$:** Port 0 Bit 4, or USART0 TR clock input.	1, 2
P0.5	95	I/O	**P0.5_$\overline{\text{RTClk0}}$:** Port 0 Bit 5, or USART0 RT clock input.	1, 2
P0.6	99	I/O	**P0.6:** Port 0 Bit 6	1
P0.7	100	I/O	**P0.7:** Port 0 Bit 7	1

Name	Description	SFR Address	Bit Functions and Addresses MSB							LSB	Reset Value
P0CFGA	Port 0 Configuration A	470h									5
P1CFGA	Port 1 Configuration A	471h									5
P2CFGA	Port 2 Configuration A	472h									5
P3CFGA	Port 3 Configuration A	473h									5
P0CFGB	Port 0 Configuration B	4F0h									5
P1CFGB	Port 1 Configuration B	4F1h									5
P2CFGB	Port 2 Configuration B	4F2h									5
P3CFGB	Port 3 Configuration B	4F3h									5
			227	226	225	224	223	222	221	220	
PCON*	Power Control Reg	404h	–	–	–	–	–	–	PD	IDL	00h
			20F	20E	20D	20C	20B	20A	209	208	
PSWH*	Program Status Word High	401h	SM	TM	RS1	RS0	IM3	IM2	IM1	IM0	2
			207	206	205	204	203	202	201	200	
PSWL*	Program Status Word Low	400h	C	AC	–	–	–	V	N	Z	2
			217	216	215	214	213	212	211	210	
PSW51*	80C51 Compatible PSW	402h	C	AC	F0	RS1	RS0	V	F1	P	3
RSTSRC	Reset Source Reg	463h	ROEN	–	–	–	–	R_WD	R_CMD	R_EXT	7
RTH0	Timer 0 Reload High	455h									00h
RTH1	Timer 1 Reload High	457h									00h
RTL0	Timer 0 Reload Low	454h									00h
RTL1	Timer 1 Reload Low	456h									00h
SCR	System Configuration Reg	440h	–	–	–	–	PT1	PT0	CM	PZ	00h
			21F	21E	21D	21C	21B	21A	219	218	
SSEL*	Segment Selection Reg	403h	ESWEN	R6SEG	R5SEG	R4SEG	R3SEG	R2SEG	R1SEG	R0SEG	00h
SWE	Software Interrupt Enable	47Ah	–	SWE7	SWE6	SWE5	SWE4	SWE3	SWE2	SWE1	00h
			357	356	355	354	353	352	351	350	
SWR*		42Ah	–	SWR7	SWR6	SWR5	SWR4	SWR3	SWR2	SWR1	00h
			287	286	285	284	283	282	281	280	
TCON*	Timer 0/1 Control	410h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h
TH0	Timer 0 High	451h									00h
TH1	Timer 1 High	453h									00h
TL0	Timer 0 Low	450h									00h
TL1	Timer 1 Low	452h									00h
TMOD	Timer 0/1 Mode	45Ch	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00h

Name	Description	SFR Address	Bit Functions and Addresses MSB							LSB	Reset Value
			28F	28E	28D	28C	28B	28A	289	288	
TSTAT*	Timer 0/1 Extended Status	411h	–	–	–	–	–	T1OE	–	T0OE	00h
			2FF	2FE	2FD	2FC	2FB	2FA	2F9	2F8	
WDCON*	Watchdog Control	41Fh	PRE2	PRE1	PRE0	–	–	WDRUN	WDTOF	–	6
WDL	Watchdog Timer Reload	45Fh									00h
WFEED1	Watchdog Feed 1	45Dh									x
WFEED2	Watchdog Feed 2	45Eh									x

NOTES:

* SFRs marked with an asterisk (*) are bit addressable.

\# SFRs marked with a pound sign (#) are additional SFR registers specific to the XA-H3 and XA-H4.

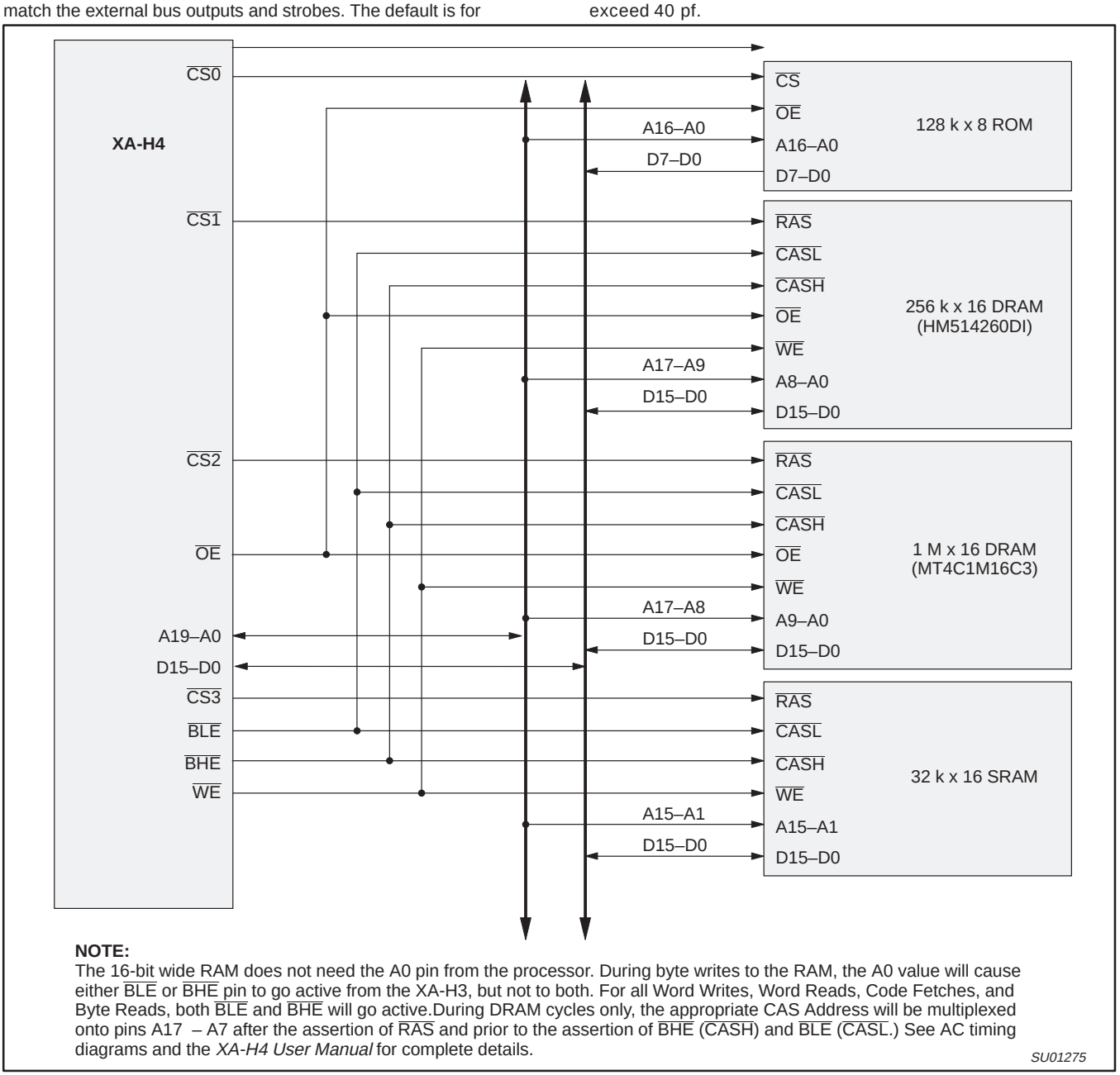
1. The XA-H4 implements an 8-bit SFR bus, as stated in Chapter 8 of the *IC25 Data Handbook XA User Guide.* All SFR accesses must be 8-bit operations. Attempts to write 16 bits to an SFR will actually write only the lower 8 bits. 16-bit SFR reads will return undefined data in the upper byte.
2. SFR is loaded from the reset vector.
3. F1, F0, and P reset to “0”. All other bits are loaded from the reset vector.
4. Unimplemented bits in SFRs are “X” (unknown) at all times. “1”s should not be written to these bits since they may be used for other purposes in future XA derivatives. The reset value shown for these bits is “0”.
5. Port configurations default to quasi-bidirectional when the XA begins execution after reset. Thus all PnCFGA registers will contain FFh and PnCFGB register will contain 00h. See warning in *XA-H4 User Manual* about P3.2_Timer0_$\overline{\text{ResetOut}}$ pin during first 258 clocks after power up. Basically, during this period, this pin may output a strongly-driven low pulse. If the pulse does occur, it will terminate in a transition to high at a time no later than the 259th system clock after valid V_{CC} power up.
6. The WDCON reset value is E6 for a Watchdog reset; E4 for all other reset causes.
7. The RSTSRC register reflects the cause of the last XA reset. One bit will be set to “1”, the others will be “0”. RSTSRC[7] enables the $\overline{\text{ResetOut}}$ function; “1” = Enabled, “0” = Disabled. See *XA-H4 User Manual* for details; RSTSRC[7] differs in function from most other XA derivatives.
8. The XA guards writes to certain bits (typically interrupt flags) that may be written by a peripheral function. This prevents loss of an interrupt or other status if a bit was written directly by a peripheral action between the read and write of an instruction that performs a read-modify-write operation. XA-H4 SFR bits that are guarded in this manner are: TF1, TF0, IE1, and IE0 (in TCON), and WDTOF (in WDCON).

MMR Name	Read/Write or Read Only	Size	Address Offset	Description	Reset Value
USART3 Registers					
USART3 Write Register 0	R/W	8	8C0h	Command register	00h
USART3 Write Register 1	R/W	8	8C2h	Tx/Rx Interrupt & data transfer mode	xx
USART3 Write Register 2	R/W	8	8C4h	Extended Features Control	xx
USART3 Write Register 3	R/W	8	8C6h	Receive Parameter and Control	00h
USART3 Write Register 4	R/W	8	8C8h	Tx/Rx miscellaneous parameters & mode	00h
USART3 Write Register 5	R/W	8	8CAh	Tx parameter and control	00h
USART3 Write Register 6	R/W	8	8CCh	HDLC/SDLC address field or Match Character 0	00h
USART3 Write Register 7	R/W	8	8CEh	HDLC/SDLC flag or Match Character 1	xx
USART3 Write Register 8	R/W	8	8D0h	Transmit Data Buffer	xx
USART3 Write Register 9	R/W	8	8D2h	Master Interrupt control	xx
USART3 Write Register 10	R/W	8	8D4h	Miscellaneous Tx/Rx control register	00h
USART3 Write Register 11	R/W	8	8D6h	Clock Mode Control	xx
USART3 Write Register 12	R/W	8	8D8h	Lower Byte of Baud rate time constant	00h
USART3 Write Register 13	R/W	8	8DAh	Upper Byte of Baud rate time constant	00h
USART3 Write Register 14	R/W	8	8DCh	Miscellaneous Control bits	xx
USART3 Write Register 15	R/W	8	8DEh	External/Status interrupt control	f8h
USART3 Write Register 16	R/W	8	8E8h	Match Character 2 (WR16)	00h
USART3 Write Register 17	R/W	8	8EAh	Match Character 3 (WR17)	00h
USART3 Read Register 0	RO	8	8E0h	Tx/Rx buffer and external status	
USART3 Read Register 1	RO	8	8E2h	Receive condition status/residue code	
Reserved			8E4h		
USART3 Read Register 3	RO	8	8E6h	Interrupt Pending Bits	
USART3 Read Register 6	RO	8	8ECh	SDLC byte count low register	
USART3 Read Register 7	RO	8	8EEh	SDLC byte count high and FIFO status	
USART3 Read Register 8	RO	8	8F0h	Receive Buffer	
Reserved			8F2h		–
USART3 Read Register 10	RO	8	8F4h	Loop/clock status	
Reserved			8F6-8FEh		
Rx DMA Registers					
DMA Control Register Ch.0 Rx	R/W	8	100h	Control Register	00h
FIFO Control & Status Reg Ch.0 Rx	R/W	8	101h	Control & Status Register	00h
Segment Register Ch.0 Rx	R/W	8	102h	Points to 64 k data segment	00h
Buffer Base Register Ch.0 Rx	R/W	8	104h	Wrap Reload Value for A15 – A8, A7 – A0 reloaded to zero by hardware	00h
Buffer Bound Register Ch.0 Rx	R/W	16	106h	Upper Bound (plus 1) on A15 – A0	0000h
Address Pointer Reg Ch.0 Rx	R/W	16	108h	Current Address pointer A15 – A0	0000h
Byte Count Register Ch.0 Rx	R/W	16	10Ah	Corresponds to A15 – A0 Byte Count, generates interrupt if enabled and byte count exceeded.	0000h
Data FIFO Register Ch.0 Lo Rx	R/W	16	10Ch	10Ch = Byte 0 = older, 10Dh = Byte 1 = younger	00h 00h
Data FIFO Register Ch.0 Hi Rx	R/W	16	10Eh	10Eh = Byte 2 = older, 10Fh = Byte 3 = younger	00h 00h
DMA Control Register Ch.1 Rx	R/W	8	110h	Control Register	00h
FIFO Control & Status Register Ch.1 Rx	R/W	8	111h	Control & Status Register	00h
Segment Register Ch. 1 Rx	R/W	8	112h	Points to 64 k data segment	00h

Clock Output

The ClkOut pin allows easier external bus interfacing in some situations. This output reflects the XTALIn clock input to the XA (referred to internally as CClk or System Clock), but is delayed to match the external bus outputs and strobes. The default is for ClkOut to be output enabled at reset, but it may be turned off (tri-state disabled) by software via the MICFG MMR.

WARNING: The capacitive loading on this output must not exceed 40 pf.



NOTE:
The 16-bit wide RAM does not need the A0 pin from the processor. During byte writes to the RAM, the A0 value will cause either $\overline{BLE}$ or $\overline{BHE}$ pin to go active from the XA-H3, but not to both. For all Word Writes, Word Reads, Code Fetches, and Byte Reads, both $\overline{BLE}$ and $\overline{BHE}$ will go active.During DRAM cycles only, the appropriate CAS Address will be multiplexed onto pins A17 – A7 after the assertion of $\overline{RAS}$ and prior to the assertion of $\overline{BHE}$ ($\overline{CASH}$) and $\overline{BLE}$ ($\overline{CASL}$.) See AC timing diagrams and the *XA-H4 User Manual* for complete details.

Figure 4. Typical system bus configuration

Table 4. Memory interface control registers

	Register Name	Reg Type	Description
MRBH	"MMR Base Address" High	SFR 8 bits	This SFR is used to relocate the MMRs. It contains address bits a23 – a16 of the base address for the 4 kB Memory Mapped Register space. See the *XA-H4 User Manual* for using this SFR to relocate the MMRs.
MRBL	"MMR Base Address" Low	SFR 8 bits	Contains address bits a15 – a12 of the base address for the 4 kB Memory Mapped Register space.
MICFG	MIF Configuration	MMR 8 bits	Contains the ClkOut Enable bit.
MBCL	Memory Bank Configuration Lock	MMR 8 bits	Contains the bits for locking and unlocking the BiCFG Registers.
BiCFG	Bank i Configuration	MMR 8 bits	Contains the size, type, bus width, and enable bits for Memory Bank i.
BiAM	Bank i Base Address/DRAM Address Multiplexer Control	MMR 8 bits	Contains the base address bits and DRAM address multiplex control bits for Memory Bank i.
BiTMG	Bank i Timing	MMR 8 bits	Contains the timing control bits for Memory Bank i.
RFSH	Refresh Timing	MMR 8 bits	Contains the refresh time constant and DRAM Refresh Timer enable bit.

EIGHT CHANNEL DMA CONTROLLER

The XA-H3/H4 has eight DMA channels; one Rx DMA channel dedicated to each USART Receive (Rx) channel, and one Tx DMA channel dedicated to each USART Transmit (Tx) channel. All DMA channels are optimized to support memory efficient circular data buffers in external memory. All DMA channels can also support traditional linear data buffers.

Transmit DMA Channel Modes

The four Tx channels have four DMA modes specifically designed for various applications of the attached USARTs. These modes are summarized in Table 5. Full details for all DMA functions can be found in the DMA chapter of the *XA-H4 User Manual*.

Table 5. Tx DMA modes summary

Mode	Byte Count Source	Maskable Interrupt	Description
Non-SDLC/HDLC Tx Chaining	Header in memory	On stop	DMA channel picks up header from memory at the end of transmission. If the byte count in the header is greater than zero, then DMA transmits the number of bytes specified in the byte count. If byte count equals 0, then a maskable interrupt is generated. This process repeats until the byte count in the data header is zero. See *XA-H4 User Manual* for details.
SDLC/HDLC Tx Chaining	Header in memory	End of packet (not end of fragment)	Same as above, except DMA header distinguishes between fragment of packet and full pack. See XA-H4 User Manual for details.
Stop on TC	Processor loads Byte Count Register (for each fragment)	Byte count completed (Tx DMA stops)	Processor loads byte count into DMA. DMA sends that number of bytes, generates maskable interrupt, and stops.
Periodic Interrupt	Porcessor loads Byte Count Register (only once)	When Byte Counter reaches zero and is reloaded by DMA hardware from the byte count register.	DMA runs until commanded to stop by processor. Every time byte counter rolls over, a new maskable interrupt is generated.

The XA-H4 has a standard XA CPU Interrupt Controller, implemented with 15 Maskable Event Interrupts. Event Interrupts are defined as maskable interrupts usually generated by hardware events. However, in the XA-H4, 4 of the 15 Event Interrupts are generated by software writing directly to the interrupt flag bit. These 4 interrupts are referred to as “High Priority Software Interrupts.”

See the *IC25 XA Data Handbook* for a full explanation of the exception structure, including event interrupts, of the XA CPU. Because the High Priority Software Interrupts are not implemented on all XA derivitives, they are explained in the *XA-H4 User Manual*.

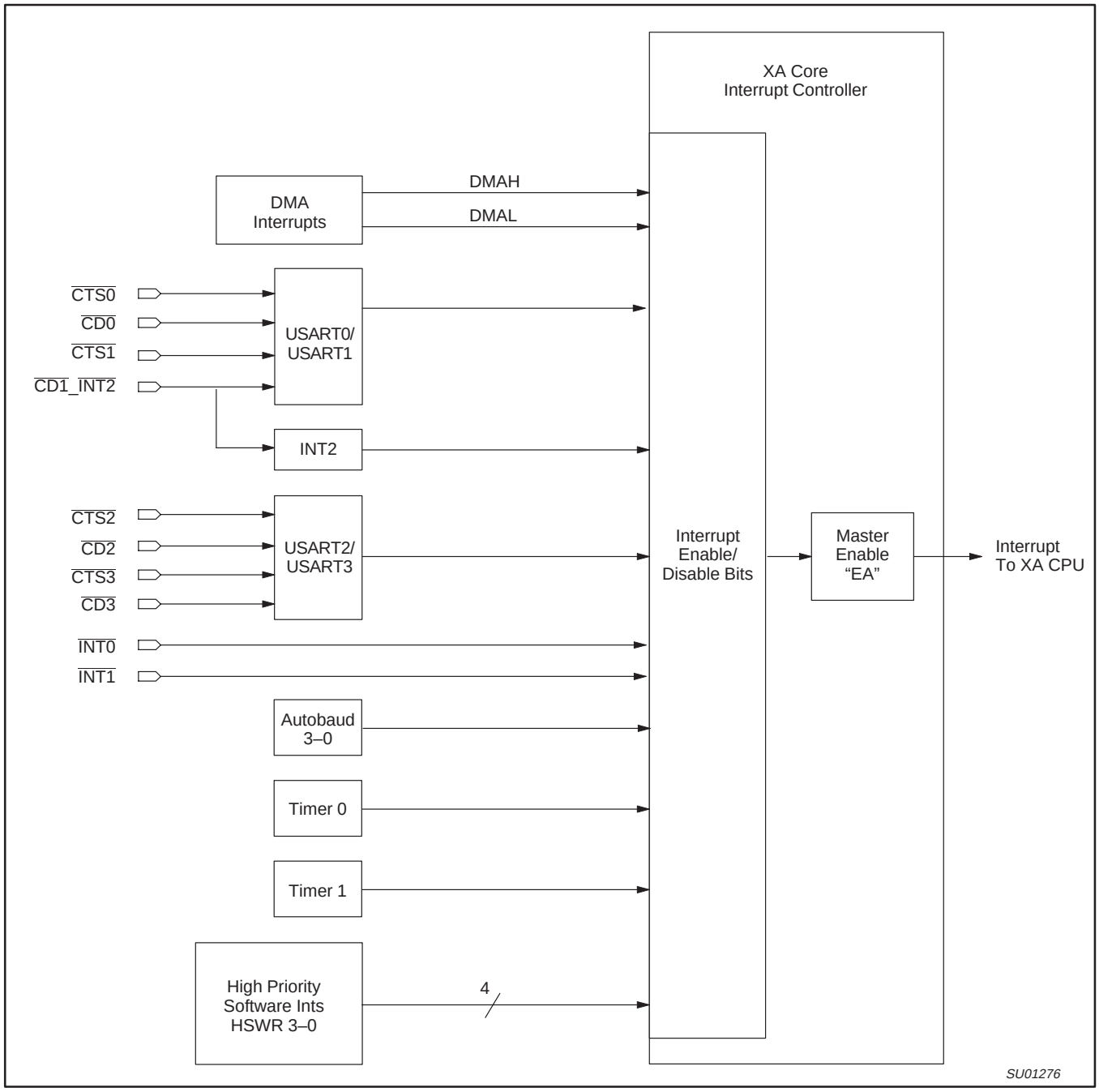


Figure 6. XA-H4 Interrupt Structure Overview

Table 7. USART0 Interrupts (Interrupt structure is the same, except for bit locations, for all 4 USARTs)

Potential USART0 Interrupt	Individual Enable Bit MMR Hex Offset	Source Bit MMR Hex Offset	Group Enable Bit(S) MMR Hex Offset	Group Flag Bit MMR Hex Offset	Master Enable Bit MMR Hex Offset
Rx Character Available	–	RR0[0] 820[0]	WR1[4:3] 802[4:3]	Even Channel Rx IP RR3[5] 826[5]	USART0/1 Master Interrupt Enable WR9[3] 812[3]
SDLC EOF (XA-H4 Only)	–	RR1[7] 822[7]			
CRC/Framing Error	–	RR1[6] 822[6]			
Rx Overrun	–	RR1[5] 822[5]			
Parity Error	WR1[2] 802[2]	RR1[4] 822[4]			
Tx Buffer Empty	See WR1[1]	RR0[2] 820[2]	Tx Interrupt Enable WR1[1] 802[1]	Even Channel Tx IP RR3[4] 826[4]	
Break/Abort	Break/ Abort IE WR15[7] 81E[7]	RR0[7] 820[7]	Master External/Status Interrupt Enable WR1[0] 802[0]	Even Channel External/Status IP RR3[3] 826[3]	
Tx Underrun/EOM	Tx Underrun/EOM IE WR15[6] 81E[6]	RR0[6] 820[6]			
CTS	CTS IE WR15[5] 81E[5]	RR0[5] 820[5]			
SYNC/HUNT (XA-H4 Only)	SYNC/ HUNT IE WR15[4] 81E[4]	RR0[4] 822[4]			
DCD	DCD IE WR15[3] 81E[3]	RR0[3] 820[3]			
Zero Count	Zero Count IE WR15[1] 81E[1]	RR0[1] 820[1]			

EXCEPTION/TRAPS PRECEDENCE

Description	Vector Address	Arbitration Ranking
Reset (h/w, watchdog, s/w)	0000–0003	0 (High)
Break Point	0004–0007	1
Trace	0008–000B	1
Stack Overflow	000C–000F	1
Divide by 0	0010–0013	1
User RETI	0014–0017	1
TRAP 0–15 (software)	0040–007F	1

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Operating temperature under bias	–55 to +125	°C
Storage temperature range	–65 to +150	°C
Voltage on any other pin to V_{SS}	–0.5 to V_{DD}+0.5 V	v
Maximum I_{OL} per I/O pin	15	mA
Power dissipation (based on package heat transfer, not device power consumption)	1.5	W

PRELIMINARY DC ELECTRICAL CHARACTERISTICS

V_{DD} = 5.0 V +/– 10% or 3.3 V +/– 10% unless otherwise specified; T_{amb} = –40°C to +85°C for industrial, unless otherwise specified.

Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ	Max	
I_{DD}	Power supply current, operating	5.0 V, 30 MHz		64	80	mA
		3.3 V, 30 MHz		55	70	mA
I_{ID}	Power supply current, Idle mode	5.0 V, 30 MHz		50	70	mA
		3.3 V, 30 MHz		44	60	mA
I_{PDI}	Power supply current, Power Down mode[1]	5.0 V, 3.0 V			500	µA
V_{RAM}	RAM keep-alive voltage		1.5			V
V_{IL}	Input low voltage		–0.5		0.22 V_{DD}	V
V_{IH}	Input high voltage, except Xtal1, RST		2.2			V
V_{IH1}	Input high voltage to Xtal1, RST	For both 3.0 & 5.0 V	0.7 V_{DD}			V
V_{OL}	Output low voltage all ports[8]	I_{OL} = 3.2 mA, V_{DD} = 4.5 V			0.5	V
		I_{OL} = 1.0 mA, V_{DD} = 3.0 V			0.4	V
V_{OH1}	Output high voltage, all ports	I_{OH} = –100 µA, V_{DD} = 4.5 V	2.4			V
		I_{OH} = –30 µA, V_{DD} = 3.0 V	2.0			V
V_{OH2}	Output high voltage, all ports	I_{OH} = 3.2 mA, V_{DD} = 4.5 V	2.4			V
		I_{OH} = 1.0 mA, V_{DD} = 3.0 V	2.2			V
C_{IO}	Input/Output pin capacitance				15	pF
I_{IL}	Logical 0 input current, all ports[7]	V_{IN} = 0.45 V			–50	µA
I_{LI}	Input leakage current, all ports[6]	V_{IN} = V_{IL} or V_{IH}			±10	µA
I_{TL}	Logical 1 to 0 transition current, all ports[5]	At V_{DD} = 5.5 V			–650	µA
		At V_{DD} = 3.6 V			–250	µA

NOTE:
1. V_{DD} must be raised to within the operating range before power down mode is exited.
2. Ports in quasi-bidirectional mode with weak pullup.
3. Ports in PUSH-PULL mode, both pullup and pulldown assumed to be the same strength.
4. In all output modes.
5. Port pins source a transition current when used in quasi-bidirectional mode and externally driven from 1 to 0. This current is highest when V_{IN} is approximately 2 V.
6. Measured with port in high impedance mode.
7. Measured with port in quasi-bidirectional mode.
8. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 15 mA (NOTE: This is +85°C specification for V_{DD} = 5 V)
   Maximum I_{OL} per 8-bit port: 26 mA
   Maximum total I_{OL} for all outputs: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

PRELIMINARY AC ELECTRICAL CHARACTERISTICS (5.0 V +/–10%)

V_{DD} = 5.0 V +/– 10%; T_{amb} = –40°C to +85°C (industrial)

Symbol	Figure	Parameter	Limits		Unit
			Min	Max	
All Cycles					
F_C		System Clock Frequency	0	30	MHz
t_C	23	System Clock Period = 1/FC	33.33	–	ns
t_{CHCX}	23	XTALIN High Time	t_C* 0.5	–	ns
t_{CLCX}	23	XTALIN Low Time	t_C* 0.4	–	ns
t_{CLCH}	23	XTALIN Rise Time	–	5	ns
t_{CHCL}	23	XTALIN Fall Time	–	5	ns
t_{AVSL}	All	Address Valid to Strobe low	t_C – 21	–	ns
t_{CHAH}	All	Address hold after ClkOut rising edge [9]	1	–	ns
t_{CHAV}	All	Delay from ClkOut rising edge to address valid	–	25	ns
t_{CHSH}	All	Delay from ClkOut rising edge to Strobe High[9]	1	21	ns
t_{CHSL}	All	Delay from ClkOut rising edge to Strobe Low[9]	1	19	ns
t_{CODH}	24	ClkOut Duty Cycle High (into 40 pF max.)	t_{CHCX}–7	t_{CHCX}+3	ns
t_{CPWH}	11, 12, 17, 18, 19, 20	$\overline{CAS}$ Pulse Width High	t_C – 12	–	ns
t_{CPWL}	11, 19	$\overline{CAS}$ Pulse Width Low	t_C – 10	–	ns
All DRAM Cycles					
t_{RP}	22	$\overline{RAS}$ precharge time, thus minimum $\overline{RAS}$ high time[8]	(n * t_C) – 16[8]	–	ns
Generic Data Read Only					
t_{AHDR}	7, 14	Address hold (A19 – A1 only, not A0) after $\overline{CS}$, $\overline{BLE}$, $\overline{BHE}$ rise at end of Generic Data Read Cycle (not code fetch)	t_C – 12	–	ns
Data Read and Instruction Fetch Cycles					
t_{DIS}	7, 8, 10, 11, 12, 14, 15, 17, 18, 19	Data In Valid setup to ClkOut rising edge	25	–	ns
t_{DIH}	7, 8, 10, 14, 15, 17, 18	Data In Valid hold after ClkOut rising edge [2]	0	–	ns
t_{OHDE}	8, 10, 11, 14, 18	$\overline{OE}$ high to XA Data Bus Driver Enable	t_C – 14	–	ns
Write Cycles					
t_{CHDV}	9, 13	Clock High to Data Valid	–	25	ns
t_{DVSL}	16, 20	Data Valid prior to Strobe Low	t_C – 23	–	ns
t_{SHAH}	9, 16	Minimum Address Hold Time after strobe goes inactive	t_C – 25	–	ns
t_{SHDH}	9, 16	Data hold after strobes ($\overline{CS}$ and $\overline{BHE}$/$\overline{BLE}$) high	t_C – 25	–	ns
Refresh					
t_{CLRL}	21	$\overline{CAS}$ low to $\overline{RAS}$ low	t_C – 15	–	ns
Wait Input					
t_{WS}	25	WAIT setup (stable high or low) to ClkOut rising edge	20	–	ns
t_{WH}	25	WAIT hold (stable high or low) after ClkOut rising edge	0	–	ns

NOTE:
1. See notes after the 3.3 V AC Timing Table

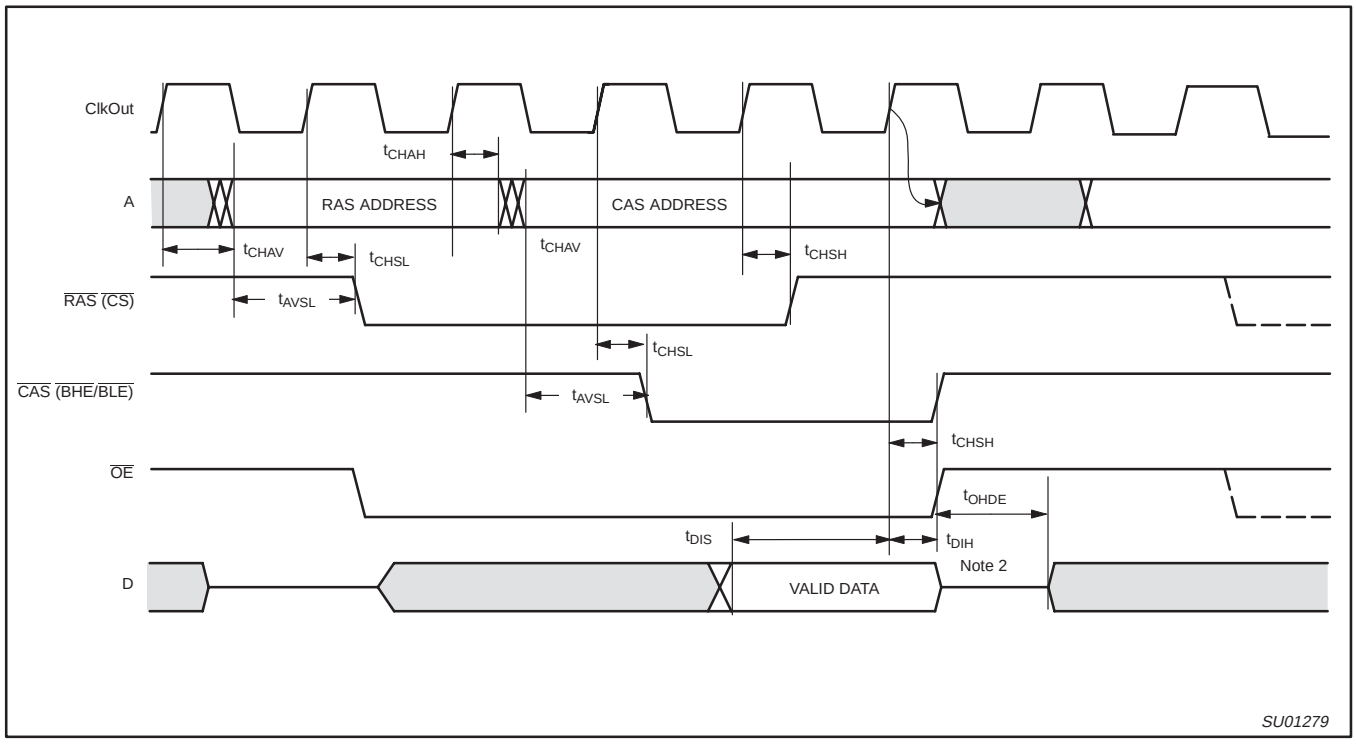


Figure 10. DRAM Single Read Cycle

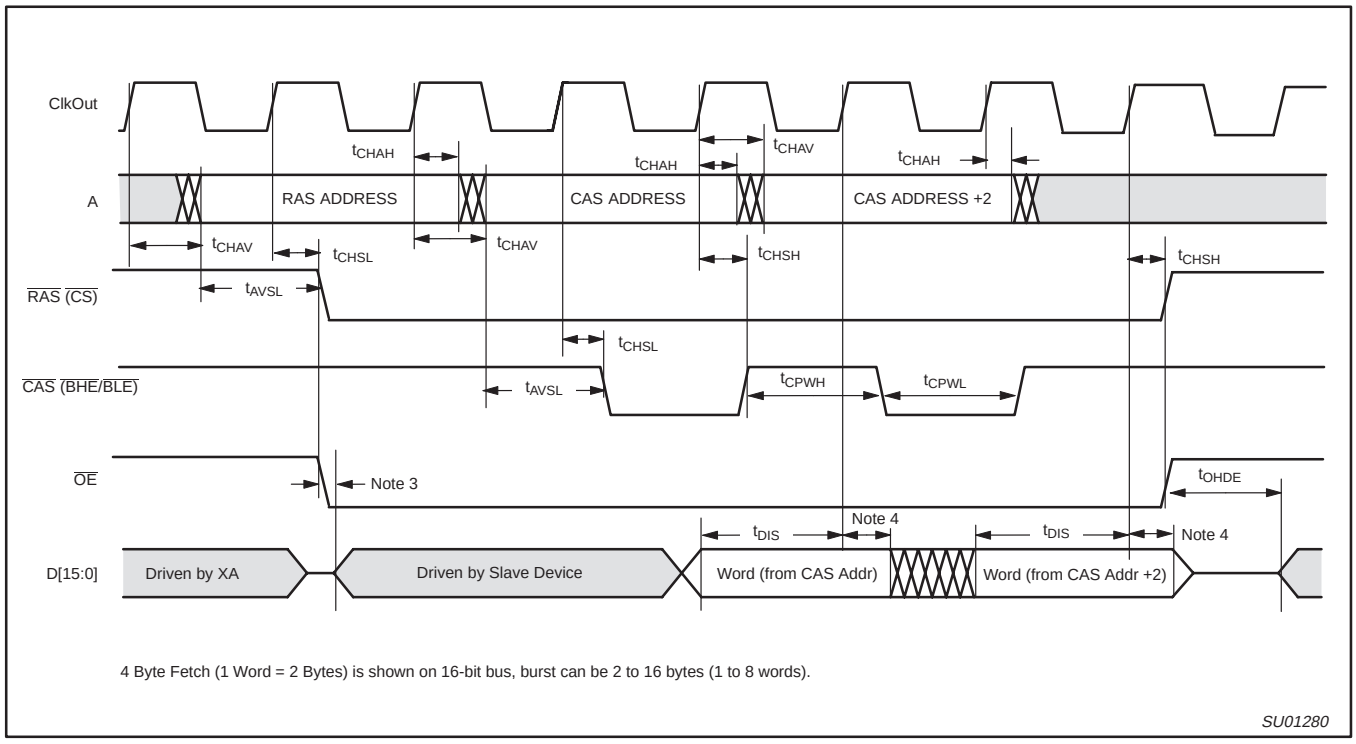


Figure 11. DRAM EDO Burst Code Fetch on 16-Bit Bus

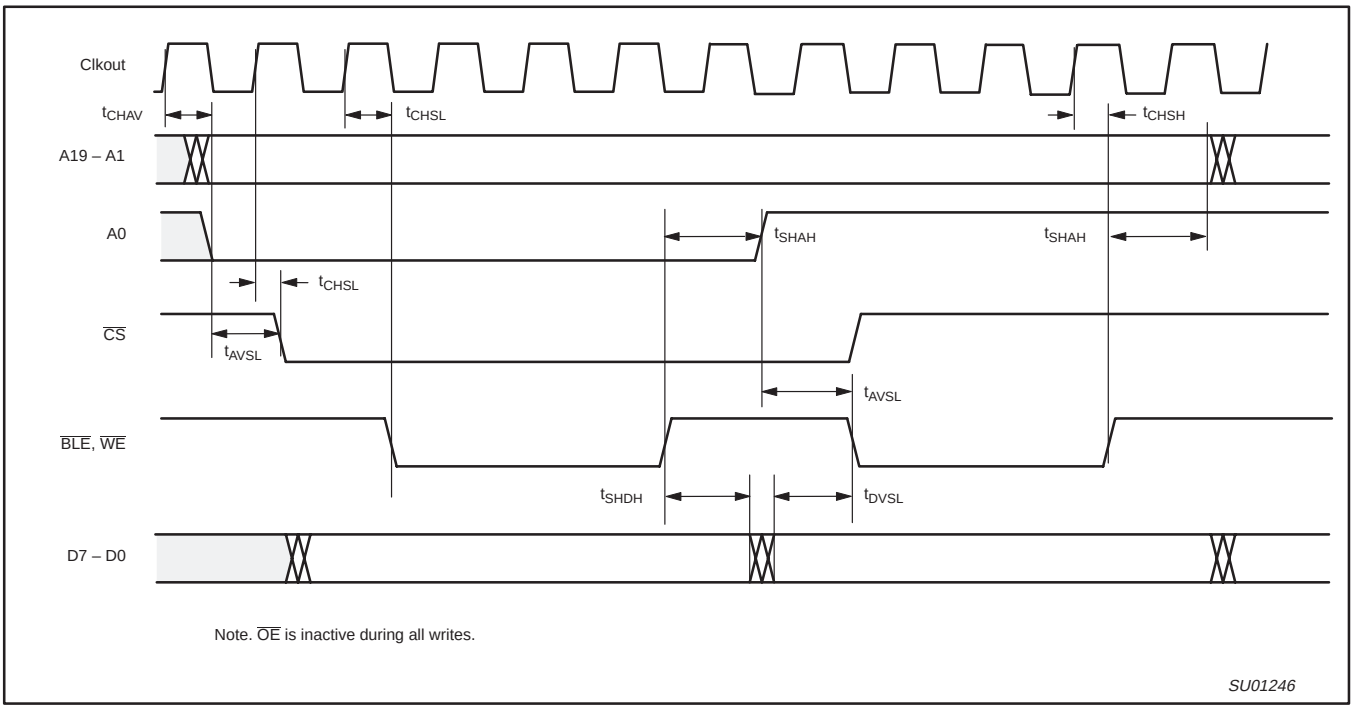


Figure 16. Generic 16-Bit Write on 8-Bit Bus

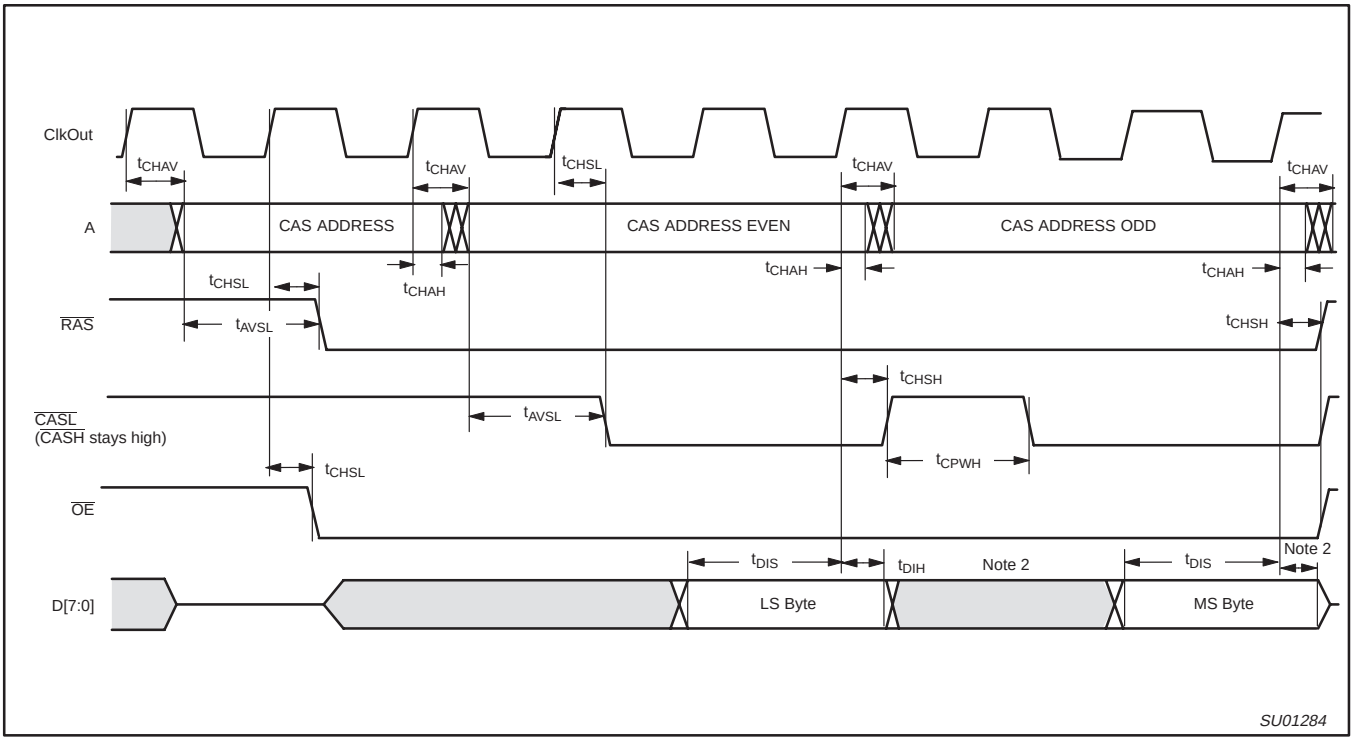


Figure 17. 16-Bit Read on 8-Bit Bus, DRAM (both FPM and EDO)

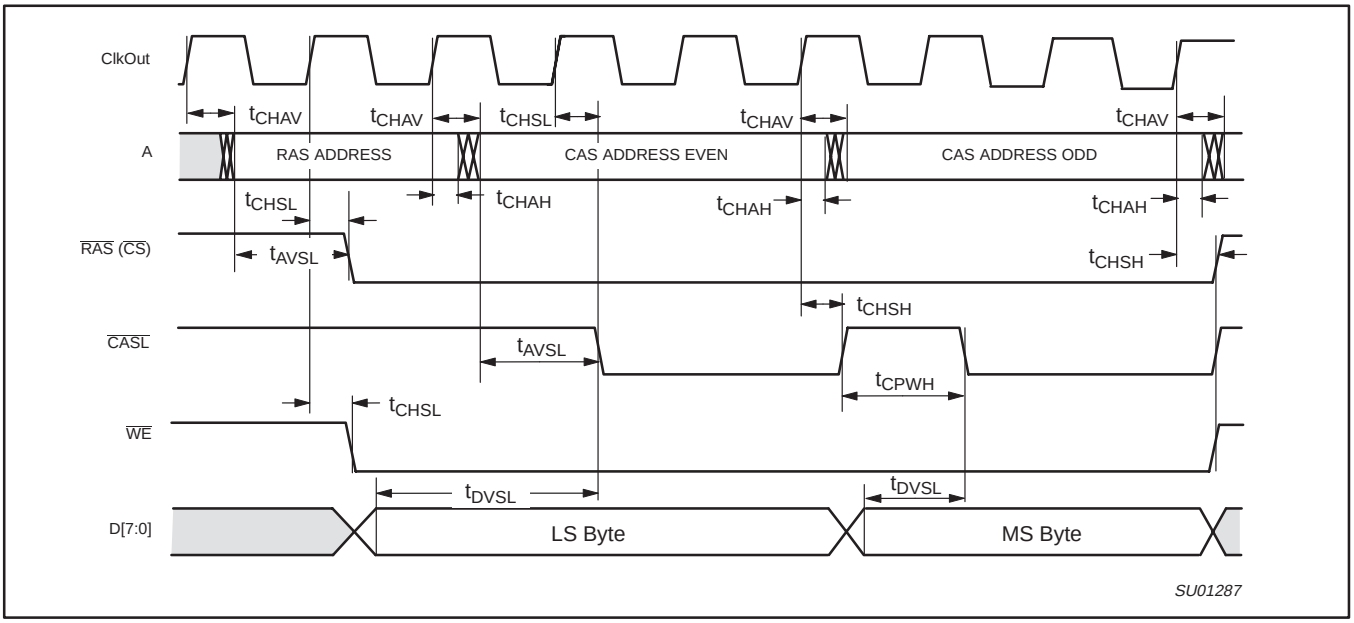


Figure 20. DRAM 16-Bit Write on 8-Bit Bus (FPM or EDO DRAMs)

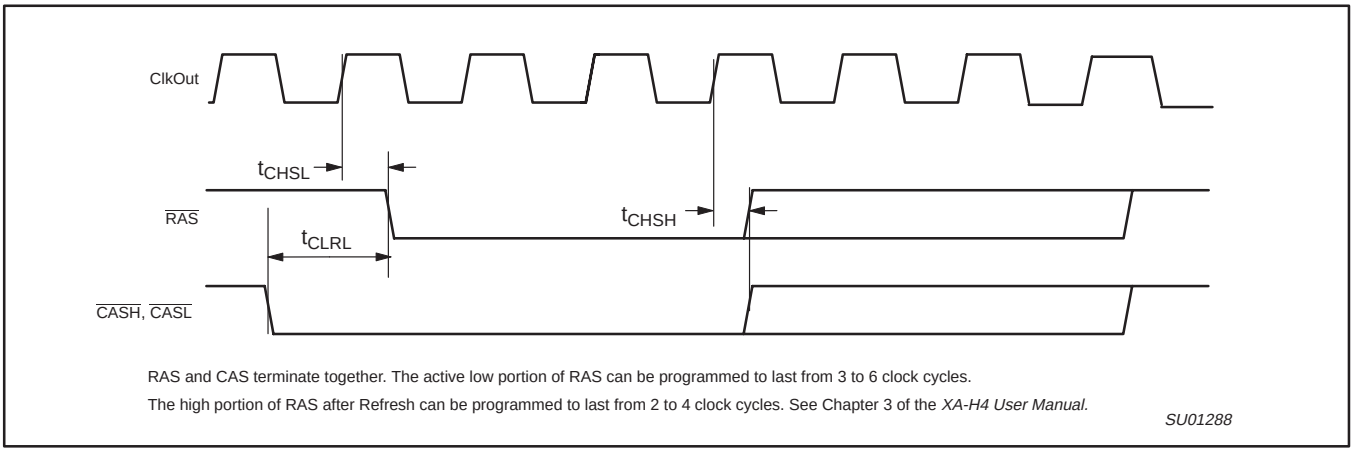


Figure 21. REFRESH

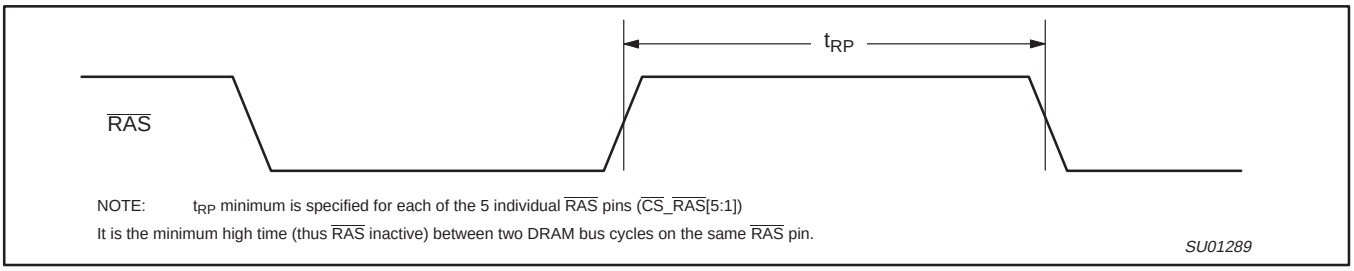


Figure 22. RAS Precharge Time

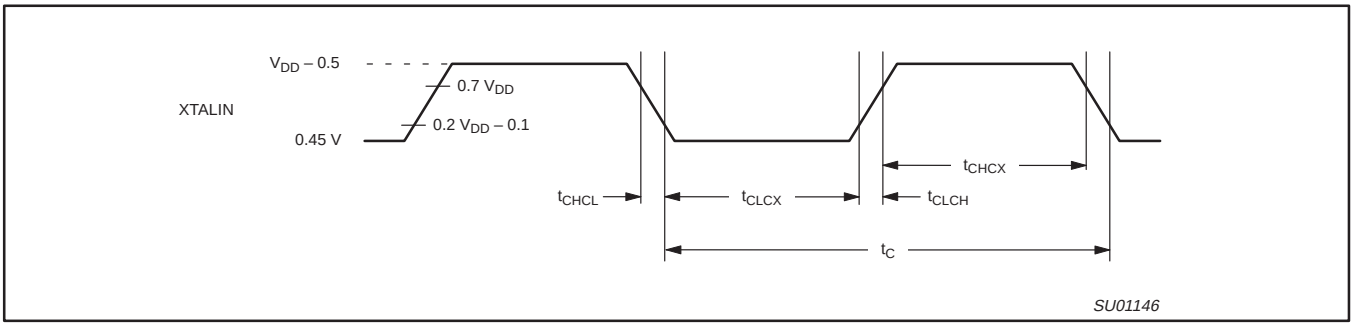


Figure 23. External Clock Input Drive

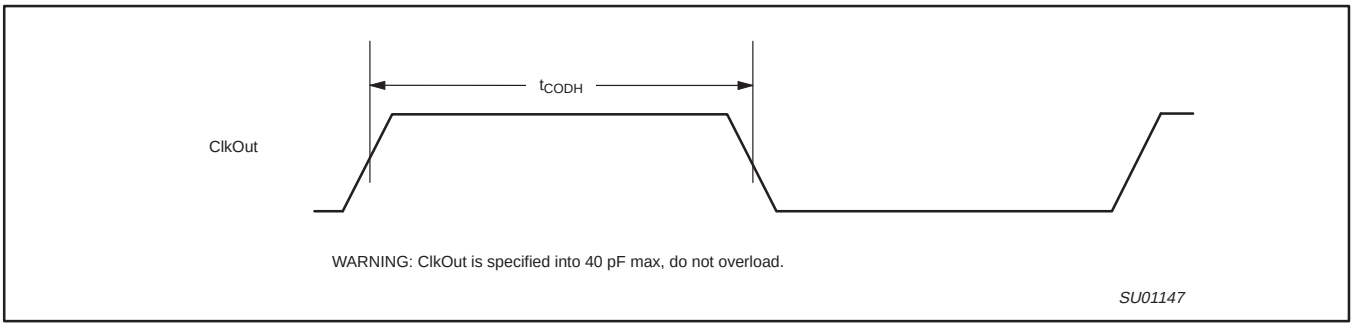


Figure 24. ClkOut Duty Cycle

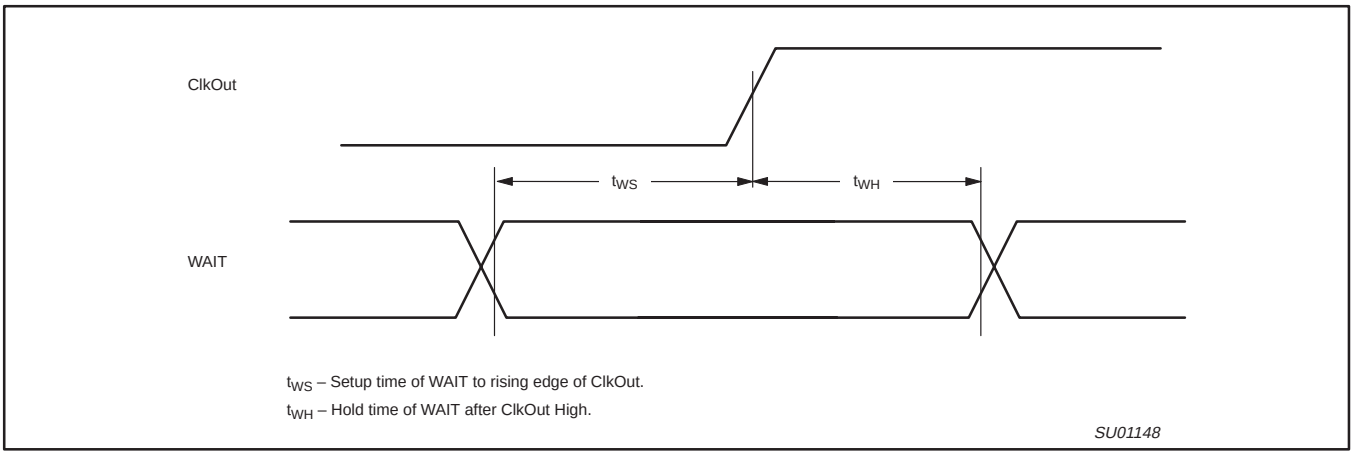
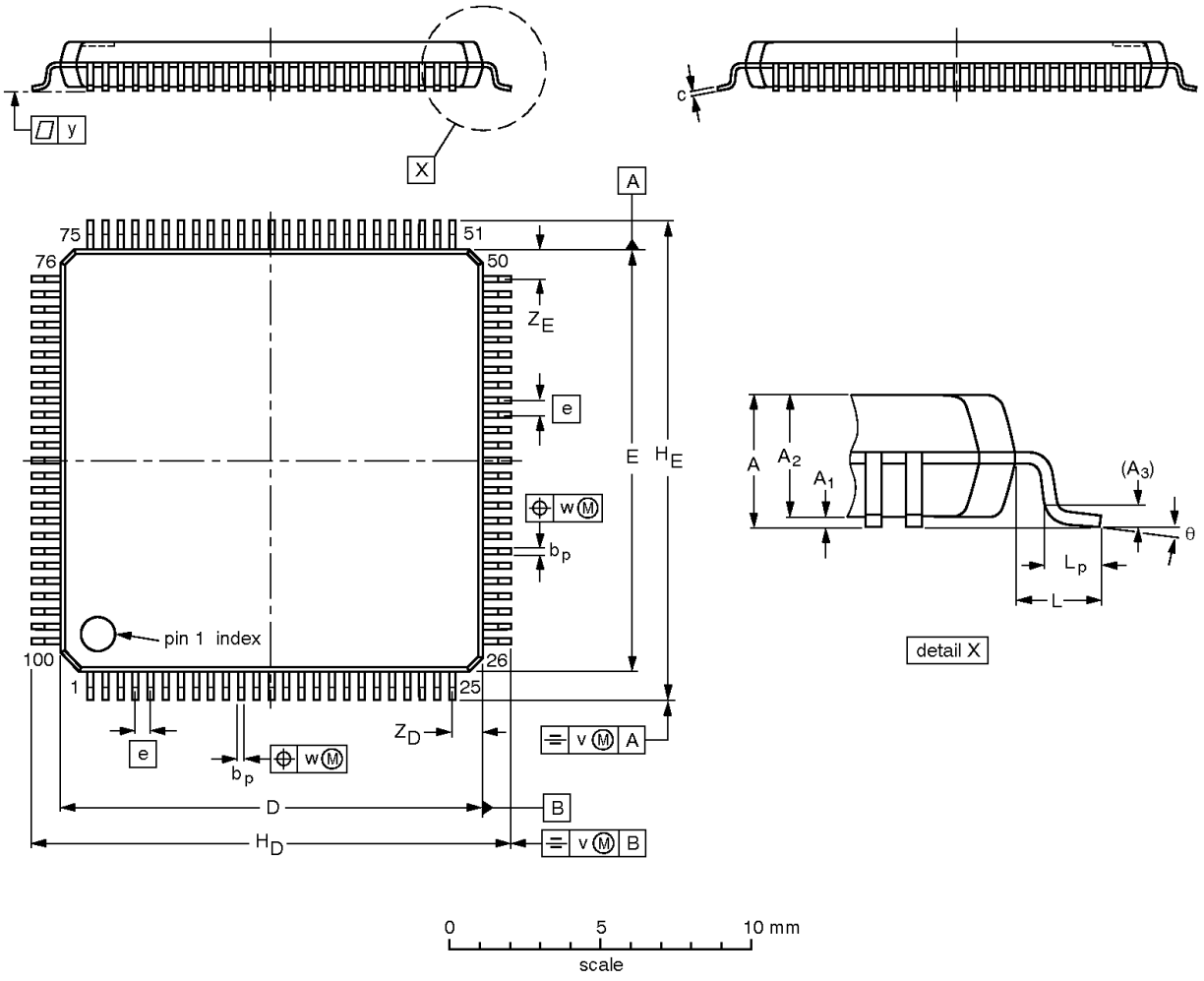


Figure 25. External WAIT Pin Timing

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.5 1.3	0.25	0.28 0.16	0.18 0.12	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1.0	0.75 0.45	0.2	0.12	0.1	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT407-1						~~95-12-19~~ 97-08-04

NOTES

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Data sheet status	Product status	Definition [1]
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