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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SCI
Peripherals	PWM, WDT
Number of I/O	29
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64f3694fpv

- Compact package

Package	Code	Body Size	Pin Pitch
LQFP-64	FP-64E	10.0 × 10.0 mm	0.5 mm
QFP-64	FP-64A	14.0 × 14.0 mm	0.8 mm
LQFP-48	FP-48F	10.0 × 10.0 mm	0.65 mm
LQFP-48	FP-48B	7.0 × 7.0 mm	0.5 mm
QFN-48	TNP-48	7.0 × 7.0 mm	0.5 mm

Only LQFP-64 (FP-64E) for H8/3694N package

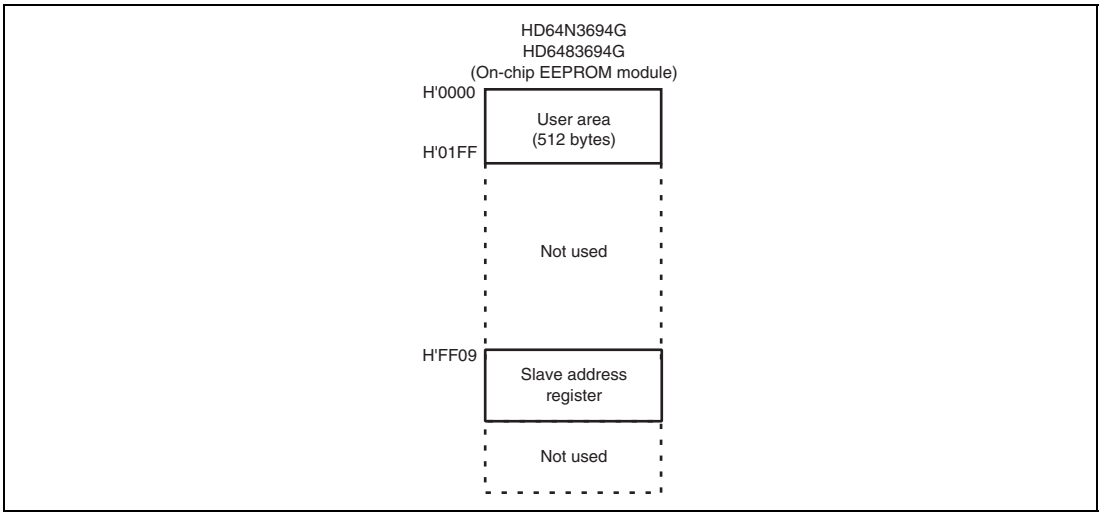


Figure 2.1 Memory Map (3)

Bit	Bit Name	Initial Value	R/W	Description
2	IWPF2	0	R/W	WKP2 Interrupt Request Flag [Setting condition] When $\overline{\text{WKP2}}$ pin is designated for interrupt input and the designated signal edge is detected. [Clearing condition] When IWPF2 is cleared by writing 0.
1	IWPF1	0	R/W	WKP1 Interrupt Request Flag [Setting condition] When $\overline{\text{WKP1}}$ pin is designated for interrupt input and the designated signal edge is detected. [Clearing condition] When IWPF1 is cleared by writing 0.
0	IWPF0	0	R/W	WKP0 Interrupt Request Flag [Setting condition] When $\overline{\text{WKP0}}$ pin is designated for interrupt input and the designated signal edge is detected. [Clearing condition] When IWPF0 is cleared by writing 0.

3.3 Reset Exception Handling

When the $\overline{\text{RES}}$ pin goes low, all processing halts and this LSI enters the reset. The internal state of the CPU and the registers of the on-chip peripheral modules are initialized by the reset. To ensure that this LSI is reset at power-up, hold the $\overline{\text{RES}}$ pin low until the clock pulse generator output stabilizes. To reset the chip during operation, hold the $\overline{\text{RES}}$ pin low for at least 10 system clock cycles. When the $\overline{\text{RES}}$ pin goes high after being held low for the necessary time, this LSI starts reset exception handling. The reset exception handling sequence is shown in figure 3.1.

The reset exception handling sequence is as follows. However, for the reset exception handling sequence of the product with on-chip power-on reset circuit, refer to section 18, Power-On Reset and Low-Voltage Detection Circuits (Optional).

1. Set the I bit in the condition code register (CCR) to 1.
2. The CPU generates a reset exception handling vector address (from H'0000 to H'0001), the data in that address is sent to the program counter (PC) as the start address, and program execution starts from that address.

Section 10 Timer A

Timer A is an 8-bit timer with interval timing and real-time clock time-base functions. The clock time-base function is available when a 32.768kHz crystal oscillator is connected. Figure 10.1 shows a block diagram of timer A.

10.1 Features

- Timer A can be used as an interval timer or a clock time base.
- An interrupt is requested when the counter overflows.
- Any of eight clock signals can be output from pin TMOW: 32.768 kHz divided by 32, 16, 8, or 4 (1 kHz, 2 kHz, 4 kHz, 8 kHz), or the system clock divided by 32, 16, 8, or 4.

Interval Timer

- Choice of eight internal clock sources (ϕ/8192, ϕ/4096, ϕ/2048, ϕ/512, ϕ/256, ϕ/128, ϕ/32, ϕ8)

Clock Time Base

- Choice of four overflow periods (1 s, 0.5 s, 0.25 s, 31.25 ms) when timer A is used as a clock time base (using a 32.768 kHz crystal oscillator).

13.3 Operation

The watchdog timer is provided with an 8-bit counter. If 1 is written to WDON while writing 0 to B2WI when the TCSRWE bit in TCSRWD is set to 1, TCWD begins counting up. (To operate the watchdog timer, two write accesses to TCSRWD are required.) When a clock pulse is input after the TCWD count value has reached H'FF, the watchdog timer overflows and an internal reset signal is generated. The internal reset signal is output for a period of 256 ϕ_{osc} clock cycles. TCWD is a writable counter, and when a value is set in TCWD, the count-up starts from that value. An overflow period in the range of 1 to 256 input clock cycles can therefore be set, according to the TCWD set value.

Figure 13.2 shows an example of watchdog timer operation.

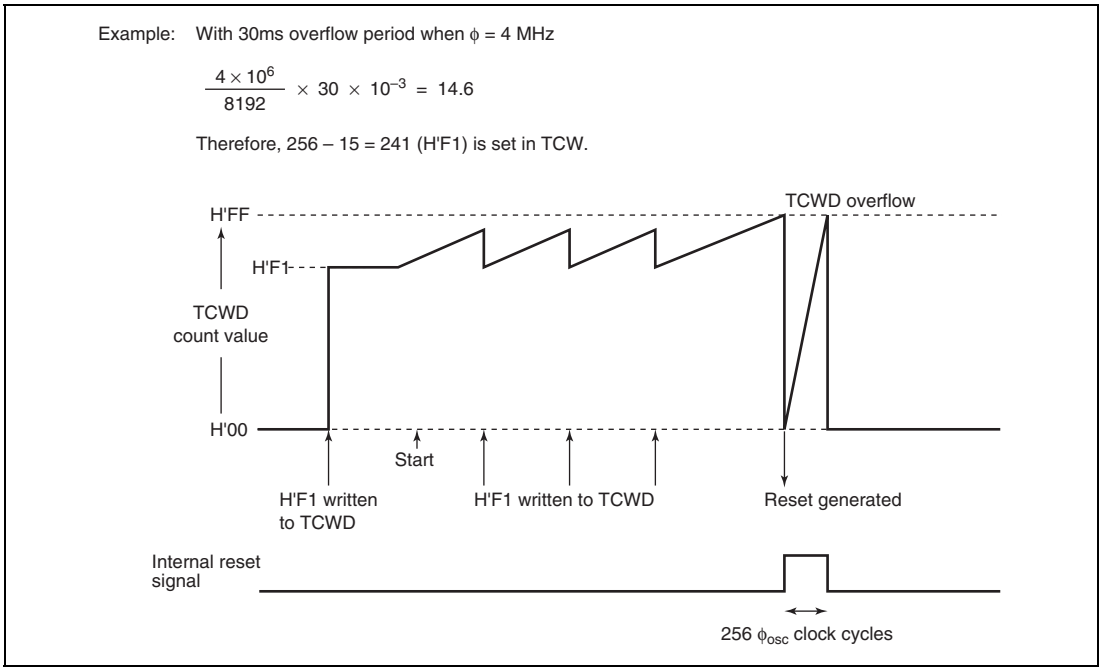
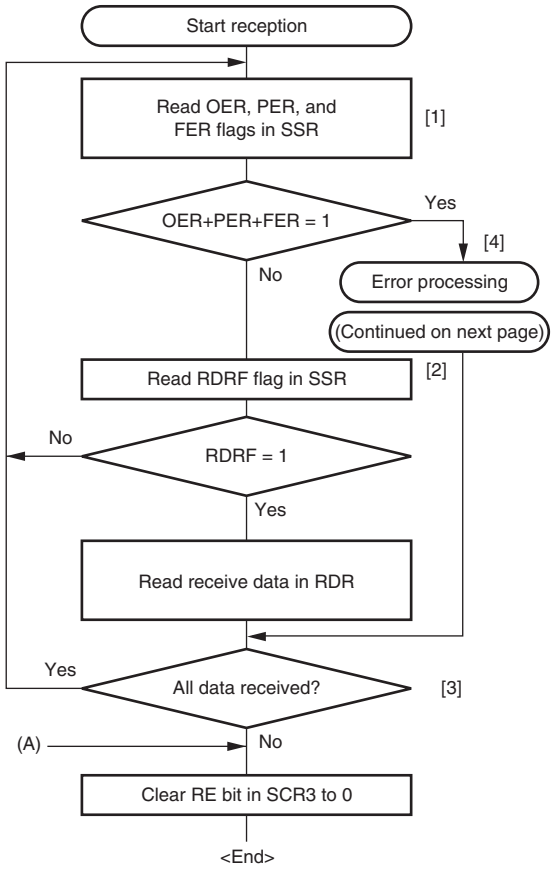


Figure 13.2 Watchdog Timer Operation Example

Table 14.3 Maximum Bit Rate for Each Frequency (Asynchronous Mode)

ϕ (MHz)	Maximum Bit Rate (bit/s)	n	N	ϕ (MHz)	Maximum Bit Rate (bit/s)	n	N
2	62500	0	0	8	250000	0	0
2.097152	65536	0	0	9.8304	307200	0	0
2.4576	76800	0	0	10	312500	0	0
3	93750	0	0	12	375000	0	0
3.6864	115200	0	0	12.288	384000	0	0
4	125000	0	0	14	437500	0	0
4.9152	153600	0	0	14.7456	460800	0	0
5	156250	0	0	16	500000	0	0
6	187500	0	0	17.2032	537600	0	0
6.144	192000	0	0	18	562500	0	0
7.3728	230400	0	0	20	625000	0	0



[1] Read the OER, PER, and FER flags in SSR to identify the error. If a receive error occurs, performs the appropriate error processing.

[2] Read SSR and check that RDRF = 1, then read the receive data in RDR. The RDRF flag is cleared automatically.

[3] To continue serial reception, before the stop bit for the current frame is received, read the RDRF flag and read RDR.
The RDRF flag is cleared automatically.

[4] If a receive error occurs, read the OER, PER, and FER flags in SSR to identify the error. After performing the appropriate error processing, ensure that the OER, PER, and FER flags are all cleared to 0. Reception cannot be resumed if any of these flags are set to 1. In the case of a framing error, a break can be detected by reading the value of the input port corresponding to the RxD pin.

Figure 14.8 Sample Serial Data Reception Flowchart (Asynchronous mode) (1)

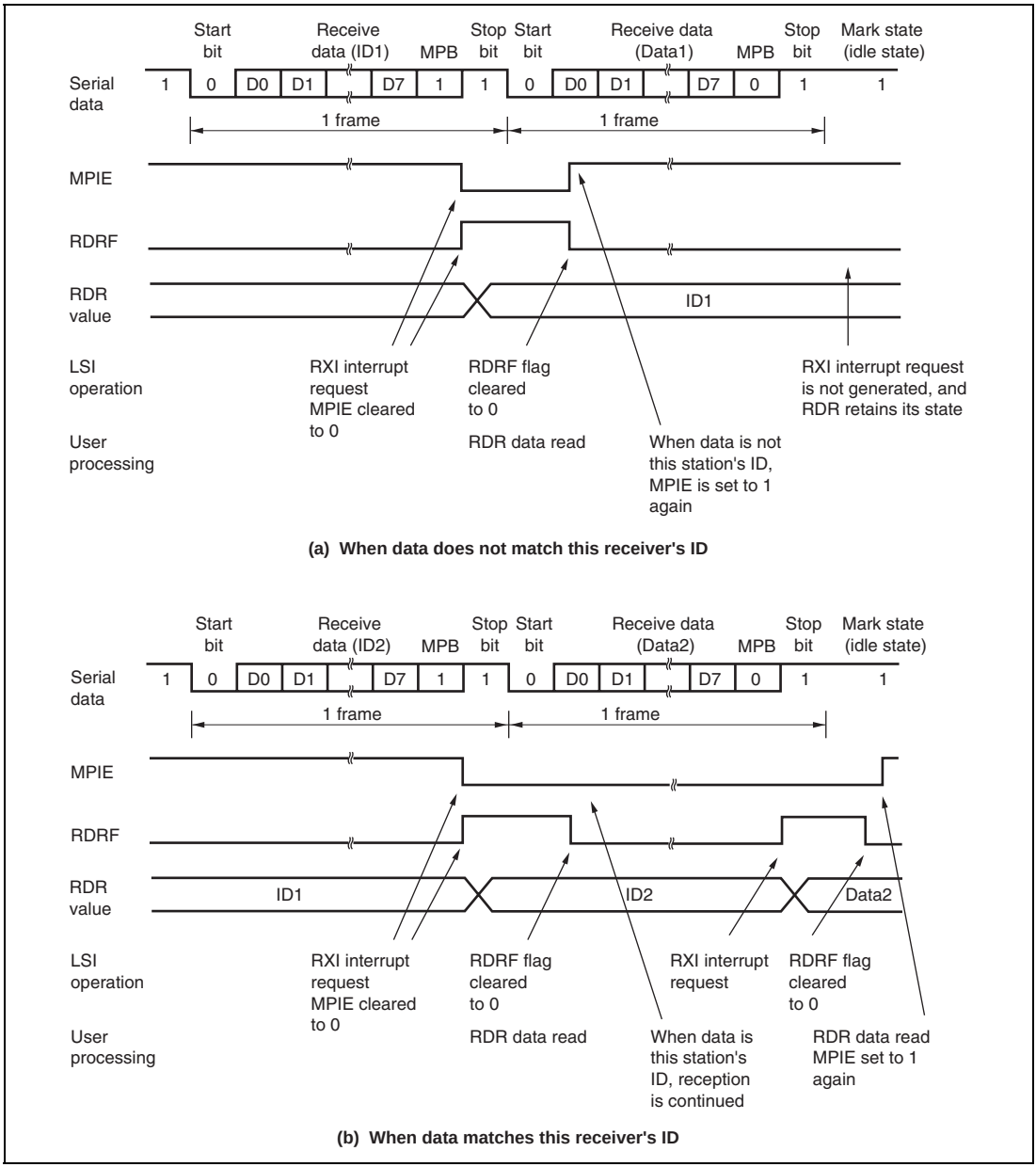


Figure 14.18 Example of SCI3 Operation in Reception Using Multiprocessor Format (Example with 8-Bit Data, Multiprocessor Bit, One Stop Bit)

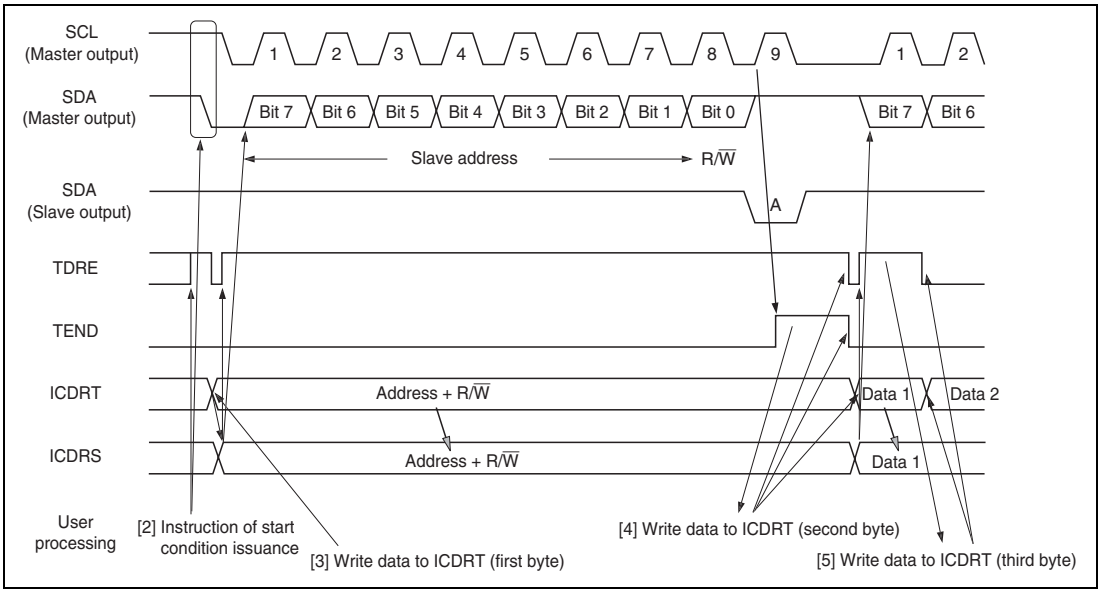


Figure 15.5 Master Transmit Mode Operation Timing (1)

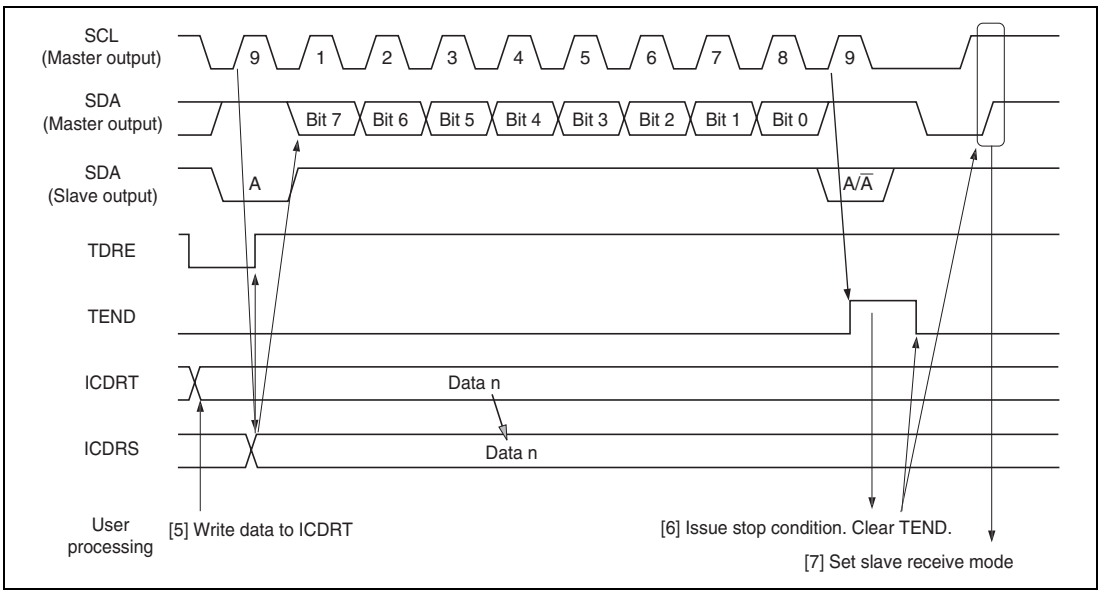


Figure 15.6 Master Transmit Mode Operation Timing (2)

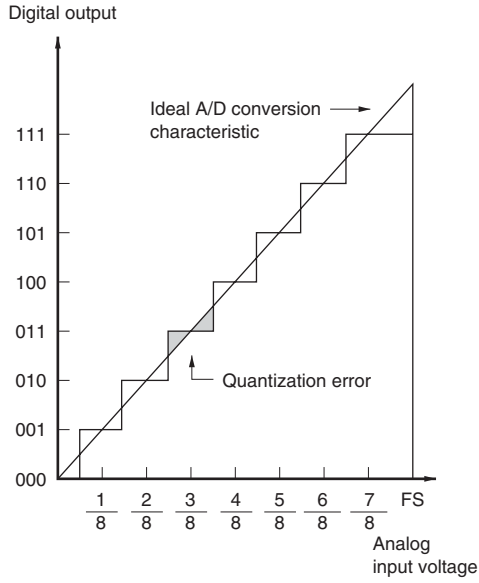


Figure 16.4 A/D Conversion Accuracy Definitions (1)

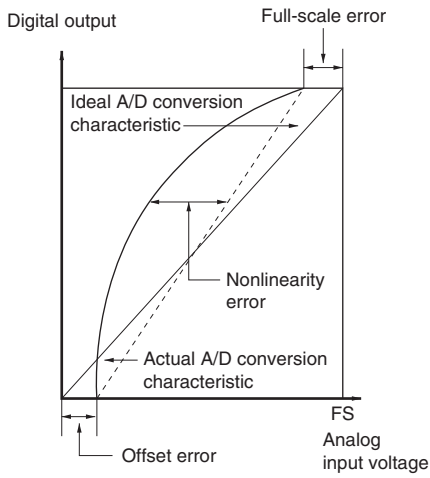


Figure 16.5 A/D Conversion Accuracy Definitions (2)

Register Name	Reset	Active	Sleep	Subactive	Subsleep	Standby	Module
PMR1	Initialized	—	—	—	—	—	I/O port
PMR5	Initialized	—	—	—	—	—	
PCR1	Initialized	—	—	—	—	—	
PCR2	Initialized	—	—	—	—	—	
PCR5	Initialized	—	—	—	—	—	
PCR7	Initialized	—	—	—	—	—	
PCR8	Initialized	—	—	—	—	—	
SYSCR1	Initialized	—	—	—	—	—	Power-down
SYSCR2	Initialized	—	—	—	—	—	Power-down
IEGR1	Initialized	—	—	—	—	—	Interrupts
IEGR2	Initialized	—	—	—	—	—	Interrupts
IENR1	Initialized	—	—	—	—	—	Interrupts
IRR1	Initialized	—	—	—	—	—	Interrupts
IWPR	Initialized	—	—	—	—	—	Interrupts
MSTCR1	Initialized	—	—	—	—	—	Power-down

- EEPROM

Register Name	Reset	Active	Sleep	Subactive	Subsleep	Standby	Module
EKR	—	—	—	—	—	—	EEPROM

Notes: — is not initialized

1. LVDC: Low-voltage detection circuits (optional)
2. WDT: Watchdog timer

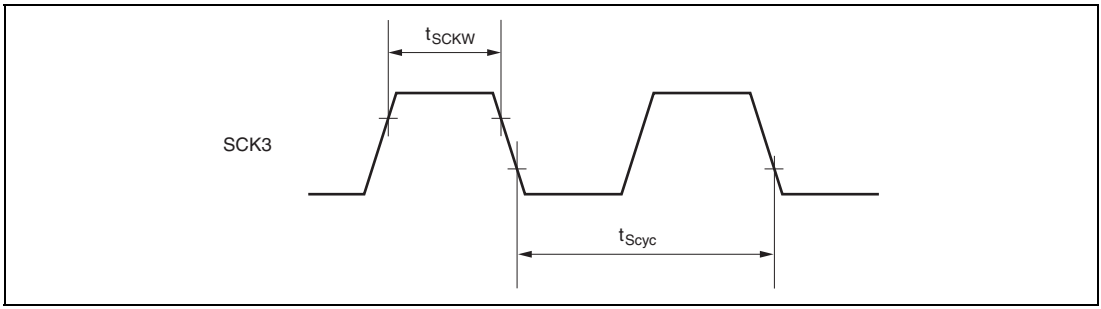
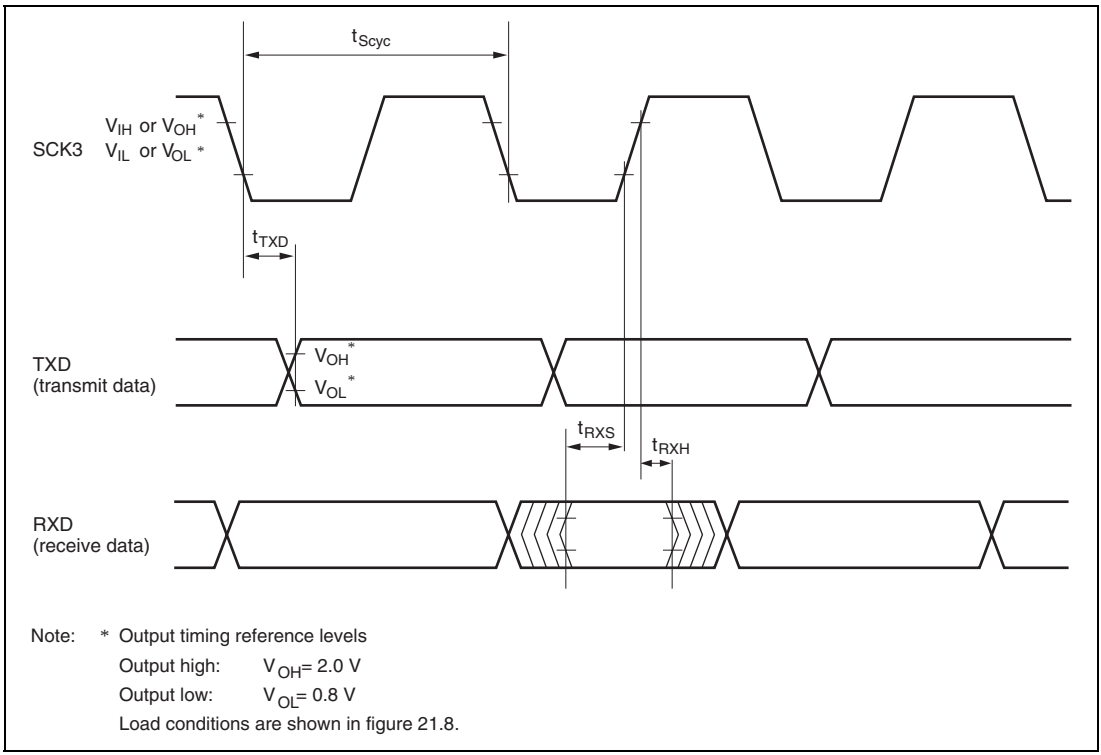


Figure 21.5 SCK3 Input Clock Timing



Note: * Output timing reference levels
Output high: V_{OH}= 2.0 V
Output low: V_{OL}= 0.8 V
Load conditions are shown in figure 21.8.

Figure 21.6 SCI Input/Output Timing in Clocked Synchronous Mode

Table A.3 Number of Cycles in Each Instruction

Execution Status (Instruction Cycle)		Access Location	
		On-Chip Memory	On-Chip Peripheral Module
Instruction fetch	S_I	2	—
Branch address read	S_J		
Stack operation	S_K		
Byte data access	S_L		2 or 3*
Word data access	S_M		2 or 3*
Internal operation	S_N	1	

Note: * Depends on which on-chip peripheral module is accessed. See section 20.1, Register Addresses (Address Order).

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
Bcc	BLT d:8	2					
	BGT d:8	2					
	BLE d:8	2					
	BRA d:16(BT d:16)	2					2
	BRN d:16(BF d:16)	2					2
	BHI d:16	2					2
	BLS d:16	2					2
	BCC d:16(BHS d:16)	2					2
	BCS d:16(BLO d:16)	2					2
	BNE d:16	2					2
	BEQ d:16	2					2
	BVC d:16	2					2
	BVS d:16	2					2
	BPL d:16	2					2
	BMI d:16	2					2
	BGE d:16	2					2
	BLT d:16	2					2
	BGT d:16	2					2
	BLE d:16	2					2
BCLR	BCLR #xx:3, Rd	1					
	BCLR #xx:3, @ERd	2			2		
	BCLR #xx:3, @aa:8	2			2		
	BCLR Rn, Rd	1					
	BCLR Rn, @ERd	2			2		
	BCLR Rn, @aa:8	2			2		
BIAND	BIAND #xx:3, Rd	1					
	BIAND #xx:3, @ERd	2			1		
	BIAND #xx:3, @aa:8	2			1		
BILD	BILD #xx:3, Rd	1					
	BILD #xx:3, @ERd	2			1		
	BILD #xx:3, @aa:8	2			1		

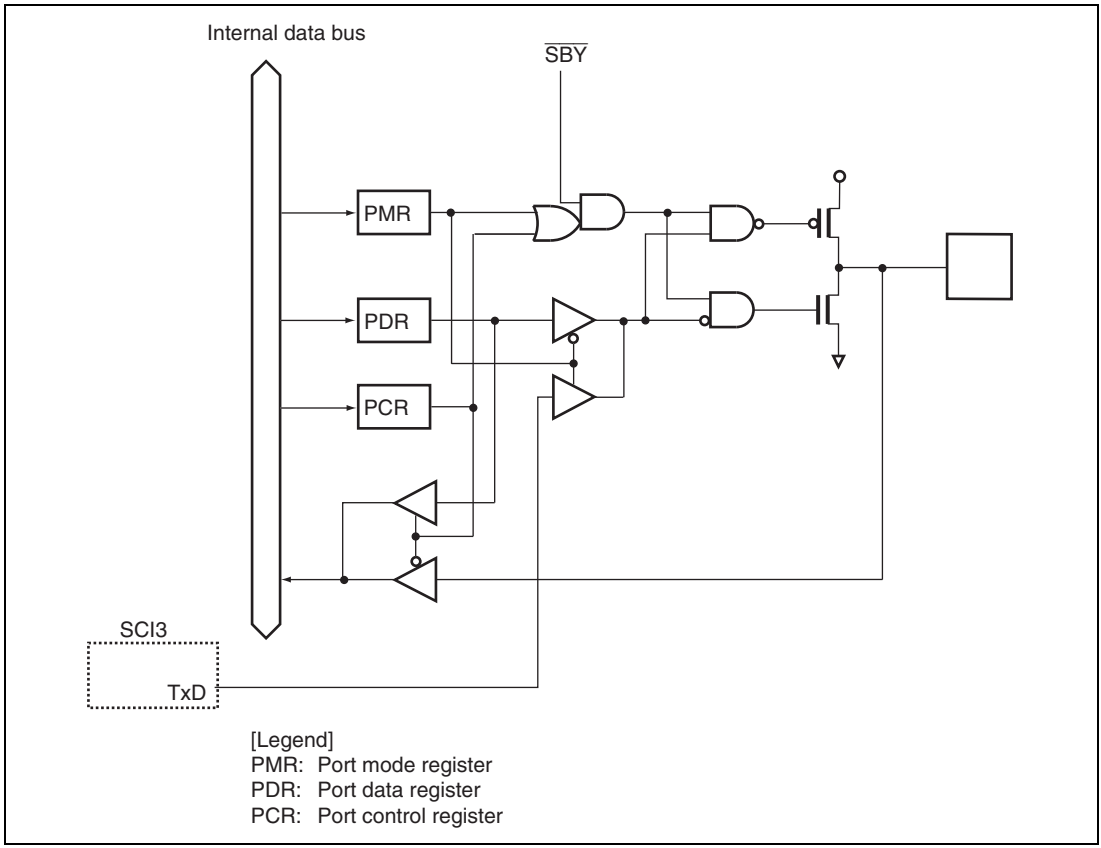


Figure B.5 Port 2 Block Diagram (P22)

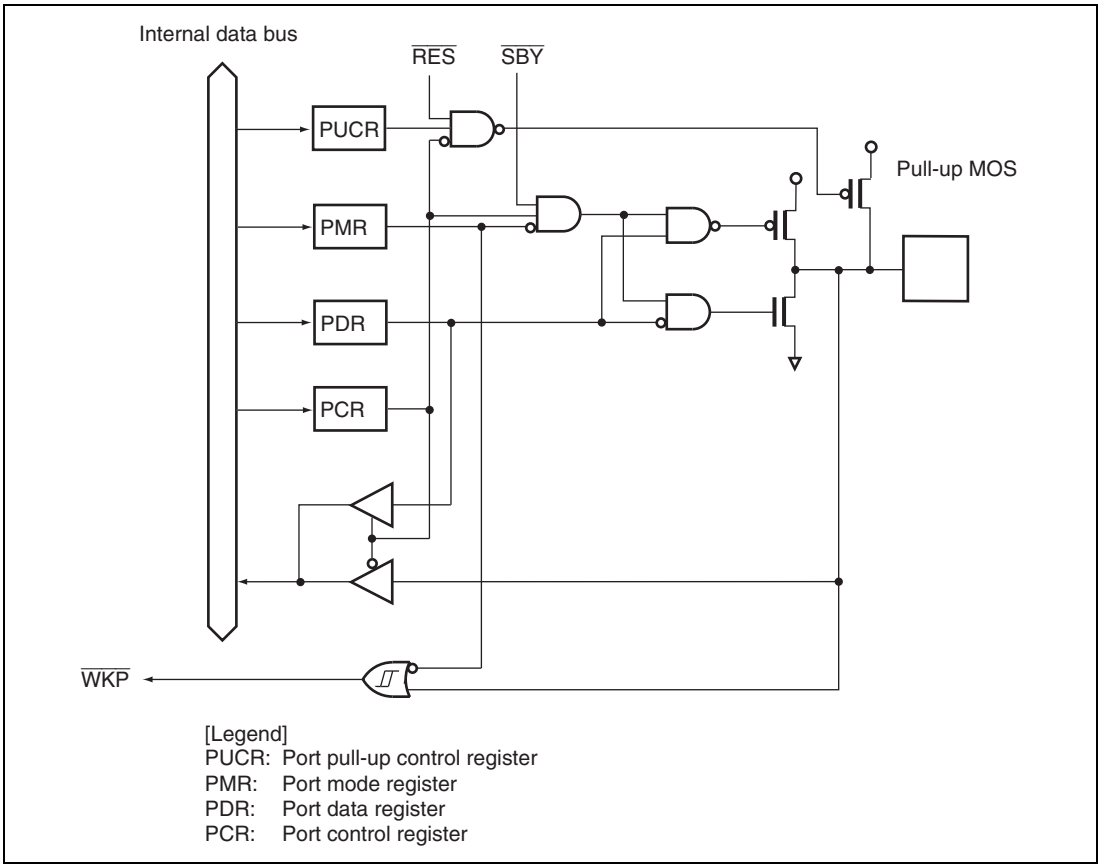


Figure B.10 Port 5 Block Diagram (P54 to P50)

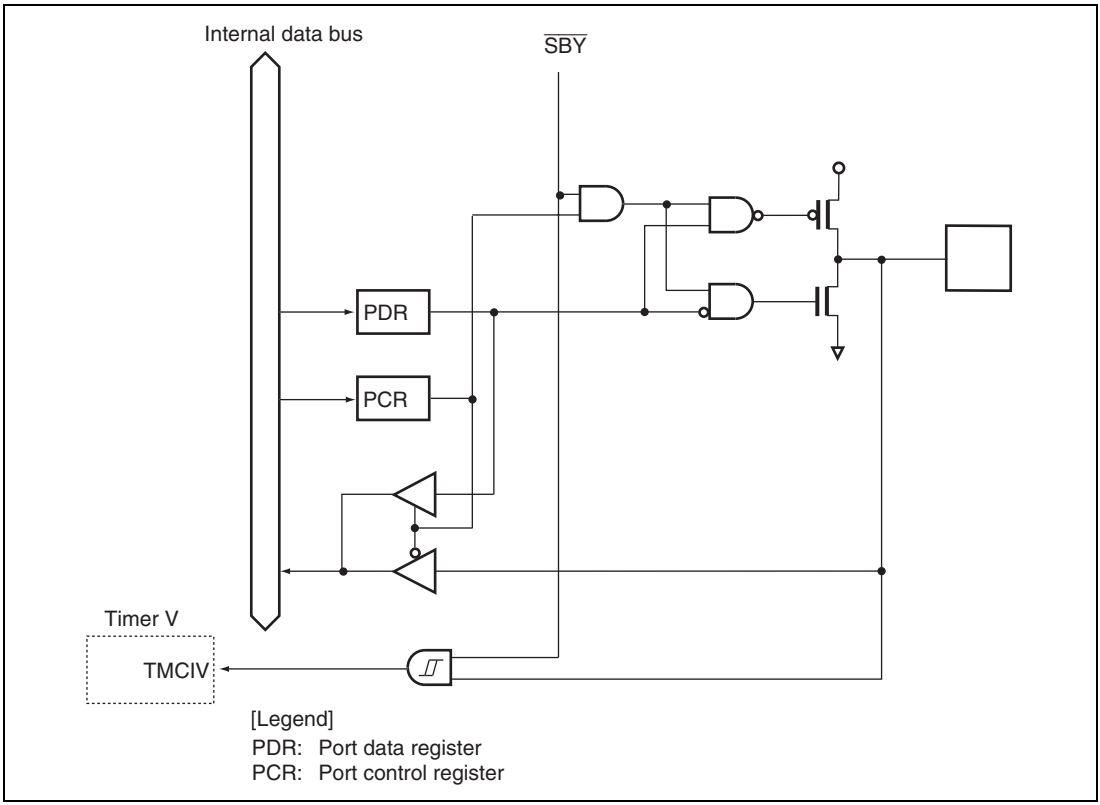
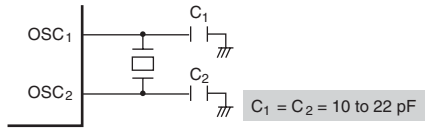
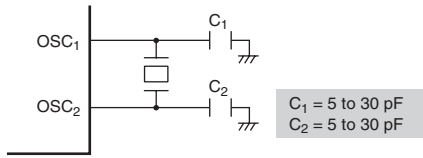


Figure B.12 Port 7 Block Diagram (P75)

Item	Page	Revision (See Manual for Details)
Section 5 Clock Pulse Generators Figure 5.3 Typical Connection to Crystal Resonator	70	
Figure 5.5 Typical Connection to Ceramic Resonator	71	
Section 6 Power-Down Modes 6.1.1 System Control Register 1 (SYSCR1)	76	**Bit** / **Bit Name** / **Description** 3 / NESEL / Noise Elimination Sampling Frequency Select The subclock pulse generator generates the watch clock signal (ϕ_w) and the system clock pulse generator generates the oscillator clock (ϕ_{OSC}). This bit selects the sampling frequency of the oscillator clock when the watch clock signal (ϕ_w) is sampled. When ϕ_{OSC} = 4 to 20 MHz, clear NESEL to 0.
Section 8 RAM	107	Note: * When the E7 or E8 is used, area H'F780 to H'FB7F must not be accessed.
Section 13 Watchdog Timer 13.2.1 Timer Control/Status Register WD (TCSRWD)	184	**Bit** / **Bit Name** / **Description** 4 / TCSRWE / Timer Control/Status Register WD Write Enable