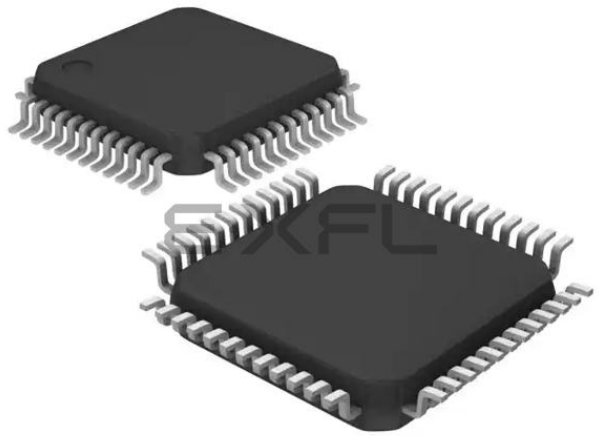

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SCI
Peripherals	PWM, WDT
Number of I/O	29
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64f3694fyv

2.3 Data Formats

The H8/300H CPU can process 1-bit, 4-bit (BCD), 8-bit (byte), 16-bit (word), and 32-bit (longword) data. Bit-manipulation instructions operate on 1-bit data by accessing bit n (n = 0, 1, 2, …, 7) of byte operand data. The DAA and DAS decimal-adjust instructions treat byte data as two digits of 4-bit BCD data.

2.3.1 General Register Data Formats

Figure 2.5 shows the data formats in general registers.

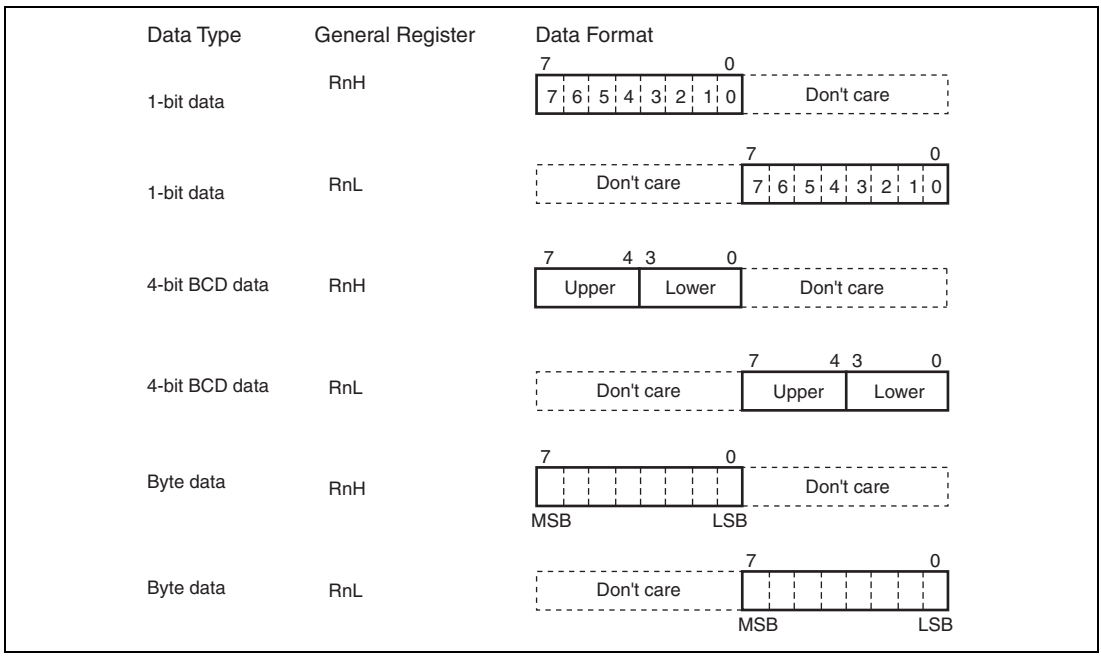


Figure 2.5 General Register Data Formats (1)

- Prior to executing BCLR instruction

```
MOV.B   #3F,  R0L
MOV.B   R0L,  @RAM0
MOV.B   R0L,  @PCR5
```

The PCR5 value (H'3F) is written to a work area in memory (RAM0) as well as to PCR5.

	P57	**P56**	**P55**	**P54**	**P53**	**P52**	**P51**	**P50**
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	Low level
PCR5	0	0	1	1	1	1	1	1
PDR5	1	0	0	0	0	0	0	0
RAM0	0	0	1	1	1	1	1	1

- BCLR instruction executed

```
BCLR    #0,     @RAM0
```

The BCLR instructions executed for the PCR5 work area (RAM0).

- After executing BCLR instruction

```
MOV.B   @RAM0, R0L
MOV.B   R0L,  @PCR5
```

The work area (RAM0) value is written to PCR5.

	P57	**P56**	**P55**	**P54**	**P53**	**P52**	**P51**	**P50**
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	High level
PCR5	0	0	1	1	1	1	1	0
PDR5	1	0	0	0	0	0	0	0
RAM0	0	0	1	1	1	1	1	0

3.5 Usage Notes

3.5.1 Interrupts after Reset

If an interrupt is accepted after a reset and before the stack pointer (SP) is initialized, the PC and CCR will not be saved correctly, leading to a program crash. To prevent this, all interrupt requests, including NMI, are disabled immediately after a reset. Since the first instruction of a program is always executed immediately after the reset state ends, make sure that this instruction initializes the stack pointer (example: MOV.W #xx: 16, SP).

3.5.2 Notes on Stack Area Use

When word data is accessed, the least significant bit of the address is regarded as 0. Access to the stack always takes place in word size, so the stack pointer (SP: R7) should never indicate an odd address. Use PUSH Rn (MOV.W Rn, @–SP) or POP Rn (MOV.W @SP+, Rn) to save or restore register values.

3.5.3 Notes on Rewriting Port Mode Registers

When a port mode register is rewritten to switch the functions of external interrupt pins, $\overline{\text{IRQ3}}$ to $\overline{\text{IRQ0}}$, and $\overline{\text{WKP5}}$ to $\overline{\text{WKP0}}$, the interrupt request flag may be set to 1.

When switching a pin function, mask the interrupt before setting the bit in the port mode register. After accessing the port mode register, execute at least one instruction (e.g., NOP), then clear the interrupt request flag from 1 to 0.

Figure 3.4 shows a port mode register setting and interrupt request flag clearing procedure.

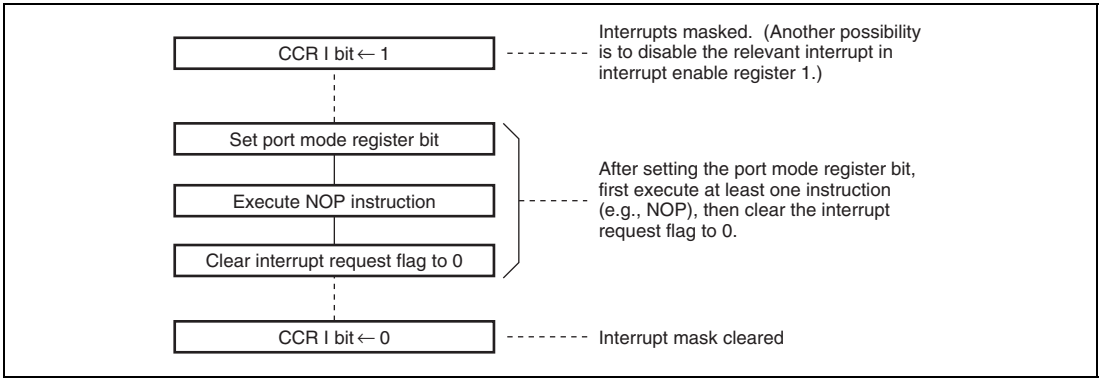


Figure 3.4 Port Mode Register Setting and Interrupt Request Flag Clearing Procedure

Table 7.7 Flash Memory Operating States

	Flash Memory Operating State	
LSI Operating State	**PDWND = 0 (Initial value)**	**PDWND = 1**
Active mode	Normal operating mode	Normal operating mode
Subactive mode	Power-down mode	Normal operating mode
Sleep mode	Normal operating mode	Normal operating mode
Subsleep mode	Standby mode	Standby mode
Standby mode	Standby mode	Standby mode

P15/$\overline{\text{IRQ1}}$ pin

Register	PMR1	PCR1	
Bit Name	**IRQ1**	**PCR15**	**Pin Function**
Setting value	0	0	P15 input pin
		1	P15 output pin
	1	X	$\overline{\text{IRQ1}}$ input pin

Legend: X: Don't care.

P14/$\overline{\text{IRQ0}}$ pin

Register	PMR1	PCR1	
Bit Name	**IRQ0**	**PCR14**	**Pin Function**
Setting value	0	0	P14 input pin
		1	P14 output pin
	1	X	$\overline{\text{IRQ0}}$ input pin

Legend: X: Don't care.

P12 pin

Register	PCR1	
Bit Name	**PCR12**	**Pin Function**
Setting value	0	P12 input pin
	1	P12 output pin

P11 pin

Register	PCR1	
Bit Name	**PCR11**	**Pin Function**
Setting value	0	P11 input pin
	1	P11 output pin

11.3.3 Timer Control Register V0 (TCRV0)

TCRV0 selects the input clock signals of TCNTV, specifies the clearing conditions of TCNTV, and controls each interrupt request.

Bit	Bit Name	Initial Value	R/W	Description
7	CMIEB	0	R/W	Compare Match Interrupt Enable B When this bit is set to 1, interrupt request from the CMFB bit in TCSRV is enabled.
6	CMIEA	0	R/W	Compare Match Interrupt Enable A When this bit is set to 1, interrupt request from the CMFA bit in TCSRV is enabled.
5	OVIE	0	R/W	Timer Overflow Interrupt Enable When this bit is set to 1, interrupt request from the OVF bit in TCSRV is enabled.
4	CCLR1	0	R/W	Counter Clear 1 and 0
3	CCLR0	0	R/W	These bits specify the clearing conditions of TCNTV. 00: Clearing is disabled 01: Cleared by compare match A 10: Cleared by compare match B 11: Cleared on the rising edge of the TMRIV pin. The operation of TCNTV after clearing depends on TRGE in TCRV1.
2	CKS2	0	R/W	Clock Select 2 to 0 These bits select clock signals to input to TCNTV and the counting condition in combination with ICKS0 in TCRV1. Refer to table 11.2.
1	CKS1	0	R/W	
0	CKS0	0	R/W	

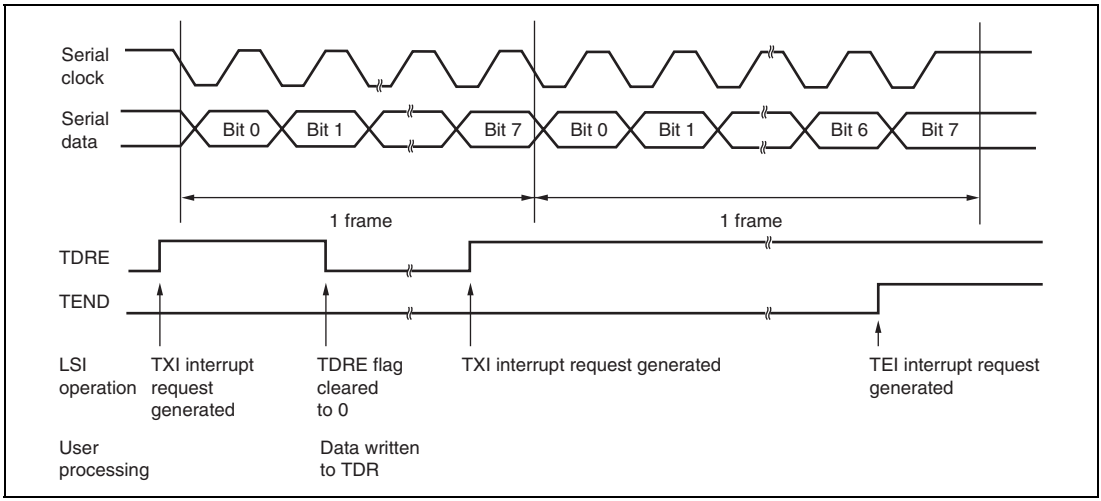


Figure 14.10 Example of SCI3 Operation in Transmission in Clocked Synchronous Mode

Bit	Bit Name	Initial Value	R/W	Description
4	SDAOP	1	R/W	SDAO Write Protect This bit controls change of output level of the SDA pin by modifying the SDAO bit. To change the output level, clear SDAO and SDAOP to 0 or set SDAO to 1 and clear SDAOP to 0 by the MOV instruction. This bit is always read as 1.
3	SCLO	1	R	This bit monitors SCL output level. When SCLO is 1, SCL pin outputs high. When SCLO is 0, SCL pin outputs low.
2	—	1	—	Reserved This bit is always read as 1, and cannot be modified.
1	IICRST	0	R/W	IIC Control Part Reset This bit resets the control part except for I²C registers. If this bit is set to 1 when hang-up occurs because of communication failure during I²C operation, I²C control part can be reset without setting ports and initializing registers.
0	—	1	—	Reserved This bit is always read as 1, and cannot be modified.

15.3.3 I²C Bus Mode Register (ICMR)

ICMR selects whether the MSB or LSB is transferred first, performs master mode wait control, and selects the transfer bit count.

Bit	Bit Name	Initial Value	R/W	Description
7	MLS	0	R/W	MSB-First/LSB-First Select 0: MSB-first 1: LSB-first Set this bit to 0 when the I²C bus format is used.
6	WAIT	0	R/W	Wait Insertion Bit In master mode with the I²C bus format, this bit selects whether to insert a wait after data transfer except the acknowledge bit. When WAIT is set to 1, after the fall of the clock for the final data bit, low period is extended for two transfer clocks. If WAIT is cleared to 0, data and acknowledge bits are transferred consecutively with no wait inserted. The setting of this bit is invalid in slave mode with the I²C bus format or with the clocked synchronous serial format.

3. Read ICDRR every time RDRF is set. If 8th receive clock pulse falls while RDRF is 1, SCL is fixed low until ICDRR is read. The change of the acknowledge before reading ICDRR, to be returned to the master device, is reflected to the next transmit frame.
4. The last byte data is read by reading ICDRR.

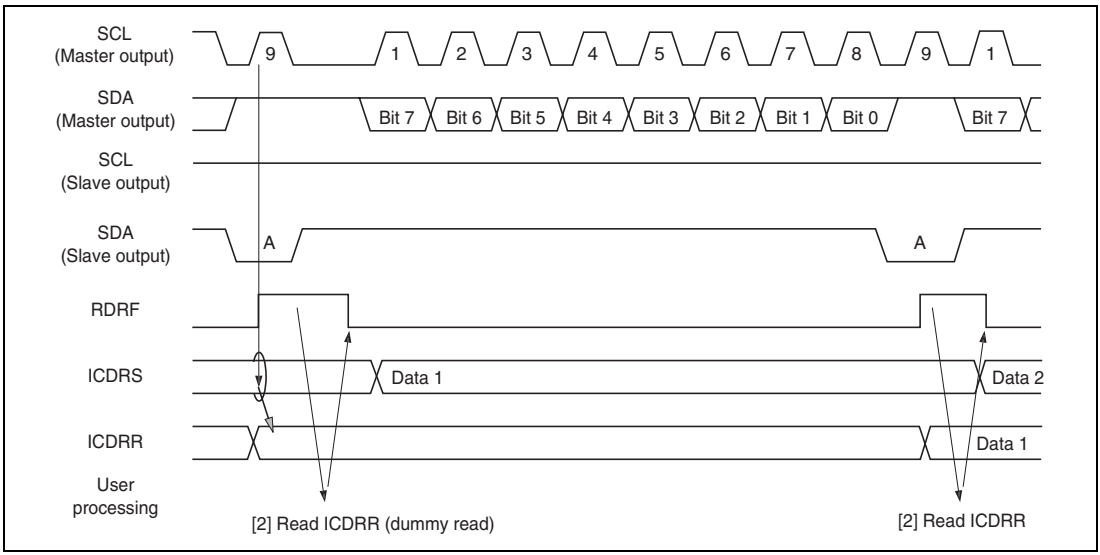


Figure 15.11 Slave Receive Mode Operation Timing (1)

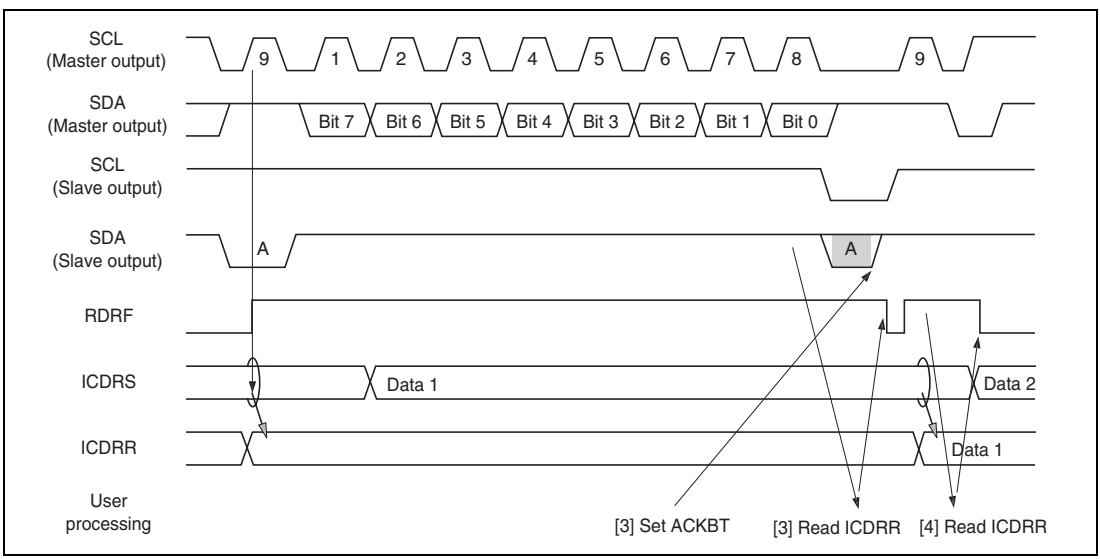


Figure 15.12 Slave Receive Mode Operation Timing (2)

15.4.6 Clocked Synchronous Serial Format

This module can be operated with the clocked synchronous serial format, by setting the FS bit in SAR to 1. When the MST bit in ICCR1 is 1, the transfer clock output from SCL is selected. When MST is 0, the external clock input is selected.

Data Transfer Format

Figure 15.13 shows the clocked synchronous serial transfer format.

The transfer data is output from the rise to the fall of the SCL clock, and the data at the rising edge of the SCL clock is guaranteed. The MLS bit in ICMR sets the order of data transfer, in either the MSB first or LSB first. The output level of SDA can be changed during the transfer wait, by the SDAO bit in ICCR2.

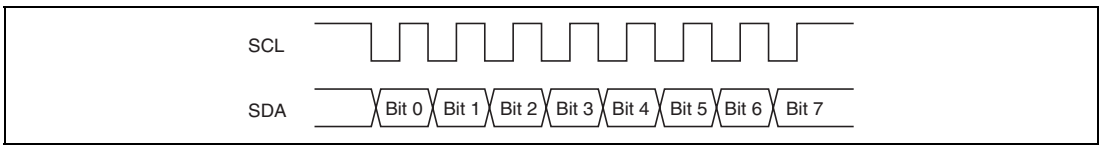


Figure 15.13 Clocked Synchronous Serial Transfer Format

Transmit Operation

In transmit mode, transmit data is output from SDA, in synchronization with the fall of the transfer clock. The transfer clock is output when MST in ICCR1 is 1, and is input when MST is 0. For transmit mode operation timing, refer to figure 15.14. The transmission procedure and operations in transmit mode are described below.

1. Set the ICE bit in ICCR1 to 1. Set the MST and CKS3 to CKS0 bits in ICCR1 to 1. (Initial setting)
2. Set the TRS bit in ICCR1 to select the transmit mode. Then, TDRE in ICSR is set.
3. Confirm that TDRE has been set. Then, write the transmit data to ICDRT. The data is transferred from ICDRT to ICDRS, and TDRE is set automatically. The continuous transmission is performed by writing data to ICDRT every time TDRE is set. When changing from transmit mode to receive mode, clear TRS while TDRE is 1.

15.5 Interrupt Request

There are six interrupt requests in this module; transmit data empty, transmit end, receive data full, NACK receive, STOP recognition, and arbitration lost/overrun. Table 15.3 shows the contents of each interrupt request.

Table 15.3 Interrupt Requests

Interrupt Request	Abbreviation	Interrupt Condition	I²C Mode	Clocked Synchronous Mode
Transmit Data Empty	TXI	(TDRE = 1) • (TIE = 1)	○	○
Transmit End	TEI	(TEND = 1) • (TEIE = 1)	○	○
Receive Data Full	RXI	(RDRF = 1) • (RIE = 1)	○	○
STOP Recognition	STPI	(STOP = 1) • (STIE = 1)	○	×
NACK Receive	NAKI	{(NACKF = 1) + (AL = 1)} • (NAKIE = 1)	○	×
Arbitration Lost/Overrun			○	○

When interrupt conditions described in table 15.3 are 1 and the I bit in CCR is 0, the CPU executes an interrupt exception processing. Interrupt sources should be cleared in the exception processing. TDRE and TEND are automatically cleared to 0 by writing the transmit data to ICDRT. RDRF are automatically cleared to 0 by reading ICDRR. TDRE is set to 1 again at the same time when transmit data is written to ICDRT. When TDRE is cleared to 0, then an excessive data of one byte may be transmitted.

Section 17 EEPROM

The H8/3694N has an on-chip 512-byte EEPROM. The block diagram of the EEPROM is shown in figure 17.1.

17.1 Features

- Two writing methods:
  1-byte write
  Page write: Page size 8 bytes
- Three reading methods:
  Current address read
  Random address read
  Sequential read
- Acknowledge polling possible
- Write cycle time:
  10 ms (power supply voltage Vcc = 2.7 V or more)
- Write/Erase endurance:
  10^4 cycles/byte (byte write mode), 10^5 cycles/page (page write mode)
- Data retention:
  10 years after the write cycle of 10^4 cycles (page write mode)
- Interface with the CPU
  I^2C bus interface (complies with the standard of Philips Corporation)
  Device code 1010
  Sleep address code can be changed (initial value: 000)
  The I^2C bus is open to the outside, so the EEPROM can be directly accessed from the outside.

17.4.7 Write Operations

There are two types write operations; byte write operation and page write operation. To initiate the write operation, input 0 to R/$\overline{W}$ code following the slave address.

1. Byte Write

   A write operation requires an 8-bit data of a 7-bit slave address with R/$\overline{W}$ code = "0". Then the EEPROM sends acknowledgement "0" at the ninth bit. This enters the write mode. Then, two bytes of the memory address are received from the MSB side in the order of upper and lower. Upon receipt of one-byte memory address, the EEPROM sends acknowledgement "0" and receives a following a one-byte write data. After receipt of write data, the EEPROM sends acknowledgement "0". If the EEPROM receives a stop condition, the EEPROM enters an internally controlled write cycle and terminates receipt of SCL and SDA inputs until completion of the write cycle. The EEPROM returns to a standby mode after completion of the write cycle.

   The byte write operation is shown in figure 17.3.

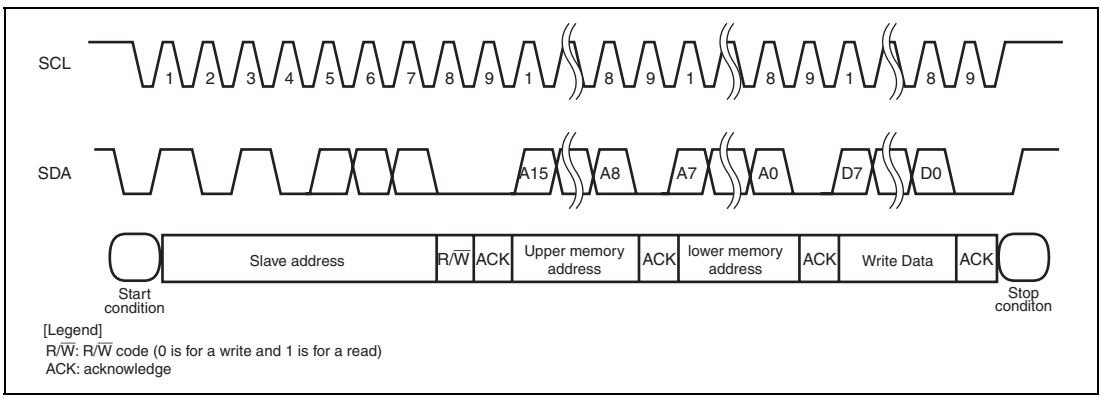


Figure 17.3 Byte Write Operation

2. Page Write

   This LSI is capable of the page write operation which allows any number of bytes up to 8 bytes to be written in a single write cycle. The write data is input in the same sequence as the byte write in the order of a start condition, slave address + R/$\overline{W}$ code, memory address (n), and write data (Dn) with every ninth bit acknowledgement "0" output. The EEPROM enters the page write operation if the EEPROM receives more write data (Dn+1) is input instead of receiving a stop condition after receiving the write data (Dn). LSB 3 bits (A2 to A0) in the EEPROM address are automatically incremented to be the (n+1) address upon receiving write data (Dn+1). Thus the write data can be received sequentially.

18.3 Operation

18.3.1 Power-On Reset Circuit

Figure 18.2 shows the timing of the operation of the power-on reset circuit. As the power-supply voltage rises, the capacitor which is externally connected to the $\overline{\text{RES}}$ pin is gradually charged via the on-chip pull-up resistor (typ. 150 kΩ). Since the state of the $\overline{\text{RES}}$ pin is transmitted within the chip, the prescaler S and the entire chip are in their reset states. When the level on the $\overline{\text{RES}}$ pin reaches the specified value, the prescaler S is released from its reset state and it starts counting. The OVF signal is generated to release the internal reset signal after the prescaler S has counted 131,072 clock (ϕ) cycles. The noise cancellation circuit of approximately 100 ns is incorporated to prevent the incorrect operation of the chip by noise on the $\overline{\text{RES}}$ pin.

To achieve stable operation of this LSI, the power supply needs to rise to its full level and settles within the specified time. The maximum time required for the power supply to rise and settle after power has been supplied (t_{PWON}) is determined by the oscillation frequency (f_{OSC}) and capacitance which is connected to $\overline{\text{RES}}$ pin ($C_{\overline{\text{RES}}}$). If t_{PWON} means the time required to reach 90 % of power supply voltage, the power supply circuit should be designed to satisfy the following formula.

$$t_{PWON}\ (\text{ms}) \leq 90 \times C_{\overline{\text{RES}}}\ (\mu\text{F}) + 162/f_{OSC}\ (\text{MHz})$$

($t_{PWON} \leq 3000$ ms, $C_{\overline{\text{RES}}} \geq 0.22$ μF, and $f_{OSC} = 10$ in 2-MHz to 10-MHz operation)

Note that the power supply voltage (Vcc) must fall below Vpor = 100 mV and rise after charge on the $\overline{\text{RES}}$ pin is removed. To remove charge on the $\overline{\text{RES}}$ pin, it is recommended that the diode should be placed near Vcc. If the power supply voltage (Vcc) rises from the point above Vpor, a power-on reset may not occur.

Section 21 Electrical Characteristics

21.1 Absolute Maximum Ratings

Table 21.1 Absolute Maximum Ratings

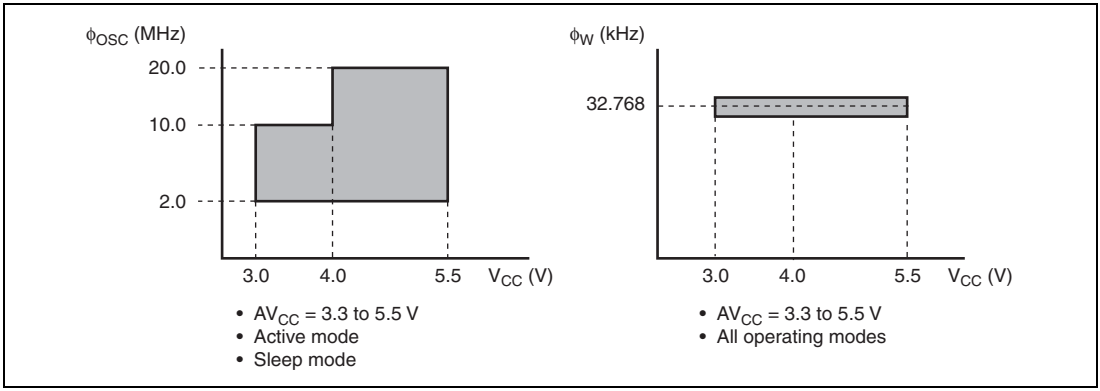
Item		Symbol	Value	Unit	Note
Power supply voltage		V_{CC}	–0.3 to +7.0	V	*
Analog power supply voltage		AV_{CC}	–0.3 to +7.0	V	
Input voltage	Ports other than ports B and X1	V_{IN}	–0.3 to V_{CC} +0.3	V	
	Port B		–0.3 to AV_{CC} +0.3	V	
	X1		–0.3 to 4.3	V	
Operating temperature		T_{opr}	–20 to +75	°C	
Storage temperature		T_{stg}	–55 to +125	°C	

Note: * Permanent damage may result if maximum ratings are exceeded. Normal operation should be under the conditions specified in Electrical Characteristics. Exceeding these values can result in incorrect operation and reduced reliability.

21.2 Electrical Characteristics (F-ZTAT™ Version, EEPROM Stacked F-ZTAT™ Version)

21.2.1 Power Supply Voltage and Operating Ranges

Power Supply Voltage and Oscillation Frequency Range



21.2.2 DC Characteristics

Table 21.2 DC Characteristics (1)

V_{CC} = 3.0 to 5.5 V, V_{SS} = 0.0 V, T_a = –20 to +75°C, unless otherwise indicated.

				Values				
Item	**Symbol**	**Applicable Pins**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**	**Notes**
Input high voltage	V_{IH}	$\overline{RES}$, $\overline{NMI}$, $\overline{WKP0}$ to $\overline{WKP5}$, $\overline{IRQ0}$ to $\overline{IRQ3}$, $\overline{ADTRG}$,TMRIV, TMCIV, FTCI, FTIOA to FTIOD, SCK3, TRGV	V_{cc} = 4.0 to 5.5 V	$V_{cc}\times 0.8$	—	V_{cc} + 0.3	V	
				$V_{cc}\times 0.9$	—	V_{cc} + 0.3		
		RXD, SCL, SDA, P10 to P12, P14 to P17, P20 to P22, P50 to P57, P74 to P76, P80 to P87	V_{cc} = 4.0 to 5.5 V	$V_{cc}\times 0.7$	—	V_{cc} + 0.3	V	
				$V_{cc}\times 0.8$	—	V_{cc} + 0.3		
		PB0 to PB7	V_{cc} = 4.0 to 5.5 V	$V_{cc}\times 0.7$	—	AV_{cc} + 0.3	V	
				$V_{cc}\times 0.8$	—	AV_{cc} + 0.3		
		OSC1	V_{cc} = 4.0 to 5.5 V	V_{cc} – 0.5	—	V_{cc} + 0.3	V	
				V_{cc} – 0.3	—	V_{cc} + 0.3		
Input low voltage	V_{IL}	$\overline{RES}$, $\overline{NMI}$, $\overline{WKP0}$ to $\overline{WKP5}$, $\overline{IRQ0}$ to $\overline{IRQ3}$, $\overline{ADTRG}$,TMRIV, TMCIV, FTCI, FTIOA to FTIOD, SCK3, TRGV	V_{cc} = 4.0 to 5.5 V	–0.3	—	$V_{cc}\times 0.2$	V	
				–0.3	—	$V_{cc}\times 0.1$		
		RXD, SCL, SDA, P10 to P12, P14 to P17, P20 to P22, P50 to P57, P74 to P76, P80 to P87 PB0 to PB7	V_{cc} = 4.0 to 5.5 V	–0.3	—	$V_{cc}\times 0.3$	V	
				–0.3	—	$V_{cc}\times 0.2$		
		OSC1	V_{cc} = 4.0 to 5.5 V	–0.3	—	0.5	V	
				–0.3	—	0.3		

Table 21.2 DC Characteristics (3)

V_{CC} = 3.0 to 5.5 V, V_{SS} = 0.0 V, T_a = –20 to +75°C, unless otherwise indicated.

Item	Symbol	Applicable Pins	Test Condition	Values Min	Typ	Max	Unit
Allowable output low current (per pin)	I_{OL}	Output pins except port 8, SCL, and SDA	V_{CC} = 4.0 to 5.5 V	—	—	2.0	mA
		Port 8		—	—	20.0	
		Port 8		—	—	10.0	
		SCL and SDA		—	—	6.0	
		Output pins except port 8, SCL, and SDA		—	—	0.5	
Allowable output low current (total)	ΣI_{OL}	Output pins except port 8, SCL, and SDA	V_{CC} = 4.0 to 5.5 V	—	—	40.0	mA
		Port 8, SCL, and SDA		—	—	80.0	
		Output pins except port 8, SCL, and SDA		—	—	20.0	
		Port 8, SCL, and SDA		—	—	40.0	
Allowable output high current (per pin)	$\lvert -I_{OH} \rvert$	All output pins	V_{CC} = 4.0 to 5.5 V	—	—	2.0	mA
				—	—	0.2	
Allowable output high current (total)	$\lvert -\Sigma I_{OH} \rvert$	All output pins	V_{CC} = 4.0 to 5.5 V	—	—	30.0	mA
				—	—	8.0	

Table 21.5 Serial Communication Interface (SCI) Timing

V_{CC} = 3.0 to 5.5 V, V_{SS} = 0.0 V, T_a = –20 to +75°C, unless otherwise indicated.

Item		Symbol	Applicable Pins	Test Condition	Values Min	Typ	Max	Unit	Reference Figure
Input clock cycle	Asynchronous	t_{Scyc}	SCK3		4	—	—	t_{cyc}	Figure 21.5
	Clocked synchronous				6	—	—		
Input clock pulse width		t_{SCKW}	SCK3		0.4	—	0.6	t_{Scyc}	
Transmit data delay time (clocked synchronous)		t_{TXD}	TXD	V_{CC} = 4.0 V to 5.5 V	—	—	1	t_{cyc}	Figure 21.6
					—	—	1		
Receive data setup time (clocked synchronous)		t_{RXS}	RXD	V_{CC} = 4.0 V to 5.5 V	50.0	—	—	ns	
					100.0	—	—		
Receive data hold time (clocked synchronous)		t_{RXH}	RXD	V_{CC} = 4.0 V to 5.5 V	50.0	—	—	ns	
					100.0	—	—		

21.2.4 A/D Converter Characteristics

Table 21.6 A/D Converter Characteristics

V_{CC} = 3.0 to 5.5 V, V_{SS} = 0.0 V, T_a = –20 to +75°C, unless otherwise indicated.

Item	Symbol	Applicable Pins	Test Condition	Values			Unit	Reference Figure
				Min	Typ	Max		
Analog power supply voltage	AV_{CC}	AV_{CC}		3.3	V_{CC}	5.5	V	*[1]
Analog input voltage	AV_{IN}	AN0 to AN7		V_{SS} – 0.3	—	AV_{CC} + 0.3	V	
Analog power supply current	AI_{OPE}	AV_{CC}	AV_{CC} = 5.0 V f_{OSC} = 20 MHz	—	—	2.0	mA	
	AI_{STOP1}	AV_{CC}		—	50	—	µA	*[2] Reference value
	AI_{STOP2}	AV_{CC}		—	—	5.0	µA	*[3]
Analog input capacitance	C_{AIN}	AN0 to AN7		—	—	30.0	pF	
Allowable signal source impedance	R_{AIN}	AN0 to AN7		—	—	5.0	kΩ	
Resolution (data length)				10	10	10	bit	
Conversion time (single mode)			AV_{CC} = 3.3 to 5.5 V	134	—	—	t_{cyc}	
Nonlinearity error				—	—	±7.5	LSB	
Offset error				—	—	±7.5	LSB	
Full-scale error				—	—	±7.5	LSB	
Quantization error				—	—	±0.5	LSB	
Absolute accuracy				—	—	±8.0	LSB	
Conversion time (single mode)			AV_{CC} = 4.0 to 5.5 V	70	—	—	t_{cyc}	
Nonlinearity error				—	—	±7.5	LSB	
Offset error				—	—	±7.5	LSB	
Full-scale error				—	—	±7.5	LSB	
Quantization error				—	—	±0.5	LSB	
Absolute accuracy				—	—	±8.0	LSB	

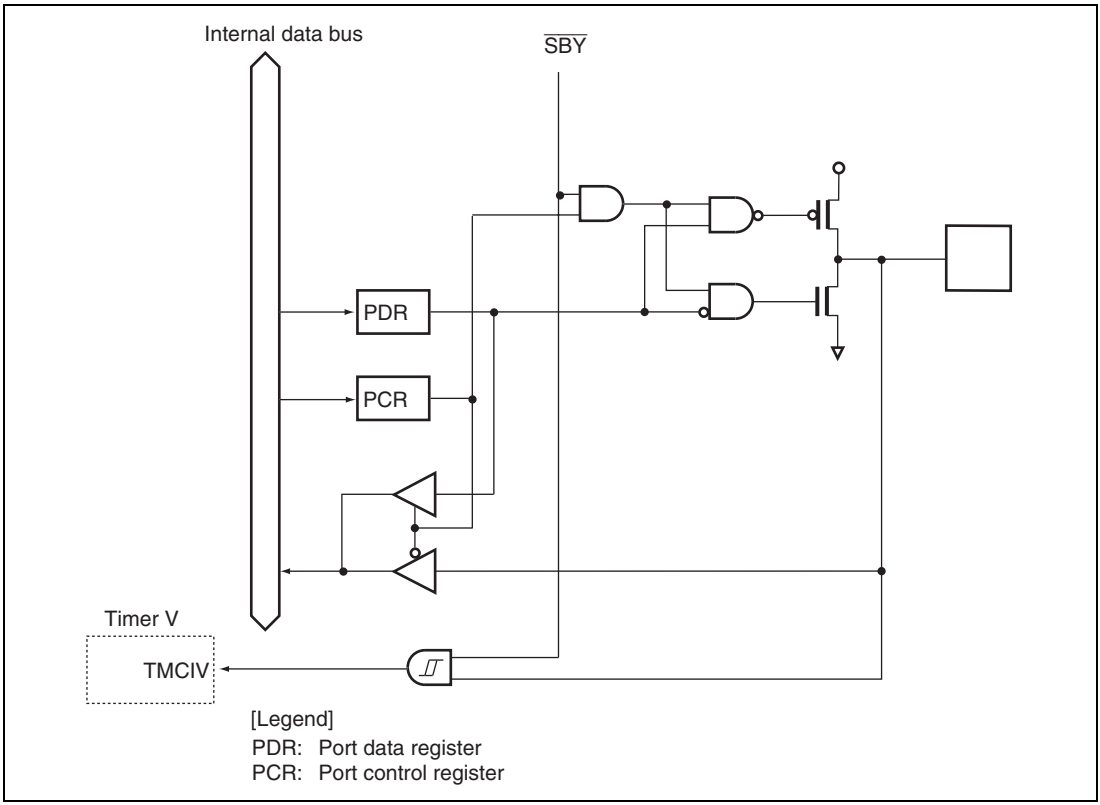


Figure B.12 Port 7 Block Diagram (P75)