Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	-
Core Size	-
Speed	-
Connectivity	-
Peripherals	-
Number of I/O	-
Program Memory Size	-
Program Memory Type	-
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64f3694ghv

Table 2.3 Arithmetic Operations Instructions (1)

Instruction	Size*	Function
ADD SUB	B/W/L	Rd ± Rs → Rd, Rd ± #IMM → Rd Performs addition or subtraction on data in two general registers, or on immediate data and data in a general register (immediate byte data cannot be subtracted from byte data in a general register. Use the SUBX or ADD instruction.)
ADDX SUBX	B	Rd ± Rs ± C → Rd, Rd ± #IMM ± C → Rd Performs addition or subtraction with carry on byte data in two general registers, or on immediate data and data in a general register.
INC DEC	B/W/L	Rd ± 1 → Rd, Rd ± 2 → Rd Increments or decrements a general register by 1 or 2. (Byte operands can be incremented or decremented by 1 only.)
ADDS SUBS	L	Rd ± 1 → Rd, Rd ± 2 → Rd, Rd ± 4 → Rd Adds or subtracts the value 1, 2, or 4 to or from data in a 32-bit register.
DAA DAS	B	Rd decimal adjust → Rd Decimal-adjusts an addition or subtraction result in a general register by referring to the CCR to produce 4-bit BCD data.
MULXU	B/W	Rd × Rs → Rd Performs unsigned multiplication on data in two general registers: either 8 bits × 8 bits → 16 bits or 16 bits × 16 bits → 32 bits.
MULXS	B/W	Rd × Rs → Rd Performs signed multiplication on data in two general registers: either 8 bits × 8 bits → 16 bits or 16 bits × 16 bits → 32 bits.
DIVXU	B/W	Rd ÷ Rs → Rd Performs unsigned division on data in two general registers: either 16 bits ÷ 8 bits → 8-bit quotient and 8-bit remainder or 32 bits ÷ 16 bits → 16-bit quotient and 16-bit remainder.

Note: * Refers to the operand size.
B: Byte
W: Word
L: Longword

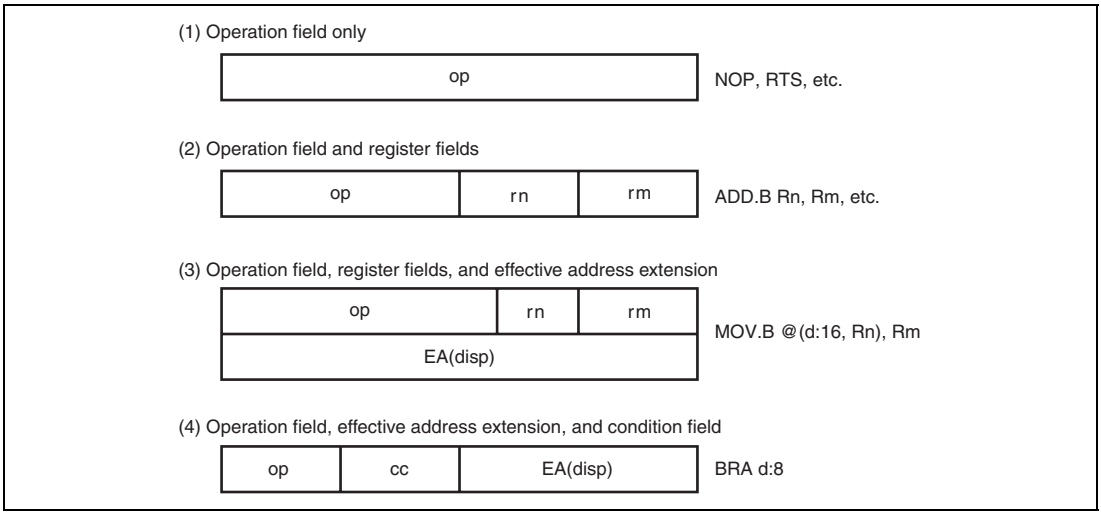


Figure 2.7 Instruction Formats

2.5 Addressing Modes and Effective Address Calculation

The following describes the H8/300H CPU. In this LSI, the upper eight bits are ignored in the generated 24-bit address, so the effective address is 16 bits.

2.5.1 Addressing Modes

The H8/300H CPU supports the eight addressing modes listed in table 2.10. Each instruction uses a subset of these addressing modes. Addressing modes that can be used differ depending on the instruction. For details, refer to appendix A.4, Combinations of Instructions and Addressing Modes.

Arithmetic and logic instructions can use the register direct and immediate modes. Data transfer instructions can use all addressing modes except program-counter relative and memory indirect. Bit manipulation instructions use register direct, register indirect, or the absolute addressing mode (@aa:8) to specify an operand, and register direct (BSET, BCLR, BNOT, and BTST instructions) or immediate (3-bit) addressing mode to specify a bit number in the operand.

3.2.4 Interrupt Flag Register 1 (IRR1)

IRR1 is a status flag register for direct transition interrupts, timer A overflow interrupts, and $\overline{\text{IRQ3}}$ to $\overline{\text{IRQ0}}$ interrupt requests.

Bit	Bit Name	Initial Value	R/W	Description
7	IRRDT	0	R/W	Direct Transfer Interrupt Request Flag [Setting condition] When a direct transfer is made by executing a SLEEP instruction while DTON in SYSCR2 is set to 1. [Clearing condition] When IRRDT is cleared by writing 0
6	IRRTA	0	R/W	Timer A Interrupt Request Flag [Setting condition] When the timer A counter value overflows [Clearing condition] When IRRTA is cleared by writing 0
5, 4	—	All 1	—	Reserved These bits are always read as 1.
3	IRRI3	0	R/W	IRQ3 Interrupt Request Flag [Setting condition] When $\overline{\text{IRQ3}}$ pin is designated for interrupt input and the designated signal edge is detected. [Clearing condition] When IRRI3 is cleared by writing 0
2	IRRI2	0	R/W	IRQ2 Interrupt Request Flag [Setting condition] When $\overline{\text{IRQ2}}$ pin is designated for interrupt input and the designated signal edge is detected. [Clearing condition] When IRRI2 is cleared by writing 0
1	IRRI1	0	R/W	IRQ1 Interrupt Request Flag [Setting condition] When $\overline{\text{IRQ1}}$ pin is designated for interrupt input and the designated signal edge is detected. [Clearing condition] When IRRI1 is cleared by writing 0

7.3 On-Board Programming Modes

There are two modes for programming/erasing of the flash memory; boot mode, which enables on-board programming/erasing, and programmer mode, in which programming/erasing is performed with a PROM programmer. On-board programming/erasing can also be performed in user program mode. At reset-start in reset mode, this LSI changes to a mode depending on the TEST pin settings, $\overline{\text{NMI}}$ pin settings, and input level of each port, as shown in table 7.1. The input level of each pin must be defined four states before the reset ends.

When changing to boot mode, the boot program built into this LSI is initiated. The boot program transfers the programming control program from the externally-connected host to on-chip RAM via SCI3. After erasing the entire flash memory, the programming control program is executed. This can be used for programming initial values in the on-board state or for a forcible return when programming/erasing can no longer be done in user program mode. In user program mode, individual blocks can be erased and programmed by branching to the user program/erase control program prepared by the user.

Table 7.1 Setting Programming Modes

TEST	$\overline{\text{NMI}}$	P85	PB0	PB1	PB2	LSI State after Reset End
0	1	X	X	X	X	User Mode
0	0	1	X	X	X	Boot Mode
1	X	X	0	0	0	Programmer Mode

Legend: X : Don't care.

7.3.1 Boot Mode

Table 7.2 shows the boot mode operations between reset end and branching to the programming control program.

1. When boot mode is used, the flash memory programming control program must be prepared in the host beforehand. Prepare a programming control program in accordance with the description in section 7.4, Flash Memory Programming/Erasing.
2. SCI3 should be set to asynchronous mode, and the transfer format as follows: 8-bit data, 1 stop bit, and no parity.
3. When the boot program is initiated, the chip measures the low-level period of asynchronous SCI communication data (H'00) transmitted continuously from the host. The chip then calculates the bit rate of transmission from the host, and adjusts the SCI3 bit rate to match that of the host. The reset should end with the RxD pin high. The RxD and TxD pins should be

7.5 Program/Erase Protection

There are three kinds of flash memory program/erase protection; hardware protection, software protection, and error protection.

7.5.1 Hardware Protection

Hardware protection refers to a state in which programming/erasing of flash memory is forcibly disabled or aborted because of a transition to reset, subactive mode, subsleep mode, or standby mode. Flash memory control register 1 (FLMCR1), flash memory control register 2 (FLMCR2), and erase block register 1 (EBR1) are initialized. In a reset via the $\overline{\text{RES}}$ pin, the reset state is not entered unless the $\overline{\text{RES}}$ pin is held low until oscillation stabilizes after powering on. In the case of a reset during operation, hold the $\overline{\text{RES}}$ pin low for the $\overline{\text{RES}}$ pulse width specified in the AC Characteristics section.

7.5.2 Software Protection

Software protection can be implemented against programming/erasing of all flash memory blocks by clearing the SWE bit in FLMCR1. When software protection is in effect, setting the P or E bit in FLMCR1 does not cause a transition to program mode or erase mode. By setting the erase block register 1 (EBR1), erase protection can be set for individual blocks. When EBR1 is set to H'00, erase protection is set for all blocks.

7.5.3 Error Protection

In error protection, an error is detected when CPU runaway occurs during flash memory programming/erasing, or operation is not performed in accordance with the program/erase algorithm, and the program/erase operation is aborted. Aborting the program/erase operation prevents damage to the flash memory due to overprogramming or overerasing.

When the following errors are detected during programming/erasing of flash memory, the FLER bit in FLMCR2 is set to 1, and the error protection state is entered.

- When the flash memory of the relevant address area is read during programming/erasing (including vector read and instruction fetch)
- Immediately after exception handling excluding a reset during programming/erasing
- When a SLEEP instruction is executed during programming/erasing

The FLMCR1, FLMCR2, and EBR1 settings are retained, however program mode or erase mode is aborted at the point at which the error occurred. Program mode or erase mode cannot be re-

Section 8 RAM

This LSI has an on-chip high-speed static RAM. The RAM is connected to the CPU by a 16-bit data bus, enabling two-state access by the CPU to both byte data and word data.

Product Classification			RAM Size	RAM Address
Flash memory version (F-ZTAT™ version)		H8/3694F	2 kbytes	H'F780 to H'FF7F*
Mask-ROM version		H8/3694	1 kbyte	H'FB80 to H'FF7F
		H8/3693	1 kbyte	H'FB80 to H'FF7F
		H8/3692	512 kbytes	H'FD80 to H'FF7F
		H8/3691	512 kbytes	H'FD80 to H'FF7F
		H8/3690	512 kbytes	H'FD80 to H'FF7F
EEPROM stacked version	Flash memory version	H8/3694N	2 kbytes	H'F780 to H'FF7F*
	Mask-ROM version		1 kbyte	H'FB80 to H'FF7F

Note: * When the E7 or E8 is used, area H'F780 to H'FB7F must not be accessed.

9.4.1 Port Control Register 7 (PCR7)

PCR7 selects inputs/outputs in bit units for pins to be used as general I/O ports of port 7.

Bit	Bit Name	Initial Value	R/W	Description
7	—	—	—	Reserved
6	PCR76	0	W	Setting a PCR7 bit to 1 makes the corresponding pin an output port, while clearing the bit to 0 makes the pin an input port. Note that the TCSRV setting of the timer V has priority for deciding input/output direction of the P76/TMOV pin.
5	PCR75	0	W	
4	PCR74	0	W	
3 to 0	—	—	—	Reserved

9.4.2 Port Data Register 7 (PDR7)

PDR7 is a general I/O port data register of port 7.

Bit	Bit Name	Initial Value	R/W	Description
7	—	1	—	Reserved This bit is always read as 1.
6	P76	0	R/W	PDR7 stores output data for port 7 pins.
5	P75	0	R/W	If PDR7 is read while PCR7 bits are set to 1, the value stored in PDR7 is read. If PDR7 is read while PCR7 bits are cleared to 0, the pin states are read regardless of the value stored in PDR7.
4	P74	0	R/W	
3 to 0	—	All 1	—	Reserved These bits are always read as 1.

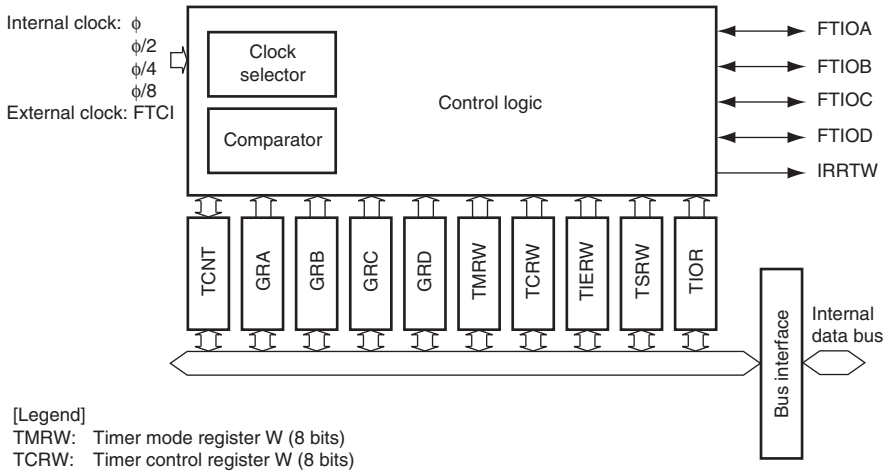
Section 12 Timer W

The timer W has a 16-bit timer having output compare and input capture functions. The timer W can count external events and output pulses with an arbitrary duty cycle by compare match between the timer counter and four general registers. Thus, it can be applied to various systems.

12.1 Features

- Selection of five counter clock sources: four internal clocks (φ, φ/2, φ/4, and φ/8) and an external clock (external events can be counted)
- Capability to process up to four pulse outputs or four pulse inputs
- Four general registers:
  - — Independently assignable output compare or input capture functions
  - — Usable as two pairs of registers; one register of each pair operates as a buffer for the output compare or input capture register
- Four selectable operating modes :
  - — Waveform output by compare match
    Selection of 0 output, 1 output, or toggle output
  - — Input capture function
    Rising edge, falling edge, or both edges
  - — Counter clearing function
    Counters can be cleared by compare match
  - — PWM mode
    Up to three-phase PWM output can be provided with desired duty ratio.
- Any initial timer output value can be set
- Five interrupt sources
  Four compare match/input capture interrupts and an overflow interrupt.

Table 12.1 summarizes the timer W functions, and figure 12.1 shows a block diagram of the timer W.



[Legend]
TMRW: Timer mode register W (8 bits)
TCRW: Timer control register W (8 bits)
TIERW: Timer interrupt enable register W (8 bits)
TSRW: Timer status register W (8 bits)
TIOR: Timer I/O control register (8 bits)
TCNT: Timer counter (16 bits)
GRA: General register A (input capture/output compare register: 16 bits)
GRB: General register B (input capture/output compare register: 16 bits)
GRC: General register C (input capture/output compare register: 16 bits)
GRD: General register D (input capture/output compare register: 16 bits)
IRRTW: Timer W interrupt request

Figure 12.1 Timer W Block Diagram

12.3.4 Timer Status Register W (TSRW)

TSRW shows the status of interrupt requests.

Bit	Bit Name	Initial Value	R/W	Description
7	OVF	0	R/W	Timer Overflow Flag [Setting condition] When TCNT overflows from H'FFFF to H'0000 [Clearing condition] Read OVF when OVF = 1, then write 0 in OVF
6 to 4	—	All 1	—	Reserved These bits are always read as 1.
3	IMFD	0	R/W	Input Capture/Compare Match Flag D [Setting conditions] • TCNT = GRD when GRD functions as an output compare register • The TCNT value is transferred to GRD by an input capture signal when GRD functions as an input capture register [Clearing condition] Read IMFD when IMFD = 1, then write 0 in IMFD
2	IMFC	0	R/W	Input Capture/Compare Match Flag C [Setting conditions] • TCNT = GRC when GRC functions as an output compare register • The TCNT value is transferred to GRC by an input capture signal when GRC functions as an input capture register [Clearing condition] Read IMFC when IMFC = 1, then write 0 in IMFC

- I²C bus transmit data register (ICDRT)
- I²C bus receive data register (ICDRR)
- I²C bus shift register (ICDRS)

15.3.1 I²C Bus Control Register 1 (ICCR1)

ICCR1 enables or disables the I²C bus interface 2, controls transmission or reception, and selects master or slave mode, transmission or reception, and transfer clock frequency in master mode.

Bit	Bit Name	Initial Value	R/W	Description
7	ICE	0	R/W	I²C Bus Interface Enable 0: This module is halted. (SCL and SDA pins are set to port function.) 1: This bit is enabled for transfer operations. (SCL and SDA pins are bus drive state.)
6	RCVD	0	R/W	Reception Disable This bit enables or disables the next operation when TRS is 0 and ICDRR is read. 0: Enables next reception 1: Disables next reception
5	MST	0	R/W	Master/Slave Select
4	TRS	0	R/W	Transmit/Receive Select In master mode with the I²C bus format, when arbitration is lost, MST and TRS are both reset by hardware, causing a transition to slave receive mode. Modification of the TRS bit should be made between transfer frames. After data receive has been started in slave receive mode, when the first seven bits of the receive data agree with the slave address that is set to SAR and the eighth bit is 1, TRS is automatically set to 1. If an overrun error occurs in master mode with the clock synchronous serial format, MST is cleared to 0 and slave receive mode is entered. Operating modes are described below according to MST and TRS combination. When clocked synchronous serial format is selected and MST is 1, clock is output. 00: Slave receive mode 01: Slave transmit mode 10: Master receive mode 11: Master transmit mode

Section 17 EEPROM

The H8/3694N has an on-chip 512-byte EEPROM. The block diagram of the EEPROM is shown in figure 17.1.

17.1 Features

- Two writing methods:
  1-byte write
  Page write: Page size 8 bytes
- Three reading methods:
  Current address read
  Random address read
  Sequential read
- Acknowledge polling possible
- Write cycle time:
  10 ms (power supply voltage Vcc = 2.7 V or more)
- Write/Erase endurance:
  10^4 cycles/byte (byte write mode), 10^5 cycles/page (page write mode)
- Data retention:
  10 years after the write cycle of 10^4 cycles (page write mode)
- Interface with the CPU
  I^2C bus interface (complies with the standard of Philips Corporation)
  Device code 1010
  Sleep address code can be changed (initial value: 000)
  The I^2C bus is open to the outside, so the EEPROM can be directly accessed from the outside.

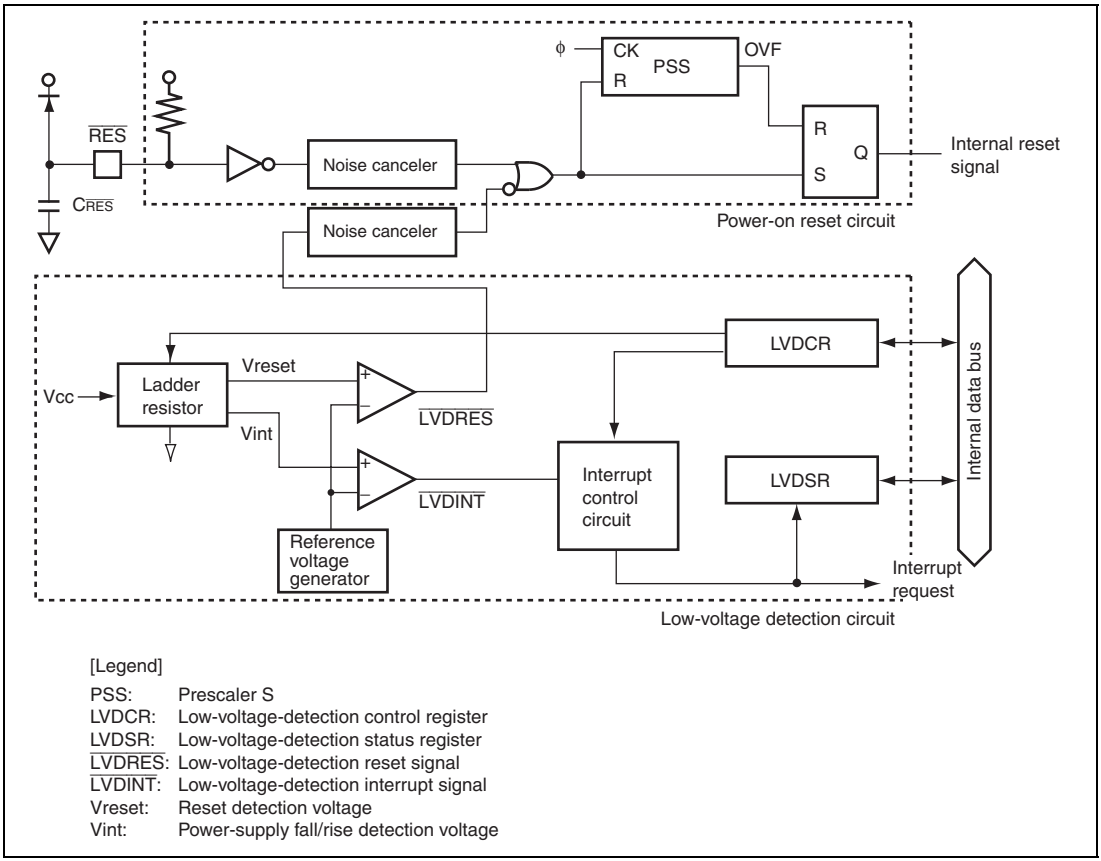


Figure 18.1 Block Diagram of Power-On Reset Circuit and Low-Voltage Detection Circuit

18.2 Register Descriptions

The low-voltage detection circuit has the following registers.

- Low-voltage-detection control register (LVDCR)
- Low-voltage-detection status register (LVDSR)

18.2.1 Low-Voltage-Detection Control Register (LVDCR)

LVDCR is used to enable or disable the low-voltage detection circuit, set the detection levels for the LVDR function, enable or disable the LVDR function, and enable or disable generation of an interrupt when the power-supply voltage rises above or falls below the respective levels.

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name
TMWD	—	—	—	—	CKS3	CKS2	CKS1	CKS0	WDT*[2]
—	—	—	—	—	—	—	—	—	—
ABRKCR	RTINTE	CSEL1	CSEL0	ACMP2	ACMP1	ACMP0	DCMP1	DCMP0	Address break
ABRKSR	ABIF	ABIE	—	—	—	—	—	—	
BARH	BARH7	BARH6	BARH5	BARH4	BARH3	BARH2	BARH1	BARH0	
BARL	BARL7	BARL6	BARL5	BARL4	BARL3	BARL2	BARL1	BARL0	
BDRH	BDRH7	BDRH6	BDRH5	BDRH4	BDRH3	BDRH2	BDRH1	BDRH0	
BDRL	BDRL7	BDRL6	BDRL5	BDRL4	BDRL3	BDRL2	BDRL1	BDRL0	
—	—	—	—	—	—	—	—	—	—
PUCR1	PUCR17	PUCR16	PUCR15	PUCR14	—	PUCR12	PUCR11	PUCR10	I/O port
PUCR5	—	—	PUCR55	PUCR54	PUCR53	PUCR52	PUCR51	PUCR50	
PDR1	P17	P16	P15	P14	—	P12	P11	P10	
PDR2	—	—	—	—	—	P22	P21	P20	
PDR5	P57*[3]	P56*[3]	P55	P54	P53	P52	P51	P50	
PDR7	—	P76	P75	P74	—	—	—	—	
PDR8	P87	P86	P85	P84	P83	P82	P81	P80	
PDRB	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	
PMR1	IRQ3	IRQ2	IRQ1	IRQ0	—	—	TXD	TMOW	
PMR5	—	—	WKP5	WKP4	WKP3	WKP2	WKP1	WKP0	
PCR1	PCR17	PCR16	PCR15	PCR14	—	PCR12	PCR11	PCR10	
PCR2	—	—	—	—	—	PCR22	PCR21	PCR20	
PCR5	PCR57*[3]	PCR56*[3]	PCR55	PCR54	PCR53	PCR52	PCR51	PCR50	
PCR7	—	PCR76	PCR75	PCR74	—	—	—	—	
PCR8	PCR87	PCR86	PCR85	PCR84	PCR83	PCR82	PCR81	PCR80	
SYSCR1	SSBY	STS2	STS1	STS0	NESEL	—	—	—	Power-down
SYSCR2	SMSEL	LSON	DTON	MA2	MA1	MA0	SA1	SA0	
IEGR1	NMIEG	—	—	—	IEG3	IEG2	IEG1	IEG0	Interrupts
IEGR2	—	—	WPEG5	WPEG4	WPEG3	WPEG2	WPEG1	WPEG0	
IENR1	IENDT	IENTA	IENWP	—	IEN3	IEN2	IEN1	IEN0	
IRR1	IRRDT	IRRTA	—	—	IRRI3	IRRI2	IRRI1	IRRI0	
IWPR	—	—	IWPF5	IWPF4	IWPF3	IWPF2	IWPF1	IWPF0	
MSTCR1	—	MSTIIC	MSTS3	MSTAD	MSTWD	MSTTW	MSTTV	MSTTA	Power-down
—	—	—	—	—	—	—	—	—	—

- EEPROM

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name
EKR									EEPROM

Notes: 1. LVDC: Low-voltage detection circuits (optional)
2. WDT: Watchdog timer
3. These bits are reserved in the EEPROM stacked F-ZTAT™ and mask-ROM versions.

21.3.2 DC Characteristics

Table 21.12 DC Characteristics (1)

V_{CC} = 2.7 to 5.5 V, V_{SS} = 0.0 V, T_a = –20 to +75°C, unless otherwise indicated.

Item	Symbol	Applicable Pins	Test Condition	Values Min	Typ	Max	Unit	Notes
Input high voltage	V_{IH}	$\overline{RES}$, $\overline{NMI}$, $\overline{WKP0}$ to $\overline{WKP5}$, $\overline{IRQ0}$ to $\overline{IRQ3}$, $\overline{ADTRG}$,TMRIV, TMCIV, FTCI, FTIOA to FTIOD, SCK3, TRGV	V_{cc} = 4.0 to 5.5 V	$V_{cc}\times 0.8$	—	V_{cc} + 0.3	V	
				$V_{cc}\times 0.9$	—	V_{cc} + 0.3		
		RXD, SCL, SDA, P10 to P12, P14 to P17, P20 to P22, P50 to P57, P74 to P76, P80 to P87	V_{cc} = 4.0 to 5.5 V	$V_{cc}\times 0.7$	—	V_{cc} + 0.3	V	
				$V_{cc}\times 0.8$	—	V_{cc} + 0.3		
		PB0 to PB7	V_{cc} = 4.0 to 5.5 V	$V_{cc}\times 0.7$	—	AV_{cc} + 0.3	V	
				$V_{cc}\times 0.8$	—	AV_{cc} + 0.3		
		OSC1	V_{cc} = 4.0 to 5.5 V	V_{cc} – 0.5	—	V_{cc} + 0.3	V	
				V_{cc} – 0.3	—	V_{cc} + 0.3		
Input low voltage	V_{IL}	$\overline{RES}$, $\overline{NMI}$, $\overline{WKP0}$ to $\overline{WKP5}$, $\overline{IRQ0}$ to $\overline{IRQ3}$, $\overline{ADTRG}$,TMRIV, TMCIV, FTCI, FTIOA to FTIOD, SCK3, TRGV	V_{cc} = 4.0 to 5.5 V	–0.3	—	$V_{cc}\times 0.2$	V	
				–0.3	—	$V_{cc}\times 0.1$		
		RXD, SCL, SDA, P10 to P12, P14 to P17, P20 to P22, P50 to P57, P74 to P76, P80 to P87, PB0 to PB7	V_{cc} = 4.0 to 5.5 V	–0.3	—	$V_{cc}\times 0.3$	V	
				–0.3	—	$V_{cc}\times 0.2$		
		OSC1	V_{cc} = 4.0 to 5.5 V	–0.3	—	0.5	V	
				–0.3	—	0.3		

Item	Symbol	Applicable Pins	Test Condition	Values Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	P10 to P12, P14 to P17, P20 to P22,	V_{CC} = 4.0 to 5.5 V $-I_{OH}$ = 1.5 mA	V_{CC} – 1.0	—	—	V	
		P50 to P55, P74 to P76, P80 to P87	$-I_{OH}$ = 0.1 mA	V_{CC} – 0.5	—	—		
		P56, P57	V_{CC} = 4.0 to 5.5 V $-I_{OH}$ = 0.1 mA	V_{CC} – 2.5	—	—	V	
			V_{CC} =2.7 to 4.0 V $-I_{OH}$ = 0.1 mA	V_{CC} – 2.0	—	—		
Output low voltage	V_{OL}	P10 to P12, P14 to P17, P20 to P22,	V_{CC} = 4.0 to 5.5 V I_{OL} = 1.6 mA	—	—	0.6	V	
		P50 to P57, P74 to P76	I_{OL} = 0.4 mA	—	—	0.4		
		P80 to P87	V_{CC} = 4.0 to 5.5 V I_{OL} = 20.0 mA	—	—	1.5	V	
			V_{CC} = 4.0 to 5.5 V I_{OL} = 10.0 mA	—	—	1.0		
			V_{CC} = 4.0 to 5.5 V I_{OL} = 1.6 mA	—	—	0.4		
			I_{OL} = 0.4 mA	—	—	0.4		
		SCL, SDA	V_{CC} = 4.0 to 5.5 V I_{OL} = 6.0 mA	—	—	0.6	V	
			I_{OL} = 3.0 mA	—	—	0.4		
Input/ output leakage current	$\lvert I_{IL} \rvert$	OSC1, $\overline{\text{NMI}}$, $\overline{\text{WKP0}}$ to $\overline{\text{WKP5}}$, $\overline{\text{IRQ0}}$ to $\overline{\text{IRQ3}}$, $\overline{\text{ADTRG}}$, TRGV, TMRIV, TMCIV, FTCI, FTIOA to FTIOD, RXD, SCK3, SCL, SDA	V_{IN} = 0.5 V to (V_{CC} – 0.5 V)	—	—	1.0	µA	
		P10 to P12, P14 to P17, P20 to P22, P50 to P57, P74 to P76, P80 to P87	V_{IN} = 0.5 V to (V_{CC} – 0.5 V)	—	—	1.0	µA	
		PB0 to PB7	V_{IN} = 0.5 V to (AV_{CC} – 0.5 V)	—	—	1.0	µA	

Item	Symbol	Applicable Pins	Test Condition	Values Min	Values Typ	Values Max	Unit	Reference Figure
Input pin high width	t_{IH}	$\overline{NMI}$, $\overline{IRQ0}$ to $\overline{IRQ3}$, $\overline{WKP0}$ to $\overline{WKP5}$, TMCIV, TMRIV, TRGV, $\overline{ADTRG}$, FTCI, FTIOA to FTIOD		2	—	—	t_{cyc} t_{subcyc}	Figure 21.3
Input pin low width	t_{IL}	$\overline{NMI}$, $\overline{IRQ0}$ to $\overline{IRQ3}$, $\overline{WKP0}$ to $\overline{WKP5}$, TMCIV, TMRIV, TRGV, $\overline{ADTRG}$, FTCI, FTIOA to FTIOD		2	—	—	t_{cyc} t_{subcyc}	

Notes: 1 When an external clock is input, the minimum system clock oscillation frequency is 1.0 MHz.

2. Determined by MA2, MA1, MA0, SA1, and SA0 of system control register 2 (SYSCR2).

Table 21.14 I²C Bus Interface Timing

V_{CC} = 2.7 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20 to +75°C, unless otherwise specified.

Item	Symbol	Test Condition	Values			Unit	Reference Figure
			Min	Typ	Max		
SCL input cycle time	t_{SCL}		$12t_{cyc}$ + 600	—	—	ns	Figure 21.4
SCL input high width	t_{SCLH}		$3t_{cyc}$ + 300	—	—	ns	
SCL input low width	t_{SCLL}		$5t_{cyc}$ + 300	—	—	ns	
SCL and SDA input fall time	t_{Sf}		—	—	300	ns	
SCL and SDA input spike pulse removal time	t_{SP}		—	—	$1t_{cyc}$	ns	
SDA input bus-free time	t_{BUF}		$5t_{cyc}$	—	—	ns	
Start condition input hold time	t_{STAH}		$3t_{cyc}$	—	—	ns	
Retransmission start condition input setup time	t_{STAS}		$3t_{cyc}$	—	—	ns	
Setup time for stop condition input	t_{STOS}		$3t_{cyc}$	—	—	ns	
Data-input setup time	t_{SDAS}		$1t_{cyc}$+20	—	—	ns	
Data-input hold time	t_{SDAH}		0	—	—	ns	
Capacitive load of SCL and SDA	c_b		0	—	400	pF	
SCL and SDA output fall time	t_{Sf}	V_{CC} = 4.0 to 5.5 V	—	—	250	ns	
			—	—	300		