Analog Devices Inc./Maxim Integrated - MAXQ3120-FFN+ Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	-
Core Size	16-Bit
Speed	8MHz
Connectivity	UART/USART
Peripherals	LCD, POR, PWM, WDT
Number of I/O	32
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.8V ~ 3.6V
Data Converters	A/D 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-MQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/maxq3120-ffn

High-Precision ADC Mixed-Signal Microcontroller

ABSOLUTE MAXIMUM RATINGS

Voltage Range on DV_{DD} Relative to DGND .....-0.3V to +4.0V
Voltage Range on AV_{DD} Relative to AGND.....-0.3V to +4.0V
Voltage Range on AGND Relative to DGND .....-0.3V to +0.3V
Voltage Range on AV_{DD} Relative to DV_{DD}.....-0.3V to +0.3V
Voltage Range on Any Pin Relative to DGND
Except AN0+, AN0-, AN1+, AN1-.....-0.3V to (DV_{DD} + 0.5V)
Voltage Range on AN0+, AN0-, AN1+,
AN1- Relative to AGND .....-4.0V to +4.0V
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Soldering Temperature .....See IPC/JEDEC J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(DV_{DD}, AV_{DD} = V_{RST} to 3.6V, V_{REF} = 1.25V (external), f_{HFXIN} = 8MHz, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Supply Voltage	DV_{DD}		V_{RST}	3.3	3.6	V
Digital Supply Ramp Rate		Can be controlled by placing a 1µF or higher capacitor between DV_{DD} and ground	-16		+16	V/ms
Digital Power-Fail Reset	V_{RST}		2.8	2.9	3.03	V
Active Current (Note 2)	I_{DD1}	/1 mode		21	28	mA
	I_{DD2}	/2 mode		11		
	I_{DD3}	/4 mode		5.7		
	I_{DD4}	/8 mode		3.1		
	I_{DD5}	PMM mode		1.0		
Stop-Mode Current (DV_{DD} plus AV_{DD})	I_{STOP}			320	760	µA
Battery Supply Voltage	V_{BAT}		1.8		3.8	V
Battery Current	I_{BAT}	RTCE = 1, DV_{DD} = 0V, V_{BAT} = 3.6V		5.1	10	µA
Input High Voltage	V_{IH}		0.7 x DV_{DD}		DV_{DD} + 0.3	V
Input Low Voltage	V_{IL}		-0.3		0.3 x DV_{DD}	V
Input Hysteresis (Schmitt)	V_{IHYS}			0.6		V
Output High Voltage (All Ports)	V_{OH}	I_{OH} = +1.5mA	DV_{DD} - 0.4			V
		I_{OH} = +2.5mA	DV_{DD} - 0.5			
Output Low Voltage (All Ports, $\overline{RESET}$)	V_{OL}	I_{OL} = 3mA sink current			0.4	V
		I_{OL} = 3.65mA sink current			0.5	
Input Low Current (All Ports)	I_{IL}	V_{IL} = 0.4V; weak pullup enabled	-50			µA
$\overline{RESET}$ Pullup Resistance	R_{RST}		50	100	200	kΩ
Input Leakage (All Ports)	I_L	Weak pullup disabled	-1		+1	µA

ELECTRICAL CHARACTERISTICS (continued)

(DV_{DD}, AV_{DD} = V_{RST} to 3.6V, V_{REF} = 1.25V (external), f_{HFXIN} = 8MHz, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Supply Voltage	AV_{DD}	AV_{DD} = DV_{DD}	2.8	3.3	3.6	V
Active Analog Supply Current	I_{AVDD}	Normal operation		2.65	3.5	mA
Power-Down Analog Supply Current		APD2:0 = 111b		250	635	µA
ANALOG-TO-DIGITAL CONVERTER DC ACCURACY						
ADC Resolution		No missing codes, with software lowpass filter (see Appendix A)		16		bits
Offset Error		Gain = 1		±5.0		mV
Gain Error		Gain = 1		±5.0		%
Gain-Error Drift				±10		ppm
Gain-Error Match				±0.5		%
DC Power-Supply Rejection	PSRR	AN0+, AN0- = AGND; AV_{DD} = 3.0V to 3.6V		80		dB
ANALOG-TO-DIGITAL CONVERTER DYNAMIC SPECIFICATIONS						
Signal-to-Noise Ratio	SNR	DV_{DD} = 3.3V, AV_{DD} = 3.3V, AN0 = 25mV, peak-to-peak sine wave at 65Hz, gain = 16	48	57		dB
		With software lowpass filter, cutoff at 21st harmonic (see Appendix A)		71		
		With software lowpass filter, cutoff at 7th harmonic (see Appendix A)		74		
Total Harmonic Distortion	THD	DV_{DD} = 3.3V, AV_{DD} = 3.3V, AN0 = 25mV, peak-to-peak sine wave at 65Hz, gain = 16 (up to 21st harmonic)		-79	-55	dB
ANALOG-TO-DIGITAL CONVERTER INPUTS						
Input-Voltage Range		AN0+, AN0-; AN1+, AN1- to AGND	-1		+1	V
Input Sampling Capacitance (Note 3)	C_{IN}	Channel 0, Gain = 1		1		pF
		Channel 0, Gain = 16		16		
Input Sampling Rate	f_S	(Note 4)		1.33		MHz
Sample Output Rate				f_{HFXIN} / 384		sample / sec
Input Impedance to AGND (Note 5)		Gain = 1		750		kΩ
		Gain = 16		46		
Differential Input Impedance (Note 6)		Gain = 1		1500		kΩ
		Gain = 16		93		
Input Bandwidth (-3dB)				5.5		kHz
Reference Input Voltage	V_{REF}		1.2	1.25	1.3	V
Reference Input Sampling Capacitance				2		pF
Reference Input Sampling Rate	f_S			1.33		MHz

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ELECTRICAL CHARACTERISTICS (continued)

(DV_{DD}, AV_{DD} = V_{RST} to 3.6V, V_{REF} = 1.25V (external), f_{HFXIN} = 8MHz, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL REFERENCE						
Reference Output Voltage				1.25		V
Reference-Output Temperature Coefficient				±120		ppm/°C
		With V_{REF} bandgap trimming (ATRM[4:0] = 01111b)		±35		
Load Regulation		I_{REF} = ±2µA, C_L = 12pF		±50	±500	µV/µA
LCD INTERFACE						
LCD Reference Voltage	V_{LCD}				DV_{DD}	V
LCD Bias Voltage 1	V_{LCD1}	Guaranteed by design	V_{ADJ} + 2/3 (V_{LCD} - V_{ADJ})			V
LCD Bias Voltage 2	V_{LCD2}	Guaranteed by design	V_{ADJ} + 1/3 (V_{LCD} - V_{ADJ})			V
LCD Adjustment Voltage (Note 7)	V_{ADJ}	Guaranteed by design	0		0.4 x V_{LCD}	V
LCD Bias Resistor	R_{LCD}			20		kΩ
LCD Adjust Resistor	R_{LADJ}	LRA4:LRA0 = 0		40		kΩ
LCD Segment Voltage	V_{SEGxx}	Segment is driven at V_{LCD}; V_{LCD} = 3V, I_{SEGxx} = -3µA, guaranteed by design	V_{LCD} - 0.02		V_{LCD}	V
		Segment is driven at V_{LCD1}; V_{LCD1} = 2V, I_{SEGxx} = -3µA, guaranteed by design	V_{LCD1} - 0.02		V_{LCD1}	V
		Segment is driven at V_{LCD2}; V_{LCD2} = 1V, I_{SEGxx} = -3µA, guaranteed by design	V_{LCD2} - 0.02		V_{LCD2}	V
		Segment is driven at V_{ADJ}; V_{ADJ} = 0V, I_{SEGxx} = +3µA, guaranteed by design	V_{ADJ}		0.1	V
CLOCK SOURCE						
External Crystal Frequency	f_{HFXIN}		1		8	

Note 1: Specifications to -40°C are guaranteed by design and not production tested. All typical values are guaranteed by design characterization and are not production tested.
Note 2: Tested with T_A = +25°C, DV_{DD} = 3.3V, and all peripherals inactive except for port pins.
Note 3: These numbers are guaranteed by design and are not tested.
Note 4: Can be calculated as (f_{HFXIN} / 6).
Note 5: Can be calculated as 6 / (f_{HFXIN} x C_{IN}).
Note 6: Can be calculated as 12 / (f_{HFXIN} x C_{IN}).
Note 7: Assumes that no external components are connected to V_{LCD}, V_{LCD1}, V_{LCD2}, or V_{ADJ}.

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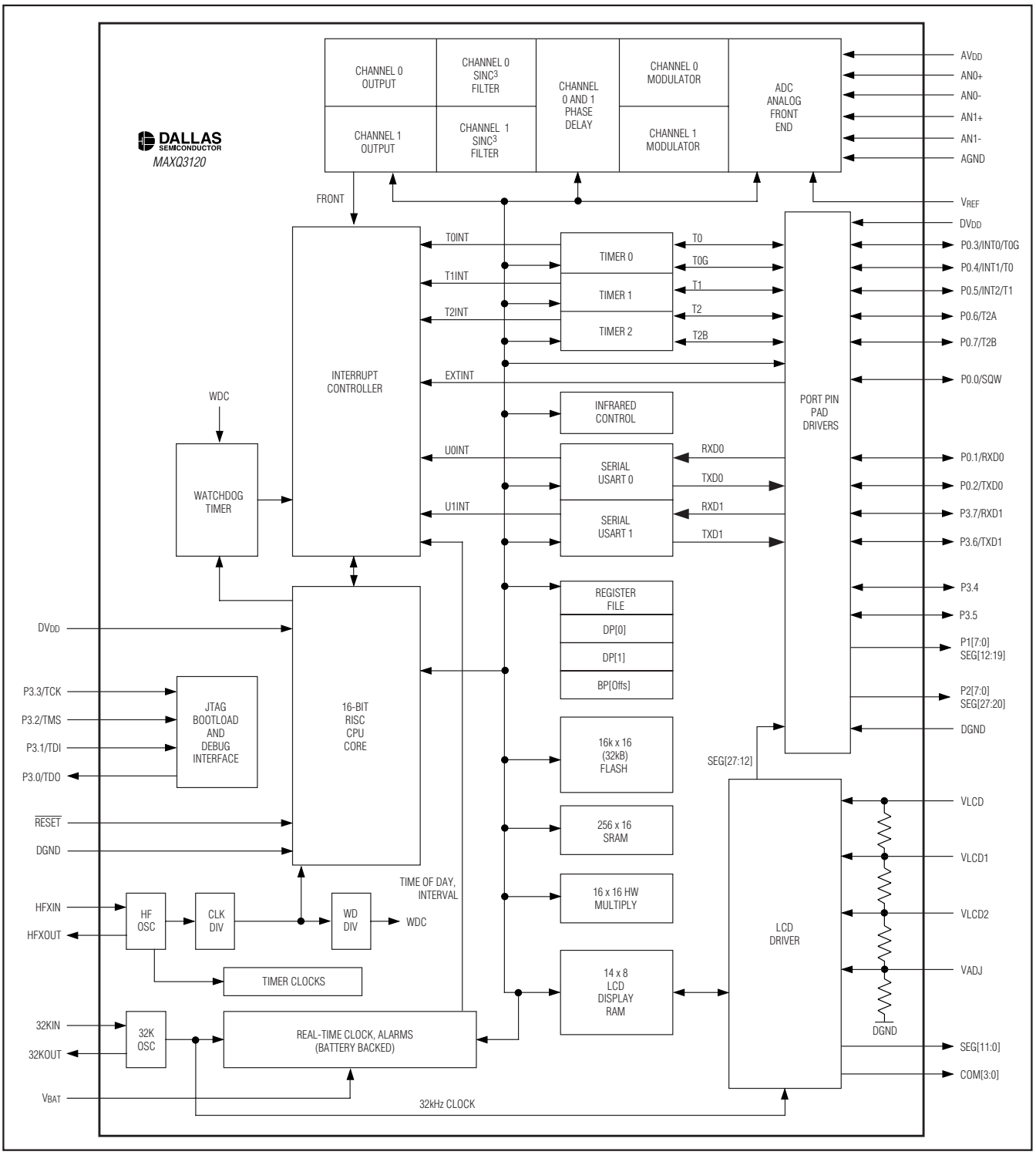
Pin Description

PIN	NAME	FUNCTION
22, 38, 60, 74	DV_{DD}	**Digital Supply Voltage (+3.3V)**
19, 37, 43, 59, 75	DGND	**Digital Ground**
44	AV_{DD}	**Analog Supply Voltage**
52	AGND	**Analog Ground**
12	V_{LCD}	**LCD Bias-Control Voltage.** Highest LCD drive voltage used in all bias modes. This pin must be connected to an external supply when using the LCD display controller.
13	V_{LCD1}	**LCD Bias, Voltage 1.** Next highest LCD drive voltage, used in 1/2 and 1/3 LCD bias modes. An internal resistor-divider sets the voltage at this pin. External resistors and capacitors can be used to change LCD voltage or drive capability at this pin. This pin must be shunted externally to V_{LCD2} when using 1/2 bias mode.
14	V_{LCD2}	**LCD Bias, Voltage 2.** Third highest LCD drive voltage, used in 1/3 LCD bias mode only. An internal resistor-divider sets the voltage at this pin. External resistors and capacitors can be used to change LCD voltage or drive capability at this pin. This pin must be shunted externally to V_{LCD1} when using 1/2 bias mode.
15	V_{ADJ}	**LCD Adjustment Voltage.** Lowest LCD drive voltage, used in all bias modes. Connect to DGND through an external resistor to provide external control of the LCD contrast. Leave disconnected for internal contrast adjustment.
63	$\overline{RESET}$	**Digital, Active-Low, Reset Input/Output.** The CPU is held in reset when this is low and begins executing from the reset vector when released. The pin includes a pullup current source and should be driven by an open-drain, external source capable of sinking in excess of 2mA. This pin is driven low as an output when an internal reset condition occurs.
20	HFXIN	**High-Frequency Crystal Input.** Connect an external crystal between HFXIN and HFXOUT to generate the high-frequency system clock. HFXIN and HFXOUT contain integral 16pF load capacitors, so no external capacitor is required.
21	HFXOUT	**High-Frequency Crystal Output.** Connect an external crystal between HFXIN and HFXOUT to generate the high-frequency system clock. HFXIN and HFXOUT contain integral 16pF load capacitors, so no external capacitor is required.
53	V_{BAT}	**Digital Battery-Backup Supply.** This supply provides an optional battery backup for the RTC when DV_{DD} power is removed. If this supply is not provided, all functions of the device operate as normal, but the RTC is cleared upon power-on reset (POR).
61	32KIN	**32kHz Crystal Input.** Connect an external, 32kHz watch crystal between 32KIN and 32KOUT to generate the 32kHz system clock. This clock is required for the RTC to operate.
62	32KOUT	**32kHz Crystal Output.** Connect an external, 32kHz watch crystal between 32KIN and 32KOUT to generate the 32kHz system clock. This clock is required for the RTC to operate.
51	V_{REF}	**Voltage Reference Input/Output.** Bias voltage (+1.25V) for the ADCs. An external reference voltage can be connected to this pin when extremely high accuracy is required.
45	AN0-	**Negative Input for Sigma-Delta ADC Channel 0**
46	AN0+	**Positive Input for Sigma-Delta ADC Channel 0**
47	AN1-	**Negative Input for Sigma-Delta ADC Channel 1**
48	AN1+	**Positive Input for Sigma-Delta ADC Channel 1**

Functional Diagram



Refer to the user's guide supplement for this device for more details.

In all cases, whichever memory segment is currently being executed from cannot be accessed in data space. To allow the use of lookup tables and similar constructs in the flash memory, the utility ROM contains a set of lookup and block copy routines (refer to the user's guide supplement for this device for more details).

The incorporation of flash memory allows the device to be reprogrammed, eliminating the expense of throwing away one-time programmable devices during development and field upgrades. Flash memory can be password protected with a 16-word key, denying access to program memory by unauthorized individuals.

Stack Memory

A 16-bit-wide internal stack provides storage for program return addresses and general-purpose use. The stack is used automatically by the processor when the CALL, RET, and RETI instructions are executed and interrupts serviced. The stack can also be used explicitly to store and retrieve data by using the PUSH, POP, and POPI instructions.

On reset, the stack pointer, SP, initializes to the top of the stack (0Fh). The CALL, PUSH, and interrupt-vectoring operations increment SP, then store a value at the stack location pointed to by SP. The RET, RETI, POP, and POPI operations retrieve the value at the stack location pointed to by SP, and then decrement SP.

Utility ROM

The utility ROM is a 2kWord block of internal ROM memory that defaults to a starting address of 8000h. The utility ROM consists of subroutines that can be called from application software. These include:

- In-system programming (bootloader) over the JTAG interface
- In-circuit debug routines
- Test routines (internal memory tests, memory loader, etc.)
- User-callable routines for in-application flash programming and code space table lookup

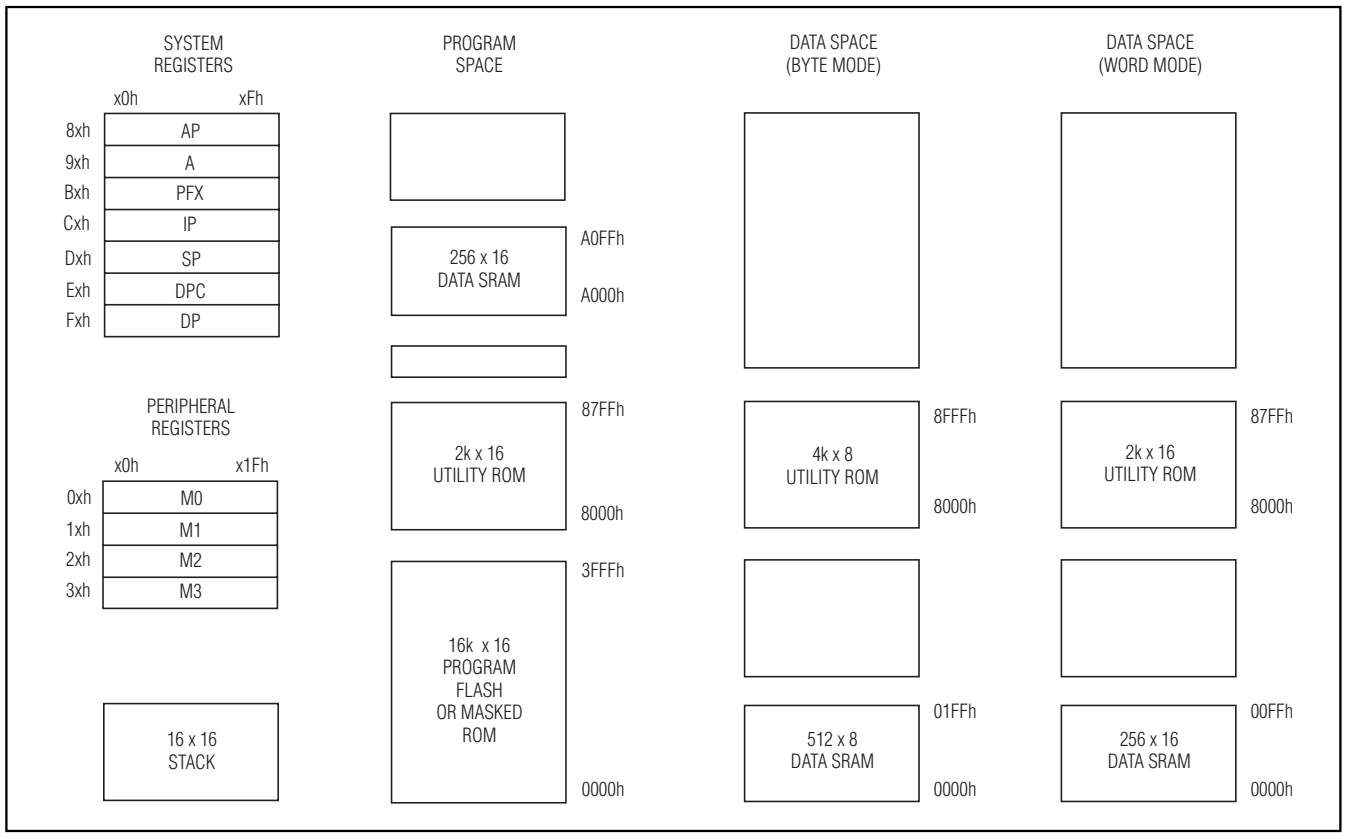


Figure 1. Memory Map

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Table 4. Peripheral Register Map

REGISTER INDEX	M0 (0h)	M1 (1h)	M2 (2h)	M3 (3h)	M4 (4h)	M5 (5h)
00h	PO0	T0CN	T1CN	MCNT	—	—
01h	PO1	T0L	T1L	**MA**	—	—
02h	PO2	T0H	T1H	**MB**	—	—
03h	PO3	SCON0	T2CNA	**MC2**	—	—
04h	—	SBUF0	T2H	**MC1**	—	—
05h	—	SCON1	T2RH	**MC0**	—	—
06h	EIF0	SBUF1	T2CH	***MC1R***	—	—
07h	EIE0	—	IRCN	***MC0R***	—	—
08h	*PI0*	—	T1CL	**ADCN**	—	—
09h	*PI1*	SMD0	T1CH	**PHC**	—	—
0Ah	*PI2*	**PR0**	T1MD	***AD0***	—	—
0Bh	*PI3*	SMD1	T2CNB	***AD1***	—	—
0Ch	EIES0	**PR1**	**T2V**	ATRM	—	—
0Dh	—	—	**T2R**	**LCRA**	—	—
0Eh	—	—	**T2C**	LCFG	—	—
0Fh	—	—	T2CFG	—	—	—
10h	PD0	—	—	LCD0	—	—
11h	PD1	—	—	LCD1	—	—
12h	PD2	—	—	LCD2	—	—
13h	PD3	—	—	LCD3	—	—
14h	—	—	—	LCD4	—	—
15h	—	—	—	LCD5	—	—
16h	—	—	—	LCD6	—	—
17h	—	—	—	LCD7	—	—
18h	RTRM	—	—	LCD8	—	—
19h	**RCNT**	—	—	LCD9	—	—
1Ah	RTSS	—	—	LCD10	—	—
1Bh	**RTSH**	ICDF	—	LCD11	—	—
1Ch	**RTSL**	—	—	LCD12	—	—
1Dh	**RSSA**	—	—	LCD13	—	—
1Eh	RASH	—	—	—	—	—
1Fh	**RASL**	—	—	—	—	—

Note: *Names that appear in italics indicate that all bits of a register are read-only. Names that appear in bold indicate that a register is 16 bits wide. Registers in module AP are bit addressable.*

Table 5. Peripheral Register Bit Functions

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 6. Peripheral Register Bit Reset Values

REGISTER	REGISTER BIT

System Timing

The MAXQ3120 generates its internal system clock from an external high-frequency crystal. Because the MAXQ3120 includes internal capacitors for this purpose, no external capacitors are required to use the high-frequency crystal. The MAXQ3120 should not be driven directly by an external clock source.

A crystal warmup counter enhances operational reliability. Each time the external crystal oscillation must restart, such as after exiting stop mode, the device initiates a crystal warmup period of 65,536 oscillations. This allows time for the crystal amplitude and frequency to stabilize before using it as a clock source.

Power Management

Advanced power-management features minimize power consumption by dynamically matching the processing speed of the device to the required performance level. This means device operation can be slowed and power consumption minimized during periods of reduced activity. When more processing power is required, the microcontroller can increase its operating frequency. Software-selectable clock-divide operations allow flexibility, selecting whether a system clock cycle is 1, 2, 4, or 8 oscillator cycles. By performing this function in software, a lower power state can be entered without the cost of additional hardware.

For extremely power-sensitive applications, two additional low-power modes are available.

- Divide-by-256 power-management mode (PMM) (PMME = 1, CD1:0 = 00b)
- Stop mode (STOP = 1)

In PMM, one system clock is 256 oscillator cycles, significantly reducing power consumption while the microcontroller functions at reduced speed. The optional switchback feature allows enabled interrupt sources, such as the external interrupts and USARTs, to cause the processor to quickly exit PMM mode and return to a faster internal clock rate.

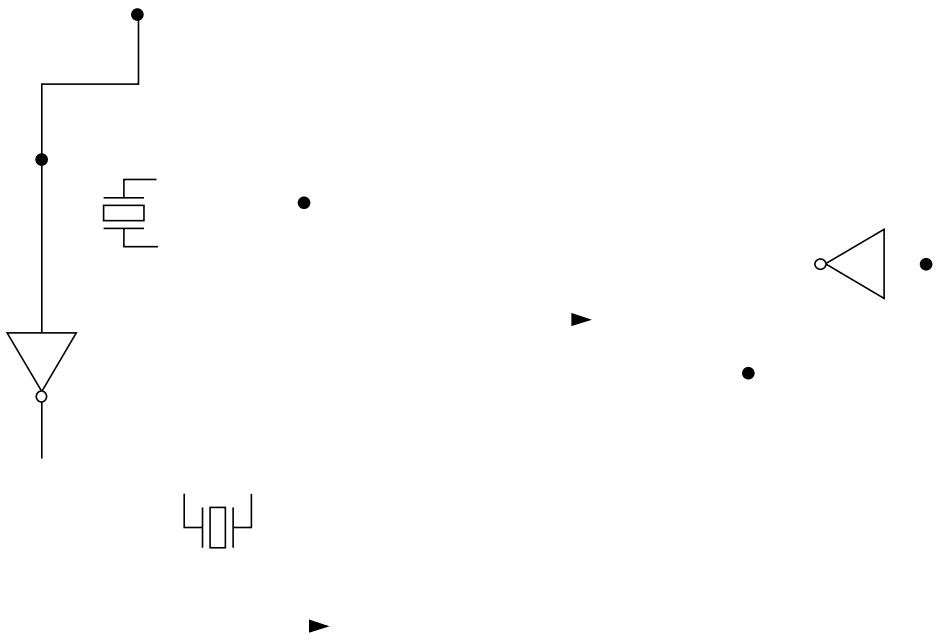

Figure 2. Clock Sources

Analog Front-End

The MAXQ3120 microcontroller incorporates an analog front-end for dedicated analog-to-digital conversion. This peripheral converts and digitally filters two differential signal channels with no CPU overhead.

The two conversion channels operate completely in parallel, running at the same sample rate whether one channel or both channels are enabled. If one or both channels are not in use, they may be powered down to conserve supply current.

The two input signals for each channel form a true differential pair. Each of the two signals (AN0+ and AN0- for channel 0, AN1+ and AN1- for channel 1) can vary across the entire +1V to -1V analog input range, without regard to the level of the other signal in the pair. The initial stage for each channel is a programmable gain function (1x, 16x) that can be set by software independently for each channel. Next, a second-order sigma-delta modulator samples each input signal.

When using both channels to measure the same signal (as is the case when measuring voltage and current for power calculations), a phase-correction buffer is provided to compensate for any phase shift between the two channels caused by external circuitry. The phase-correction buffer operates digitally on the output bit stream of one of the two channels and can delay either channel's bit stream with respect to the other channel's bit stream by up to 140 bits.

Next, the bit streams for the two channels travel through two digital sinc^3 lowpass filters, which convert the bit streams to 16-bit PCM values for additional processing.

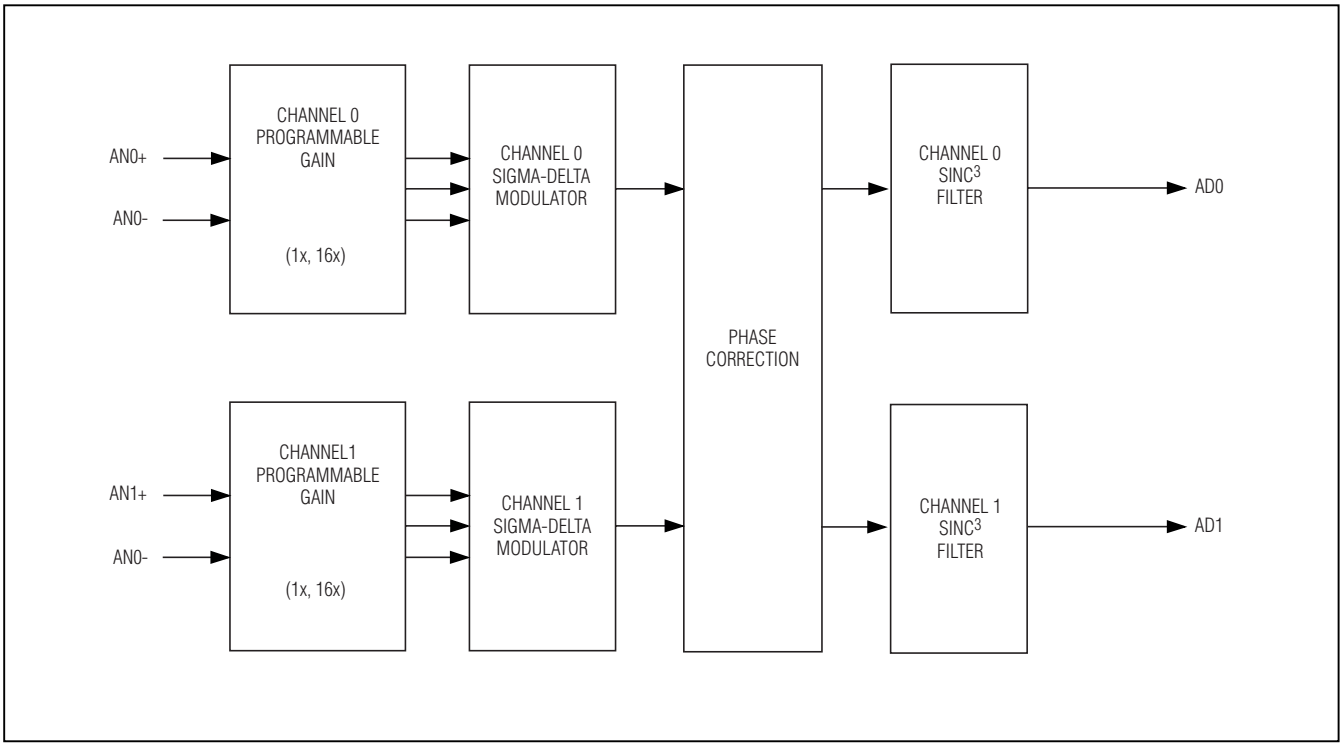

Figure 6. Analog Front-End Block Diagram

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Applications Information

The low-power, high-performance RISC architecture of the MAXQ3120 makes it an excellent fit for many portable or battery-powered applications that require cost-effective computing. The high-throughput core is complemented by a dual-differential channel, 16-bit sigma-delta ADC, and 16-bit hardware multiplier-accumulator, allowing the implementation of sophisticated computational algorithms. Applications benefit from a wide range of peripheral interfaces, allowing the microcontroller to communicate with many external devices. With integrated LCD support of up to 112 segments (4 x 28), applications can support complex user interfaces. Displays are driven directly with no additional external hardware required. Contrast can be adjusted using a built-in, adjustable resistor. The simplified architecture reduces component count and board space, critical factors in the design of portable systems.

The MAXQ3120 is ideally suited for single-phase electricity metering applications as well as other applications that require high-precision analog-to-digital conversion and signal processing.

Additional Documentation

Designers must have four documents to fully use all the features of this device. This data sheet contains pin descriptions, feature overviews, and electrical specifications. Errata sheets contain deviations from published specifications. The user's guides offer detailed information about programming, device features, and operation. The following documents can be downloaded from www.maxim-ic.com/microcontrollers.

- The MAXQ3120 data sheet, which contains electrical/timing specifications and pin descriptions, available at www.maxim-ic.com/MAXQ3120.
- The MAXQ3120 errata sheet, available at www.maxim-ic.com/errata.
- The *MAXQ Family User's Guide*, which contains detailed information on core features and operation, including programming, avaliable at www.maxim-ic.com/MAXQUG.
- The *MAXQ Family User's Guide: MAXQ3120 Supplement*, which contains detailed information on features specific to the MAXQ3120, available at www.maxim-ic.com/MAXQ3120UG.

Development and Technical Support

A variety of highly versatile, affordably priced development tools for this microcontroller are available from Maxim/Dallas Semiconductor and third-party suppliers, including:

- Compilers
- In-circuit emulators
- Integrated development environments (IDEs)
- JTAG-to-serial converters for programming and debugging

A partial list of development tool vendors can be found on our website at www.maxim-ic.com/microcontrollers. Technical support is available through email at maxq.support@dalsemi.com.

Definitions

Offset Error

For an ideal converter, the first transition occurs at 0.5 LSB above zero. Offset error is the amount of deviation between the measured first transition point and the ideal point.

Gain Error

With a full-scale analog voltage applied to the ADC (resulting in all ones in the digital code), gain error is defined as the amount of deviation between the ideal transfer function and the measured transfer function (with the offset error removed). Gain error is usually expressed in LSB or as a percentage of full-scale range (%FSR).

Power-Supply Rejection Ratio

Power-supply rejection ratio (PSRR) is the ratio of changes in the power supply (V) to changes in the converter output (V). It is typically measured in decibels.

Appendix A: Applying a Lowpass Filter (LPF) for Application-Optimized ADC Performance

The MAXQ3120 gives a user application program direct access to the ADC data stream right after its sinc3 filters. This unique feature permits the MAXQ3120 to be optimized for its target applications. With the device's 8MIPS processing power and the 1-cycle MAC, a linear FIR filter can be easily computed in the user application program. This section provides a simple LP FIR filter to improve the SNR and THD performance of the MAXQ3120 for the power-metering application.

Filter Specifications and Coefficients

Input signal frequency (f_{IN}) = 60Hz

Sampling frequency (f_S) = 20833Hz

Window = hamming

Cutoff frequency (attenuates after 7th harmonic) = 0.06π = 625Hz

Cutoff frequency (for 21st harmonic) = 0.18π = 1875Hz

Transition width = 0.35π = 3646Hz

Filter length = 23

1) LPF coefficients (up to 21st harmonic). Note that these coefficients have been converted to 16-bit fixed-point numbers. A shift of 17 places is required after the multiply-accumulate operation.

FILTER_COEFFICIENT_0	-19	FILTER_COEFFICIENT_12	21893
FILTER_COEFFICIENT_1	-288	FILTER_COEFFICIENT_13	17547
FILTER_COEFFICIENT_2	-786	FILTER_COEFFICIENT_14	11739
FILTER_COEFFICIENT_3	-1402	FILTER_COEFFICIENT_15	6018
FILTER_COEFFICIENT_4	-1670	FILTER_COEFFICIENT_16	1627
FILTER_COEFFICIENT_5	-876	FILTER_COEFFICIENT_17	-876
FILTER_COEFFICIENT_6	1627	FILTER_COEFFICIENT_18	-1670
FILTER_COEFFICIENT_7	6018	FILTER_COEFFICIENT_19	-1402
FILTER_COEFFICIENT_8	11739	FILTER_COEFFICIENT_20	-786
FILTER_COEFFICIENT_9	17547	FILTER_COEFFICIENT_21	-288
FILTER_COEFFICIENT_10	21893	FILTER_COEFFICIENT_22	-19
FILTER_COEFFICIENT_11	23506	—	—

2) LPF coefficients (up to 7th harmonic). Note that these coefficients have been converted to 16-bit fixed-point numbers. A shift of 18 places is required after the multiply-accumulate operation.

FILTER_COEFFICIENT_0	849	FILTER_COEFFICIENT_12	23295
FILTER_COEFFICIENT_1	1420	FILTER_COEFFICIENT_13	21720
FILTER_COEFFICIENT_2	2553	FILTER_COEFFICIENT_14	19291
FILTER_COEFFICIENT_3	4334	FILTER_COEFFICIENT_15	16269
FILTER_COEFFICIENT_4	6754	FILTER_COEFFICIENT_16	12966
FILTER_COEFFICIENT_5	9700	FILTER_COEFFICIENT_17	9700
FILTER_COEFFICIENT_6	12966	FILTER_COEFFICIENT_18	6754
FILTER_COEFFICIENT_7	16269	FILTER_COEFFICIENT_19	4334
FILTER_COEFFICIENT_8	19291	FILTER_COEFFICIENT_20	2553
FILTER_COEFFICIENT_9	21720	FILTER_COEFFICIENT_21	1420
FILTER_COEFFICIENT_10	23295	FILTER_COEFFICIENT_22	849
FILTER_COEFFICIENT_11	23840	—	—

High-Precision ADC Mixed-Signal Microcontroller

Filter Results

Below is the summary of the SNR and THD values before and after applying the above LPFs, for 60 MAXQ3120 units.

An application engineer can easily implement his own favorite lowpass filters to optimize MAXQ3120 for his target applications. However, he does need to consider the filter complexity and its processor resource requirement (CPU cycles and storage space) to strike an optimal balance. The above 23-tap LPF takes 23 x 2 bytes of RAM and 107 clock cycles of the MAXQ3120 to complete. Note that the number of cycles varies from filter to filter because the number of shifts required to normalize the multiply-accumulate result will vary.

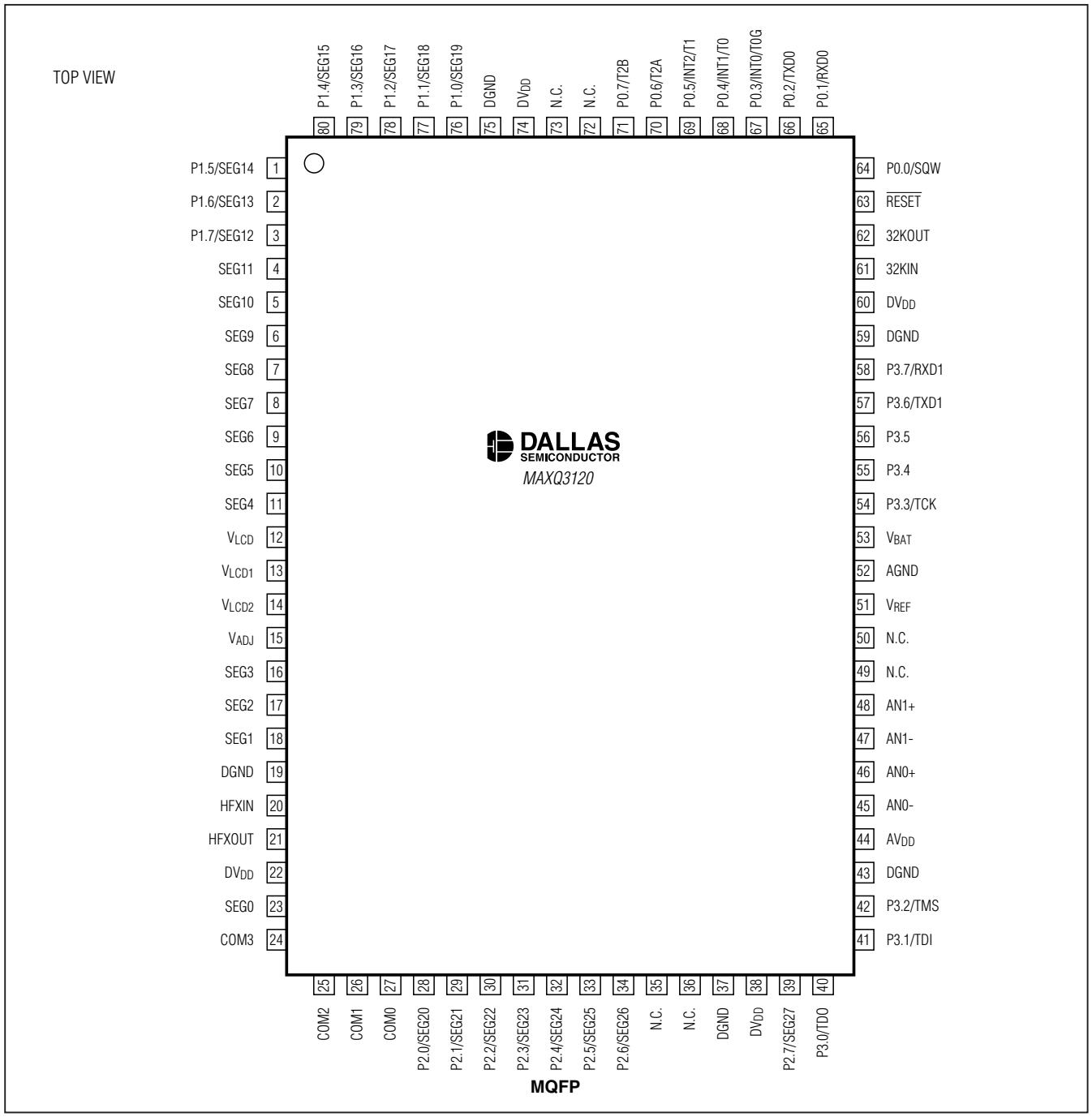
CONDITION	SNR			THD		
	MIN	AVG	MAX	MIN	AVG	MAX
Before LPF	56.5	56.8	57.1	-84.5	-81.1	-77.3
After LPF, 21st Harmonic	68.2	70.7	71.4	-85.8	-83.1	-79.4
After LPF, 7th Harmonic	71.5	73.8	74.7	-88.9	-85.7	-82.0

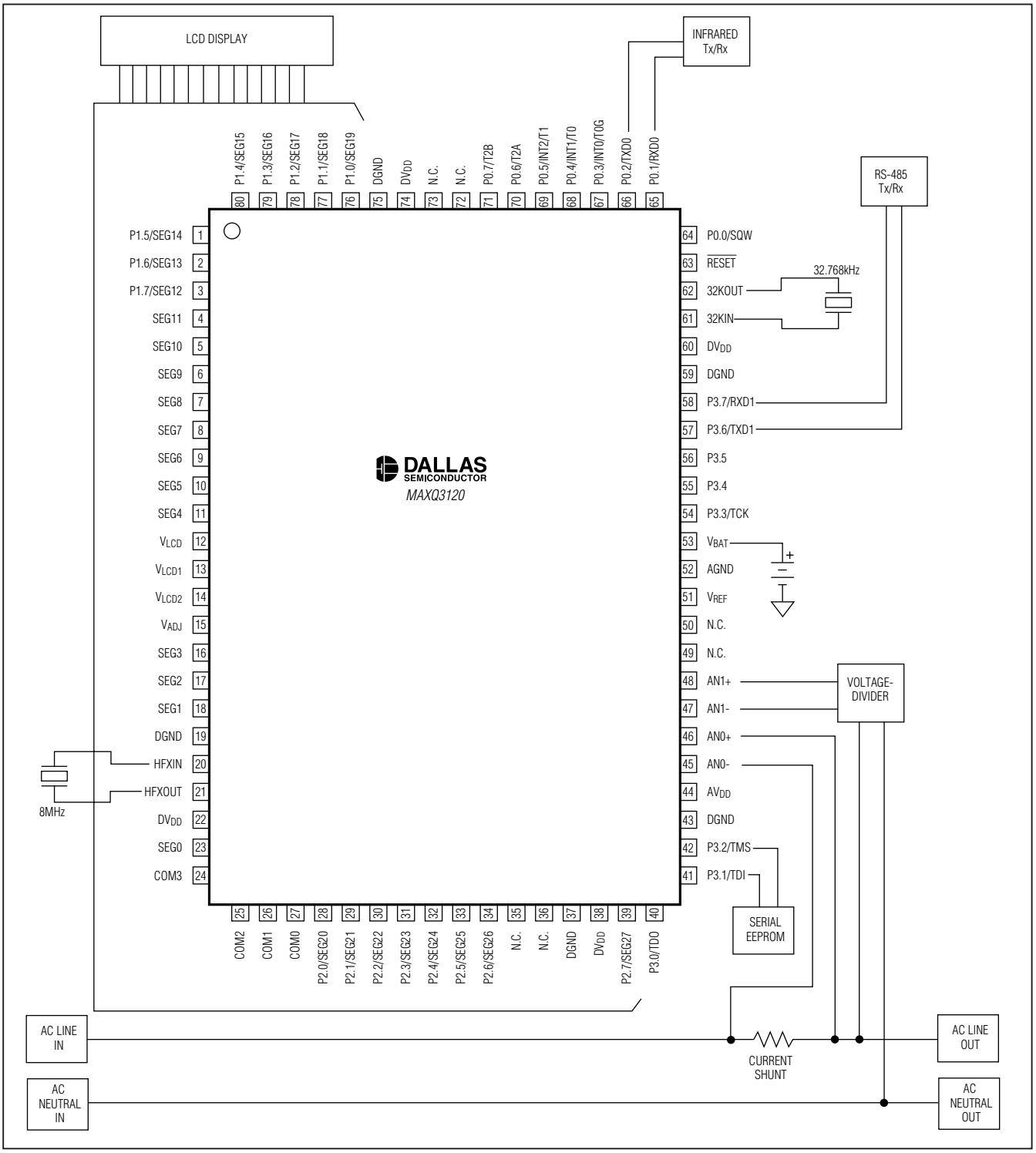
Selector Guide

PART	TEMP RANGE	PROGRAM MEMORY	DATA MEMORY	LCD SEGMENTS	EXTERNAL INTERRUPTS	USARTS	PIN-PACKAGE
MAXQ3120-FFN	-40°C to +85°C	16kWord Flash	256 Word SRAM	112	3	2	80 MQFP
MAXQ3120-FFN+	-40°C to +85°C	16kWord Flash	256 Word SRAM	112	3	2	80 MQFP

+Denotes a Pb-free/RoHS-compliant device.

Pin Configuration



High-Precision ADC Mixed-Signal Microcontroller

Typical Operating Circuit