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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |                                                                                                                                                                       |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Active                                                                                                                                                                |
| Core Processor             | PIC                                                                                                                                                                   |
| Core Size                  | 8-Bit                                                                                                                                                                 |
| Speed                      | 32MHz                                                                                                                                                                 |
| Connectivity               | I <sup>2</sup> C, LINbus, SPI, UART/USART                                                                                                                             |
| Peripherals                | Brown-out Detect/Reset, POR, PWM, WDT                                                                                                                                 |
| Number of I/O              | 25                                                                                                                                                                    |
| Program Memory Size        | 56KB (32K x 14)                                                                                                                                                       |
| Program Memory Type        | FLASH                                                                                                                                                                 |
| EEPROM Size                | 256 x 8                                                                                                                                                               |
| RAM Size                   | 4K x 8                                                                                                                                                                |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V                                                                                                                                                           |
| Data Converters            | A/D 24x10b; D/A 1x5b                                                                                                                                                  |
| Oscillator Type            | Internal                                                                                                                                                              |
| Operating Temperature      | -40°C ~ 85°C (TA)                                                                                                                                                     |
| Mounting Type              | Surface Mount                                                                                                                                                         |
| Package / Case             | 28-SOIC (0.295", 7.50mm Width)                                                                                                                                        |
| Supplier Device Package    | 28-SOIC                                                                                                                                                               |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18857-i-so">https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18857-i-so</a> |

# PIC16(L)F1885X/7X

## Full-Featured 28/40-Pin Microcontroller Product Brief

### Description

PIC16(L)F1885X/7X microcontrollers feature Analog, Core Independent Peripherals and communication peripherals, combined with eXtreme Low Power (XLP) for a wide range of general purpose and low-power applications. The family will feature the CRC/SCAN, HLT and Windowed WDT to support customers looking to add safety to their application. Additionally, this family includes up to 56 KB of Flash memory, along with a 10-bit ADC with MATHPAK extensions for automated signal analysis to reduce the complexity of the application.

### Core Features

- C Compiler Optimized RISC Architecture
- Only 49 Instructions
- Operating Speed:
  - DC – 32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Three 8-Bit Timers (TMR2/4/6) with Hardware Limit Timer (HLT) Extensions
- Four 16-Bit Timers (TMR0/1/3/5)
- Low Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRTE)
- Brown-out Reset (BOR) with Fast Recovery
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
  - Variable prescaler selection
  - Variable window size selection
  - All sources configurable in hardware or software
- Programmable Code Protection

### Memory

- Up to 56 KB Flash Program Memory
- Up to 4 KB Data SRAM Memory
- 256B of EEPROM
- Direct, Indirect and Relative Addressing modes

### Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF188XX)
  - 2.3V to 5.5V (PIC16F188XX)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

### Power-Saving Functionality

- Doze mode: Ability to run the CPU core slower than the system clock
- Idle mode: Ability to halt CPU core while internal peripherals continue operating
- Sleep mode: Lowest Power Consumption
- Peripheral Module Disable (PMD):
  - Ability to disable hardware module to minimize power consumption of unused peripherals

### eXtreme Low-Power (XLP) Features

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 uA @ 32 kHz, 1.8V, typical
  - 32 uA/MHz @ 1.8V, typical

### Digital Peripherals

- Four Configurable Logic Cells (CLC):
  - Integrated combinational and sequential logic
- Complementary Waveform Generator (CWG):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
- Five Capture/Compare/PWM (CCP) modules
- PWM: Two 10-bit Pulse-Width Modulators
- Numerically Controlled Oscillator (NCO):
  - Generates true linear frequency control and increased frequency resolution
  - Input Clock:  $0 \text{ Hz} < f_{\text{NCO}} < 32 \text{ MHz}$
  - Resolution:  $f_{\text{NCO}}/220$
- Two Signal Measurement Timers (SMT):
  - 24-bit Signal Measurement Timer
  - Up to 12 different Acquisition modes
- Cyclical Redundancy Check (CRC/SCAN):
  - 16-bit CRC
  - Scans memory for NVM integrity

# PIC16(L)F1885X/7X

- Serial Communications:
  - SPI, I<sup>2</sup>C™, EUSART
  - RS-232, RS-485, LIN compatible
  - Auto-Baud Detect, Auto-Wake-up on start
- Up to 36 I/O Pins:
  - Individually programmable pull-ups, slew rate control interrupt-on-change with edge-select
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O
- Data Signal Modulator (DSM)
- 5-Bit Digital-to-Analog Converter (DAC):
  - 5-bit resolution, rail-to-rail
  - Positive Reference Selection
  - Unbuffered I/O pin output
  - Internal connections to ADCs and comparators
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels

## Analog Peripherals

- Analog-to-Digital Converter (ADC) with MATHPAK Extensions:
  - 10-bit with up to 35 external channels
  - Automated post-processing
  - Automates math functions on input signals: averaging, filter calculations, oversampling and threshold comparison
  - Operates in Sleep
- Two Comparators:
  - Fixed Voltage Reference at (non) inverting input(s)
  - Comparator outputs externally accessible

## Clocking Structure

- High-Precision Internal Oscillator:
  - Selectable frequency range up to 32 MHz
  - x2/x4 PLL with Internal and External Sources
- Low-Power Internal 31 kHz Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOSC)

**TABLE 1: PIC16(L)F188XX FAMILY TYPES**

| Device         | Data Sheet Index | Program Flash Memory (words) | Program Flash Memory (KB) | EEPROM (bytes) | Data SRAM (bytes) | I/O Pins <sup>(2)</sup> | 10-bit ADC MATHPAK (ch) | 5-bit DAC | Comparator | 8-bit (w/HL-T)/16-bit Timers | SMT | Windowed Watchdog Timer | CRC + Memory Scan | CCP/10-bit PWM | Zero-Cross Detect | CWG | NCO | CLC | DSM | EUSART/I <sup>2</sup> C™/SPI | Peripheral Pin Select |
|----------------|------------------|------------------------------|---------------------------|----------------|-------------------|-------------------------|-------------------------|-----------|------------|------------------------------|-----|-------------------------|-------------------|----------------|-------------------|-----|-----|-----|-----|------------------------------|-----------------------|
| PIC16(L)F18854 | (A)              | 4096                         | 7                         | 256            | 512               | 25                      | 24                      | 1         | 2          | 3/4                          | 2   | Y                       | Y                 | 5/2            | Y                 | 3   | 1   | 4   | 1   | 1/2                          | Y                     |
| PIC16(L)F18855 | (B)              | 8192                         | 14                        | 256            | 1024              | 25                      | 24                      | 1         | 2          | 3/4                          | 2   | Y                       | Y                 | 5/2            | Y                 | 3   | 1   | 4   | 1   | 1/2                          | Y                     |
| PIC16(L)F18875 | (B)              | 8192                         | 14                        | 256            | 1024              | 36                      | 35                      | 1         | 2          | 3/4                          | 2   | Y                       | Y                 | 5/2            | Y                 | 3   | 1   | 4   | 1   | 1/2                          | Y                     |
| PIC16(L)F18856 | (C)              | 16384                        | 28                        | 256            | 2048              | 25                      | 24                      | 1         | 2          | 3/4                          | 2   | Y                       | Y                 | 5/2            | Y                 | 3   | 1   | 4   | 1   | 1/2                          | Y                     |
| PIC16(L)F18876 | (C)              | 16384                        | 28                        | 256            | 2048              | 36                      | 35                      | 1         | 2          | 3/4                          | 2   | Y                       | Y                 | 5/2            | Y                 | 3   | 1   | 4   | 1   | 1/2                          | Y                     |
| PIC16(L)F18857 | (D)              | 32768                        | 56                        | 256            | 4096              | 25                      | 24                      | 1         | 2          | 3/4                          | 2   | Y                       | Y                 | 5/2            | Y                 | 3   | 1   | 4   | 1   | 1/2                          | Y                     |
| PIC16(L)F18877 | (D)              | 32768                        | 56                        | 256            | 4096              | 36                      | 35                      | 1         | 2          | 3/4                          | 2   | Y                       | Y                 | 5/2            | Y                 | 3   | 1   | 4   | 1   | 1/2                          | Y                     |

**Note 1:** One pin is input-only.

### Data Sheet Index:

- A** Future Release PIC16(L)F18854 Data Sheet, 28-Pin, Full-Featured 8-bit Microcontrollers
- B** Future Release PIC16(L)F18855/75 Data Sheet, 28/40-Pin, Full-Featured 8-bit Microcontrollers
- C** Future Release PIC16(L)F18856/76 Data Sheet, 28/40-Pin, Full-Featured 8-bit Microcontrollers
- D** Future Release PIC16(L)F18857/77 Data Sheet, 28/40-Pin, Full-Featured 8-bit Microcontrollers

**Note:** For other small form-factor package availability and marking information, please visit <http://www.microchip.com/packaging> or contact your local sales office.

# PIC16(L)F1885X/7X

**TABLE 2: PACKAGES**

| Packages       | (S)PDIP | SOIC | SSOP | QFN<br>(6x6) | UQFN<br>(4x4) | TQFP | QFN<br>(8x8) | UQFN<br>(5x5) |
|----------------|---------|------|------|--------------|---------------|------|--------------|---------------|
| PIC16(L)F18854 | X       | X    | X    | X            | X             |      |              |               |
| PIC16(L)F18855 | X       | X    | X    | X            | X             |      |              |               |
| PIC16(L)F18875 | X       |      |      |              |               | X    | X            | X             |
| PIC16(L)F18856 | X       | X    | X    | X            | X             |      |              |               |
| PIC16(L)F18876 | X       |      |      |              |               | X    | X            | X             |
| PIC16(L)F18857 | X       | X    | X    | X            |               |      |              |               |
| PIC16(L)F18877 | X       |      |      |              |               | X    | X            | X             |

**Note:** Pin details are subject to change.

# PIC16(L)F1885X/7X

## PIN DIAGRAMS

### Pin Diagram – 28-Pin (S)PDIP, SOIC, SSOP



**Note 1:** See Table 3 for location of all peripheral functions.

**2:** All VDD and all VSS pins must be connected at the circuit board level. Allowing one or more VSS or VDD pins to float may result in degraded electrical performance or non-functionality.

### Pin Diagram – 28-Pin UQFN (4x4) (except for PIC16F18857) and QFN (6x6)



**Note 1:** See Table 3 for location of all peripheral functions.

**2:** All VDD and all VSS pins must be connected at the circuit board level. Allowing one or more VSS or VDD pins to float may result in degraded electrical performance or non-functionality.

**3:** The bottom pad of the QFN/UQFN package should be connected to VSS at the circuit board level.

# PIC16(L)F1885X/7X

## Pin Diagram – 40-Pin PDIP

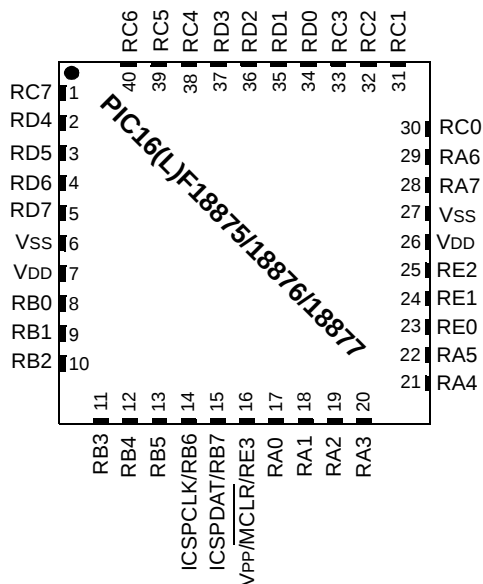


## Pin Diagram – 44-Pin TQFP



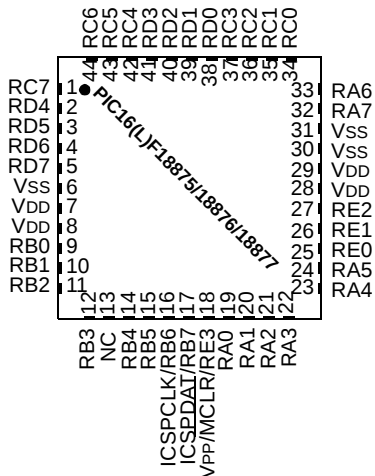
# PIC16(L)F1885X/7X

## Pin Diagram – 40-Pin UQFN (5x5)



- Note 1:** See Table 4 for location of all peripheral functions.
- 2:** All VDD and all VSS pins must be connected at the circuit board level. Allowing one or more VSS or VDD pins to float may result in degraded electrical performance or non-functionality.
- 3:** The bottom pad of the QFN/UQFN package should be connected to VSS at the circuit board level.

## Pin Diagram – 44-Pin QFN (8x8)



- Note 1:** See Table 4 for location of all peripheral functions.
- 2:** All VDD and all VSS pins must be connected at the circuit board level. Allowing one or more VSS or VDD pins to float may result in degraded electrical performance or non-functionality.
- 3:** The bottom pad of the QFN/UQFN package should be connected to VSS at the circuit board level.

## PIN ALLOCATION TABLES

TABLE 3: 28-PIN ALLOCATION TABLE (PIC16(L)F1885X)

| I/O | 28-Pin SPDIP/SOIC/SSOP | 28-Pin (U)QFN | ADC                           | Voltage Reference | DAC      | Comparators      | Zero-Cross Detect | MSSP (SPI/I <sup>2</sup> C™)                 | EUSART | DSM                   | Timers/SMT                                   | CCP and PWM         | CWG                   | CLC                   | NCO | Clock Reference (CLKR) | Interrupt-on-Change         | Basic          |
|-----|------------------------|---------------|-------------------------------|-------------------|----------|------------------|-------------------|----------------------------------------------|--------|-----------------------|----------------------------------------------|---------------------|-----------------------|-----------------------|-----|------------------------|-----------------------------|----------------|
| RA0 | 2                      | 27            | ANA0                          | —                 | —        | C1IN0-<br>C2IN0- | —                 | —                                            | —      | —                     | —                                            | —                   | —                     | CLCIN0 <sup>(1)</sup> | —   | —                      | IOCA0                       | —              |
| RA1 | 3                      | 28            | ANA1                          | —                 | —        | C1IN1-<br>C2IN1- | —                 | —                                            | —      | —                     | —                                            | —                   | —                     | CLCIN1 <sup>(1)</sup> | —   | —                      | IOCA1                       | —              |
| RA2 | 4                      | 1             | ANA2                          | VREF-             | DAC1OUT1 | C1IN0+<br>C2IN0+ | —                 | —                                            | —      | —                     | —                                            | —                   | —                     | —                     | —   | —                      | IOCA2                       | —              |
| RA3 | 5                      | 2             | ANA3                          | VREF+             | —        | C1IN1+           | —                 | —                                            | —      | MDCIN1 <sup>(1)</sup> | —                                            | —                   | —                     | —                     | —   | —                      | IOCA3                       | —              |
| RA4 | 6                      | 3             | ANA4                          | —                 | —        | —                | —                 | —                                            | —      | MDCIN2 <sup>(1)</sup> | T0CKI <sup>(1)</sup>                         | CCP5 <sup>(1)</sup> | —                     | —                     | —   | —                      | IOCA4                       | —              |
| RA5 | 7                      | 4             | ANA5                          | —                 | —        | —                | —                 | SS1 <sup>(1)</sup>                           | —      | MDMIN <sup>(1)</sup>  | —                                            | —                   | —                     | —                     | —   | —                      | IOCA5                       | —              |
| RA6 | 10                     | 7             | ANA6                          | —                 | —        | —                | —                 | —                                            | —      | —                     | —                                            | —                   | —                     | —                     | —   | —                      | IOCA6                       | OSC2<br>CLKOUT |
| RA7 | 9                      | 6             | ANA7                          | —                 | —        | —                | —                 | —                                            | —      | —                     | —                                            | —                   | —                     | —                     | —   | —                      | IOCA7                       | OSC1<br>CLKIN  |
| RB0 | 21                     | 18            | ANB0                          | —                 | —        | C2IN1+           | ZCD               | SS2 <sup>(1)</sup>                           | —      | —                     | —                                            | CCP4 <sup>(1)</sup> | CWG1IN <sup>(1)</sup> | —                     | —   | —                      | INT <sup>(1)</sup><br>IOCB0 | —              |
| RB1 | 22                     | 19            | ANB1                          | —                 | —        | C1IN3-<br>C2IN3- | —                 | SCL2 <sup>(3,4)</sup><br>SCK2 <sup>(1)</sup> | —      | —                     | —                                            | —                   | CWG2IN <sup>(1)</sup> | —                     | —   | —                      | IOCB1                       | —              |
| RB2 | 23                     | 20            | ANB2                          | —                 | —        | —                | —                 | SDA2 <sup>(3,4)</sup><br>SDI2 <sup>(1)</sup> | —      | —                     | —                                            | —                   | CWG3IN <sup>(1)</sup> | —                     | —   | —                      | IOCB2                       | —              |
| RB3 | 24                     | 21            | ANB3                          | —                 | —        | C1IN2-<br>C2IN2- | —                 | —                                            | —      | —                     | —                                            | —                   | —                     | —                     | —   | —                      | IOCB3                       | —              |
| RB4 | 25                     | 22            | ANB4<br>ADCACT <sup>(1)</sup> | —                 | —        | —                | —                 | —                                            | —      | —                     | T5G <sup>(1)</sup><br>SMTWIN2 <sup>(1)</sup> | —                   | —                     | —                     | —   | —                      | IOCB4                       | —              |

- Note** 1: This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 5 for details on which PORT pins may be used for this signal.
- 2: All output signals shown in this row are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 6.
- 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
- 4: These pins are configured for I<sup>2</sup>C™ logic levels.; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I<sup>2</sup>C specific or SMBUS input buffer thresholds.

**TABLE 3: 28-PIN ALLOCATION TABLE (PIC16(L)F1885X)**

| I/O             | 28-Pin SPDIP/SOIC/SSOP | 28-Pin (U)QFN | ADC  | Voltage Reference | DAC      | Comparators | Zero-Cross Detect | MSSP (SPI/I <sup>2</sup> C™)                 | EUSART                                 | DSM | Timers/SMT                                                                                   | CCP and PWM         | CWG | CLC                   | NCO | Clock Reference (CLKR) | Interrupt-on-Change | Basic                   |
|-----------------|------------------------|---------------|------|-------------------|----------|-------------|-------------------|----------------------------------------------|----------------------------------------|-----|----------------------------------------------------------------------------------------------|---------------------|-----|-----------------------|-----|------------------------|---------------------|-------------------------|
| RB5             | 26                     | 23            | ANB5 | —                 | —        | —           | —                 | —                                            | —                                      | —   | T1G <sup>(1)</sup><br>SMTSIG2 <sup>(1)</sup>                                                 | CCP3 <sup>(1)</sup> | —   | —                     | —   | —                      | IOCB5               | —                       |
| RB6             | 27                     | 24            | ANB6 | —                 | —        | —           | —                 | —                                            | —                                      | —   | —                                                                                            | —                   | —   | CLCIN2 <sup>(1)</sup> | —   | —                      | IOCB6               | ICSPCLK                 |
| RB7             | 28                     | 25            | ANB7 | —                 | DAC1OUT2 | —           | —                 | —                                            | —                                      | —   | T6IN <sup>(1)</sup>                                                                          | —                   | —   | CLCIN3 <sup>(1)</sup> | —   | —                      | IOCB7               | ICSPDAT                 |
| RC0             | 11                     | 6             | ANC0 | —                 | —        | —           | —                 | —                                            | —                                      | —   | T1CKI <sup>(1)</sup><br>T3CKI <sup>(1)</sup><br>T3G <sup>(1)</sup><br>SMTWIN1 <sup>(1)</sup> | —                   | —   | —                     | —   | —                      | IOCC0               | SOSCO                   |
| RC1             | 12                     | 9             | ANC1 | —                 | —        | —           | —                 | —                                            | —                                      | —   | SMTSIG1 <sup>(1)</sup>                                                                       | CCP2 <sup>(1)</sup> | —   | —                     | —   | —                      | IOCC1               | SOSCI                   |
| RC2             | 13                     | 10            | ANC2 | —                 | —        | —           | —                 | —                                            | —                                      | —   | T5CKI <sup>(1)</sup>                                                                         | CCP1 <sup>(1)</sup> | —   | —                     | —   | —                      | IOCC2               | —                       |
| RC3             | 14                     | 11            | ANC3 | —                 | —        | —           | —                 | SCL1 <sup>(3,4)</sup><br>SCK1 <sup>(1)</sup> | —                                      | —   | T2IN <sup>(1)</sup>                                                                          | —                   | —   | —                     | —   | —                      | IOCC3               | —                       |
| RC4             | 15                     | 12            | ANC4 | —                 | —        | —           | —                 | SDA1 <sup>(3,4)</sup><br>SDI1 <sup>(1)</sup> | —                                      | —   | —                                                                                            | —                   | —   | —                     | —   | —                      | IOCC4               | —                       |
| RC5             | 16                     | 13            | ANC5 | —                 | —        | —           | —                 | —                                            | —                                      | —   | T4IN <sup>(1)</sup>                                                                          | —                   | —   | —                     | —   | —                      | IOCC5               | —                       |
| RC6             | 17                     | 14            | ANC6 | —                 | —        | —           | —                 | —                                            | CK(3)                                  | —   | —                                                                                            | —                   | —   | —                     | —   | —                      | IOCC6               | —                       |
| RC7             | 18                     | 15            | ANC7 | —                 | —        | —           | —                 | —                                            | RX <sup>(1)</sup><br>DT <sup>(3)</sup> | —   | —                                                                                            | —                   | —   | —                     | —   | —                      | IOCC7               | —                       |
| RE3             | 1                      | 26            | —    | —                 | —        | —           | —                 | —                                            | —                                      | —   | —                                                                                            | —                   | —   | —                     | —   | —                      | IOCE3               | MCLR<br>V <sub>PP</sub> |
| V <sub>DD</sub> | 20                     | 17            | —    | —                 | —        | —           | —                 | —                                            | —                                      | —   | —                                                                                            | —                   | —   | —                     | —   | —                      | —                   | —                       |
| V <sub>SS</sub> | 8,<br>19               | 5,<br>16      | —    | —                 | —        | —           | —                 | —                                            | —                                      | —   | —                                                                                            | —                   | —   | —                     | —   | —                      | —                   | —                       |

- Note**
- 1: This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 5 for details on which PORT pins may be used for this signal.
  - 2: All output signals shown in this row are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 6.
  - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
  - 4: These pins are configured for I<sup>2</sup>C™ logic levels.; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I<sup>2</sup>C specific or SMBUS input buffer thresholds.

TABLE 3: 28-PIN ALLOCATION TABLE (PIC16(L)F1885X)

| I/O                | 28-Pin SPDIP/SOIC/SSOP | 28-Pin (U)QFN | ADC              | Voltage Reference | DAC | Comparators    | Zero-Cross Detect | MSSP (SPI/I <sup>2</sup> C™) | EUSART                                        | DSM | Timers/SMT | CCP and PWM                                                | CWG                                                                                                      | CLC                                      | NCO | Clock Reference (CLKR) | Interrupt-on-Change | Basic |
|--------------------|------------------------|---------------|------------------|-------------------|-----|----------------|-------------------|------------------------------|-----------------------------------------------|-----|------------|------------------------------------------------------------|----------------------------------------------------------------------------------------------------------|------------------------------------------|-----|------------------------|---------------------|-------|
| OUT <sup>(2)</sup> | —                      | —             | ADGRDA<br>ADGRDB | —                 | —   | C1OUT<br>C2OUT | —                 | SDO1<br>SCK1<br>SDO2<br>SCK2 | TX/<br>CK <sup>(3)</sup><br>DT <sup>(3)</sup> | DSM | TMR0       | CCP1<br>CCP2<br>CCP3<br>CCP4<br>CCP5<br>PWM6OUT<br>PWM7OUT | CWG1A<br>CWG1B<br>CWG1C<br>CWG1D<br>CWG2A<br>CWG2B<br>CWG2C<br>CWG2D<br>CWG3A<br>CWG3B<br>CWG3C<br>CWG3D | CLC1OUT<br>CLC2OUT<br>CLC3OUT<br>CLC4OUT | NCO | CLKR                   | —                   | —     |

- Note** 1: This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 5 for details on which PORT pins may be used for this signal.
- 2: All output signals shown in this row are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 6.
- 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
- 4: These pins are configured for I<sup>2</sup>C™ logic levels.; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I<sup>2</sup>C specific or SMBUS input buffer thresholds.

**TABLE 4: 40/44-PIN ALLOCATION TABLE (PIC16(L)F1887X)**

| I/O | 40-Pin PDIP | 44-Pin TQFP | 40-Pin UQFN | 44-Pin QFN | ADC                        | Voltage Reference | DAC      | Comparators  | Zero-Cross Detect | MSSP (SPI/I <sup>2</sup> C™)              | EUSART | DSM                   | Timers/SMT                                | CCP and PWM         | CWG                   | CLC                   | NCO | Clock Reference (CLKR) | Interrupt-on-Change      | Basic       |
|-----|-------------|-------------|-------------|------------|----------------------------|-------------------|----------|--------------|-------------------|-------------------------------------------|--------|-----------------------|-------------------------------------------|---------------------|-----------------------|-----------------------|-----|------------------------|--------------------------|-------------|
| RA0 | 2           | 19          | 17          | 19         | ANA0                       | —                 | —        | C1IN0-C2IN0- | —                 | —                                         | —      | —                     | —                                         | —                   | —                     | CLCIN0 <sup>(1)</sup> | —   | —                      | IOCA0                    | —           |
| RA1 | 3           | 20          | 18          | 20         | ANA1                       | —                 | —        | C1IN1-C2IN1- | —                 | —                                         | —      | —                     | —                                         | —                   | —                     | CLCIN1 <sup>(1)</sup> | —   | —                      | IOCA1                    | —           |
| RA2 | 4           | 21          | 19          | 21         | ANA2                       | VREF-             | DAC1OUT1 | C1IN0+C2IN0+ | —                 | —                                         | —      | —                     | —                                         | —                   | —                     | —                     | —   | —                      | IOCA2                    | —           |
| RA3 | 5           | 22          | 20          | 22         | ANA3                       | VREF+             | —        | C1IN1+       | —                 | —                                         | —      | MDCIN1 <sup>(1)</sup> | —                                         | —                   | —                     | —                     | —   | —                      | IOCA3                    | —           |
| RA4 | 6           | 23          | 21          | 23         | ANA4                       | —                 | —        | —            | —                 | —                                         | —      | MDCIN2 <sup>(1)</sup> | T0CKI <sup>(1)</sup>                      | CCP5 <sup>(1)</sup> | —                     | —                     | —   | —                      | IOCA4                    | —           |
| RA5 | 7           | 24          | 22          | 24         | ANA5                       | —                 | —        | —            | —                 | SS1 <sup>(1)</sup>                        | —      | MDMIN <sup>(1)</sup>  | —                                         | —                   | —                     | —                     | —   | —                      | IOCA5                    | —           |
| RA6 | 14          | 31          | 29          | 33         | ANA6                       | —                 | —        | —            | —                 | —                                         | —      | —                     | —                                         | —                   | —                     | —                     | —   | —                      | IOCA6                    | OSC2 CLKOUT |
| RA7 | 13          | 30          | 28          | 32         | ANA7                       | —                 | —        | —            | —                 | —                                         | —      | —                     | —                                         | —                   | —                     | —                     | —   | —                      | IOCA7                    | OSC1 CLKIN  |
| RB0 | 33          | 8           | 8           | 9          | ANB0                       | —                 | —        | C2IN1+       | ZCD               | SS2 <sup>(1)</sup>                        | —      | —                     | —                                         | CCP4 <sup>(1)</sup> | CWG1IN <sup>(1)</sup> | —                     | —   | —                      | INT <sup>(1)</sup> IOCB0 | —           |
| RB1 | 34          | 9           | 9           | 10         | ANB1                       | —                 | —        | C1IN3-C2IN3- | —                 | SCL2 <sup>(3,4)</sup> SCK2 <sup>(1)</sup> | —      | —                     | —                                         | —                   | CWG2IN <sup>(1)</sup> | —                     | —   | —                      | IOCB1                    | —           |
| RB2 | 35          | 10          | 10          | 11         | ANB2                       | —                 | —        | —            | —                 | SDA2 <sup>(3,4)</sup> SDI2 <sup>(1)</sup> | —      | —                     | —                                         | —                   | CWG3IN <sup>(1)</sup> | —                     | —   | —                      | IOCB2                    | —           |
| RB3 | 36          | 11          | 11          | 12         | ANB3                       | —                 | —        | C1IN2-C2IN2- | —                 | —                                         | —      | —                     | —                                         | —                   | —                     | —                     | —   | —                      | IOCB3                    | —           |
| RB4 | 37          | 14          | 12          | 14         | ANB4 ADCACT <sup>(1)</sup> | —                 | —        | —            | —                 | —                                         | —      | —                     | T5G <sup>(1)</sup> SMTWIN2 <sup>(1)</sup> | —                   | —                     | —                     | —   | —                      | IOCB4                    | —           |
| RB5 | 38          | 15          | 13          | 15         | ANB5                       | —                 | —        | —            | —                 | —                                         | —      | —                     | T1G <sup>(1)</sup> SMTSIG2 <sup>(1)</sup> | CCP3 <sup>(1)</sup> | —                     | —                     | —   | —                      | IOCB5                    | —           |
| RB6 | 39          | 16          | 14          | 16         | ANB6                       | —                 | —        | —            | —                 | —                                         | —      | —                     | —                                         | —                   | —                     | CLCIN2 <sup>(1)</sup> | —   | —                      | IOCB6                    | ICSPCLK     |
| RB7 | 40          | 17          | 15          | 17         | ANB7                       | —                 | DAC1OUT2 | —            | —                 | —                                         | —      | —                     | T6IN <sup>(1)</sup>                       | —                   | —                     | CLCIN3 <sup>(1)</sup> | —   | —                      | IOCB7                    | ICSPDAT     |

- Note**
- 1: This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 5 for details on which PORT pins may be used for this signal.
  - 2: All output signals shown in this row are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 6.
  - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
  - 4: These pins are configured for I<sup>2</sup>C™ logic levels.; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I<sup>2</sup>C specific or SMBUS input buffer thresholds.

**TABLE 4: 40/44-PIN ALLOCATION TABLE (PIC16(L)F1887X)**

| I/O | 40-Pin PDIP | 44-Pin TQFP | 40-Pin UQFN | 44-Pin QFN | ADC  | Voltage Reference | DAC | Comparators | Zero-Cross Detect | MSSP (SPI/I <sup>2</sup> C™)                 | EUSART                                 | DSM | Timers/SMT                                                                                   | CCP and PWM         | CWG | CLC | NCO | Clock Reference (CLKR) | Interrupt-on-Change | Basic |
|-----|-------------|-------------|-------------|------------|------|-------------------|-----|-------------|-------------------|----------------------------------------------|----------------------------------------|-----|----------------------------------------------------------------------------------------------|---------------------|-----|-----|-----|------------------------|---------------------|-------|
| RC0 | 15          | 32          | 30          | 34         | ANC0 | —                 | —   | —           | —                 | —                                            | —                                      | —   | T1CKI <sup>(1)</sup><br>T3CKI <sup>(1)</sup><br>T3G <sup>(1)</sup><br>SMTWIN1 <sup>(1)</sup> | —                   | —   | —   | —   | —                      | IOCC0               | SOSCO |
| RC1 | 16          | 35          | 31          | 35         | ANC1 | —                 | —   | —           | —                 | —                                            | —                                      | —   | SMTSIG1 <sup>(1)</sup>                                                                       | CCP2 <sup>(1)</sup> | —   | —   | —   | —                      | IOCC1               | SOSCI |
| RC2 | 17          | 36          | 32          | 36         | ANC2 | —                 | —   | —           | —                 | —                                            | —                                      | —   | T5CKI <sup>(1)</sup>                                                                         | CCP1 <sup>(1)</sup> | —   | —   | —   | —                      | IOCC2               | —     |
| RC3 | 18          | 37          | 33          | 37         | ANC3 | —                 | —   | —           | —                 | SCL1 <sup>(3,4)</sup><br>SCK1 <sup>(1)</sup> | —                                      | —   | T2IN <sup>(1)</sup>                                                                          | —                   | —   | —   | —   | —                      | IOCC3               | —     |
| RC4 | 23          | 42          | 38          | 42         | ANC4 | —                 | —   | —           | —                 | SDA1 <sup>(3,4)</sup><br>SDI1 <sup>(1)</sup> | —                                      | —   | —                                                                                            | —                   | —   | —   | —   | —                      | IOCC4               | —     |
| RC5 | 24          | 43          | 39          | 43         | ANC5 | —                 | —   | —           | —                 | —                                            | —                                      | —   | T4IN <sup>(1)</sup>                                                                          | —                   | —   | —   | —   | —                      | IOCC5               | —     |
| RC6 | 25          | 44          | 40          | 44         | ANC6 | —                 | —   | —           | —                 | —                                            | CK <sup>(3)</sup>                      | —   | —                                                                                            | —                   | —   | —   | —   | —                      | IOCC6               | —     |
| RC7 | 26          | 1           | 1           | 1          | ANC7 | —                 | —   | —           | —                 | —                                            | RX <sup>(1)</sup><br>DT <sup>(3)</sup> | —   | —                                                                                            | —                   | —   | —   | —   | —                      | IOCC7               | —     |
| RD0 | 19          | 38          | 34          | 38         | AND0 | —                 | —   | —           | —                 | —                                            | —                                      | —   | —                                                                                            | —                   | —   | —   | —   | —                      | —                   | —     |
| RD1 | 20          | 39          | 35          | 39         | AND1 | —                 | —   | —           | —                 | —                                            | —                                      | —   | —                                                                                            | —                   | —   | —   | —   | —                      | —                   | —     |
| RD2 | 21          | 40          | 36          | 40         | AND2 | —                 | —   | —           | —                 | —                                            | —                                      | —   | —                                                                                            | —                   | —   | —   | —   | —                      | —                   | —     |
| RD3 | 22          | 41          | 37          | 41         | AND3 | —                 | —   | —           | —                 | —                                            | —                                      | —   | —                                                                                            | —                   | —   | —   | —   | —                      | —                   | —     |
| RD4 | 27          | 2           | 2           | 2          | AND4 | —                 | —   | —           | —                 | —                                            | —                                      | —   | —                                                                                            | —                   | —   | —   | —   | —                      | —                   | —     |
| RD5 | 28          | 3           | 3           | 3          | AND5 | —                 | —   | —           | —                 | —                                            | —                                      | —   | —                                                                                            | —                   | —   | —   | —   | —                      | —                   | —     |
| RD6 | 29          | 4           | 4           | 4          | AND6 | —                 | —   | —           | —                 | —                                            | —                                      | —   | —                                                                                            | —                   | —   | —   | —   | —                      | —                   | —     |
| RD7 | 30          | 5           | 5           | 5          | AND7 | —                 | —   | —           | —                 | —                                            | —                                      | —   | —                                                                                            | —                   | —   | —   | —   | —                      | —                   | —     |
| RE0 | 8           | 25          | 23          | 25         | ANE0 | —                 | —   | —           | —                 | —                                            | —                                      | —   | —                                                                                            | —                   | —   | —   | —   | —                      | —                   | —     |
| RE1 | 9           | 26          | 24          | 26         | ANE1 | —                 | —   | —           | —                 | —                                            | —                                      | —   | —                                                                                            | —                   | —   | —   | —   | —                      | —                   | —     |
| RE2 | 10          | 27          | 25          | 27         | ANE2 | —                 | —   | —           | —                 | —                                            | —                                      | —   | —                                                                                            | —                   | —   | —   | —   | —                      | —                   | —     |

- Note**
- 1: This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 5 for details on which PORT pins may be used for this signal.
  - 2: All output signals shown in this row are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 6.
  - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
  - 4: These pins are configured for I<sup>2</sup>C™ logic levels.; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I<sup>2</sup>C specific or SMBUS input buffer thresholds.

**TABLE 4: 40/44-PIN ALLOCATION TABLE (PIC16(L)F1887X)**

| I/O                | 40-Pin PDIP | 44-Pin TQFP | 40-Pin UQFN | 44-Pin QFN      | ADC              | Voltage Reference | DAC | Comparators    | Zero-Cross Detect | MSSP (SPI/I <sup>2</sup> C™) | EUSART                                        | DSM | Timers/SMT | CCP and PWM                                                | CWG                                                                                                      | CLC                                      | NCO | Clock Reference (CLKR) | Interrupt-on-Change | Basic                   |
|--------------------|-------------|-------------|-------------|-----------------|------------------|-------------------|-----|----------------|-------------------|------------------------------|-----------------------------------------------|-----|------------|------------------------------------------------------------|----------------------------------------------------------------------------------------------------------|------------------------------------------|-----|------------------------|---------------------|-------------------------|
| RE3                | 1           | 18          | 16          | 18              | —                | —                 | —   | —              | —                 | —                            | —                                             | —   | —          | —                                                          | —                                                                                                        | —                                        | —   | —                      | IOCE3               | MCLR<br>V <sub>PP</sub> |
| V <sub>DD</sub>    | 11,<br>32   | 7,<br>28    | 7,<br>26    | 8,<br>28        | —                | —                 | —   | —              | —                 | —                            | —                                             | —   | —          | —                                                          | —                                                                                                        | —                                        | —   | —                      | —                   | —                       |
| V <sub>SS</sub>    | 12,<br>31   | 6,<br>29    | 6,<br>27    | 6,<br>31,<br>30 | —                | —                 | —   | —              | —                 | —                            | —                                             | —   | —          | —                                                          | —                                                                                                        | —                                        | —   | —                      | —                   | —                       |
| OUT <sup>(2)</sup> | —           | —           | —           | —               | ADGRDA<br>ADGRDB | —                 | —   | C1OUT<br>C2OUT | —                 | SDO1<br>SCK1<br>SDO2<br>SCK2 | TX/<br>CK <sup>(3)</sup><br>DT <sup>(3)</sup> | DSM | TMR0       | CCP1<br>CCP2<br>CCP3<br>CCP4<br>CCP5<br>PWM6OUT<br>PWM7OUT | CWG1A<br>CWG1B<br>CWG1C<br>CWG1D<br>CWG2A<br>CWG2B<br>CWG2C<br>CWG2D<br>CWG3A<br>CWG3B<br>CWG3C<br>CWG3D | CLC1OUT<br>CLC2OUT<br>CLC3OUT<br>CLC4OUT | NCO | CLKR                   | —                   | —                       |

- Note**
- 1: This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 5 for details on which PORT pins may be used for this signal.
  - 2: All output signals shown in this row are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 6.
  - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
  - 4: These pins are configured for I<sup>2</sup>C™ logic levels.; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I<sup>2</sup>C specific or SMBUS input buffer thresholds.

**TABLE 5: PPS INPUT SIGNAL ROUTING OPTIONS DETAILS**

| Input Signal Name | Input Register Name | Default Location at POR | Re-mappable to any one of these PORTx pins |                                 | PPS Input Register Value to PORT Pin Mapping Reference Table |                                           |
|-------------------|---------------------|-------------------------|--------------------------------------------|---------------------------------|--------------------------------------------------------------|-------------------------------------------|
|                   |                     |                         | PIC16F1885X (28-Pin devices)               | PIC16F1887X (40/44-Pin devices) | Desired Input Pin                                            | Value to Write to Register <sup>(1)</sup> |
| INT               | INTPPS              | RB0                     | PORTA, PORTB                               | PORTA, PORTB                    | RA0                                                          | 0x00                                      |
| T0CKI             | T0CKIPPS            | RA4                     | PORTA, PORTB                               | PORTA, PORTB                    | RA1                                                          | 0x01                                      |
| T1CKI             | T1CKIPPS            | RC0                     | PORTA, PORTC                               | PORTA, PORTC                    | RA2                                                          | 0x02                                      |
| T1G               | T1GPPS              | RB5                     | PORTB, PORTC                               | PORTB, PORTC                    | RA3                                                          | 0x03                                      |
| T3CKI             | T3CKIPPS            | RC0                     | PORTB, PORTC                               | PORTB, PORTC                    | RA4                                                          | 0x04                                      |
| T3G               | T3GPPS              | RC0                     | PORTA, PORTC                               | PORTA, PORTC                    | RA5                                                          | 0x05                                      |
| T5CKI             | T5CKIPPS            | RC2                     | PORTA, PORTC                               | PORTA, PORTC                    | RA6                                                          | 0x06                                      |
| T5G               | T5GPPS              | RB4                     | PORTB, PORTC                               | PORTB, PORTD                    | RA7                                                          | 0x07                                      |
| T2IN              | T2INPPS             | RC3                     | PORTA, PORTC                               | PORTA, PORTC                    | RB0                                                          | 0x08                                      |
| T4IN              | T4INPPS             | RC5                     | PORTB, PORTC                               | PORTB, PORTC                    | RB1                                                          | 0x09                                      |
| T6IN              | T6INPPS             | RB7                     | PORTB, PORTC                               | PORTB, PORTD                    | RB2                                                          | 0x0A                                      |
| CCP1              | CCP1PPS             | RC2                     | PORTB, PORTC                               | PORTB, PORTC                    | RB3                                                          | 0x0B                                      |
| CCP2              | CCP2PPS             | RC1                     | PORTB, PORTC                               | PORTB, PORTC                    | RB4                                                          | 0x0C                                      |
| CCP3              | CCP3PPS             | RB5                     | PORTB, PORTC                               | PORTB, PORTD                    | RB5                                                          | 0x0D                                      |
| CCP4              | CCP4PPS             | RB0                     | PORTB, PORTC                               | PORTB, PORTD                    | RB6                                                          | 0x0E                                      |
| CCP5              | CCP5PPS             | RA4                     | PORTA, PORTC                               | PORTA, PORTE                    | RB7                                                          | 0x0F                                      |
| SMTWIN1           | SMTWIN1PPS          | RC0                     | PORTB, PORTC                               | PORTB, PORTC                    | RC0                                                          | 0x10                                      |
| SMTSIG1           | SMTSIG1PPS          | RC1                     | PORTB, PORTC                               | PORTB, PORTC                    | RC1                                                          | 0x11                                      |
| SMTWIN2           | SMTWIN2PPS          | RB4                     | PORTB, PORTC                               | PORTB, PORTD                    | RC2                                                          | 0x12                                      |
| SMTSIG2           | SMTSIG2PPS          | RB5                     | PORTB, PORTC                               | PORTB, PORTD                    | RC3                                                          | 0x13                                      |
| CWG1IN            | CWG1PPS             | RB0                     | PORTB, PORTC                               | PORTB, PORTD                    | RC4                                                          | 0x14                                      |
| CWG2IN            | CWG2PPS             | RB1                     | PORTB, PORTC                               | PORTB, PORTD                    | RC5                                                          | 0x15                                      |
| CWG3IN            | CWG3PPS             | RB2                     | PORTB, PORTC                               | PORTB, PORTD                    | RC6                                                          | 0x16                                      |
| MDCIN1            | MDCIN1PPS           | RA3                     | PORTA, PORTC                               | PORTA, PORTD                    | RC7                                                          | 0x17                                      |
| MDCIN2            | MDCIN2PPS           | RA4                     | PORTA, PORTC                               | PORTA, PORTD                    | RD0                                                          | 0x18                                      |
| MDMIN             | MDMINPPS            | RA5                     | PORTA, PORTC                               | PORTA, PORTD                    | RD1                                                          | 0x19                                      |
| CLCIN0            | CLCIN0PPS           | RA0                     | PORTA, PORTC                               | PORTA, PORTC                    | RD2                                                          | 0x1A                                      |
| CLCIN1            | CLCIN1PPS           | RA1                     | PORTB, PORTC                               | PORTA, PORTC                    | RD3                                                          | 0x1B                                      |
| CLCIN2            | CLCIN2PPS           | RB6                     | PORTB, PORTC                               | PORTB, PORTD                    | RD4                                                          | 0x1C                                      |
| CLCIN3            | CLCIN3PPS           | RB7                     | PORTB, PORTC                               | PORTB, PORTD                    | RD5                                                          | 0x1D                                      |
| ADCACT            | ADCACTPPS           | RB4                     | PORTB, PORTC                               | PORTB, PORTD                    | RD6                                                          | 0x1E                                      |
| SCK1/SCL1         | SSP1CLKPPS          | RC3                     | PORTB, PORTC                               | PORTB, PORTC                    | RD7                                                          | 0x1F                                      |
| SDI1/SDA1         | SSP1DATPPS          | RC4                     | PORTA, PORTC                               | PORTB, PORTC                    | RE0                                                          | 0x20                                      |
| SS1               | SSPSS1PPS           | RA5                     | PORTB, PORTC                               | PORTA, PORTD                    | RE1                                                          | 0x21                                      |
| SCK2/SCL2         | SSP2CLKPPS          | RB1                     | PORTB, PORTC                               | PORTB, PORTD                    | RE2                                                          | 0x22                                      |
| SDI2/SDA2         | SSP2DATPPS          | RB2                     | PORTB, PORTC                               | PORTB, PORTD                    | RE3                                                          | 0x23                                      |
| SS2               | SSP2SSPPS           | RB0                     | PORTB, PORTC                               | PORTB, PORTD                    |                                                              |                                           |
| RX/DT             | RXPPS               | RC7                     | PORTB, PORTC                               | PORTB PORTC                     |                                                              |                                           |
| TX/CK             | CKPPS               | RC6                     | PORTA, PORTB                               | PORTB PORTC                     |                                                              |                                           |

**Note 1:** Only a few of the values in this column are valid for any given signal. For example, since the INT signal can only be mapped to PORTA or PORTB pins, only the register values 0x00-0x0F (corresponding to RA0-RA7 and RB0-RB7) are valid values to write to the INTPPS register.

# PIC16(L)F1885X/7X

**TABLE 6: PPS OUTPUT SIGNAL ROUTING OPTIONS**

| Output Signal Name | Re-mappable to any one of these PORTx pins |                                    | By writing this value to the Corresponding RxyPPS <sup>(2)</sup> Register |
|--------------------|--------------------------------------------|------------------------------------|---------------------------------------------------------------------------|
|                    | PIC16F1885X<br>(28-Pin devices)            | PIC16F1887X<br>(40/44-Pin devices) |                                                                           |
| ADGRDB             | PORTA, PORTC                               | PORTA, PORTC                       | 0x25                                                                      |
| ADGRDA             | PORTA, PORTC                               | PORTA, PORTC                       | 0x24                                                                      |
| CWG3D              | PORTA, PORTC                               | PORTA, PORTD                       | 0x23                                                                      |
| CWG3C              | PORTA, PORTC                               | PORTA, PORTD                       | 0x22                                                                      |
| CWG3B              | PORTA, PORTC                               | PORTA, PORTE <sup>(1)</sup>        | 0x21                                                                      |
| CWG3A              | PORTB, PORTC                               | PORTB, PORTC                       | 0x20                                                                      |
| CWG2D              | PORTB, PORTC                               | PORTB, PORTD                       | 0x1F                                                                      |
| CWG2C              | PORTB, PORTC                               | PORTB, PORTD                       | 0x1E                                                                      |
| CWG2B              | PORTB, PORTC                               | PORTB, PORTD                       | 0x1D                                                                      |
| CWG2A              | PORTB, PORTC                               | PORTB, PORTC                       | 0x1C                                                                      |
| DSM                | PORTA, PORTC                               | PORTA, PORTD                       | 0x1B                                                                      |
| CLKR               | PORTB, PORTC                               | PORTB, PORTC                       | 0x1A                                                                      |
| NCO                | PORTA, PORTC                               | PORTA, PORTD                       | 0x19                                                                      |
| TMR0               | PORTB, PORTC                               | PORTB, PORTC                       | 0x18                                                                      |
| SDO2/SDA2          | PORTB, PORTC                               | PORTB, PORTD                       | 0x17                                                                      |
| SCK2/SCL2          | PORTB, PORTC                               | PORTB, PORTD                       | 0x16                                                                      |
| SDO1/SDA1          | PORTB, PORTC                               | PORTB, PORTC                       | 0x15                                                                      |
| SCK1/SCL1          | PORTB, PORTC                               | PORTB, PORTC                       | 0x14                                                                      |
| C2OUT              | PORTA, PORTC                               | PORTA, PORTE <sup>(1)</sup>        | 0x13                                                                      |
| C1OUT              | PORTA, PORTC                               | PORTA, PORTD                       | 0x12                                                                      |
| DT                 | PORTB, PORTC                               | PORTB, PORTC                       | 0x11                                                                      |
| TX/CK              | PORTB, PORTC                               | PORTB, PORTC                       | 0x10                                                                      |
| PWM7OUT            | PORTA, PORTC                               | PORTA, PORTC                       | 0x0F                                                                      |
| PWM6OUT            | PORTA, PORTC                               | PORTA, PORTD                       | 0x0E                                                                      |
| CCP5               | PORTA, PORTC                               | PORTA, PORTE <sup>(1)</sup>        | 0x0D                                                                      |
| CCP4               | PORTB, PORTC                               | PORTB, PORTD                       | 0x0C                                                                      |
| CCP3               | PORTB, PORTC                               | PORTB, PORTD                       | 0x0B                                                                      |
| CCP2               | PORTB, PORTC                               | PORTB, PORTC                       | 0x0A                                                                      |
| CCP1               | PORTB, PORTC                               | PORTB, PORTC                       | 0x09                                                                      |
| CWG1D              | PORTB, PORTC                               | PORTB, PORTD                       | 0x08                                                                      |
| CWG1C              | PORTB, PORTC                               | PORTB, PORTD                       | 0x07                                                                      |
| CWG1B              | PORTB, PORTC                               | PORTB, PORTD                       | 0x06                                                                      |
| CWG1A              | PORTB, PORTC                               | PORTB, PORTC                       | 0x05                                                                      |
| CLC4OUT            | PORTB, PORTC                               | PORTB, PORTD                       | 0x04                                                                      |
| CLC3OUT            | PORTB, PORTC                               | PORTB, PORTD                       | 0x03                                                                      |
| CLC2OUT            | PORTA, PORTC                               | PORTA, PORTC                       | 0x02                                                                      |
| CLC1OUT            | PORTA, PORTC                               | PORTA, PORTC                       | 0x01                                                                      |

**Note 1:** RE3 is an input-only pin. Therefore, this signal may only be mapped to RE0, RE1 or RE2 (or a PORTA pin).

**2:** In "RxyPPS", the "x" is a PORT letter (e.g., "C"), and the "y" is a port pin number (e.g., "6"). For example, to map the UART TX/CK signal to output onto RC6, write 0x10 to the RC6PPS register.

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