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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SD, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	80
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/rochester-electronics/mb9bf566npmc-g-jne2

Contents

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
68	58	47	36	J11	H12	P16 AN06 SIN2_2 INT14_1 MAD13_0	F	M
69	59	48	37	H12	H11	P17 AN07 SOT2_2 (SDA2_2) WKUP3 MAD14_0	F	P
70	60	49	38	H13	K13	AVCC	-	-
71	61	50	39	G13	J13	AVSS	-	-
72	62	51	40	F13	H13	AVRL	-	-
73	63	52	41	E13	G13	AVRH	-	-
74	64	53	42	H11	H10	P18 AN08 SCK2_2 (SCL2_2) MAD15_0	F	L
75	65	54	43	G12	G12	P19 AN09 SIN4_1 IC00_1 INT05_1 MAD16_0	F	M
76	66	55	44	G11	G11	P1A AN10 SOT4_1 (SDA4_1) IC01_1 MAD17_0	M	L
77	67	56	45	F12	G10	P1B AN11 SCK4_1 (SCL4_1) IC02_1 MAD18_0	M	L
78	68	-	46	F11	F13	P1C AN12 CTS4_1 IC03_1 MAD19_0	F	L
79	69	-	47	E12	F12	P1D AN13 RTS4_1 DTTI0X_1 MAD20_0	F	L

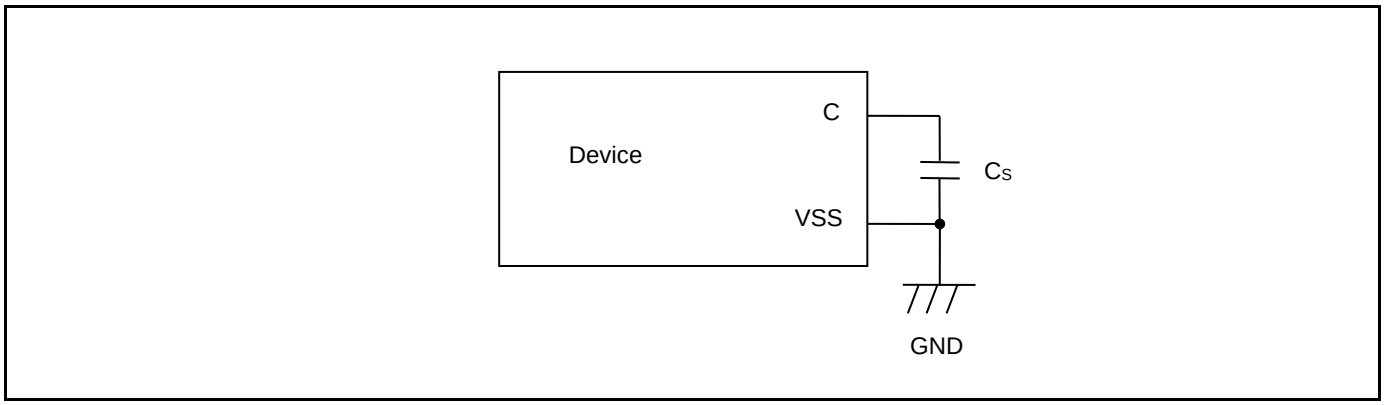
Pin Function	Pin Name	Function Description	Pin No					
			LQFP 120	LQFP 100	LQFP 80	QFP 100	BGA 112	BGA 144
Multi-function Timer 1	DTTI1X_0	Input signal controlling wave form generator outputs RTO10 to RTO15 of Multi-function timer 1.	8	8	8	86	E2	E2
	DTTI1X_1		55	-	-	-	-	L10
	FRCK1_0	16-bit free-run timer ch.1 external clock input pin	96	81	66	59	A9	D9
	FRCK1_1		50	45	35	23	L9	L8
	IC10_0	16-bit input capture ch.1 input pin of Multi-function timer 1. ICxx describes channel number.	95	80	65	58	A10	B10
	IC10_1		54	-	-	-	-	M10
	IC11_0		94	79	64	57	B10	A11
	IC11_1		53	-	-	-	-	K9
	IC12_0		93	78	63	56	B11	C10
	IC12_1		52	-	-	-	-	L9
	IC13_0		92	77	62	55	A12	B13
	IC13_1		51	-	-	-	-	K8
	RTO10_0 (PPG10_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	2	2	2	80	C1	C1
	RTO10_1 (PPG10_1)		32	27	-	5	N2	N2
	RTO11_0 (PPG10_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	3	3	3	81	C2	C2
	RTO11_1 (PPG10_1)		33	28	-	6	N3	L2
	RTO12_0 (PPG12_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	4	4	4	82	C3	D1
	RTO12_1 (PPG12_1)		34	29	-	7	M3	N3
	RTO13_0 (PPG12_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	5	5	5	83	D1	D2
	RTO13_1 (PPG12_1)		35	30	-	8	L3	M3
	RTO14_0 (PPG14_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	6	6	6	84	D2	D3
	RTO14_1 (PPG14_1)		36	31	21	9	M4	L4
	RTO15_0 (PPG14_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	7	7	7	85	E1	E1
	RTO15_1 (PPG14_1)		37	32	22	10	L5	K5

Handling when Using Multi-function Serial Pin as I²C Pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled.
However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
A smoothing capacitor of about 4.7 µF would be recommended for this series.



Mode Pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

Notes on Power-on

Turn power on/off in the following order or at the same time. The device operates normally after all power on.

VBAT only Power-on is possible when VBAT and VCC turns Power-on and Hibernation control is setting and then VCC turns Power-off. About Hibernation control, see Chapter 7-2: VBAT Domain(A) in FM4 Family Peripheral Manual Main Part(002-04856).
If not using the A/D converter and D/A converter, connect AVCC = VCC and AVSS = VSS.

Turning on:	VBAT → VCC → USBVCC
	VCC → AVCC → AVRH
Turning off:	AVRH → AVCC → VCC
	USBVCC → VCC → VBAT

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.

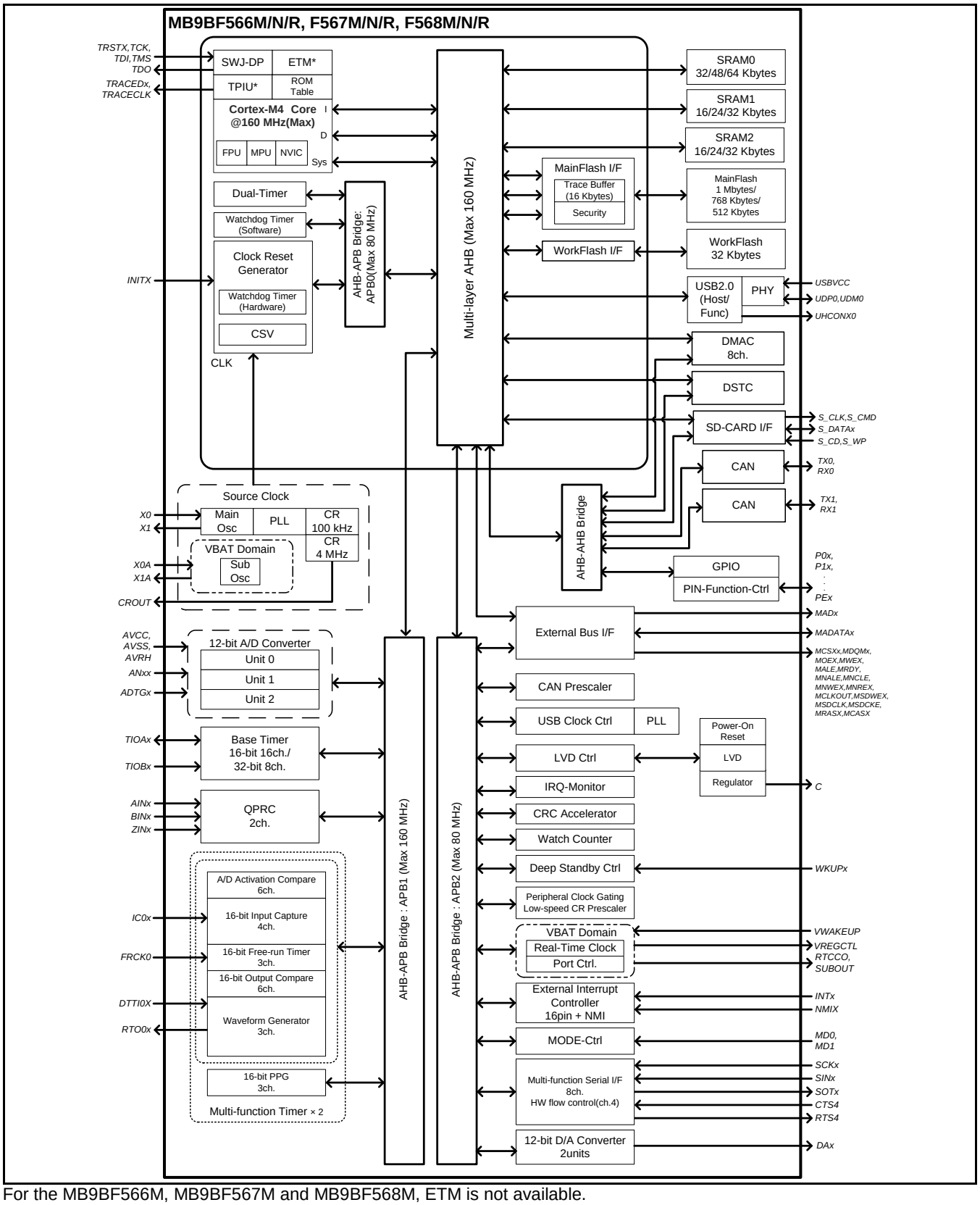
Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

Differences in Features among the Products with Different Memory Sizes and between Flash Products and MASK Products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

8. Block Diagram



*: For the MB9BF566M, MB9BF567M and MB9BF568M, ETM is not available.

Pin status Type	Function Group	Power-on Reset or Low-voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode, RTC Mode, or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
Q	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected							GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									
R	GPIO selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	USB I/O pin	Setting disabled	Setting disabled	Setting disabled		Hi-Z at trans-mission/ Input enabled / Internal input fixed at 0 at reception	Hi-Z at trans-mission/ Input enabled/ Internal input fixed at 0 at reception	Hi-Z / Input enabled	Hi-Z / Input enabled	Hi-Z / Input enabled

*1: Oscillation is stopped at Sub timer mode, sub CR timer mode, RTC mode, Stop mode, Deep Standby RTC mode, and Deep Standby Stop mode.

*2: Maintain previous state at timer mode. GPIO selected Internal input fixed at 0 at RTC mode, Stop mode.

*3: Maintain previous state at timer mode. Hi-Z/Internal input fixed at 0 at RTC mode, Stop mode.

Calculation Method of Power Dissipation (Pd)

The power dissipation is shown in the following formula.

$Pd = V_{CC} \times I_{CC} + \Sigma (I_{OL} \times V_{OL}) + \Sigma ((V_{CC}-V_{OH}) \times (-I_{OH}))$

I_{OL}: "L" level output current

I_{OH}: "H" level output current

V_{OL}: "L" level output voltage

V_{OH}: "H" level output voltage

I_{CC} is a current consumed in device.
It can be analyzed as follows.

$I_{CC} = I_{CC}(INT) + \Sigma I_{CC}(IO)$

$I_{CC}(INT)$: Current consumed in internal logic and memory, etc. through regulator

$\Sigma I_{CC}(IO)$: Sum of current (I/O switching current) consumed in output pin

For I_{CC} (INT), it can be anticipated by "(1) Current Rating" in "3. DC Characteristics" (This rating value does not include I_{CC} (IO) for a value at pin fixed).
For Icc (IO), it depends on system used by customers.
The calculation formula is shown below.

$I_{CC}(IO) = (C_{INT} + C_{EXT}) \times V_{CC} \times fsw$

C_{INT}: Pin internal load capacitance

C_{EXT}: External load capacitance of output pin

f_{SW}: Pin switching frequency

Parameter	Symbol	Conditions	Capacitance Value
Pin internal load capacitance	C_{INT}	4 mA type	1.93 pF
		8 mA type	3.45 pF
		12 mA type	3.42 pF

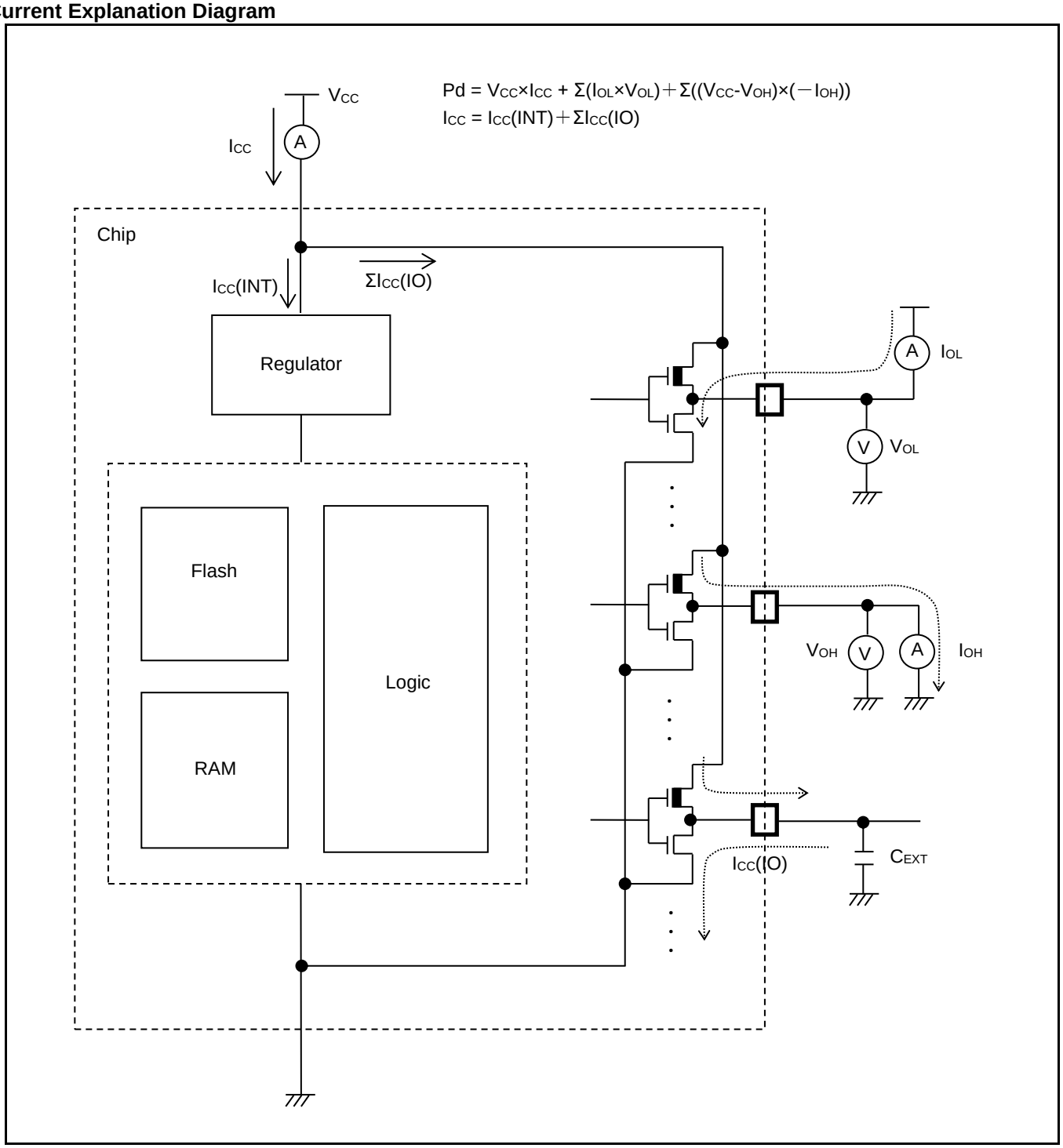
Calculate I_{CC} (Max) as follows when the power dissipation can be evaluated.

1. Measure current value I_{CC} (Typ) at normal temperature (+25°C).
2. Add maximum leak current value I_{CC} (leak_max) at operating on a value in (1).

$I_{CC}(Max) = I_{CC}(Typ) + I_{CC}(leak\_max)$

Parameter	Symbol	Conditions	Current Value
Maximum leak current at operating	I_{CC}(leak_max)	Tj = +125 °C	45.5 mA
		Tj = +105 °C	26.8 mA
		Tj = +85 °C	16.2 mA

Current Explanation Diagram



12.3 DC Characteristics

12.3.1 Current Rating

Table 12-1. Typical and maximum current consumption in Normal operation(PLL), code running from Flash memory (Flash accelerator mode and trace buffer function enabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation (PLL)	*5, *6	160 MHz	54	103	mA	*3 When all peripheral clocks are ON
					144 MHz	49	98		
					120 MHz	41	90		
					100 MHz	35	84		
					80 MHz	28	77		
					60 MHz	22	71		
					40 MHz	16	64		
					20 MHz	8.9	58		
					8 MHz	5.1	54		
					4 MHz	3.8	53		
					160 MHz	34	83	mA	*3 When all peripheral clocks are OFF
					144 MHz	31	80		
					120 MHz	26	75		
					100 MHz	22	71		
					80 MHz	18	67		
					60 MHz	14	63		
					40 MHz	10	59		
					20 MHz	6.2	55		
					8 MHz	3.8	53		
					4 MHz	3.1	52		

Table 12-2. Typical and maximum current consumption in Normal operation(PLL), code with data accessing running from Flash memory (Flash accelerator mode and trace buffer function disabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*7	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation (PLL)	*8	160 MHz	74	126	mA	*3 When all peripheral clocks are ON
					144 MHz	68	120		
					120 MHz	59	112		
					100 MHz	52	104		
					80 MHz	44	97		
					60 MHz	36	89		
					40 MHz	27	79		
					20 MHz	17	67		
					8 MHz	8.3	58		
					4 MHz	5.4	55		
					160 MHz	51	103	mA	*3 When all peripheral clocks are OFF
					144 MHz	47	100		
					120 MHz	42	94		
					100 MHz	37	90		
					80 MHz	33	85		
					60 MHz	28	80		
					40 MHz	21	73		
					20 MHz	13	64		
					8 MHz	6.9	56		
					4MHz	4.6	54		

Table 12-8. Typical and maximum current consumption in STOP mode, TIMER mode and RTC mode

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCH}	VCC	STOP mode	-	0.33	1.8	mA	*3, *4 Ta=+25°C
					-	15	mA	*3, *4 Ta=+85°C
					-	22	mA	*3, *4 Ta=+105°C
	I_{CCT}		TIMER mode (built-in high-speed CR)	4 MHz	0.70	2.2	mA	*3, *4 Ta=+25°C
					-	16	mA	*3, *4 Ta=+85°C
					-	22	mA	*3, *4 Ta=+105°C
			TIMER mode (sub oscillation)	32 kHz	0.33	1.8	mA	*3, *4 Ta=+25°C
					-	15	mA	*3, *4 Ta=+85°C
					-	22	mA	*3, *4 Ta=+105°C
			TIMER mode (built-in low-speed CR)	100 kHz	0.34	1.8	mA	*3, *4 Ta=+25°C
					-	15	mA	*3, *4 Ta=+85°C
					-	22	mA	*3, *4 Ta=+105°C
	I_{CCR}		RTC mode (sub oscillation)	32 kHz	0.33	1.8	mA	*3, *4 Ta=+25°C
					-	15	mA	*3, *4 Ta=+85°C
					-	22	mA	*3, *4 Ta=+105°C

*1: V_{CC}=3.3 V

*2: V_{CC}=5.5 V

*3: When all ports are fixed.

*4: When LVD is OFF

12.3.2 Pin Characteristics

(V_{CC} = $USBV_{CC}$ = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V)

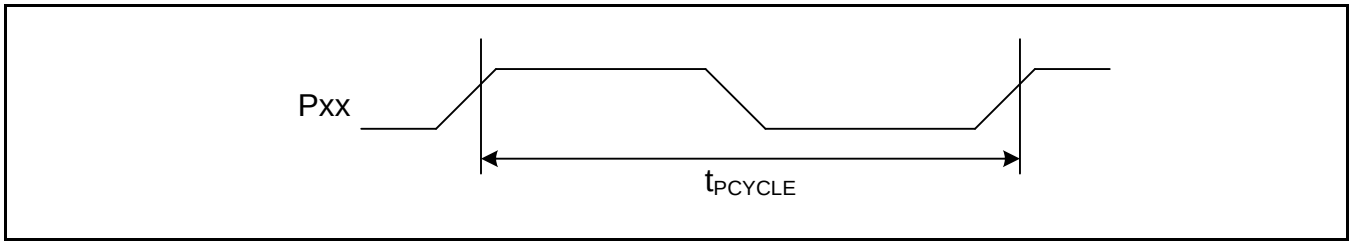
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	-	V_{CC}×0.8	-	V_{CC} + 0.3	V	
		5V tolerant input pin	-	V_{CC}×0.8	-	V_{SS} + 5.5	V	
		Input pin doubled as I^2C Fm+	-	V_{CC}×0.7	-	V_{SS} + 5.5	V	
"L" level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		5V tolerant input pin	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		Input pin doubled as I^2C Fm+	-	V_{SS}	-	V_{CC}×0.3	V	
"H" level output voltage	V_{OH}	4mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 4 mA V_{CC} < 4.5 V, I_{OH} = - 2 mA	V_{CC} - 0.5	-	V_{CC}	V	
		8mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 8 mA V_{CC} < 4.5 V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
		12mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 12 mA V_{CC} < 4.5 V, I_{OH} = - 8 mA	V_{CC} - 0.5	-	V_{CC}	V	
		The pin doubled as USB I/O	$USBV_{CC}$ ≥ 4.5 V, I_{OH} = - 20.5 mA $USBV_{CC}$ < 4.5 V, I_{OH} = - 13.0 mA	$USBV_{CC}$ - 0.4	-	$USBV_{CC}$	V	
		The pin doubled as I^2C Fm+	V_{CC} ≥ 4.5 V, I_{OH} = - 4 mA V_{CC} < 4.5 V, I_{OH} = - 3 mA	V_{CC} - 0.5	-	V_{CC}	V	At GPIO

12.4.9 GPIO Output Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{PCYCLE}	Pxx*	$V_{CC} \geq 4.5$ V	-	50	MHz
			$V_{CC} < 4.5$ V	-	32	MHz

*: GPIO is a target.



12.4.10 External Bus Timing

External Bus Clock Output Characteristics

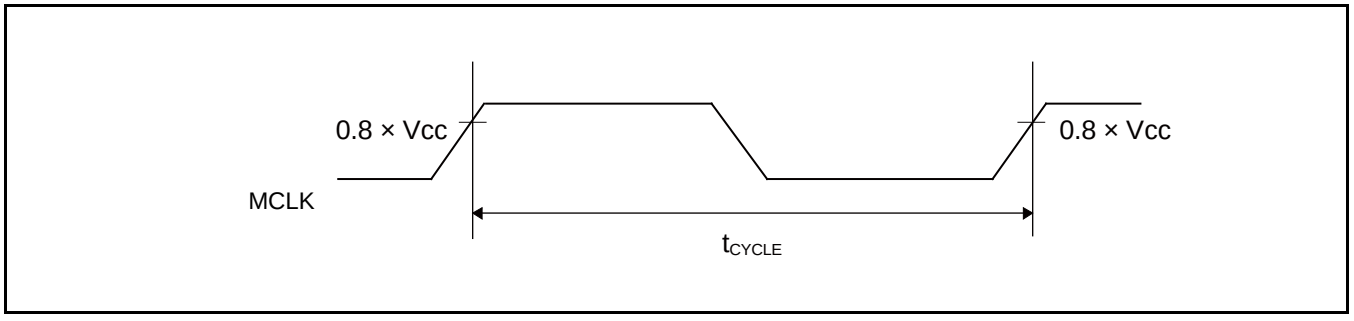
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{CYCLE}	MCLKOUT*1	$V_{CC} \geq 4.5$ V	-	50*2	MHz
			$V_{CC} < 4.5$ V	-	32*3	MHz

*1: The external bus clock (MCLKOUT) is a divided clock of HCLK.
For more information about setting of clock divider, see CHAPTER 14: External Bus Interface in FM4 Family Peripheral Manual Main part (002-04856).

*2: Generate MCLKOUT at setting more than 4 division when the AHB bus clock exceeds 100 MHz.

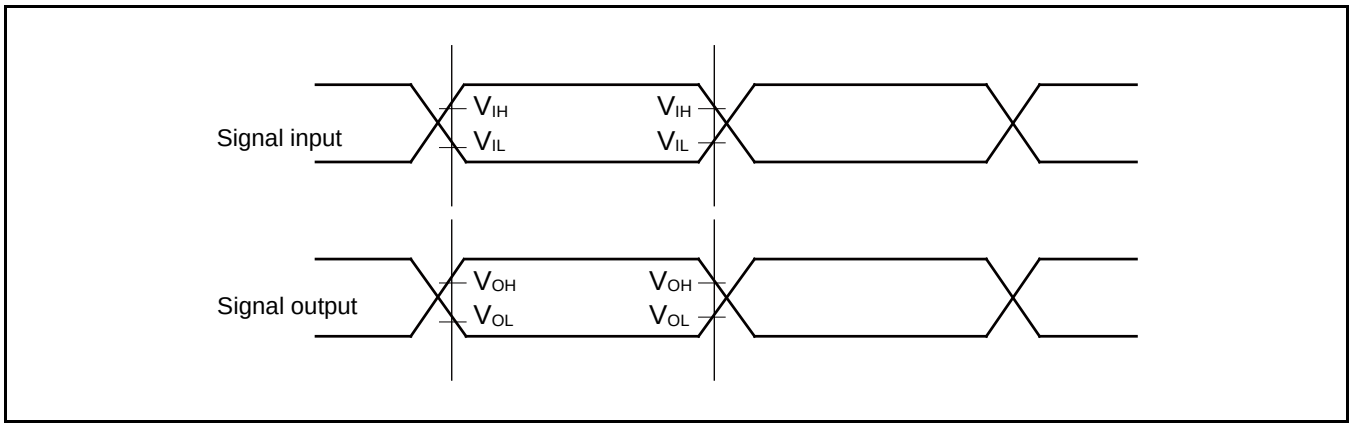
*3: Generate MCLKOUT at setting more than 4 division when the AHB bus clock exceeds 64 MHz.



External Bus Signal Input/output Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	V_{IH}	-	0.8 × V_{CC}	V	
	V_{IL}		0.2 × V_{CC}	V	
Signal output characteristics	V_{OH}		0.8 × V_{CC}	V	
	V_{OL}		0.2 × V_{CC}	V	



NAND Flash Mode

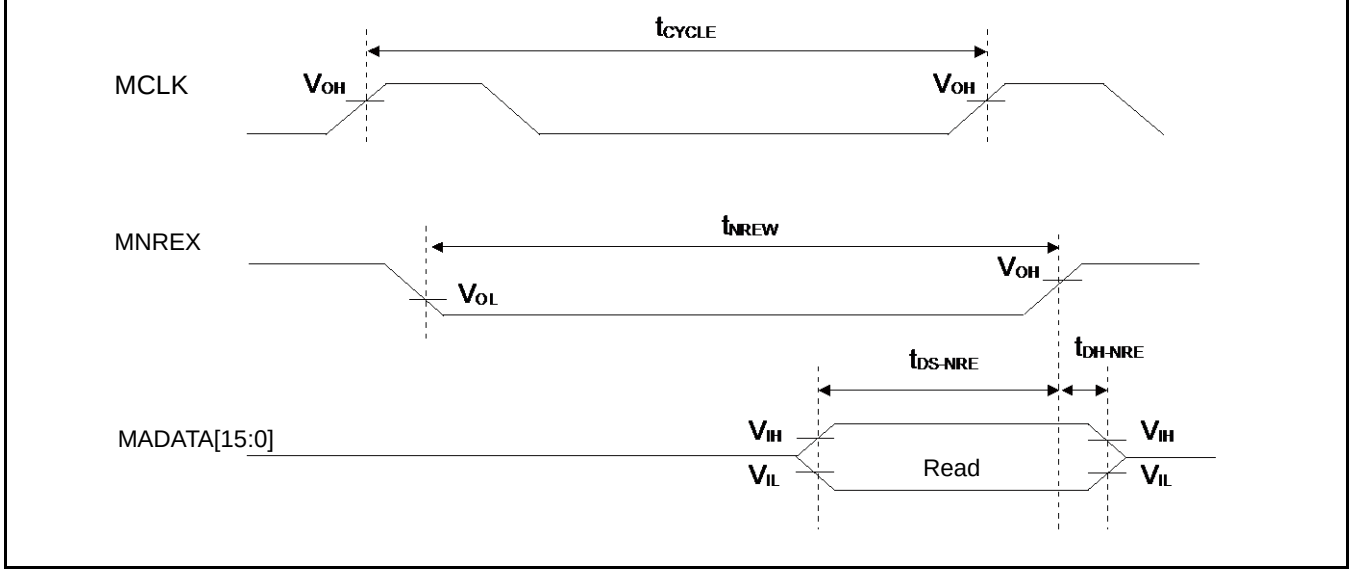
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

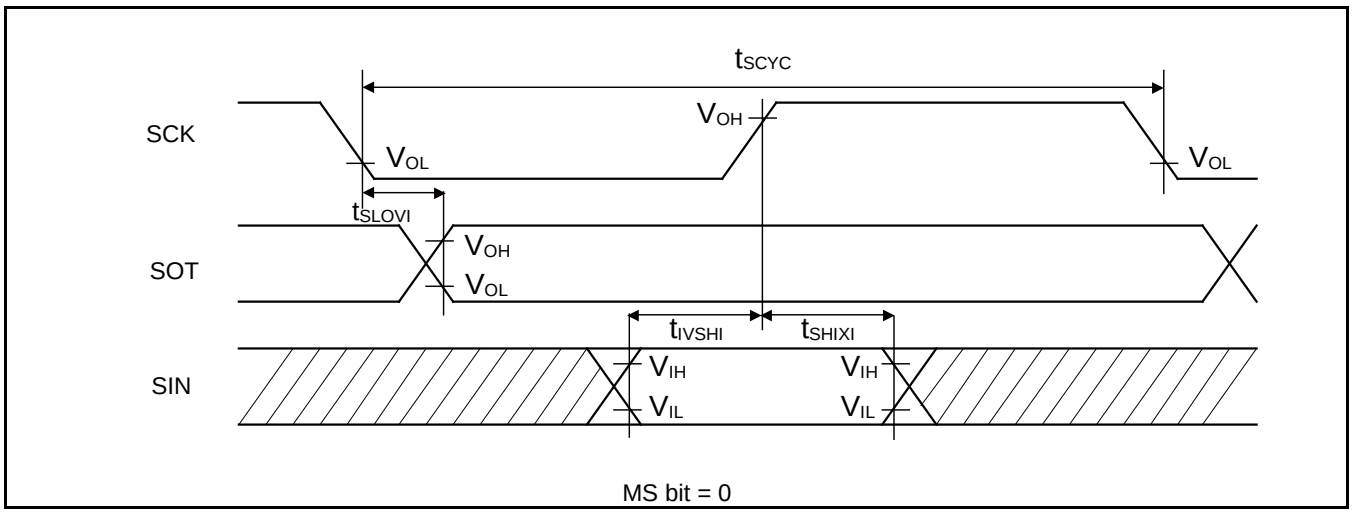
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
MNREX Min pulse width	t_{NREW}	MNREX	$V_{CC} \geq 4.5$ V	MCLK×n-3	-	ns
			$V_{CC} < 4.5$ V			
Data set up →MNREX↑ time	t_{DS-NRE}	MNREX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	20	-	ns
			$V_{CC} < 4.5$ V	38	-	
MNREX↑→ Data hold time	t_{DH-NRE}	MNREX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	-	ns
			$V_{CC} < 4.5$ V			
MNALE↑→ MNWEX delay time	$t_{ALEH-NWEL}$	MNALE, MNWEX	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
MNALE↓→ MNWEX delay time	$t_{ALEL-NWEL}$	MNALE, MNWEX	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
MNCLE↑→ MNWEX delay time	$t_{CLEH-NWEL}$	MNCLE, MNWEX	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
MNWEX↑→ MNCLE delay time	$t_{NWEH-CLEL}$	MNCLE, MNWEX	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MNWEX Min pulse width	t_{NWEW}	MNWEX	$V_{CC} \geq 4.5$ V	MCLK×n-3	-	ns
			$V_{CC} < 4.5$ V			
MNWEX↓→ Data output time	$t_{NWEL-DV}$	MNWEX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	- 9	+ 9	ns
			$V_{CC} < 4.5$ V	-12	+12	
MNWEX↑→ Data hold time	$t_{NWEH-DX}$	MNWEX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	

Note:

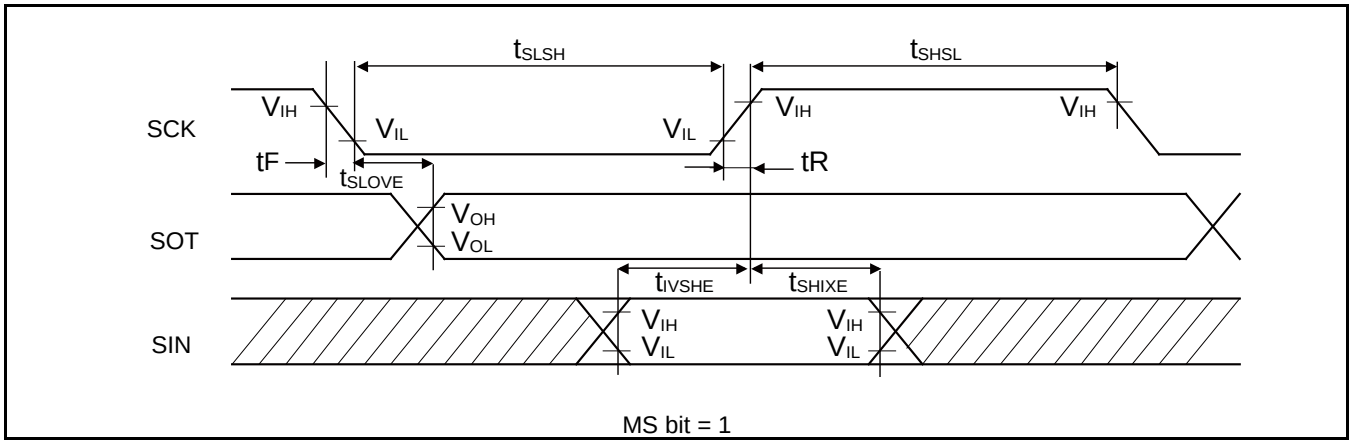
- *When the external load capacitance C_L = 30 pF (m=0 to 15, n=1 to 16)*

NAND Flash Read





MS bit = 0



MS bit = 1

High-speed Synchronous Serial (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	5	-	ns
SOT→SCK↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ – 10	-	$2t_{CYCP}$ – 10	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ – 5	-	$2t_{CYCP}$ – 5	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	5	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	5	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*

  No chip select: SIN4_1, SOT4_1, SCK4_1
  Chip select: SIN6_1, SOT6_1, SCK6_1, SCS6_1
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*

12.4.15 I^2C Timing

Standard-mode, Fast-mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	F_{SCL}	C_L = 30 pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock "L" width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock "H" width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	2 MHz ≤ t_{CYCP}<40 MHz	$2t_{CYCP}$*4	-	$2t_{CYCP}$*4	-	ns	*5
		40 MHz ≤ t_{CYCP}<60 MHz	$4t_{CYCP}$*4	-	$4t_{CYCP}$*4	-	ns	
		60 MHz ≤ t_{CYCP}<80 MHz	$6t_{CYCP}$*4	-	$6t_{CYCP}$*4	-	ns	
		80 MHz ≤ t_{CYCP}<100 MHz	$8t_{CYCP}$*4	-	$8t_{CYCP}$*4	-	ns	
		100 MHz ≤ t_{CYCP}<120 MHz	$10t_{CYCP}$*4	-	$10t_{CYCP}$*4	-	ns	
		120 MHz ≤ t_{CYCP}<140 MHz	$12t_{CYCP}$*4	-	$12t_{CYCP}$*4	-	ns	
		140 MHz ≤ t_{CYCP}<160 MHz	$14t_{CYCP}$*4	-	$14t_{CYCP}$*4	-	ns	
		160 MHz ≤ t_{CYCP}<180 MHz	$16t_{CYCP}$*4	-	$16t_{CYCP}$*4	-	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

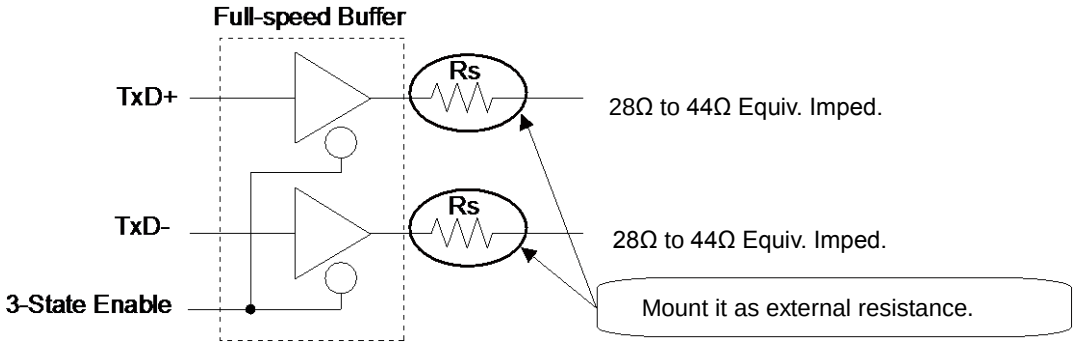
*2: The maximum $t_{HDDA}T$ must satisfy that it does not extend at least "L" period (t_{LOW}) of device's SCL signal.

*3: A Fast-mode I^2C bus device can be used on a Standard-mode I^2C bus system as long as the device satisfies the requirement of t_{SUDAT} ≥ 250 ns.

*4: t_{CYCP} is the APB bus clock cycle time.
About the APB bus number that I^2C is connected to, see "8. Block Diagram" in this data sheet.

*5: The noise filter time can be changed by register settings.
Change the number of the noise filter steps according to APB bus clock frequency.

*6: USB Full-speed connection is performed via twist pair cable shield with 90 Ω ± 15% characteristic impedance (Differential Mode).
USB standard defines that output impedance of USB driver must be in range from 28 Ω to 44 Ω. So, discrete series resistor (Rs) addition is defined in order to satisfy the above definition and keep balance.
When using this USB I/O, use it with 25 Ω to 30 Ω (recommendation value 27 Ω) Series resistor Rs.

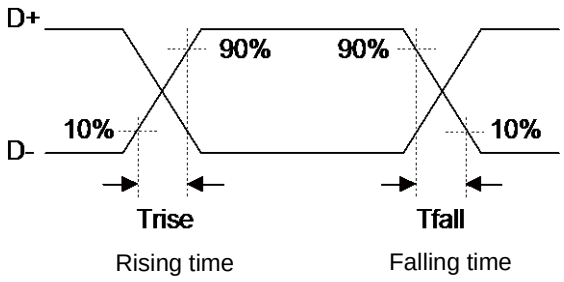


Rs series resistor 25 Ω to 30 Ω

Series resistor of 27 Ω (recommendation value) must be added.

And, use "resistance with an uncertainty of 5% by E24 sequence".

*7: They indicate rising time (Trise) and falling time (Tfall) of the low-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.



See Low-Speed Load (Compliance Load) for conditions of external load.

Page	Section	Change Results
Revision 1.1		
-	-	Company name and layout design change
Revision 2.0		
1,3	Title	Added the following product. MB9BF568F
5	2. Features	Added the Voice Function
13,14	3. Product Lineup	Added the following product. MB9BF568F
15	4. Packages	Added the following product. MB9BF568F
169	15. Ordering Information	Added the following product. MB9BF568FBGL-000GE1

NOTE: Please see “Document History” about later revised information.