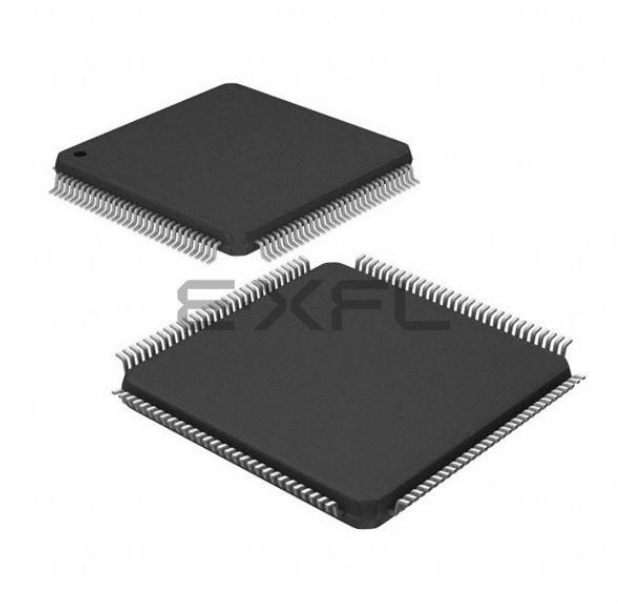
Infineon Technologies - MB9BF566RPMC-G-JNE2 Datasheet



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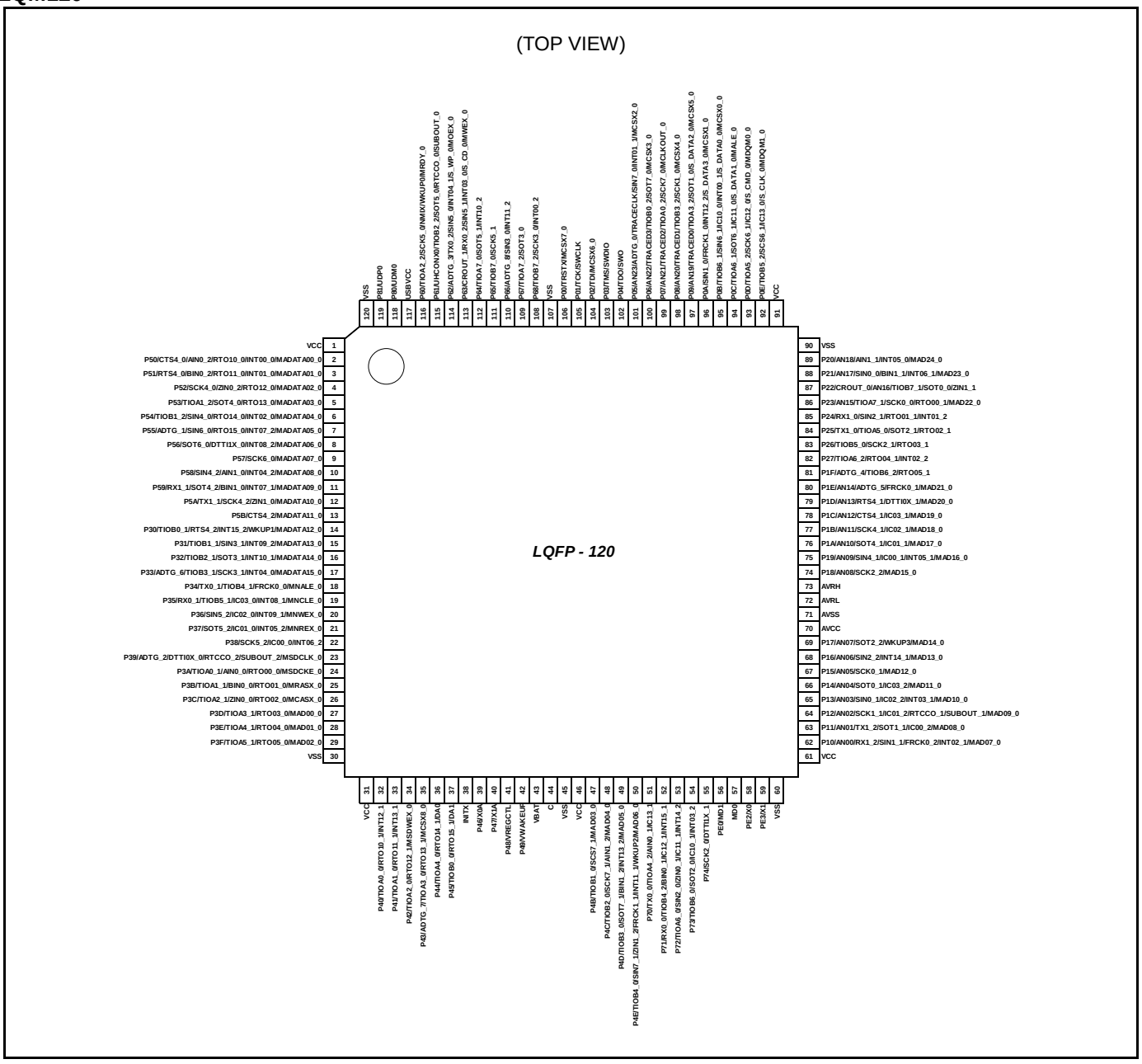
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SD, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9bf566rpmc-g-jne2

LQM120



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
22	17	-	95	H3	H4	P38 SCK5_2 (SCL5_2) IC00_0 INT06_2	E	K
-					-	MADATA15_0		
23	18	13	96	J1	J1	P39 ADTG_2 DTTI0X_0 RTCCO_2 SUBOUT_2	L	I
		-				MSDCLK_0		
24	19	14	97	J2	J2	P3A TIOA0_1 AIN0_0 RTO00_0 (PPG00_0)	G	I
		-				MSDCKE_0		
25	20	15	98	J3	J3	P3B TIOA1_1 BIN0_0 RTO01_0 (PPG00_0)	G	I
		-				MRASX_0		
26	21	16	99	K1	J4	P3C TIOA2_1 ZIN0_0 RTO02_0 (PPG02_0)	G	I
		-				MCASX_0		
27	22	17	100	K2	K2	P3D TIOA3_1 RTO03_0 (PPG02_0)	G	I
						MAD00_0		
28	23	18	1	L1	K3	P3E TIOA4_1 RTO04_0 (PPG04_0)	G	I
						MAD01_0		
29	24	19	2	L2	L1	P3F TIOA5_1 RTO05_0 (PPG04_0)	G	I
						MAD02_0		
30	25	20	3	N1	N1	VSS	-	-
31	26	-	4	M1	M1	VCC	-	-

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
104	89	70	67	C6	C7	P02 TDI MCSX6_0	E	H
105	90	71	68	A6	B7	P01 TCK SWCLK	E	G
106	91	72	69	B6	D6	P00 TRSTX MCSX7_0	E	H
107	92	-	70	A5	A7	VSS	-	-
108	-	-	-	-	C6	P68 TIOB7_2 SCK3_0 (SCL3_0) INT00_2	E	K
109	-	-	-	-	B6	P67 TIOA7_2 SOT3_0 (SDA3_0)	E	I
110	-	-	-	-	A6	P66 ADTG_8 SIN3_0 INT11_2	E	K
111	-	-	-	-	D5	P65 TIOB7_0 SCK5_1 (SCL5_1)	E	I
112	-	-	-	-	C5	P64 TIOA7_0 SOT5_1 (SDA5_1) INT10_2	E	K
113	93	73	71	C5	B5	P63 CROUT_1 RX0_2	E	K
	-	-	-	-		SIN5_1		
	93	73	71	C5		INT03_0 S_CD_0 MWEX_0		
114	94	74	72	B5	C4	P62 ADTG_3 TX0_2 SIN5_0 INT04_1 S_WP_0 MOEX_0	I	K

Pin Function	Pin Name	Function Description	Pin No					
			LQFP 120	LQFP 100	LQFP 80	QFP 100	BGA 112	BGA 144
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	33	28	-	6	N3	L2
	TIOA1_1		25	20	15	98	J3	J3
	TIOA1_2		5	5	5	83	D1	D2
	TIOB1_0	Base timer ch.1 TIOB pin	47	42	32	20	L7	L7
	TIOB1_1		15	10	10	88	F1	G1
	TIOB1_2		6	6	6	84	D2	D3
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	34	29	-	7	M3	N3
	TIOA2_1		26	21	16	99	K1	J4
	TIOA2_2		116	96	76	74	B3	B3
	TIOB2_0	Base timer ch.2 TIOB pin	48	43	33	21	L8	K7
	TIOB2_1		16	11	11	89	F2	G2
	TIOB2_2		115	95	75	73	B4	B4
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	35	30	-	8	L3	M3
	TIOA3_1		27	22	17	100	K2	K2
	TIOA3_2		97	82	67	60	B9	C9
	TIOB3_0	Base timer ch.3 TIOB pin	49	44	34	22	M9	M8
	TIOB3_1		17	12	12	90	F3	G3
	TIOB3_2		98	83	-	61	C9	B9
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	36	31	21	9	M4	L4
	TIOA4_1		28	23	18	1	L1	K3
	TIOA4_2		51	-	-	-	-	K8
	TIOB4_0	Base timer ch.4 TIOB pin	50	45	35	23	L9	L8
	TIOB4_1		18	13	-	91	G1	G4
	TIOB4_2		52	-	-	-	-	L9
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	84	-	-	-	-	E11
	TIOA5_1		29	24	19	2	L2	L1
	TIOA5_2		93	78	63	56	B11	C10
	TIOB5_0	Base timer ch.5 TIOB pin	83	-	-	-	-	E12
	TIOB5_1		19	14	-	92	G2	H1
	TIOB5_2		92	77	62	55	A12	B13
Base Timer 6	TIOA6_0	Base timer ch.6 TIOA pin	53	-	-	-	-	K9
	TIOA6_1		94	79	64	57	B10	A11
	TIOA6_2		82	-	-	-	-	E13
	TIOB6_0	Base timer ch.6 TIOB pin	54	-	-	-	-	M10
	TIOB6_1		95	80	65	58	A10	B10
	TIOB6_2		81	-	-	-	-	F10
Base Timer 7	TIOA7_0	Base timer ch.7 TIOA pin	112	-	-	-	-	C5
	TIOA7_1		86	71	57	49	D13	D13
	TIOA7_2		109	-	-	-	-	B6
	TIOB7_0	Base timer ch.7 TIOB pin	111	-	-	-	-	D5
	TIOB7_1		87	72	58	50	D12	D12
	TIOB7_2		108	-	-	-	-	C6
CAN 0	TX0_0	CAN interface ch.0 TX output pin	51	-	-	-	-	K8
	TX0_1		18	13	-	91	G1	G4
	TX0_2		114	94	74	72	B5	C4
	RX0_0	CAN interface ch.0 RX output pin	52	-	-	-	-	L9
	RX0_1		19	14	-	92	G2	H1
	RX0_2		113	93	73	71	C5	B5
CAN 1	TX1_0	CAN interface ch.1 TX output pin	84	-	-	-	-	E11
	TX1_1		12	-	-	-	-	F2
	TX1_2		63	53	42	31	L12	K12
	RX1_0	CAN interface ch.1 RX output pin	85	-	-	-	-	E10
	RX1_1		11	-	-	-	-	F1
	RX1_2		62	52	41	30	L13	L12

Pin Function	Pin Name	Function Description	Pin No					
			LQFP 120	LQFP 100	LQFP 80	QFP 100	BGA 112	BGA 144
Debugger	SWCLK	Serial wire debug interface clock input pin	105	90	71	68	A6	B7
	SWDIO	Serial wire debug interface data input / output pin	103	88	69	66	B7	D7
	SWO	Serial wire viewer output pin	102	87	68	65	C7	B8
	TCK	JTAG test clock input pin	105	90	71	68	A6	B7
	TDI	JTAG test data input pin	104	89	70	67	C6	C7
	TDO	JTAG debug data output pin	102	87	68	65	C7	B8
	TMS	JTAG test mode state input/output pin	103	88	69	66	B7	D7
	TRACECLK	Trace CLK output pin of ETM	101	86	-	64	C8	C8
	TRACED0	Trace data output pin of ETM	97	82	-	60	B9	C9
	TRACED1		98	83	-	61	C9	B9
	TRACED2		99	84	-	62	A8	A9
	TRACED3		100	85	-	63	B8	D8
	TRSTX	JTAG test reset input pin	106	91	72	69	B6	D6
External Bus	MAD00_0	External bus interface address bus	27	22	17	100	K2	K2
	MAD01_0		28	23	18	1	L1	K3
	MAD02_0		29	24	19	2	L2	L1
	MAD03_0		47	42	32	20	L7	L7
	MAD04_0		48	43	33	21	L8	K7
	MAD05_0		49	44	34	22	M9	M8
	MAD06_0		50	45	35	23	L9	L8
	MAD07_0		62	52	41	30	L13	L12
	MAD08_0		63	53	42	31	L12	K12
	MAD09_0		64	54	43	32	K13	K11
	MAD10_0		65	55	44	33	K12	J12
	MAD11_0		66	56	45	34	J13	J11
	MAD12_0		67	57	46	35	J12	J10
	MAD13_0		68	58	47	36	J11	H12
	MAD14_0		69	59	48	37	H12	H11
	MAD15_0		74	64	53	42	H11	H10
	MAD16_0		75	65	54	43	G12	G12
	MAD17_0		76	66	55	44	G11	G11
	MAD18_0		77	67	56	45	F12	G10
	MAD19_0		78	68	-	46	F11	F13
	MAD20_0		79	69	-	47	E12	F12
	MAD21_0		80	70	-	48	E11	F11
	MAD22_0		86	71	-	49	D13	D13
	MAD23_0		88	73	-	51	C13	D11
	MAD24_0		89	74	-	52	C12	C12

Pin Function	Pin Name	Function Description	Pin No					
			LQFP 120	LQFP 100	LQFP 80	QFP 100	BGA 112	BGA 144
GPIO	P60	General-purpose I/O port 6	116	96	76	74	B3	B3
	P61		115	95	75	73	B4	B4
	P62		114	94	74	72	B5	C4
	P63		113	93	73	71	C5	B5
	P64		112	-	-	-	-	C5
	P65		111	-	-	-	-	D5
	P66		110	-	-	-	-	A6
	P67		109	-	-	-	-	B6
	P68		108	-	-	-	-	C6
	P70	General-purpose I/O port 7	51	-	-	-	-	K8
	P71		52	-	-	-	-	L9
	P72		53	-	-	-	-	K9
	P73		54	-	-	-	-	M10
	P74		55	-	-	-	-	L10
	P80	General-purpose I/O port 8	118	98	78	76	A3	A3
	P81		119	99	79	77	A2	A2
	PE0	General-purpose I/O port E	56	46	36	24	M10	N10
	PE2		58	48	38	26	N11	N11
	PE3		59	49	39	27	N12	N12
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	88	73	59	51	C13	D11
	SIN0_1		65	55	44	33	K12	J12
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I^2C (operation mode 4).	87	72	58	50	D12	D12
	SOT0_1 (SDA0_1)		66	56	45	34	J13	J11
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SCL0 when it is used in an I^2C (operation mode 4).	86	71	57	49	D13	D13
	SCK0_1 (SCL0_1)		67	57	46	35	J12	J10
Multi-function Serial 1	SIN1_0	Multi-function serial interface ch.1 input pin	96	81	66	59	A9	D9
	SIN1_1		62	52	41	30	L13	L12
	SOT1_0 (SDA1_0)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I^2C (operation mode 4).	97	82	67	60	B9	C9
	SOT1_1 (SDA1_1)		63	53	42	31	L12	K12
	SCK1_0 (SCL1_0)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a CSIO (operation modes 4) and as SCL1 when it is used in an I^2C (operation mode 4).	98	83	-	61	C9	B9
	SCK1_1 (SCL1_1)		64	54	43	32	K13	K11

6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.

3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Package thermal resistance and maximum permissible power for each package are shown below.
The operation is guaranteed maximum permissible power or less for semiconductor devices.

Table for Package Thermal Resistance and Maximum Permissible Power

Package	Printed Circuit Board	Thermal Resistance θja (°C/W)	Maximum Permissible Power (mW)	
			Ta=+85 °C	Ta=+105 °C
LQH080 (0.5 mm pitch)	Single-layered both sides	60	667	333
	4 layers	39	1026	513
LQJ080 (0.65 mm pitch)	Single-layered both sides	58	690	335
	4 layers	38	1053	526
LQI100 (0.5 mm pitch)	Single-layered both sides	57	702	351
	4 layers	38	1053	526
PQH100 (0.65 mm pitch)	Single-layered both sides	48	833	417
	4 layers	34	1177	588
LQM120 (0.5 mm pitch)	Single-layered both sides	62	645	323
	4 layers	43	930	465
LDC112 (0.5 mm pitch)	Single-layered both sides	60	667	333
	4 layers	40	1000	500
LDC144 (0.5 mm pitch)	Single-layered both sides	55	727	364
	4 layers	40	1000	500

WARNING:

- *The recommended operating conditions are required to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.*
  Any use of semiconductor devices will be under their recommended operating condition.
  Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
  No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

Table 12-6. Typical and maximum current consumption in Sleep operation(PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK

Parameter	Symbol	Pin Name	Conditions	Frequency*5	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	SLEEP operation (PLL)	72 MHz	22	71	mA	*3 When all peripheral clocks are ON
				60 MHz	19	68		
				48 MHz	16	64		
				36 MHz	12	61		
				24 MHz	9.0	58		
				12 MHz	5.8	55		
				8 MHz	4.6	54		
				4 MHz	3.6	52		
				72 MHz	9.5	58	mA	*3 When all peripheral clocks are OFF
				60 MHz	8.3	57		
				48 MHz	7.1	56		
				36 MHz	5.8	55		
				24 MHz	4.6	53		
				12 MHz	3.5	52		
				8 MHz	3.0	52		
				4 MHz	2.7	51		

*1: Ta=+25 °C, V_{CC}=3.3 V

*2: Tj=+125 °C, V_{CC}=5.5 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK

Table 12-7. Typical and maximum current consumption in Sleep operation(other than PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	SLEEP operation (built-in high-speed CR)	4 MHz	1.5	49	mA	*3 When all peripheral clocks are ON
					1.0	49	mA	*3 When all peripheral clocks are OFF
			SLEEP operation (sub oscillation)	32 kHz	0.59	48	mA	*3 When all peripheral clocks are ON
					0.51	48	mA	*3 When all peripheral clocks are OFF
			SLEEP operation (built-in low-speed CR)	100 kHz	0.61	48	mA	*3 When all peripheral clocks are ON
					0.53	48	mA	*3 When all peripheral clocks are OFF

*1: Ta=+25 °C, V_{CC}=3.3 V

*2: Tj=+125 °C, V_{CC}=5.5 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

Separate Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
MOEX Mininum pulse width	t_{OEW}	MOEX	$V_{CC} \geq 4.5V$	MCLK×n-3	-	ns
			$V_{CC} < 4.5V$			
MCSX↓→Address output delay time	t_{CSL-AV}	MCSX[7:0], MAD[24:0]	$V_{CC} \geq 4.5V$	-9	+9	ns
			$V_{CC} < 4.5V$	-12	+12	
MOEX↑→Address hold time	t_{OEH-AX}	MOEX, MAD[24:0]	$V_{CC} \geq 4.5V$	0	MCLK×m+9	ns
			$V_{CC} < 4.5V$		MCLK×m+12	
MCSX↓→ MOEX↓ delay time	$t_{CSL-OEL}$	MOEX, MCSX[7:0]	$V_{CC} \geq 4.5V$	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5V$	MCLK×m-12	MCLK×m+12	
MOEX↑→ MCSX↑ time	$t_{OEH-CSH}$		$V_{CC} \geq 4.5V$	0	MCLK×m+9	ns
			$V_{CC} < 4.5V$		MCLK×m+12	
MCSX↓→MDQM↓ delay time	$t_{CSL-RDQML}$	MCSX, MDQM[1:0]	$V_{CC} \geq 4.5V$	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5V$	MCLK×m-12	MCLK×m+12	
Data set up→MOEX↑ time	t_{DS-OE}	MOEX, MADATA[15:0]	$V_{CC} \geq 4.5V$	20	-	ns
			$V_{CC} < 4.5V$	38	-	
MOEX↑→ Data hold time	t_{DH-OE}	MOEX, MADATA[15:0]	$V_{CC} \geq 4.5V$	0	-	ns
			$V_{CC} < 4.5V$			
MWEX Mininum pulse width	t_{WEW}	MWEX	$V_{CC} \geq 4.5V$	MCLK×n-3	-	ns
			$V_{CC} < 4.5V$			
MWEX↑→Address output delay time	t_{WEH-AX}	MWEX, MAD[24:0]	$V_{CC} \geq 4.5V$	0	MCLK×m+9	ns
			$V_{CC} < 4.5V$		MCLK×m+12	
MCSX↓→MWEX↓ delay time	$t_{CSL-WEL}$	MWEX, MCSX[7:0]	$V_{CC} \geq 4.5V$	MCLK×n-9	MCLK×n+9	ns
			$V_{CC} < 4.5V$	MCLK×n-12	MCLK×n+12	
MWEX↑→MCSX↑ delay time	$t_{WEH-CSH}$		$V_{CC} \geq 4.5V$	0	MCLK×m+9	ns
			$V_{CC} < 4.5V$		MCLK×m+12	
MCSX↓→MDQM↓ delay time	$t_{CSL-WDQML}$	MCSX, MDQM[1:0]	$V_{CC} \geq 4.5V$	MCLK×n-9	MCLK×n+9	ns
			$V_{CC} < 4.5V$	MCLK×n-12	MCLK×n+12	
MWEX↓→ Data output time	t_{CSL-DX}	MCSX, MADATA[15:0]	$V_{CC} \geq 4.5V$	MCLK-9	MCLK+9	ns
			$V_{CC} < 4.5V$	MCLK-12	MCLK+12	
MWEX↑→ Data hold time	t_{WEH-DX}	MWEX, MADATA[15:0]	$V_{CC} \geq 4.5V$	0	MCLK×m+9	ns
			$V_{CC} < 4.5V$		MCLK×m+12	

Note:

- *When the external load capacitance C_L = 30 pF (m=0 to 15, n=1 to 16)*

Synchronous Serial (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT→SCK↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*

When Using Synchronous Serial Chip Select (SCINV = 1, CSLVL=1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↑setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5tC_{YCP}	(*3)+50 +5t_{CYCP}	ns
SCS↓→SCK↑setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↓→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

High-speed Synchronous Serial (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Internal shift clock operation	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ →SOT delay time	t_{SLOVI}	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK ↑ →SIN hold time	t_{SHIXI}	SCKx, SINx		5	-	5	-	ns
SOT→SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ – 10	-	$2t_{CYCP}$ – 10	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ – 5	-	$2t_{CYCP}$ – 5	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ →SOT delay time	t_{SLOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		5	-	5	-	ns
SCK ↑ →SIN hold time	t_{SHIXE}	SCKx, SINx		5	-	5	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*

  No chip select: SIN4_1, SOT4_1, SCK4_1
  Chip select: SIN6_1, SOT6_1, SCK6_1, SCS6_1
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*

When Using High-speed Synchronous Serial Chip Select (SCINV = 1, CSLVL=0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↑setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↓→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↑→SCK↑setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↑→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

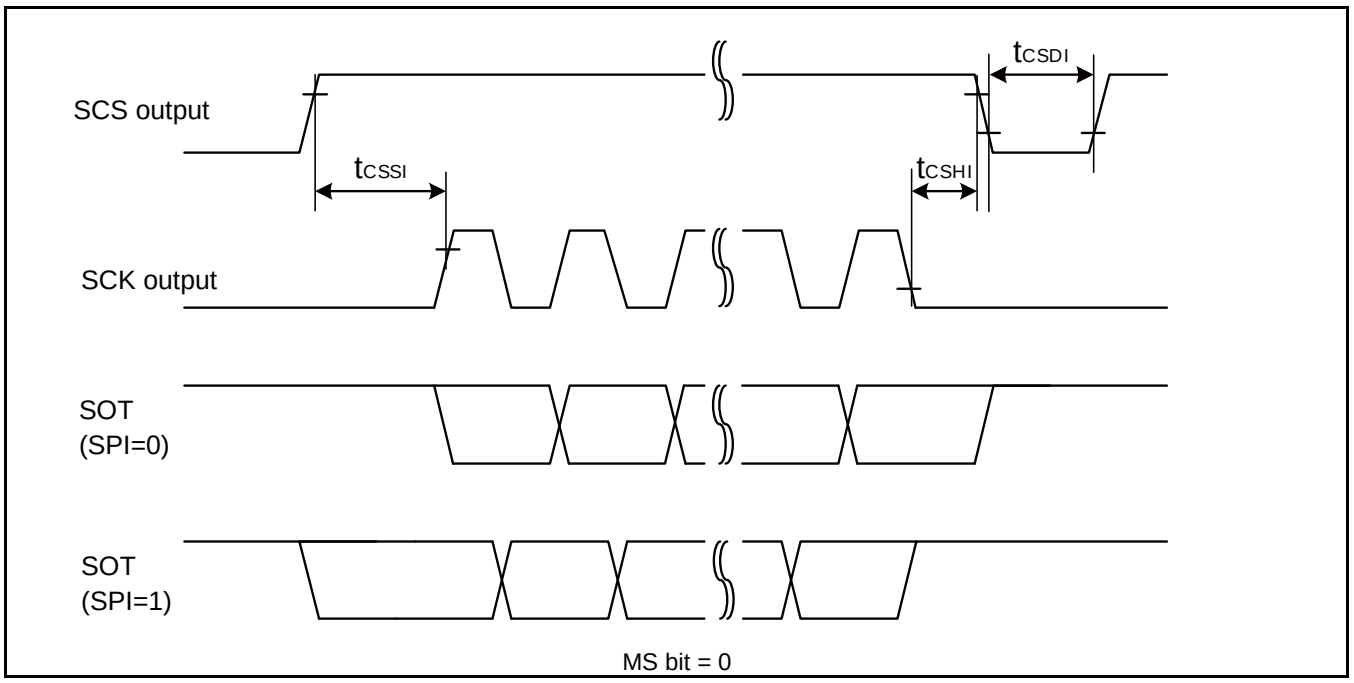
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

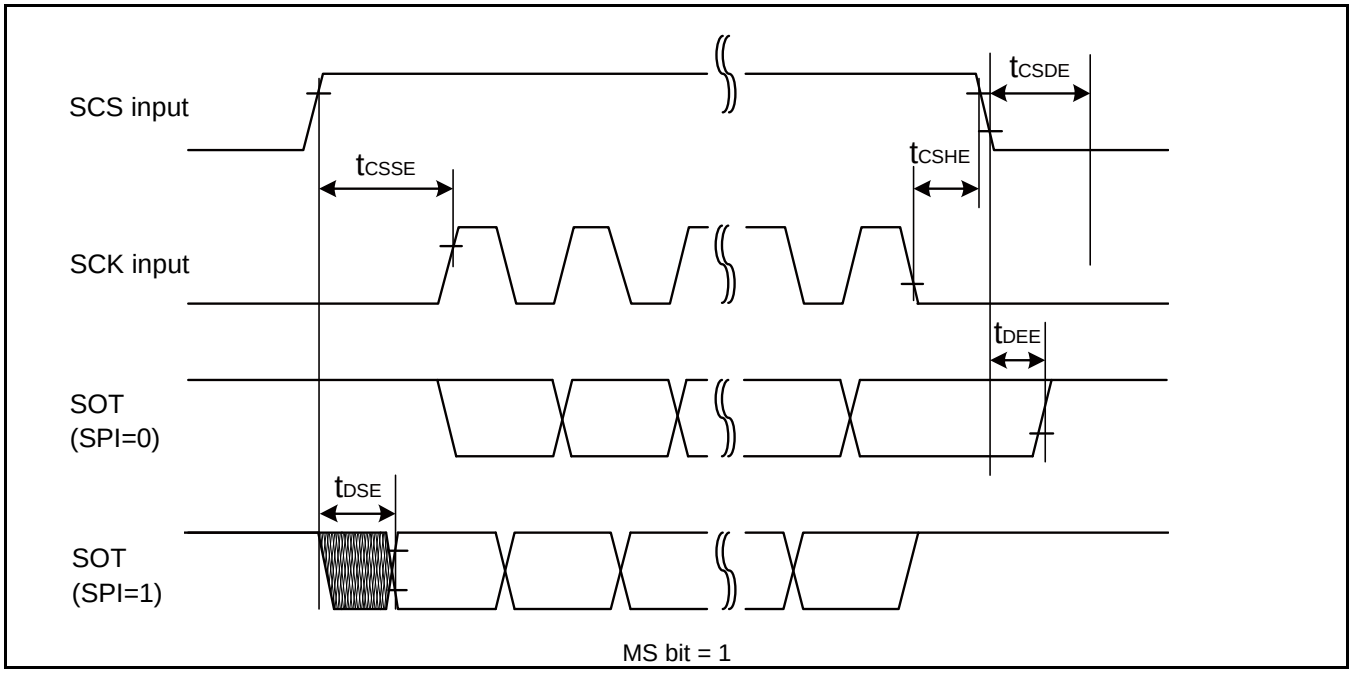
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

Fast-mode Plus (Fm+)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Fast-mode Plus (Fm+)*6		Unit	Remarks
			Min	Max		
SCL clock frequency	F_{SCL}	C_L = 30 pF, R = (V_p/I_{OL})*1	0	1000	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		0.26	-	µs	
SCL clock "L" width	t_{LOW}		0.5	-	µs	
SCL clock "H" width	t_{HIGH}		0.26	-	µs	
SCL clock frequency	t_{SUSTA}		0.26	-	µs	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDDAT}		0	0.45*2, *3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		50	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		0.26	-	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}		0.5	-	µs	
Noise filter	t_{SP}	60 MHz ≤ t_{CYCP}<80 MHz	6 t_{CYCP}*4	-	ns	*5
		80 MHz ≤ t_{CYCP}<100 MHz	8 t_{CYCP}*4	-	ns	
		100 MHz ≤ t_{CYCP}<120 MHz	10 t_{CYCP}*4	-	ns	
		120 MHz ≤ t_{CYCP}<140 MHz	12 t_{CYCP}*4	-	ns	
		140 MHz ≤ t_{CYCP}<160 MHz	14 t_{CYCP}*4	-	ns	
		160 MHz ≤ t_{CYCP}<180 MHz	16 t_{CYCP}*4	-	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} must satisfy that it does not extend at least L period (t_{LOW}) of device's SCL signal.

*3: A Fast-mode mode I^2C bus device can be used on a Standard-mode I^2C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CYCP} is the APB bus clock cycle time.
About the APB bus number that I^2C is connected to, see 8. Block Diagram in this data sheet.
To use Fast-mode Plus (Fm+), set the peripheral bus clock at 64 MHz or more.

*5: The noise filter time can be changed by register settings.
Change the number of the noise filter steps according to APB bus clock frequency.

*6: When using Fast-mode Plus (Fm+), set the I/O pin to the mode corresponding to I^2C Fm+ in the EPFR register. See CHAPTER 12: I/O Port in FM4 Family Peripheral Manual Main part (MN709-00001) for the details.

High-Speed Mode

■Clock CLK (All values are referred to V_{IH} and V_{IL})

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Clock frequency Data Transfer Mode	f_{PP}	S_CLK	C_{CARD} ≤ 10 pF (1 card)	0	32	MHz
Clock low time	t_{WL}	S_CLK		7	-	ns
Clock high time	t_{WH}	S_CLK		7	-	ns
Clock rising time	t_{TLH}	S_CLK		-	3	ns
Clock falling time	t_{THL}	S_CLK		-	3	ns

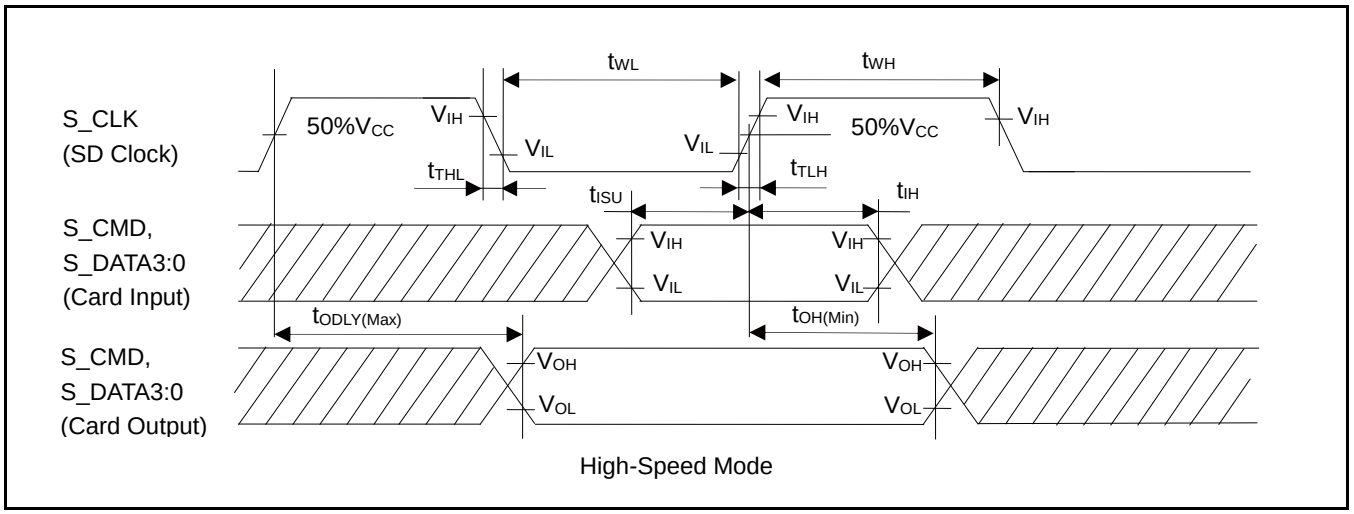
■Card Inputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Input set-up time	t_{ISU}	S_CMD, S_DATA3:0	C_{CARD} ≤ 10 pF (1 card)	8	-	ns
Input hold time	t_{IH}	S_CMD, S_DATA3:0		2	-	ns

■Card Outputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Output Delay time during Data Transfer Mode	t_{ODLY}	S_CMD, S_DATA3:0	C_L ≤ 40 pF (1 card)	-	22	ns
Output Hold time	t_{OH}	S_CMD, S_DATA3:0	C_L ≥ 15 pF (1 card)	2.5	-	ns
Total System capacitance for each line *	C_L	-	1 card	-	40	pF

*: In order to satisfy severe timing, host shall drive only one card.



High-Speed Mode

Notes:

- *The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.*
- *In high-speed mode, set the Clock frequency (f_{PP}) and the AHB Bus Clock frequency to the same values.*

12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	-4.5	-	+4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential Nonlinearity	-	-	-2.5	-	+2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	-15	-	+15	mV	
Full-scale transition voltage	V_{FST}	ANxx	AVRH - 15	-	AVRH + 15	mV	
Conversion time	-	-	0.5 *1	-	-	µs	AV_{CC} ≥ 4.5V
Sampling time *2	Ts	-	0.15	-	10	µs	AV_{CC} ≥ 4.5V
			0.3	-			AV_{CC} < 4.5V
Compare clock cycle *3	Tcck	-	25	-	1000	ns	AV_{CC} ≥ 4.5V
			50	-	1000		AV_{CC} < 4.5V
State transition time to operation permission	Tstt	-	-	-	1.0	µs	
Power supply current (analog + digital)	-	AVCC	-	0.69	0.92	mA	A/D 1 unit operation
			-	1.0	18	µA	When A/D stop
Reference power supply current (AVRH)	-	AVRH	-	1.1	1.97	mA	A/D 1unit operation AVRH=5.5 V
				0.3	6.3	µA	When A/D stop
Analog input capacity	C_{AIN}	-	-	-	12.05	pF	
Analog input resistance	R_{AIN}	-	-	-	1.2	kΩ	AV_{CC} ≥ 4.5 V
					1.8		AV_{CC} < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AV_{SS}	-	AVRH	V	
Reference voltage	-	AVRH	4.5	-	AV_{CC}	V	Tcck < 50 ns
			2.7	-	AV_{CC}		Tcck ≥ 50 ns

*1: The conversion time is the value of sampling time (Ts) + compare time (Tc).
The condition of the minimum conversion time is when the value of sampling time: 150 ns, the value of compare time: 350 ns (AV_{CC} ≥ 4.5 V). Ensure that it satisfies the value of sampling time (Ts) and compare clock cycle (Tcck). For setting*4 of sampling time and compare clock cycle, see CHAPTER 1-1: A/D Converter in FM4 Family Peripheral Manual Analog macro part (MN709-00001). The register setting of the A/D Converter is reflected by the peripheral clock timing. The sampling and compare clock are set at Base clock (HCLK).

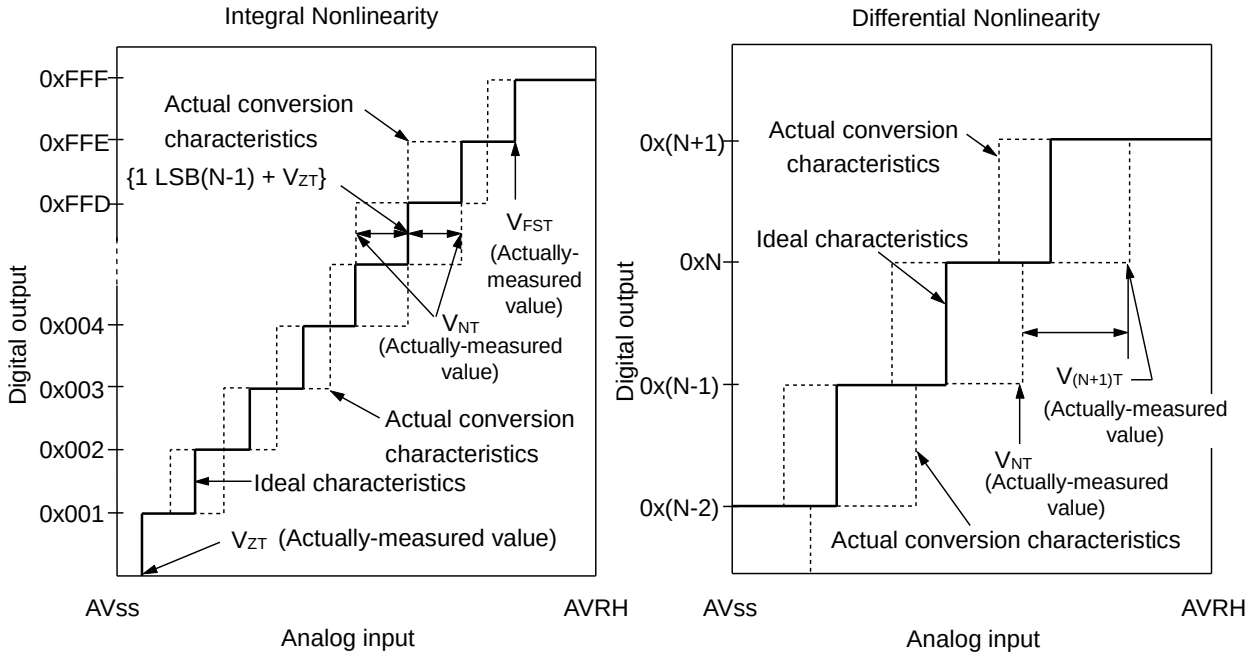
*2: A necessary sampling time changes by external impedance. Ensure that it set the sampling time to satisfy (Equation 1).

*3: The compare time (Tc) is the value of (Equation 2).

*4: The register setting of the A/D Converter is reflected by the timing of the APB bus clock. The sampling clock and compare clock are set in base clock (HCLK). About the APB bus number which the A/D Converter is connected to, see 8. Block Diagram in this data sheet.

Definition of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)}T - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.

V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.

V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.

V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

12.8 Low-Voltage Detection Characteristics

12.8.1 Low-Voltage Detection Reset

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.25	2.45	2.65	V	When voltage drops
Released voltage	VDH	-	2.30	2.50	2.70	V	When voltage rises

12.8.2 Interrupt of Low-Voltage Detection

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00111	2.58	2.8	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.9	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.76	3.0	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.1	3.34	V	When voltage rises
Detected voltage	VDL	SVHI = 01100	2.94	3.2	3.45	V	When voltage drops
Released voltage	VDH		3.04	3.3	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 01111	3.31	3.6	3.88	V	When voltage drops
Released voltage	VDH		3.40	3.7	3.99	V	When voltage rises
Detected voltage	VDL	SVHI = 01110	3.40	3.7	3.99	V	When voltage drops
Released voltage	VDH		3.50	3.8	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	3.68	4.0	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.1	4.42	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	3.77	4.1	4.42	V	When voltage drops
Released voltage	VDH		3.86	4.2	4.53	V	When voltage rises
Detected voltage	VDL	SVHI = 11000	3.86	4.2	4.53	V	When voltage drops
Released voltage	VDH		3.96	4.3	4.64	V	When voltage rises
LVD stabilization wait time	T_{LVDW}	-	-	-	$4480 \times t_{CYCP}$*	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.