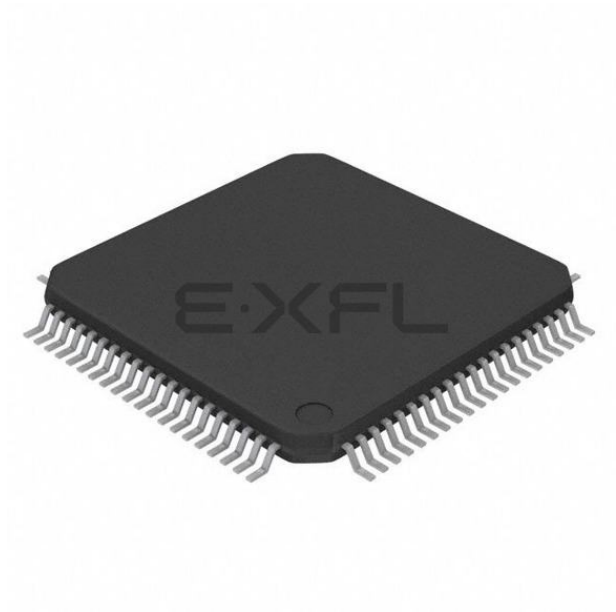

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SD, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	63
Program Memory Size	1.03125MB (1.03125M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9bf568mpmc-g-jne2

[USB host]

- USB2.0 Full/Low-speed supported
- Bulk-transfer, interrupt-transfer and Isochronous-transfer support
- USB Device connected/dis-connected automatically detect
- IN/OUT token handshake packet automatically
- Max 256-byte packet-length supported
- Wake-up function supported

CAN Interface (Max two channels)

- Compatible with CAN Specification 2.0A/B
- Maximum transfer rate: 1 Mbps
- Built-in 32 message buffer

Multi-function Serial Interface (Max eight channels)

- 64 bytes with FIFO (the FIFO step numbers are variable depending on the settings of the communication mode or bit length.)
- Operation mode is selectable from the followings for each channel.
  - UART
  - CSIO
  - LIN
  - I^2C
- UART
  - Full-duplex double buffer
  - Selection with or without parity supported
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Hardware Flow control : Automatically control the transmission by CTS/RTS (only ch.4)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- CSIO
  - Full-duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detect function available
  - Serial chip select function (ch.6 and ch.7 only)
  - Supports high-speed SPI (ch.4 and ch.6 only)
  - Data length 5 to 16-bit
- LIN
  - LIN protocol Rev.2.1 supported
  - Full-duplex double buffer
  - Master/Slave mode supported
  - LIN break field generation (can change to 13 to 16-bit length)
  - LIN break delimiter generation (can change to 1 to 4-bit length)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- I^2C
  - Standard-mode (Max 100 kbps) / Fast-mode (Max 400 kbps) supported
  - Fast-mode Plus (Fm+) (Max 1000 kbps, only for ch.3=ch.A and ch.7=ch.B) supported

DMA Controller (Eight channels)

DMA Controller has an independent bus for CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 Gbytes)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: bytes/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

DSTC (Descriptor System data Transfer Controller) (128 channels)

The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the Descriptor system and, following the specified contents of the Descriptor which has already been constructed on the memory, can access directly the memory /peripheral device and performs the data transfer operation.

It supports the software activation, the hardware activation and the chain activation functions.

A/D Converter (Max 24 channels) [12-bit A/D Converter]

- Successive Approximation type
- Built-in 3 units
- Conversion time: 0.5 µs @ 5 V
- Priority conversion available (priority at 2levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16steps, for Priority conversion: 4steps)

D/A Converter (Max two channels)

- R-2R type
- 12-bit resolution

4. Pin Description

4.1 List of Pin Numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
1	1	1	79	B1	B1	VCC	-	-
2	2	2	80	C1	C1	P50 CTS4_0 AIN0_2 RTO10_0 (PPG10_0) INT00_0 MADATA00_0	E	K
3	3	3	81	C2	C2	P51 RTS4_0 BIN0_2 RTO11_0 (PPG10_0) INT01_0 MADATA01_0	E	K
4	4	4	82	C3	D1	P52 SCK4_0 (SCL4_0) ZIN0_2 RTO12_0 (PPG12_0) MADATA02_0	E	I
5	5	5	83	D1	D2	P53 TIOA1_2 SOT4_0 (SDA4_0) RTO13_0 (PPG12_0) MADATA03_0	E	I
6	6	6	84	D2	D3	P54 TIOB1_2 SIN4_0 RTO14_0 (PPG14_0) INT02_0 MADATA04_0	E	K

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
7	7	7	85	E1	E1	P55 ADTG_1 SIN6_0 RTO15_0 (PPG14_0) INT07_2 MADATA05_0	E	K
8	8	8	86	E2	E2	P56 SOT6_0 (SDA6_0) DTTI1X_0 INT08_2 MADATA06_0	E	K
9	-	-	-	-	E3	P57 SCK6_0 (SCL6_0) MADATA07_0	E	I
10	-	-	-	-	E4	P58 SIN4_2 AIN1_0 INT04_2 MADATA08_0	E	K
11	-	-	-	-	F1	P59 RX1_1 SOT4_2 (SDA4_2) BIN1_0 INT07_1 MADATA09_0	E	K
12	-	-	-	-	F2	P5A TX1_1 SCK4_2 (SCL4_2) ZIN1_0 MADATA10_0	E	I
13	-	-	-	-	F3	P5B CTS4_2 MADATA11_0	E	I
14	9	9	87	E3	F4	P30 TIOB0_1 RTS4_2 INT15_2 WKUP1	E	Q
-					-	MADATA07_0		
14	-	-	-	-	F4	MADATA12_0		

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
104	89	70	67	C6	C7	P02 TDI MCSX6_0	E	H
105	90	71	68	A6	B7	P01 TCK SWCLK	E	G
106	91	72	69	B6	D6	P00 TRSTX MCSX7_0	E	H
107	92	-	70	A5	A7	VSS	-	-
108	-	-	-	-	C6	P68 TIOB7_2 SCK3_0 (SCL3_0) INT00_2	E	K
109	-	-	-	-	B6	P67 TIOA7_2 SOT3_0 (SDA3_0)	E	I
110	-	-	-	-	A6	P66 ADTG_8 SIN3_0 INT11_2	E	K
111	-	-	-	-	D5	P65 TIOB7_0 SCK5_1 (SCL5_1)	E	I
112	-	-	-	-	C5	P64 TIOA7_0 SOT5_1 (SDA5_1) INT10_2	E	K
113	93	73	71	C5	B5	P63 CROUT_1 RX0_2	E	K
	-	-	-	-		SIN5_1		
	93	73	71	C5		INT03_0 S_CD_0 MWEX_0		
114	94	74	72	B5	C4	P62 ADTG_3 TX0_2 SIN5_0 INT04_1 S_WP_0 MOEX_0	I	K

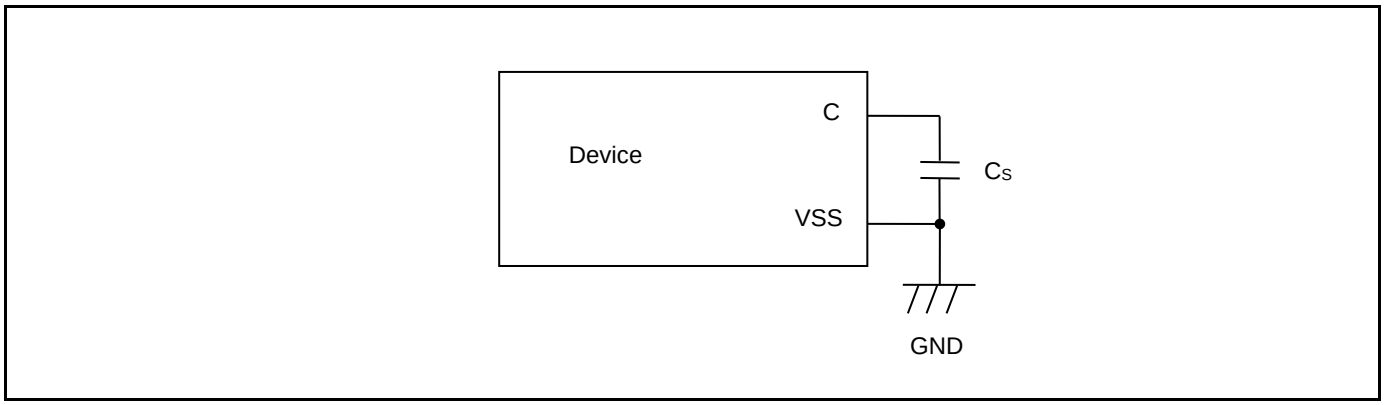
Pin Function	Pin Name	Function Description	Pin No					
			LQFP 120	LQFP 100	LQFP 80	QFP 100	BGA 112	BGA 144
External Bus	MSDCLK_0	SDRAM interface SDRAM clock output pin	23	18	-	96	J1	J1
	MSDCKE_0	SDRAM interface SDRAM clock enable pin	24	19	-	97	J2	J2
	MRASX_0	SDRAM interface SDRAM row address strobe pin	25	20	-	98	J3	J3
	MCASX_0	SDRAM interface SDRAM column address strobe pin	26	21	-	99	K1	J4
	MSDWEX_0	SDRAM interface SDRAM write enable pin	34	29	-	7	M3	N3
External Interrupt	INT00_0	External interrupt request 00 input pin	2	2	2	80	C1	C1
	INT00_1		95	80	65	58	A10	B10
	INT00_2		108	-	-	-	-	C6
	INT01_0	External interrupt request 01 input pin	3	3	3	81	C2	C2
	INT01_1		101	86	-	64	C8	C8
	INT01_2		85	-	-	-	-	E10
	INT02_0	External interrupt request 02 input pin	6	6	6	84	D2	D3
	INT02_1		62	52	41	30	L13	L12
	INT02_2		82	-	-	-	-	E13
	INT03_0	External interrupt request 03 input pin	113	93	73	71	C5	B5
	INT03_1		65	55	44	33	K12	J12
	INT03_2		54	-	-	-	-	M10
	INT04_0	External interrupt request 04 input pin	17	12	12	90	F3	G3
	INT04_1		114	94	74	72	B5	C4
	INT04_2		10	-	-	-	-	E4
	INT05_0	External interrupt request 05 input pin	89	74	-	52	C12	C12
	INT05_1		75	65	54	43	G12	G12
	INT05_2		21	16	-	94	H2	H3
	INT06_1	External interrupt request 06 input pin	88	73	59	51	C13	D11
	INT06_2		22	17	-	95	H3	H4
	INT07_1	External interrupt request 07 input pin	11	-	-	-	-	F1
	INT07_2		7	7	7	85	E1	E1
	INT08_1	External interrupt request 08 input pin	19	14	-	92	G2	H1
	INT08_2		8	8	8	86	E2	E2
	INT09_1	External interrupt request 09 input pin	20	15	-	93	G3	H2
	INT09_2		15	10	10	88	F1	G1
	INT10_1	External interrupt request 10 input pin	16	11	11	89	F2	G2
	INT10_2		112	-	-	-	-	C5
	INT11_1	External interrupt request 11 input pin	50	45	35	23	L9	L8
	INT11_2		110	-	-	-	-	A6
	INT12_1	External interrupt request 12 input pin	32	27	-	5	N2	N2
	INT12_2		96	81	66	59	A9	D9
	INT13_1	External interrupt request 13 input pin	33	28	-	6	N3	L2
	INT13_2		49	44	34	22	M9	M8
	INT14_1	External interrupt request 14 input pin	68	58	47	36	J11	H12
	INT14_2		53	-	-	-	-	K9
	INT15_1	External interrupt request 15 input pin	52	-	-	-	-	L9
	INT15_2		14	9	9	87	E3	F4

Handling when Using Multi-function Serial Pin as I²C Pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled.
However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
A smoothing capacitor of about 4.7 µF would be recommended for this series.



Mode Pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

Notes on Power-on

Turn power on/off in the following order or at the same time. The device operates normally after all power on.

VBAT only Power-on is possible when VBAT and VCC turns Power-on and Hibernation control is setting and then VCC turns Power-off. About Hibernation control, see Chapter 7-2: VBAT Domain(A) in FM4 Family Peripheral Manual Main Part(002-04856).
If not using the A/D converter and D/A converter, connect AVCC = VCC and AVSS = VSS.

Turning on:	VBAT → VCC → USBVCC
	VCC → AVCC → AVRH
Turning off:	AVRH → AVCC → VCC
	USBVCC → VCC → VBAT

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.

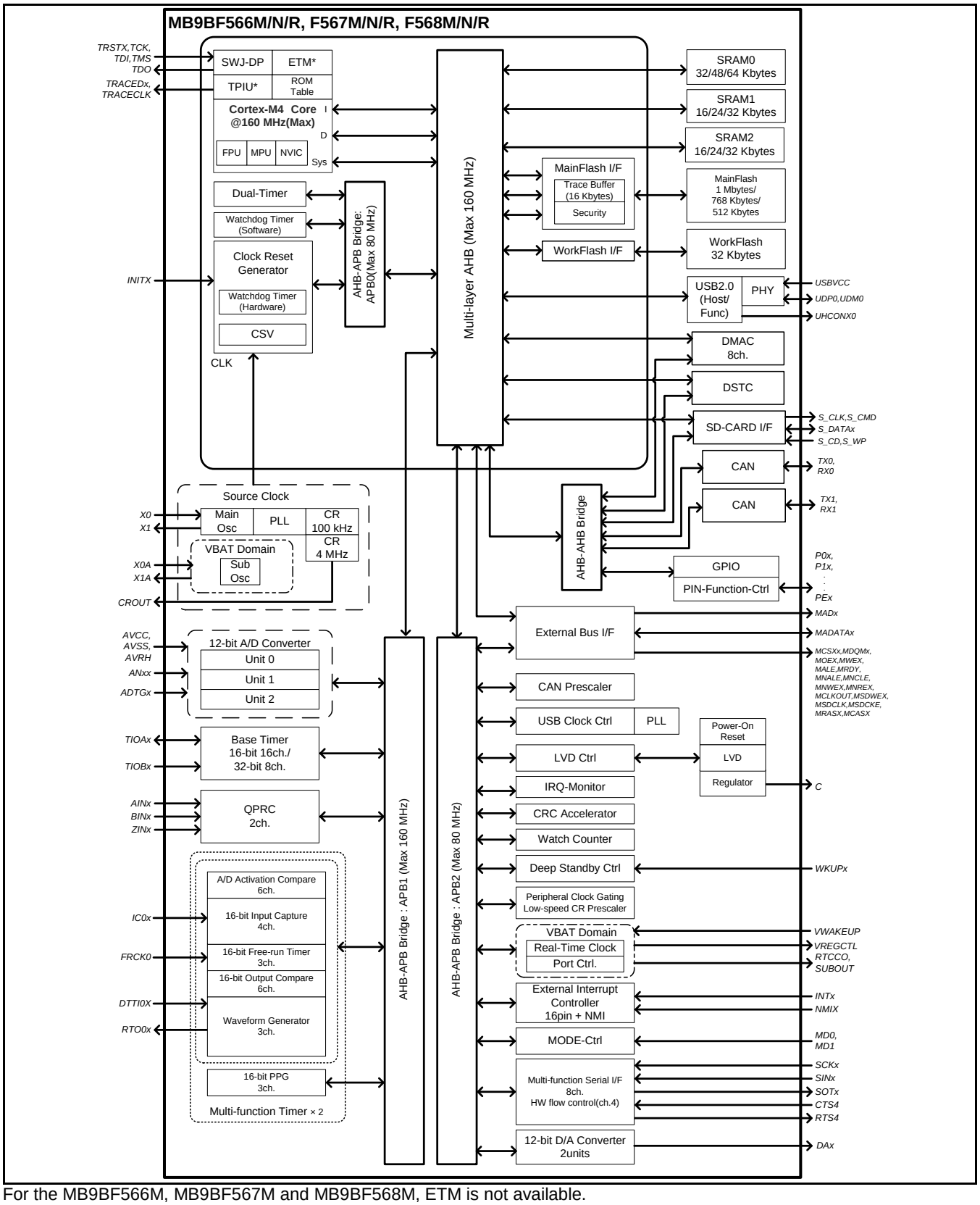
Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

Differences in Features among the Products with Different Memory Sizes and between Flash Products and MASK Products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

8. Block Diagram



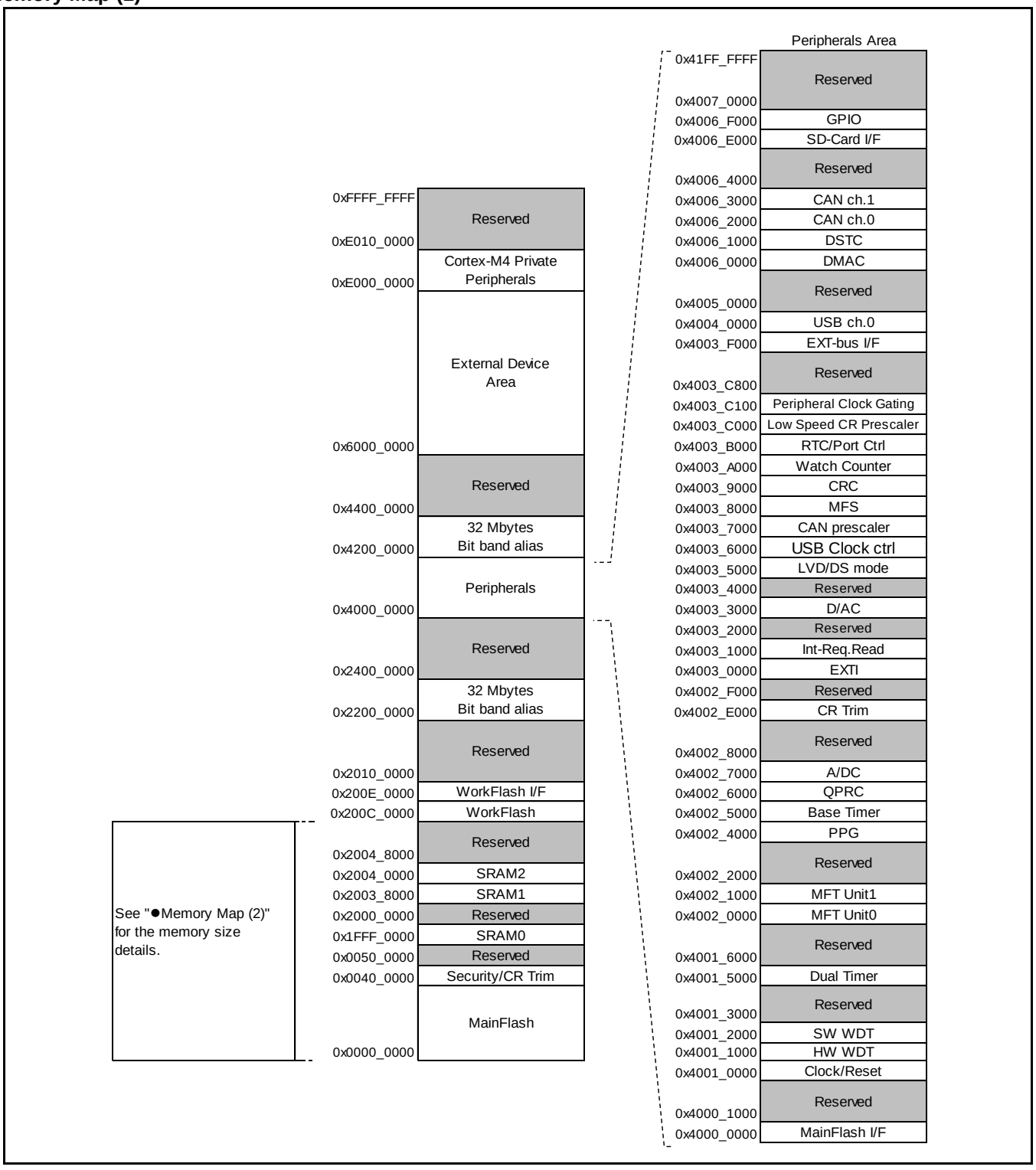
*: For the MB9BF566M, MB9BF567M and MB9BF568M, ETM is not available.

9. Memory Size

See Memory size in 1. Product Lineup to confirm the memory size.

10. Memory Map

Memory Map (1)



11. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

■INITX=0
This is the period when the INITX pin is the L level.

■INITX=1
This is the period when the INITX pin is the H level.

■SPL=0
This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 0.

■SPL=1
This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 1.

■Input enabled
Indicates that the input function can be used.

■Internal input fixed at 0
This is the status that the input function cannot be used. Internal input is fixed at L.

■Hi-Z
Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

■Setting disabled
Indicates that the setting is disabled.

■Maintain previous state
Maintains the state that was immediately prior to entering the current mode.
If a built-in peripheral function is operating, the output follows the peripheral function.
If the pin is being used as a port, that output is maintained.

■Analog input is enabled
Indicates that the analog input is enabled.

■Trace output
Indicates that the trace function can be used.

■GPIO selected
In Deep standby mode, pins switch to the general-purpose I/O port.

■Setting prohibition
Prohibition of a setting by specification limitation.

Package thermal resistance and maximum permissible power for each package are shown below.
The operation is guaranteed maximum permissible power or less for semiconductor devices.

Table for Package Thermal Resistance and Maximum Permissible Power

Package	Printed Circuit Board	Thermal Resistance θja (°C/W)	Maximum Permissible Power (mW)	
			Ta=+85 °C	Ta=+105 °C
LQH080 (0.5 mm pitch)	Single-layered both sides	60	667	333
	4 layers	39	1026	513
LQJ080 (0.65 mm pitch)	Single-layered both sides	58	690	335
	4 layers	38	1053	526
LQI100 (0.5 mm pitch)	Single-layered both sides	57	702	351
	4 layers	38	1053	526
PQH100 (0.65 mm pitch)	Single-layered both sides	48	833	417
	4 layers	34	1177	588
LQM120 (0.5 mm pitch)	Single-layered both sides	62	645	323
	4 layers	43	930	465
LDC112 (0.5 mm pitch)	Single-layered both sides	60	667	333
	4 layers	40	1000	500
LDC144 (0.5 mm pitch)	Single-layered both sides	55	727	364
	4 layers	40	1000	500

WARNING:

- *The recommended operating conditions are required to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.*
  Any use of semiconductor devices will be under their recommended operating condition.
  Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
  No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

*1: Ta=+25 °C, V_{CC}=3.3 V

*2: Tj=+125 °C, V_{CC}=5.5 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: When operating flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 1)

*6: Data access is nothing to MainFlash memory

*7: Frequency is a value of HCLK. PCLK0=PCLK2=HCLK/2, PCLK1=HCLK

*8: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 0)

Table 12-3. Typical and maximum current consumption in Normal operation(PLL), code with data accessing running from Flash memory (flash 0 wait-cycle mode and read access 0 wait)

Parameter	Symbol	Pin Name	Conditions		Frequency*4 (MHz)	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation (PLL)	*5	72 MHz	46	98	mA	*3 When all peripheral clocks are ON
					60 MHz	40	92		
					48 MHz	33	85		
					36 MHz	27	78		
					24 MHz	19	70		
					12 MHz	11	61		
					8 MHz	8.5	58		
					4 MHz	5.5	55		
					72 MHz	33	85	mA	*3 When all peripheral clocks are OFF
					60 MHz	29	81		
					48 MHz	25	76		
					36 MHz	20	71		
					24 MHz	15	65		
					12 MHz	9.2	59		
					8 MHz	6.9	56		
					4 MHz	4.6	54		

*1: Ta=+25 °C, V_{CC}=3.3 V

*2: Tj=+125 °C, V_{CC}=5.5 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK

*5: When 0 wait-cycle mode (FRWTR.RWT = 00, FSYNDN.SD = 00)

Table 12-6. Typical and maximum current consumption in Sleep operation(PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK

Parameter	Symbol	Pin Name	Conditions	Frequency*5	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	SLEEP operation (PLL)	72 MHz	22	71	mA	*3 When all peripheral clocks are ON
				60 MHz	19	68		
				48 MHz	16	64		
				36 MHz	12	61		
				24 MHz	9.0	58		
				12 MHz	5.8	55		
				8 MHz	4.6	54		
				4 MHz	3.6	52		
				72 MHz	9.5	58	mA	*3 When all peripheral clocks are OFF
				60 MHz	8.3	57		
				48 MHz	7.1	56		
				36 MHz	5.8	55		
				24 MHz	4.6	53		
				12 MHz	3.5	52		
				8 MHz	3.0	52		
				4 MHz	2.7	51		

*1: Ta=+25 °C, V_{CC}=3.3 V

*2: Tj=+125 °C, V_{CC}=5.5 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK

Table 12-7. Typical and maximum current consumption in Sleep operation(other than PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	SLEEP operation (built-in high-speed CR)	4 MHz	1.5	49	mA	*3 When all peripheral clocks are ON
					1.0	49	mA	*3 When all peripheral clocks are OFF
			SLEEP operation (sub oscillation)	32 kHz	0.59	48	mA	*3 When all peripheral clocks are ON
					0.51	48	mA	*3 When all peripheral clocks are OFF
			SLEEP operation (built-in low-speed CR)	100 kHz	0.61	48	mA	*3 When all peripheral clocks are ON
					0.53	48	mA	*3 When all peripheral clocks are OFF

*1: Ta=+25 °C, V_{CC}=3.3 V

*2: Tj=+125 °C, V_{CC}=5.5 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

12.3.2 Pin Characteristics

(V_{CC} = $USBV_{CC}$ = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	-	V_{CC}×0.8	-	V_{CC} + 0.3	V	
		5V tolerant input pin	-	V_{CC}×0.8	-	V_{SS} + 5.5	V	
		Input pin doubled as I^2C Fm+	-	V_{CC}×0.7	-	V_{SS} + 5.5	V	
"L" level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		5V tolerant input pin	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		Input pin doubled as I^2C Fm+	-	V_{SS}	-	V_{CC}×0.3	V	
"H" level output voltage	V_{OH}	4mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 4 mA V_{CC} < 4.5 V, I_{OH} = - 2 mA	V_{CC} - 0.5	-	V_{CC}	V	
		8mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 8 mA V_{CC} < 4.5 V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
		12mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 12 mA V_{CC} < 4.5 V, I_{OH} = - 8 mA	V_{CC} - 0.5	-	V_{CC}	V	
		The pin doubled as USB I/O	$USBV_{CC}$ ≥ 4.5 V, I_{OH} = - 20.5 mA $USBV_{CC}$ < 4.5 V, I_{OH} = - 13.0 mA	$USBV_{CC}$ - 0.4	-	$USBV_{CC}$	V	
		The pin doubled as I^2C Fm+	V_{CC} ≥ 4.5 V, I_{OH} = - 4 mA V_{CC} < 4.5 V, I_{OH} = - 3 mA	V_{CC} - 0.5	-	V_{CC}	V	At GPIO

Synchronous Serial (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*

When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL=0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓setup time	tC_{SSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↑→SCK↓setup time	tC_{SSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

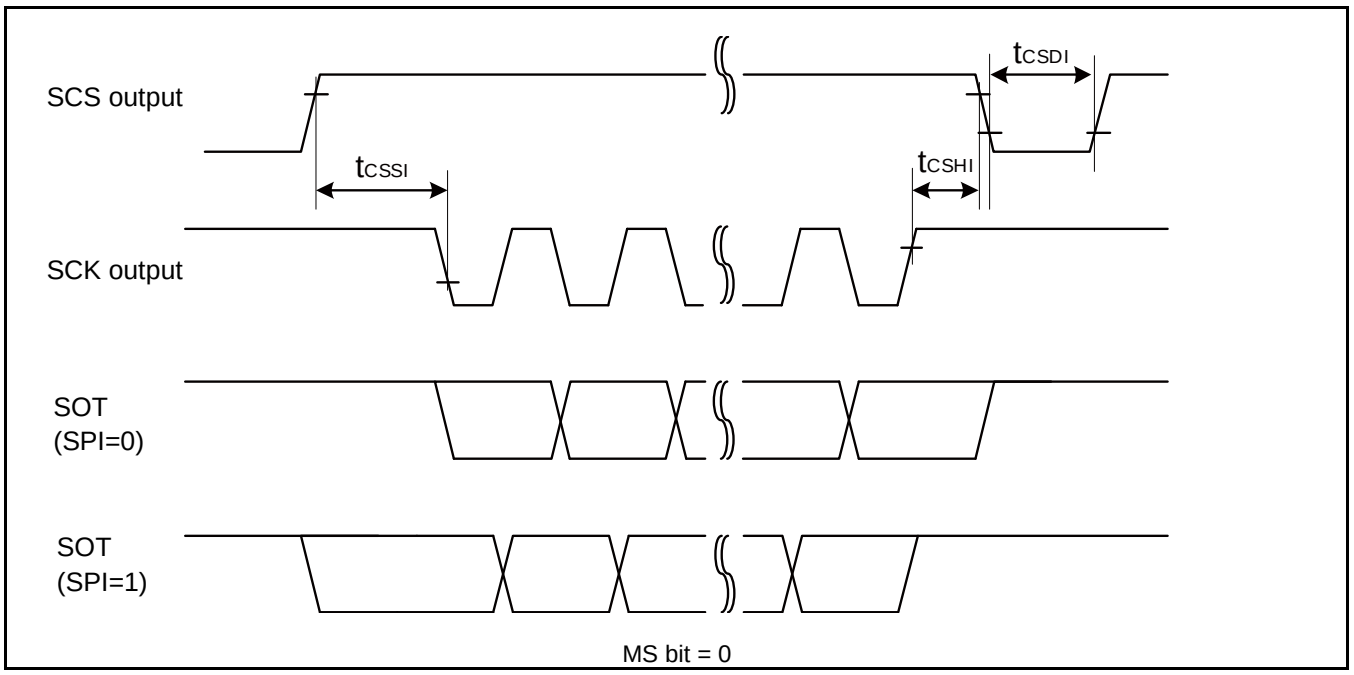
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

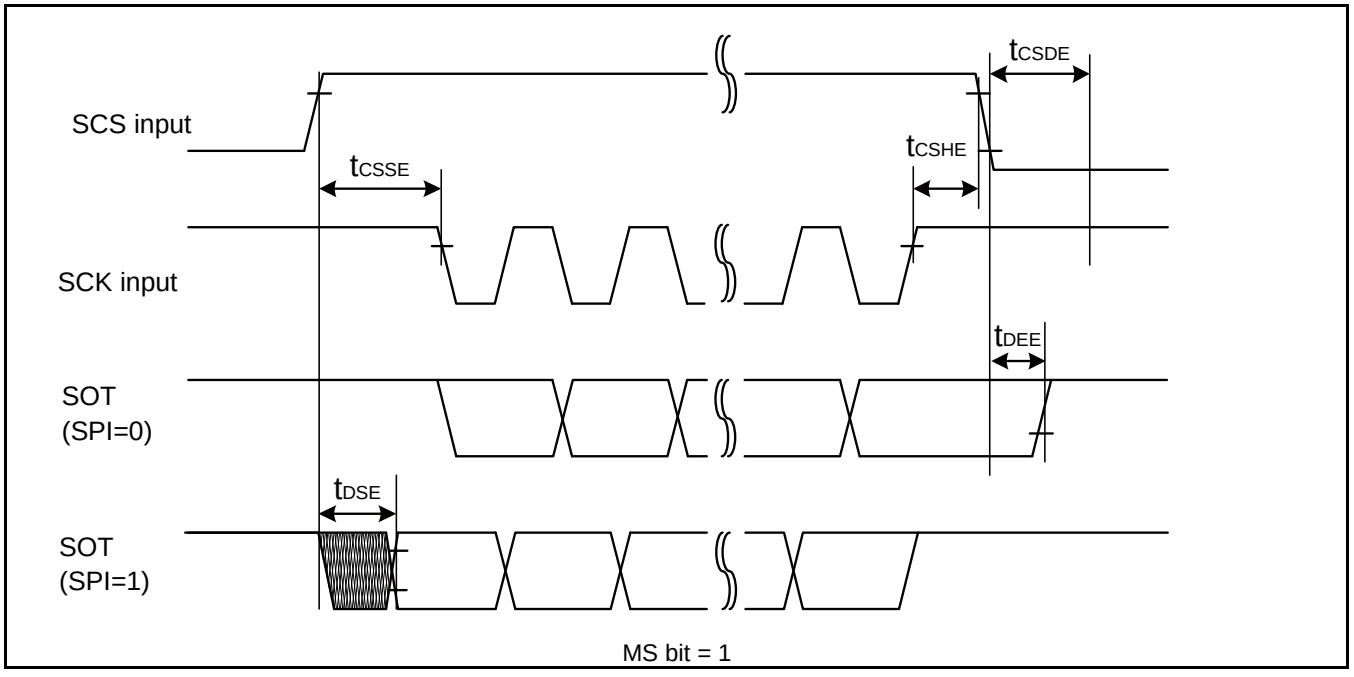
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

When Using High-speed Synchronous Serial Chip Select (SCINV = 0, CSLVL=0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↑→SCK↓setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↑→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

High-Speed Mode

■Clock CLK (All values are referred to V_{IH} and V_{IL})

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Clock frequency Data Transfer Mode	f_{PP}	S_CLK	C_{CARD} ≤ 10 pF (1 card)	0	32	MHz
Clock low time	t_{WL}	S_CLK		7	-	ns
Clock high time	t_{WH}	S_CLK		7	-	ns
Clock rising time	t_{TLH}	S_CLK		-	3	ns
Clock falling time	t_{THL}	S_CLK		-	3	ns

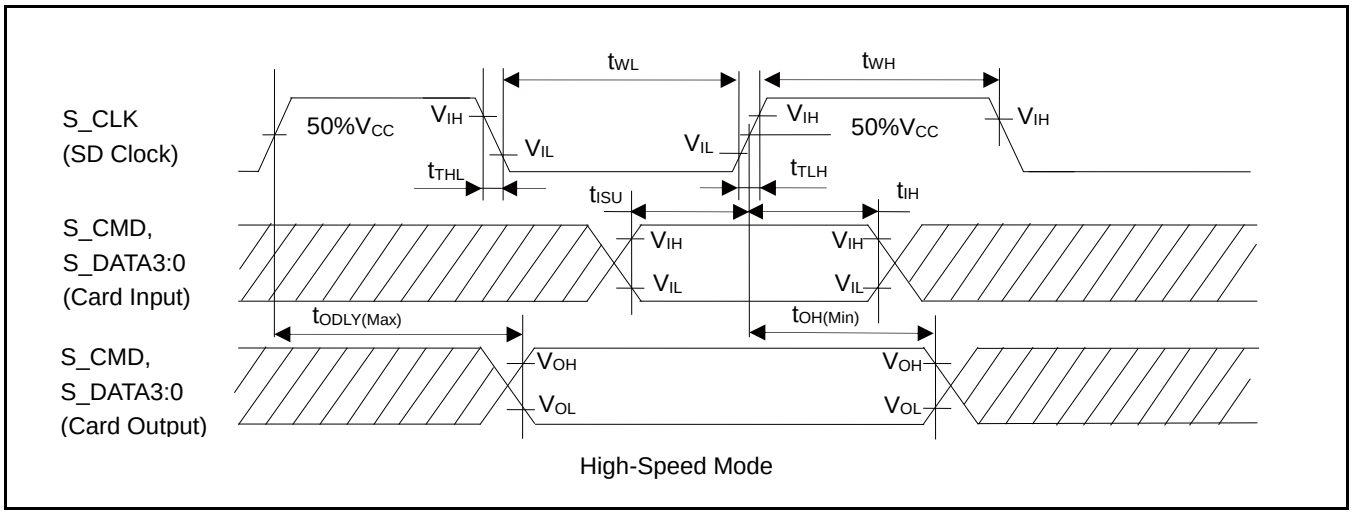
■Card Inputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Input set-up time	t_{ISU}	S_CMD, S_DATA3:0	C_{CARD} ≤ 10 pF (1 card)	8	-	ns
Input hold time	t_{IH}	S_CMD, S_DATA3:0		2	-	ns

■Card Outputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Output Delay time during Data Transfer Mode	t_{ODLY}	S_CMD, S_DATA3:0	C_L ≤ 40 pF (1 card)	-	22	ns
Output Hold time	t_{OH}	S_CMD, S_DATA3:0	C_L ≥ 15 pF (1 card)	2.5	-	ns
Total System capacitance for each line *	C_L	-	1 card	-	40	pF

*: In order to satisfy severe timing, host shall drive only one card.



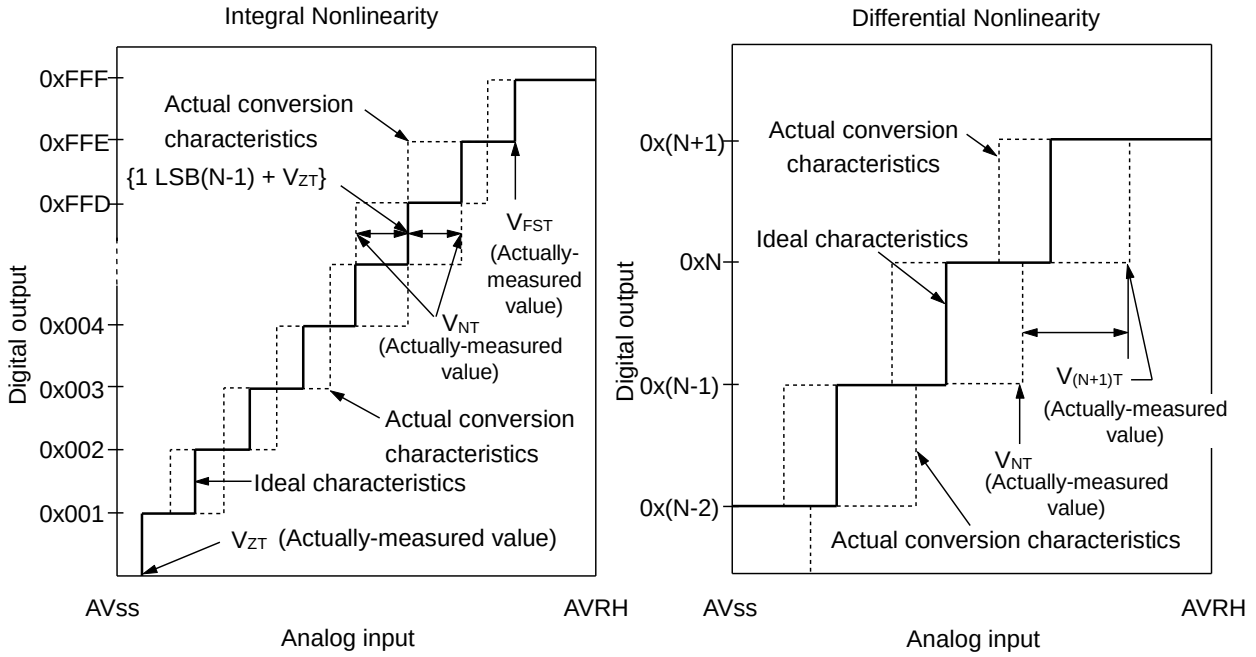
High-Speed Mode

Notes:

- *The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.*
- *In high-speed mode, set the Clock frequency (f_{PP}) and the AHB Bus Clock frequency to the same values.*

Definition of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)}T - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.

V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.

V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.

V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

12.9 MainFlash Memory Write/Erase Characteristics

(V_{CC} = 2.7V to 5.5V)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large Sector	-	0.7	3.7	s	Includes write time prior to internal erase
	Small Sector		0.3	1.1		
Half word (16-bit) write time	Write cycles < 100 times	-	12	100	µs	Not including system-level overhead time
	Write cycles > 100 times			200		
Chip erase time		-	13.6	68	s	Includes write time prior to internal erase

Write cycles and data hold time

Erase/Write cycles (cycle)	Data hold time (year)
1,000	20 *
10,000	10 *
100,000	5 *

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at +85°C) .

12.10 WorkFlash Memory Write/Erase Characteristics

(V_{CC} = 2.7V to 5.5V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.3	1.5	s	Includes write time prior to internal erase
Half word (16-bit) write time	-	20	200	µs	Not including system-level overhead time
Chip erase time	-	1.2	6	s	Includes write time prior to internal erase

Write cycles and data hold time

Erase/Write cycles (cycle)	Data hold time (year)
1,000	20 *
10,000	10 *
100,000	5 *

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at +85°C) .