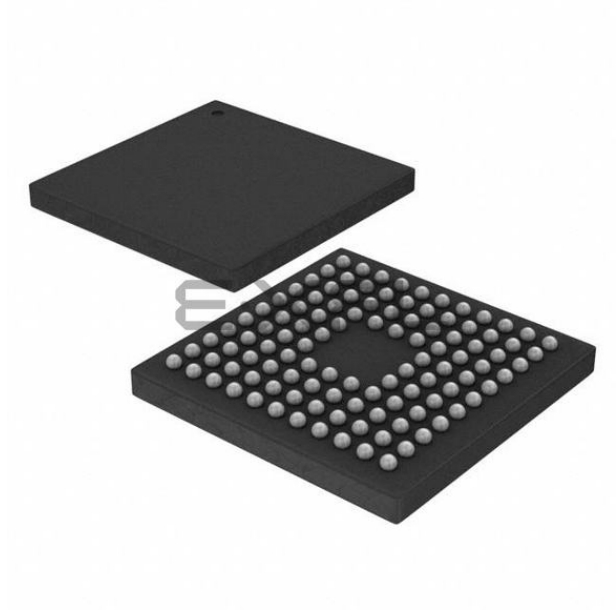

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SD, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1.03125MB (1.03125M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-FBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9bf568nbgl-ge1

CRC (Cyclic Redundancy Check) Accelerator
The CRC accelerator helps a verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

SD Card Interface
It is possible to use the SD card that conforms to the following standards.

- Part 1 Physical Layer Specification version 3.01
- Part E1 SDIO Specification version 3.00
- Part A2 SD Host Controller Standard Specification version 3.00
- 1-bit or 4-bit data bus

Clock and Reset

- Clocks

Five clock sources (2 external oscillators, 2 internal CR oscillator, and Main PLL) that are dynamically selectable.

  - Main clock: 4 MHz to 48 MHz
  - Sub Clock: 32.768 kHz
  - High-speed internal CR Clock: 4 MHz
  - Low-speed internal CR Clock: 100 kHz
  - Main PLL Clock

- Resets
  - Reset requests from INITX pin
  - Power on reset
  - Software reset
  - Watchdog timers reset
  - Low voltage detector reset
  - Clock supervisor reset

Clock Super Visor (CSV)
Clocks generated by internal CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)
This Series include 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-power Consumption Mode
Six low-power consumption modes are supported.

- SLEEP
- TIMER
- RTC
- STOP
- Deep standby RTC (selectable from with/without RAM retention)
- Deep standby stop (selectable from with/without RAM retention)

VBAT
The consumption power during the RTC operation can be reduced by supplying the power supply independent from the RTC (calendar circuit)/32 kHz oscillation circuit. The following circuits can also be used.

- RTC
- 32 kHz oscillation circuit
- Power-on circuit
- Back up register: 32 bytes
- Port circuit

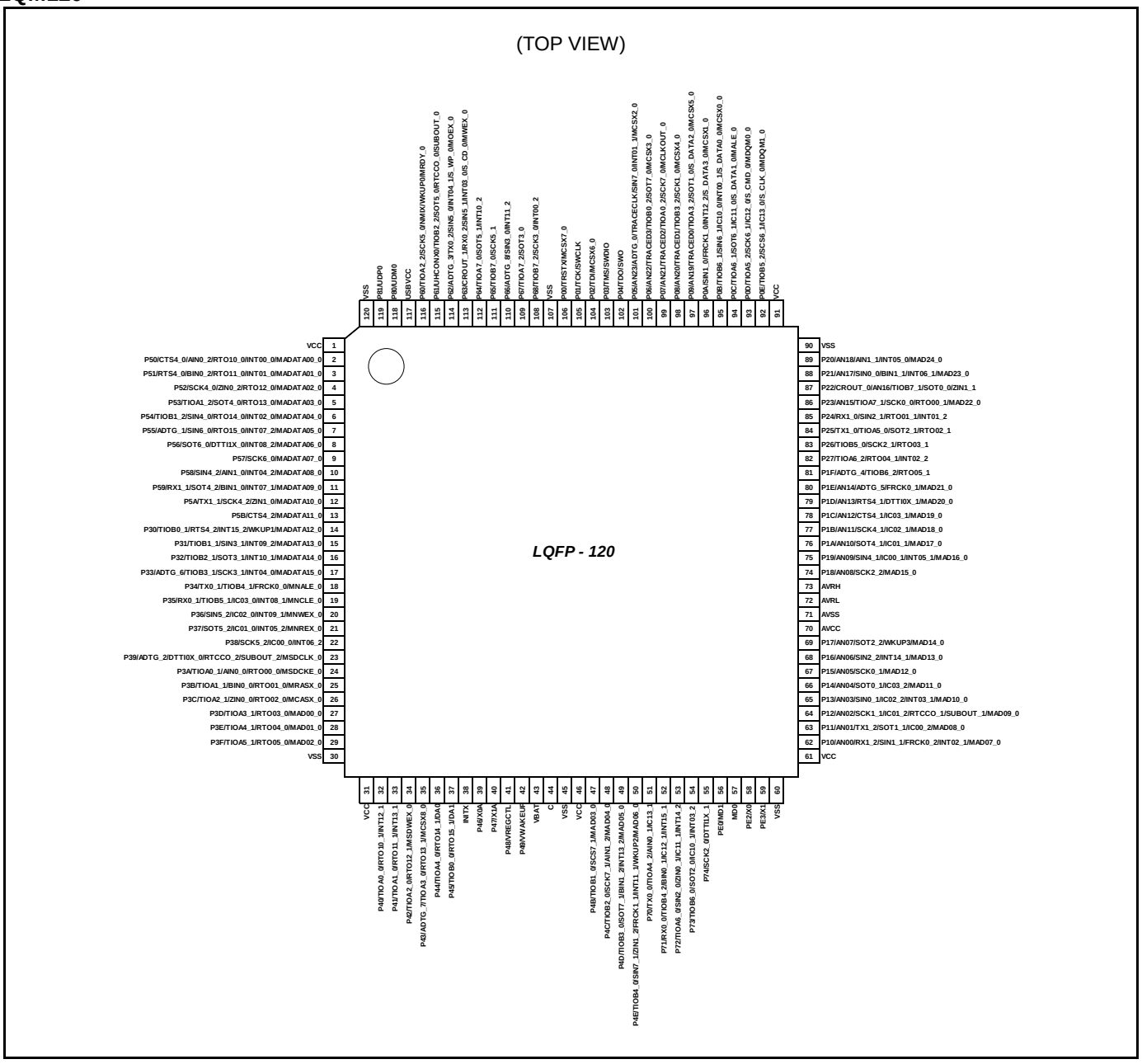
Debug
- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocells (ETM) provide comprehensive debug and trace facilities.

Unique ID
Unique value of the device (41-bit) is set.

Power Supply
Three Power Supplies

- Wide range voltage:
  VCC = 2.7 V to 5.5 V
- Power supply for USB I/O:
  USBVCC = 3.0 V to 3.6 V (when USB is used)
  = 2.7 V to 5.5 V (when GPIO is used)
- Power supply for VBAT:
  VBAT = 2.7 V to 5.5 V

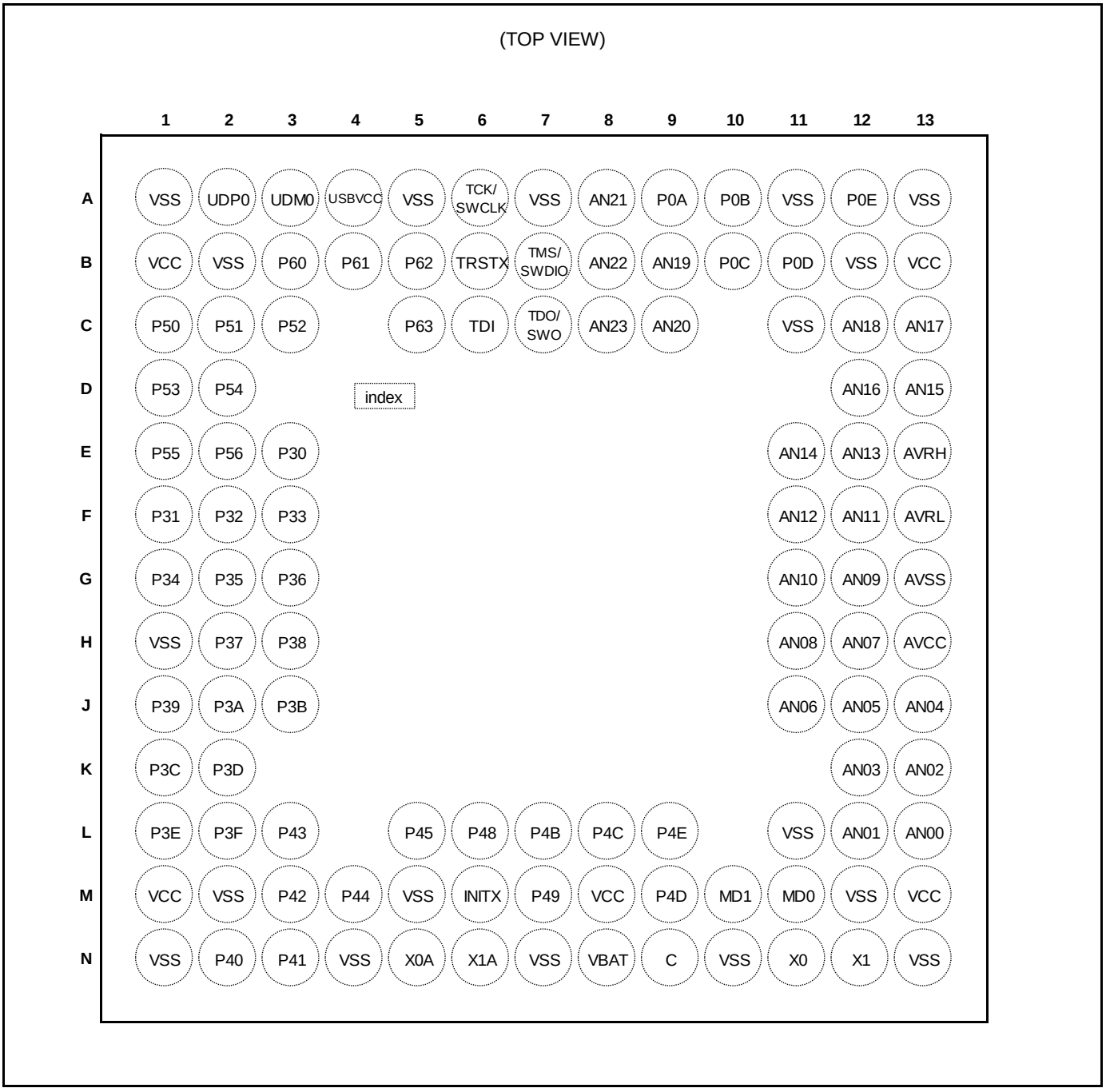
LQM120



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

LDC112



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
115	95	75	73	B4	B4	P61 UHCONX0 TIOB2_2 SOT5_0 (SDA5_0) RTCCO_0 SUBOUT_0	E	I
116	96	76	74	B3	B3	P60 TIOA2_2 SCK5_0 (SCL5_0) NMIX WKUP0 MRDY_0	I	F
117	97	77	75	A4	A4	USBVCC	-	-
118	98	78	76	A3	A3	P80 UDM0	H	R
119	99	79	77	A2	A2	P81 UDP0	H	R
120	100	80	78	A1	A1	VSS	-	-
-	-	-	-	A7	A5		-	-
-	-	-	-	B2	A8		-	-
-	-	-	-	B12	A10		-	-
-	-	-	-	C11	B2		-	-
-	-	-	-	H1	B11		-	-
-	-	-	-	N4	B12		-	-
-	-	-	-	M5	C3		-	-
-	-	-	-	N7	C11		-	-
-	-	-	-	L11	C13		-	-
-	-	-	-	A11	D4		-	-
-	-	-	-	M12	D10		-	-
-	-	-	-	M2	K1		-	-
-	-	-	-	-	K4	VSS	-	-
-	-	-	-	-	K10		-	-
-	-	-	-	-	L3		-	-
-	-	-	-	-	L5		-	-
-	-	-	-	-	L11		-	-
-	-	-	-	-	L13		-	-
-	-	-	-	-	M2		-	-
-	-	-	-	-	M4		-	-
-	-	-	-	-	M6		-	-
-	-	-	-	-	M7		-	-
-	-	-	-	-	M12		-	-
-	-	-	-	-	N6		-	-

Pin Function	Pin Name	Function Description	Pin No					
			LQFP 120	LQFP 100	LQFP 80	QFP 100	BGA 112	BGA 144
GPIO	P60	General-purpose I/O port 6	116	96	76	74	B3	B3
	P61		115	95	75	73	B4	B4
	P62		114	94	74	72	B5	C4
	P63		113	93	73	71	C5	B5
	P64		112	-	-	-	-	C5
	P65		111	-	-	-	-	D5
	P66		110	-	-	-	-	A6
	P67		109	-	-	-	-	B6
	P68		108	-	-	-	-	C6
	P70	General-purpose I/O port 7	51	-	-	-	-	K8
	P71		52	-	-	-	-	L9
	P72		53	-	-	-	-	K9
	P73		54	-	-	-	-	M10
	P74		55	-	-	-	-	L10
	P80	General-purpose I/O port 8	118	98	78	76	A3	A3
	P81		119	99	79	77	A2	A2
	PE0	General-purpose I/O port E	56	46	36	24	M10	N10
	PE2		58	48	38	26	N11	N11
	PE3		59	49	39	27	N12	N12
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	88	73	59	51	C13	D11
	SIN0_1		65	55	44	33	K12	J12
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I^2C (operation mode 4).	87	72	58	50	D12	D12
	SOT0_1 (SDA0_1)		66	56	45	34	J13	J11
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SCL0 when it is used in an I^2C (operation mode 4).	86	71	57	49	D13	D13
	SCK0_1 (SCL0_1)		67	57	46	35	J12	J10
Multi-function Serial 1	SIN1_0	Multi-function serial interface ch.1 input pin	96	81	66	59	A9	D9
	SIN1_1		62	52	41	30	L13	L12
	SOT1_0 (SDA1_0)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I^2C (operation mode 4).	97	82	67	60	B9	C9
	SOT1_1 (SDA1_1)		63	53	42	31	L12	K12
	SCK1_0 (SCL1_0)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a CSIO (operation modes 4) and as SCL1 when it is used in an I^2C (operation mode 4).	98	83	-	61	C9	B9
	SCK1_1 (SCL1_1)		64	54	43	32	K13	K11

Pin Function	Pin Name	Function Description	Pin No					
			LQFP 120	LQFP 100	LQFP 80	QFP 100	BGA 112	BGA 144
Multi-function Serial 6	SIN6_0	Multi-function serial interface ch.6 input pin	7	7	7	85	E1	E1
	SIN6_1		95	80	65	58	A10	B10
	SOT6_0 (SDA6_0)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I^2C (operation mode 4).	8	8	8	86	E2	E2
	SOT6_1 (SDA6_1)		94	79	64	57	B10	A11
	SCK6_0 (SCL6_0)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a CSIO (operation modes 2) and as SCL6 when it is used in an I^2C (operation mode 4).	9	-	-	-	-	E3
	SCK6_1 (SCL6_1)		93	78	63	56	B11	C10
	SCS6_1	Multi-function serial interface ch.6 serial chip select pin	92	77	62	55	A12	B13
Multi-function Serial 7	SIN7_0	Multi-function serial interface ch.7 input pin	101	86	-	64	C8	C8
	SIN7_1		50	45	35	23	L9	L8
	SOT7_0 (SDA7_0)	Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I^2C (operation mode 4).	100	85	-	63	B8	D8
	SOT7_1 (SDA7_1)		49	44	34	22	M9	M8
	SCK7_0 (SCL7_0)	Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a CSIO (operation modes 2) and as SCL7 when it is used in an I^2C (operation mode 4).	99	84	-	62	A8	A9
	SCK7_1 (SCL7_1)		48	43	33	21	L8	K7
	SCS7_1	Multi-function serial interface ch.7 serial chip select pin	47	42	32	20	L7	L7

Pin Function	Pin Name	Function Description	Pin No					
			LQFP 120	LQFP 100	LQFP 80	QFP 100	BGA 112	BGA 144
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch.0 AIN input pin	24	19	14	97	J2	J2
	AIN0_1		51	-	-	-	-	K8
	AIN0_2		2	2	2	80	C1	C1
	BIN0_0	QPRC ch.0 BIN input pin	25	20	15	98	J3	J3
	BIN0_1		52	-	-	-	-	L9
	BIN0_2		3	3	3	81	C2	C2
	ZIN0_0	QPRC ch.0 ZIN input pin	26	21	16	99	K1	J4
	ZIN0_1		53	-	-	-	-	K9
	ZIN0_2		4	4	4	82	C3	D1
Quadrature Position/ Revolution Counter 1	AIN1_0	QPRC ch.1 AIN input pin	10	-	-	-	-	E4
	AIN1_1		89	74	-	52	C12	C12
	AIN1_2		48	43	33	21	L8	K7
	BIN1_0	QPRC ch.1 BIN input pin	11	-	-	-	-	F1
	BIN1_1		88	73	-	51	C13	D11
	BIN1_2		49	44	34	22	M9	M8
	ZIN1_0	QPRC ch.1 ZIN input pin	12	-	-	-	-	F2
	ZIN1_1		87	72	-	50	D12	D12
	ZIN1_2		50	45	35	23	L9	L8
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of Real-time clock	115	95	75	73	B4	B4
	RTCCO_1		64	54	43	32	K13	K11
	RTCCO_2		23	18	13	96	J1	J1
	SUBOUT_0	Sub clock output pin	115	95	75	73	B4	B4
	SUBOUT_1		64	54	43	32	K13	K11
	SUBOUT_2		23	18	13	96	J1	J1
USB	UDM0	USB device/host D – pin	118	98	78	76	A3	A3
	UDP0	USB device/host D + pin	119	99	79	77	A2	A2
	UHCONX0	USB external pull-up control pin	115	95	75	73	B4	B4
Low-Power Consumption Mode	WKUP0	Deep standby mode return signal input pin 0	116	96	76	74	B3	B3
	WKUP1	Deep standby mode return signal input pin 1	14	9	9	87	E3	F4
	WKUP2	Deep standby mode return signal input pin 2	50	45	35	23	L9	L8
	WKUP3	Deep standby mode return signal input pin 3	69	59	48	37	H12	H11
DAC	DA0	D/A converter ch.0 analog output pin	36	31	21	9	M4	L4
	DA1	D/A converter ch.1 analog output pin	37	32	22	10	L5	K5
VBAT	VREGCTL	On-board regulator control pin	41	36	26	14	L6	L6
	VWAKEUP	The return signal input pin from a hibernation state	42	37	27	15	M7	K6
SD I/F	S_CLK_0	SD memory card interface SD memory card clock output pin	92	77	62	55	A12	B13
	S_CMD_0	SD memory card interface SD memory card command output	93	78	63	56	B11	C10
	S_DATA1_0	SD memory card interface SD memory card data bus	94	79	64	57	B10	A11
	S_DATA0_0		95	80	65	58	A10	B10
	S_DATA3_0		96	81	66	59	A9	D9
	S_DATA2_0		97	82	67	60	B9	C9
	S_CD_0	SD memory card interface SD memory card detection pin	113	93	73	71	C5	B5
	S_WP_0	SD memory card interface SD memory card write protection	114	94	74	72	B5	C4

Pin Function	Pin Name	Function Description	Pin No					
			LQFP 120	LQFP 100	LQFP 80	QFP 100	BGA 112	BGA 144
Reset	INITX	External Reset Input pin. A reset is valid when INITX="L".	38	33	23	11	M6	N4
Mode	MD1	Mode 1 pin. During serial programming to Flash memory, MD1="L" must be input.	56	46	36	24	M10	N10
	MD0	Mode 0 pin. During normal operation, MD0="L" must be input. During serial programming to Flash memory, MD0="H" must be input.	57	47	37	25	M11	M11
Power	VCC	Power supply Pin	1	1	1	79	B1	B1
			31	26	-	4	M1	M1
			46	41	31	19	M8	M9
			61	51	-	29	M13	M13
			91	76	61	54	B13	A12
	USBVCC	3.3 V Power supply port for USB I/O	117	97	77	75	A4	A4
GND	VSS	GND Pin	107	92	-	70	A5	A7
			30	25	20	3	N1	N1
			45	40	30	18	N10	N9
			60	50	40	28	N13	N13
			90	75	60	53	A13	A13
			120	100	80	78	A1	A1
			-	-	-	-	A7	A5
			-	-	-	-	B2	A8
			-	-	-	-	B12	A10
			-	-	-	-	C11	B2
			-	-	-	-	H1	B11
			-	-	-	-	N4	B12
			-	-	-	-	M5	C3
			-	-	-	-	N7	C11
			-	-	-	-	L11	C13
			-	-	-	-	A11	D4
			-	-	-	-	M12	D10
			-	-	-	-	M2	K1
			-	-	-	-	-	K4
			-	-	-	-	-	K10
			-	-	-	-	-	L3
			-	-	-	-	-	L5
			-	-	-	-	-	L11
			-	-	-	-	-	L13
			-	-	-	-	-	M2
			-	-	-	-	-	M4
			-	-	-	-	-	M6
			-	-	-	-	-	M7
			-	-	-	-	-	M12
			-	-	-	-	-	N6

Pin status Type	Function Group	Power-on Reset or Low-voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or SLEEP Mode State	TIMER Mode, RTC Mode, or STOP Mode State		Deep Standby RTC Mode or Deep Standby STOP Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Input enabled	GPIO selected	Hi-Z / Input enabled	GPIO selected
F	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									Maintain previous state
G	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
H	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									
I	Resource selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									

Table 12-8. Typical and maximum current consumption in STOP mode, TIMER mode and RTC mode

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCH}	VCC	STOP mode	-	0.33	1.8	mA	*3, *4 Ta=+25°C
					-	15	mA	*3, *4 Ta=+85°C
					-	22	mA	*3, *4 Ta=+105°C
	I_{CCT}		TIMER mode (built-in high-speed CR)	4 MHz	0.70	2.2	mA	*3, *4 Ta=+25°C
					-	16	mA	*3, *4 Ta=+85°C
					-	22	mA	*3, *4 Ta=+105°C
			TIMER mode (sub oscillation)	32 kHz	0.33	1.8	mA	*3, *4 Ta=+25°C
					-	15	mA	*3, *4 Ta=+85°C
					-	22	mA	*3, *4 Ta=+105°C
			TIMER mode (built-in low-speed CR)	100 kHz	0.34	1.8	mA	*3, *4 Ta=+25°C
					-	15	mA	*3, *4 Ta=+85°C
					-	22	mA	*3, *4 Ta=+105°C
	I_{CCR}		RTC mode (sub oscillation)	32 kHz	0.33	1.8	mA	*3, *4 Ta=+25°C
					-	15	mA	*3, *4 Ta=+85°C
					-	22	mA	*3, *4 Ta=+105°C

*1: V_{CC}=3.3 V

*2: V_{CC}=5.5 V

*3: When all ports are fixed.

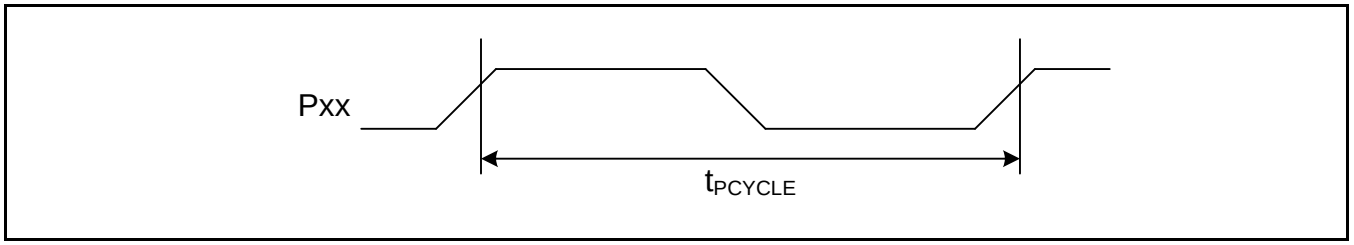
*4: When LVD is OFF

12.4.9 GPIO Output Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{PCYCLE}	Pxx*	$V_{CC} \geq 4.5$ V	-	50	MHz
			$V_{CC} < 4.5$ V	-	32	MHz

*: GPIO is a target.



12.4.10 External Bus Timing

External Bus Clock Output Characteristics

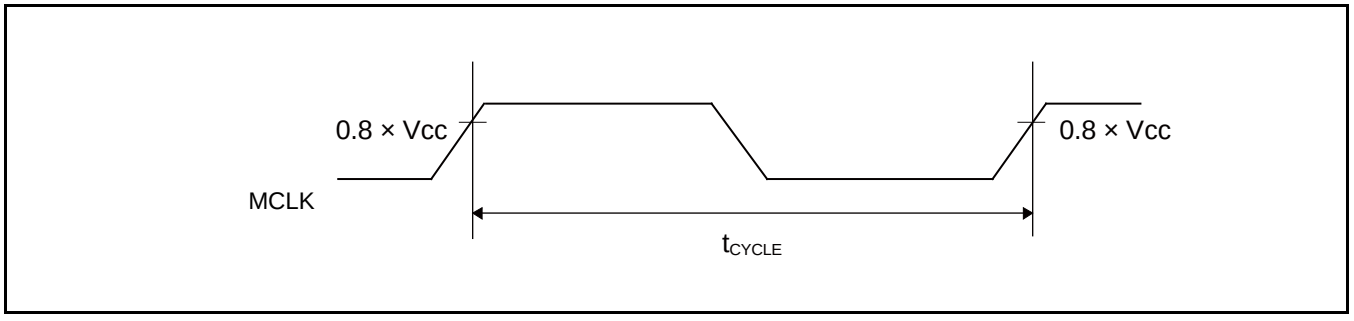
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{CYCLE}	MCLKOUT*1	$V_{CC} \geq 4.5$ V	-	50*2	MHz
			$V_{CC} < 4.5$ V	-	32*3	MHz

*1: The external bus clock (MCLKOUT) is a divided clock of HCLK.
For more information about setting of clock divider, see CHAPTER 14: External Bus Interface in FM4 Family Peripheral Manual Main part (002-04856).

*2: Generate MCLKOUT at setting more than 4 division when the AHB bus clock exceeds 100 MHz.

*3: Generate MCLKOUT at setting more than 4 division when the AHB bus clock exceeds 64 MHz.

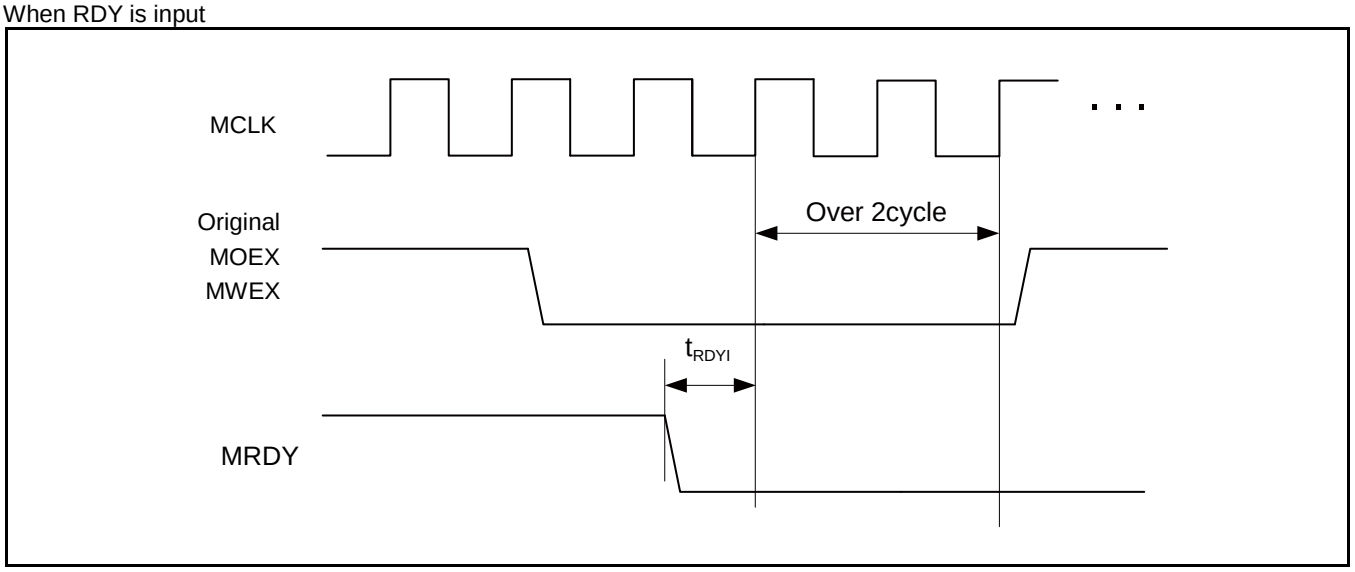


External Ready Input Timing

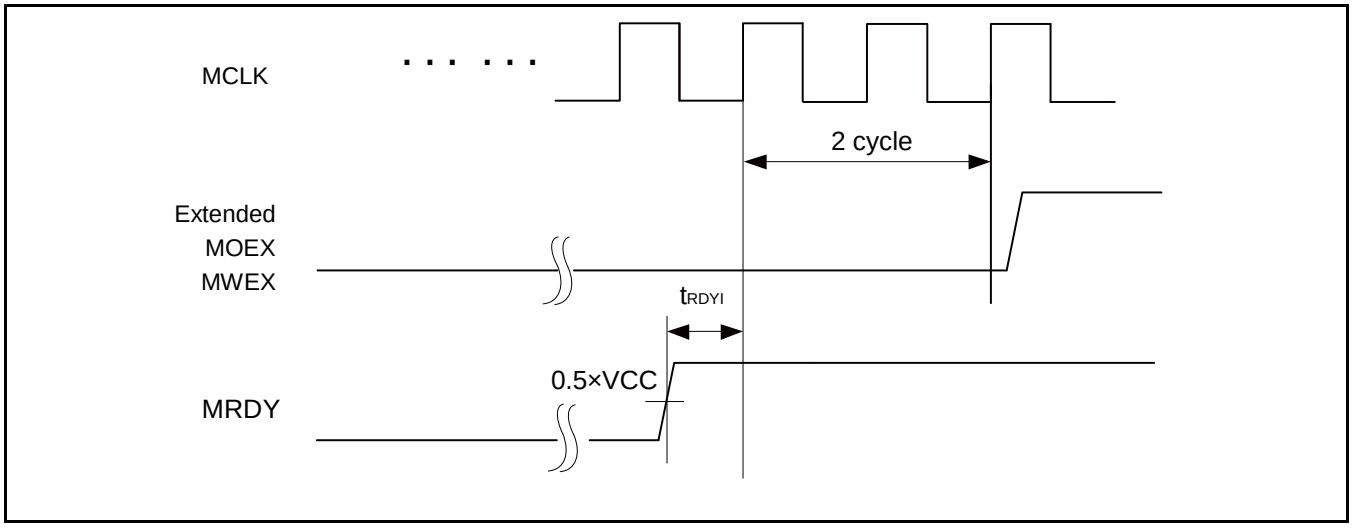
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MCLK↑ MRDY input setup time	t_{RDYI}	MCLK, MRDY	$V_{CC} \geq 4.5$ V	19	-	ns	
			$V_{CC} < 4.5$ V	37			

■When RDY is input



■When RDY is released



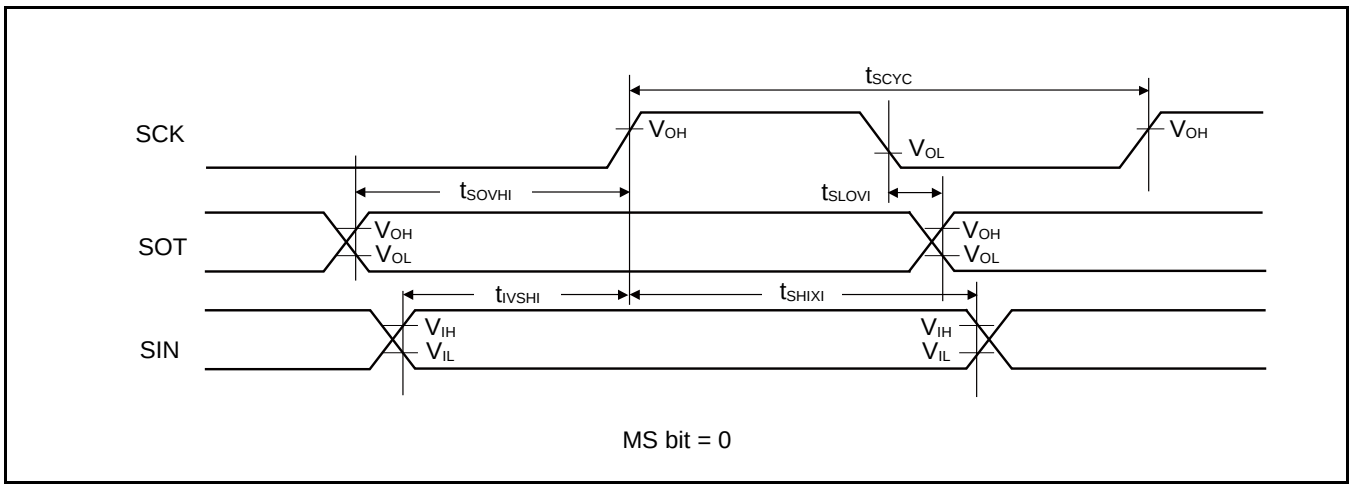
Synchronous Serial (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

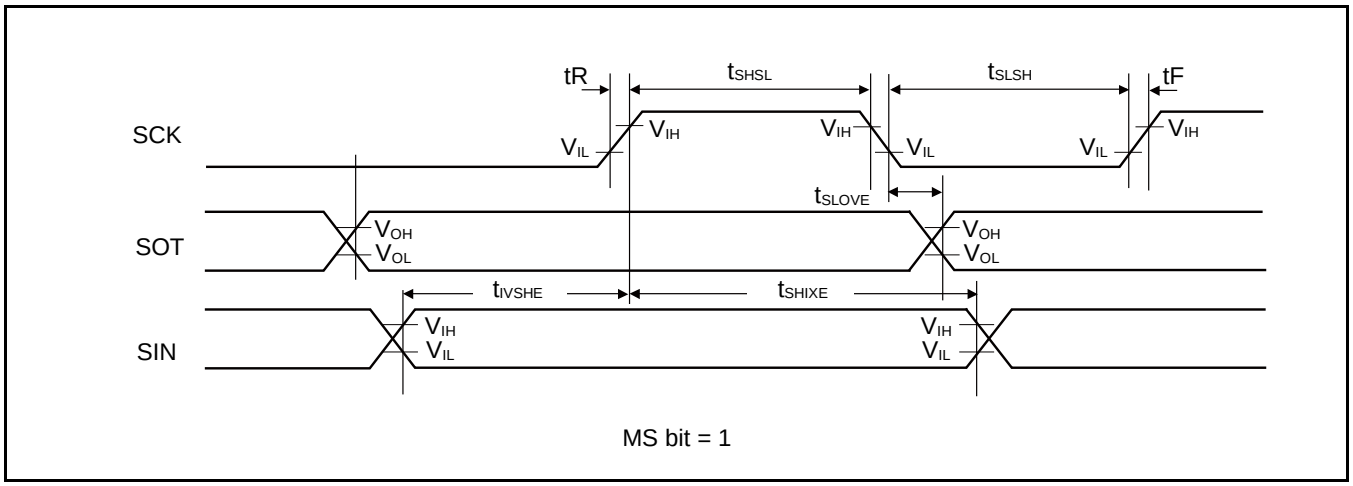
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT→SCK↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2tC_{YCP}$ - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	-4.5	-	+4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential Nonlinearity	-	-	-2.5	-	+2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	-15	-	+15	mV	
Full-scale transition voltage	V_{FST}	ANxx	AVRH - 15	-	AVRH + 15	mV	
Conversion time	-	-	0.5 *1	-	-	µs	AV_{CC} ≥ 4.5V
Sampling time *2	Ts	-	0.15	-	10	µs	AV_{CC} ≥ 4.5V
			0.3	-			AV_{CC} < 4.5V
Compare clock cycle *3	Tcck	-	25	-	1000	ns	AV_{CC} ≥ 4.5V
			50	-	1000		AV_{CC} < 4.5V
State transition time to operation permission	Tstt	-	-	-	1.0	µs	
Power supply current (analog + digital)	-	AVCC	-	0.69	0.92	mA	A/D 1 unit operation
			-	1.0	18	µA	When A/D stop
Reference power supply current (AVRH)	-	AVRH	-	1.1	1.97	mA	A/D 1unit operation AVRH=5.5 V
				0.3	6.3	µA	When A/D stop
Analog input capacity	C_{AIN}	-	-	-	12.05	pF	
Analog input resistance	R_{AIN}	-	-	-	1.2	kΩ	AV_{CC} ≥ 4.5 V
					1.8		AV_{CC} < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AV_{SS}	-	AVRH	V	
Reference voltage	-	AVRH	4.5	-	AV_{CC}	V	Tcck < 50 ns
			2.7	-	AV_{CC}		Tcck ≥ 50 ns

*1: The conversion time is the value of sampling time (Ts) + compare time (Tc).
The condition of the minimum conversion time is when the value of sampling time: 150 ns, the value of compare time: 350 ns (AV_{CC} ≥ 4.5 V). Ensure that it satisfies the value of sampling time (Ts) and compare clock cycle (Tcck). For setting*4 of sampling time and compare clock cycle, see CHAPTER 1-1: A/D Converter in FM4 Family Peripheral Manual Analog macro part (MN709-00001). The register setting of the A/D Converter is reflected by the peripheral clock timing. The sampling and compare clock are set at Base clock (HCLK).

*2: A necessary sampling time changes by external impedance. Ensure that it set the sampling time to satisfy (Equation 1).

*3: The compare time (Tc) is the value of (Equation 2).

*4: The register setting of the A/D Converter is reflected by the timing of the APB bus clock. The sampling clock and compare clock are set in base clock (HCLK). About the APB bus number which the A/D Converter is connected to, see 8. Block Diagram in this data sheet.

12.6 12-bit D/A Converter

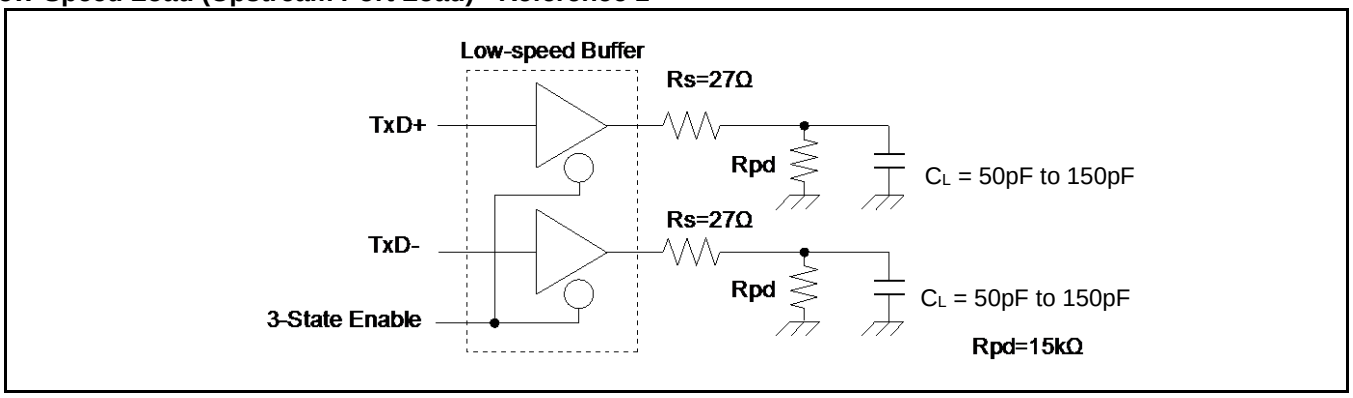
Electrical Characteristics for the D/A Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V)

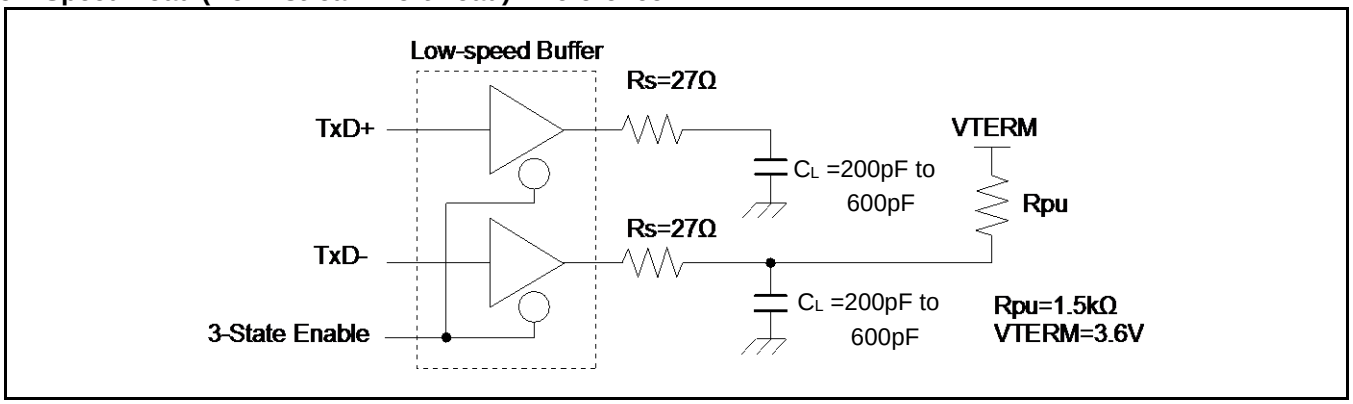
Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	DAx	-	-	12	bit	
Conversion time	tc20		0.56	0.69	0.81	µs	Load 20 pF
	tc100		2.79	3.42	4.06	µs	Load 100 pF
Integral Nonlinearity*	INL		-16	-	+16	LSB	
Differential Nonlinearity *	DNL		-0.98	-	+1.5	LSB	
Output voltage offset	V_{OFF}		-	-	10.0	mV	When setting 0x000
			-20.0	-	+1.4	mV	When setting 0xFFF
Analog output impedance	R_O		3.10	3.80	4.50	kΩ	D/A operation
			2.0	-	-	MΩ	When D/A stop
Power supply current*	IDDA	AVCC	260	330	410	µA	D/A 1unit operation AV_{CC}=3.3 V
			400	510	620	µA	D/A 1unit operation AV_{CC}=5.0 V
	IDSA		-	-	14	µA	When D/A stop

*: During no load

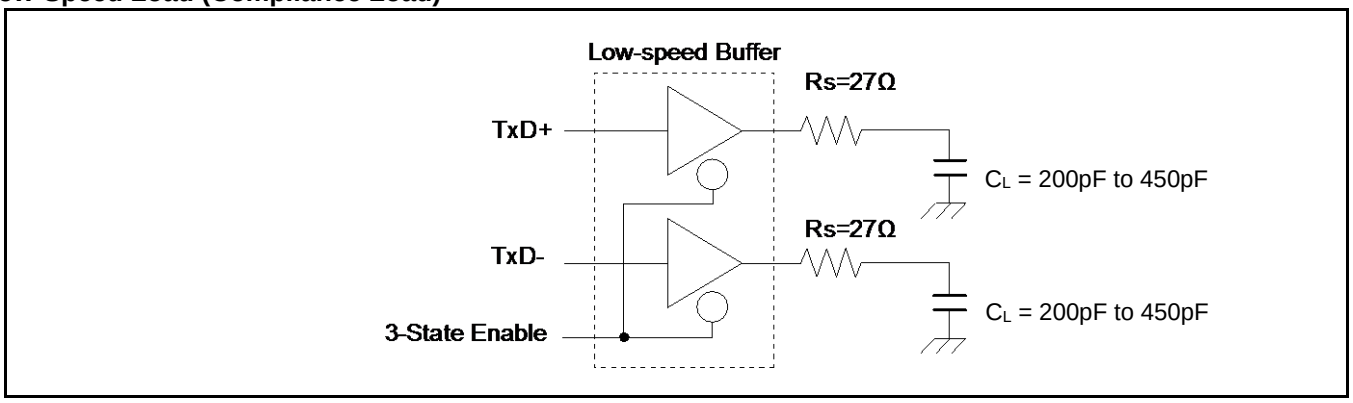
Low-Speed Load (Upstream Port Load) - Reference 1



Low-Speed Load (Downstream Port Load) - Reference 2



Low-Speed Load (Compliance Load)



12.11 Standby Recovery Time

12.11.1 Recovery cause: Interrupt/WKUP

The time from recovery cause reception of the internal circuit to the program operation start is shown.

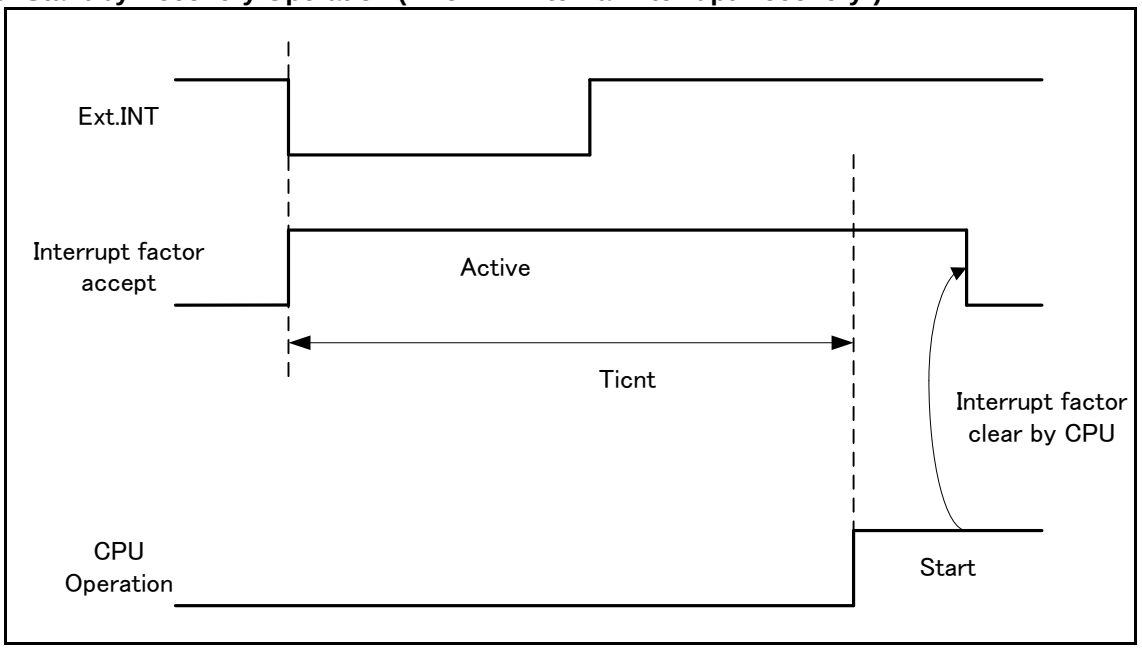
Recovery Count Time

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	Ticnt	HCLK×1		µs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		40	80	µs	
Low-speed CR timer mode		450	900	µs	
Sub timer mode		896	1136	µs	
RTC mode stop mode (High-speed CR /Main/PLL run mode return)		316	540	µs	
RTC mode stop mode (Low-speed CR/sub run mode return)		270	480		
Deep standby RTC mode with RAM retention		365	667	µs	without RAM retention
Deep standby stop mode with RAM retention		365	667	µs	with RAM retention

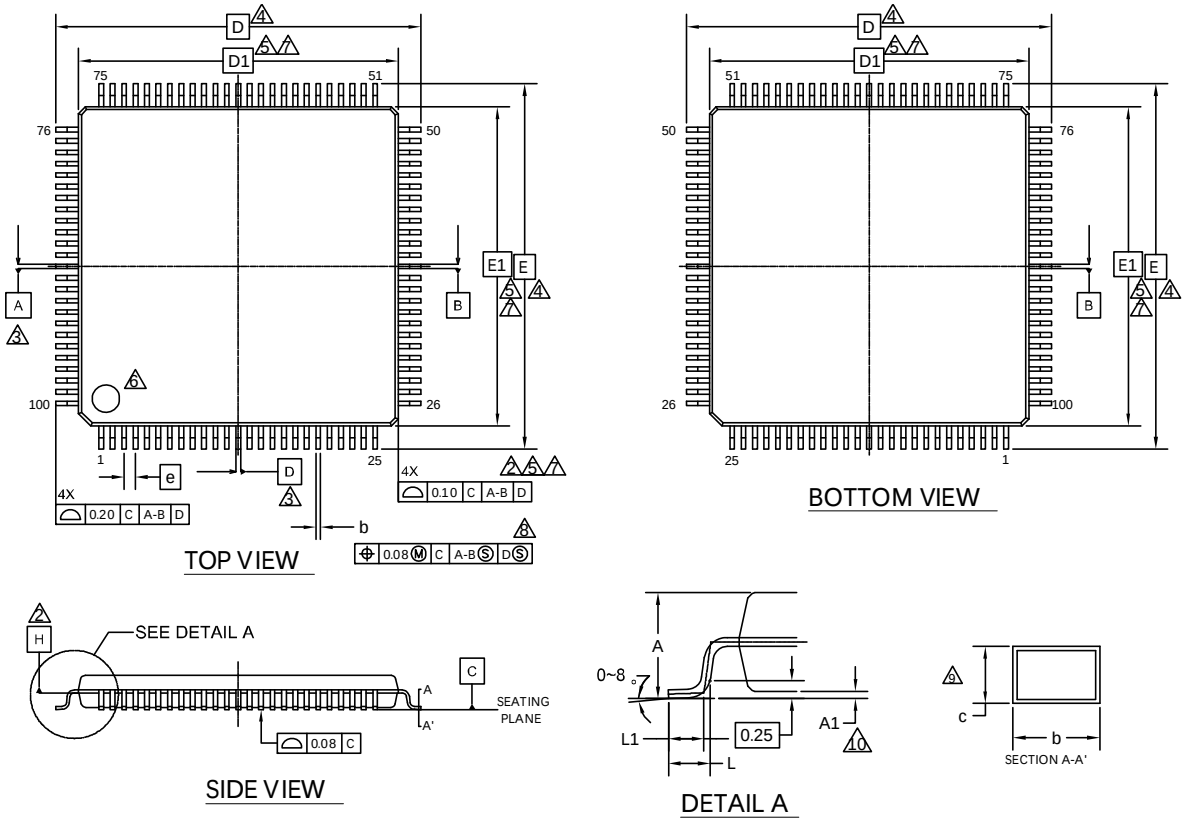
*: The maximum value depends on the built-in CR accuracy.

Example of Standby Recovery Operation (when in External Interrupt Recovery*)



*: External interrupt is set to detecting fall edge.

Package Type	Package Code
LQFP-100	LQI100



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	16.00 BSC		
D1	14.00 BSC		
e	0.50 BSC		
E	16.00 BSC		
E1	14.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-11500 **

PACKAGE OUTLINE, 100 LEAD LQFP
14.0X14.0X1.7 MM LQI100 Rev**

15. Major Changes

Spansion Publication Number: DS709-00001

Page	Section	Change Results
Revision 1.0		
-	-	Preliminary → Data Sheet
1	DESCRIPTION	Deleted the following description : The products which are described in this data sheet are placed into TYPE4 product categories in "FM4 Family PERIPHERAL MANUAL".
3	FEATURES [USB function]	Added the following description : ・The size of each endpoint is according to the follows. - Endpoint 0, 2 to 5 : 64bytes - Endpoint 1 : 256bytes
4	FEATURES ●Multi-function Serial Interface [I^2C]	Revised the following description : Fast mode Plus (Fm+) (Max 1000 kbps, only for ch.3 and ch.7) supported →Fast mode Plus (Fm+) (Max 1000 kbps, only for ch.3=ch.A and ch.7=ch.B) supported
7	FEATURES ●Unique ID	Added new section
9	PRODUCT LINEUP ●Function	Added “Unique ID”
51,52	I/O CIRCUIT TYPE	Revised the remarks of “Type O, P, Q”
59	HANDLING DEVICES ●Handling when using debug pins	Added new section
60	BLOCK DIAGRAM	Revised the block diagram
74	ELECTRICAL CHARACTERISTICS 2. Recommended Operating Conditions	Revised “Table for package thermal resistance and maximum permissible power”
77 to 82	ELECTRICAL CHARACTERISTICS 3. DC Characteristics (1) Current Rating	• Revised the value of TBD • Revised the unit of “ICCHD”, “ICCRD”, “ICCVBAT” mA → µA • Added the note to “ICCVBAT”
87	ELECTRICAL CHARACTERISTICS 4. AC Characteristics (2) Sub Clock Input Characteristics	Revised the waveform chart
87	ELECTRICAL CHARACTERISTICS 4. AC Characteristics (3) Built-in CR OscillationCharacteristics	• Revised the value of TBD • Revised the table and the note of “Built-in High-speed CR”
146	ELECTRICAL CHARACTERISTICS 5. 12-bit A/D Converter ・Electrical Characteristics for the A/D Converter	• Revised the value of TBD • Revised the condition of the electrical characteristics table
149	ELECTRICAL CHARACTERISTICS 6. 12-bit D/A Converter ・Electrical Characteristics for the D/A Converter	• Revised the value of TBD • Revised the condition and Remarks of the electrical characteristics table
156	ELECTRICAL CHARACTERISTICS 11. Standby Recovery Time (1) Recovery cause: Interrupt/WKUP	• Revised the value of TBD • Revised the table of Recovery count time
158	ELECTRICAL CHARACTERISTICS 11. Standby Recovery Time (2) Recovery cause:Reset	• Revised the value of TBD • Revised the table of Recovery count time