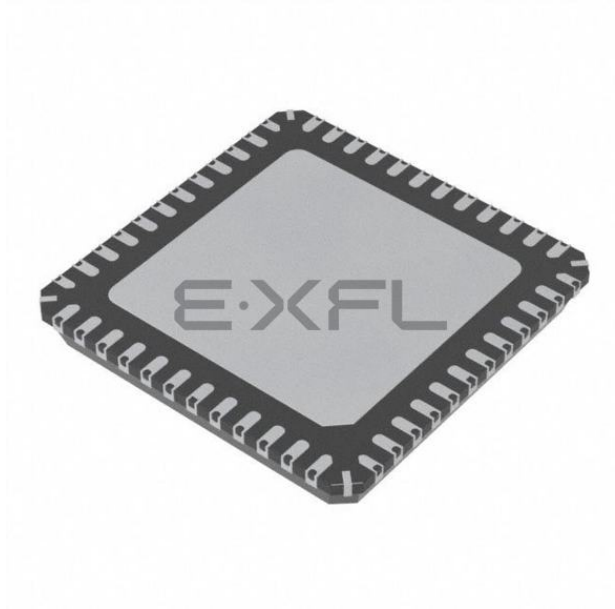

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## Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

**Embedded - Microcontrollers - Application Specific** represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

## What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

| Details | |
|---|---|
| Product Status | Active |
| Applications | Automotive |
| Core Processor | ARM® Cortex®-M0 |
| Program Memory Type | FLASH (40kB) |
| Controller Series | - |
| RAM Size | 2K x 8 |
| Interface | LIN, SSI, UART |
| Number of I/O | 10 |
| Voltage - Supply | 3V ~ 28V |
| Operating Temperature | -40°C ~ 150°C (TJ) |
| Mounting Type | Surface Mount |
| Package / Case | 48-VFQFN Exposed Pad |
| Supplier Device Package | PG-VQFN-48-31 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/tle98422qxxuma1 |

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  - Sleep Mode with cyclic sense option
  - Cyclic wake-up during Sleep Mode
  - Stop Mode with cyclic sense option
- Power-on and undervoltage/brownout reset generator
- Overtemperature protection
- Short circuit protection for all voltage regulators and actuators (High Side, Low Side)
- Loss of clock detection with fail safe mode for power switches
- Temperature Range $T_J$: -40 °C up to 150 °C
- Package VQFN-48-31 with LTI feature
- Green package (RoHS compliant)
- AEC Qualified

# 2 Block Diagram

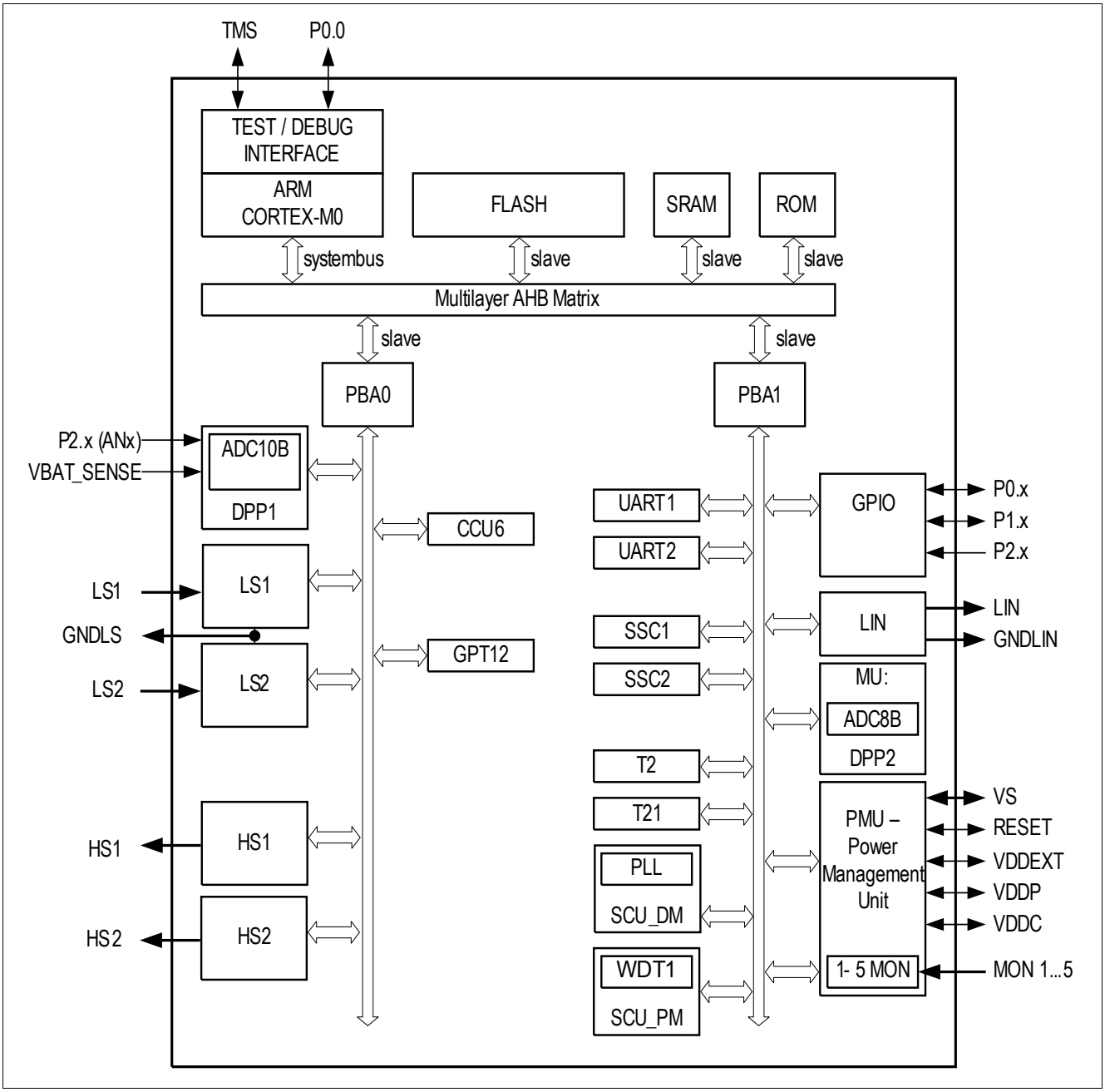


**Figure 1 Block Diagram, TLE9842-2QX**

**Table 2 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Number | Type | Reset State | Function |
|---|---|---|---|---|
| **P2** | | | | **Port 2**<br>Port 2 is an 8-Bit general purpose input-only port.<br>Alternate functions can be assigned and are listed in the Port description. Main function is listed below. |
| P2.0 | 39 | I | I | AN0 ADC1 analog input channel 12<br>Alternate function mapping see **Table 10** |
| P2.1 | 37 | I | I | AN1 ADC1 analog input channel 7<br>Alternate function mapping see **Table 10** |
| P2.2 | 33 | I | I | AN2 ADC1 analog input channel 8<br>Alternate function mapping see **Table 10** |
| P2.3 | 36 | I | I | AN3 ADC1 analog input channel 9<br>Alternate function mapping see **Table 10** |
| P2.4 | 32 | I | I | Alternate function mapping see **Table 10**<br>XTAL1[1)] External oscillator input |
| P2.5 | 31 | I<br>O | I<br>Hi-Z | Alternate function mapping see **Table 10**<br>XTAL2[1)] External oscillator output |
| P2.6 | 34 | I | I | AN6 ADC1 analog input channel 10<br>Alternate function mapping see **Table 10** |
| P2.7 | 35 | I | I | AN7 ADC1 analog input channel 11<br>Alternate function mapping see **Table 10** |
| **Power Supply** | | | | |
| VS | 47 | P | – | Battery supply input |
| VDDP | 44 | P | – | I/O port supply (5.0 V). Do not connect external loads. For buffer and bypass capacitors. |
| VDDC | 42 | P | – | Core supply (1.5 V during Active Mode,<br>0.9 V during Stop Mode). Do not connect external loads. For buffer/bypass capacitor. |
| VDDEXT | 45 | P | – | External voltage supply output (5.0 V, 20 mA) |
| GNDLS | 13 | P | – | Low-side ground LS1, LS2 |
| GNDP | 19, 30 | P | – | Core supply ground |
| GNDA | 43 | P | – | Analog supply ground |
| GNDLIN | 2 | P | – | LIN ground |
| **Monitor Inputs** | | | | |
| MON1 | 5 | I | I | High Voltage Monitor Input 1 |
| MON2 | 6 | I | I | High Voltage Monitor Input 2 |
| MON3 | 7 | I | I | High Voltage Monitor Input 3 |
| MON4 | 8 | I | I | High Voltage Monitor Input 4 |
| MON5 | 9 | I | I | High Voltage Monitor Input 5 |
| **High-Side Switch / Low-Side Switch Outputs** | | | | |
| LS1 | 11 | O | Hi-Z | Low-Side switch output 1 |

### Reset Mode

The Reset Mode is a transition mode e.g. during power-up of the device after a power-on reset. In this mode the on-chip power supplies are enabled and all other modules are initialized. Once the core supply VDDC is stable, the Active Mode is entered. In case the watchdog timer WDT1 fails for more than four times, a fail-safe transition to the Sleep Mode is done.

### Active Mode

In Active Mode all modules are activated and the TLE9842-2QX is fully operational.

### Stop Mode

The Stop Mode is one out of two major low power modes. The transition to the low power modes is done by setting the respective Bits in the mode control register. In Stop Mode the embedded microcontroller is still powered allowing faster wake-up reaction times, but not clocked. A wake-up from this mode is possible by LIN bus activity, the High Voltage Monitor Input pins or the respective 5V GPIOs.

### Sleep Mode

The Sleep Mode is a major low-power mode. The transition to the low-power modes is done by setting the respective Bits in the Micro Controller Unit mode control register. The sleep time is configurable. In Sleep Mode the embedded microcontroller power supply is deactivated, allowing the lowest system power consumption, but the wake-up time is longer compared to the Stop Mode. In this mode a 64 bit wide buffer for data storage is available. A wake-up from this mode is possible by LIN bus activity or the High Voltage Monitor Input pins and cyclic wake. A wake-up from Sleep Mode behaves similar to a power-on reset. While changing into Sleep Mode, no incoming wake-requests are lost (i.e. no dead-time). It is possible to enter sleep-mode even with LIN dominant.

### Cyclic Wake-up Mode

The cyclic wake-up mode is a special operating mode of the Sleep Mode and the Stop Mode. The transition to the cyclic wake-up mode is done by first setting the respective Bits in the mode control register followed by the SLEEP or STOP command. Additional to the cyclic wake-up behavior (wake-up after a programmable time period), the wake-up sources of the normal Stop Mode and Sleep Mode are available.

### Cyclic Sense Mode

The cyclic sense mode is a special operating mode of the Sleep Mode and the Stop Mode. The transition to the cyclic sense mode is done by first setting the respective Bits in the mode control register followed by the STOP or SLEEP command. In cyclic sense mode the High-Side Switch can be switched on periodically for biasing some switches for example. The wake-up condition is configurable, when the sense result of defined monitor inputs at a window of interest changed compared to the previous wake-up period or reached a defined state respectively. In this case the Active Mode is entered immediately.

The following table shows the possible power mode configurations of each major module or function respectively.

**Table 3 Power Mode Configurations**

| Module/function | Active Mode | Sleep Mode | Stop Mode | Comment |
|---|---|---|---|---|
| VPRE, VDDP, VDDC | ON | OFF | ON | – |
| VDDEXT | ON/OFF | OFF | cyclic ON/OFF | – |
| HSx | ON/OFF | cyclic ON/OFF | cyclic ON/OFF | cyclic sense |
| LSx | ON/OFF | OFF | OFF | – |
| LIN TRx | ON/OFF | wake-up only / OFF | wake-up only/ OFF | – |

### 5.3.2 Voltage Regulator 1.5V (VDDC)

This module represents the 1.5 V voltage regulator, which provides the supply for the microcontroller core, digital peripherals and other chip internal analog 1.5 V functions (e.g. ADC).

**Features**

- 1.5 V low-drop voltage regulator
- Overcurrent monitoring and Shutdown with MCU signalling (Interrupt)
- Overvoltage monitoring with MCU signalling (Interrupt)
- Undervoltage monitoring with MCU signalling (interrupt)
- Undervoltage monitoring with reset
- Overtemperature Shutdown with MCU signalling (Interrupt)
- Pull Down Current Source at the output for Sleep Mode only (typ. 100 µA)

The output capacitor $C_{VDDC}$ is mandatory to ensure a proper regulator functionality.

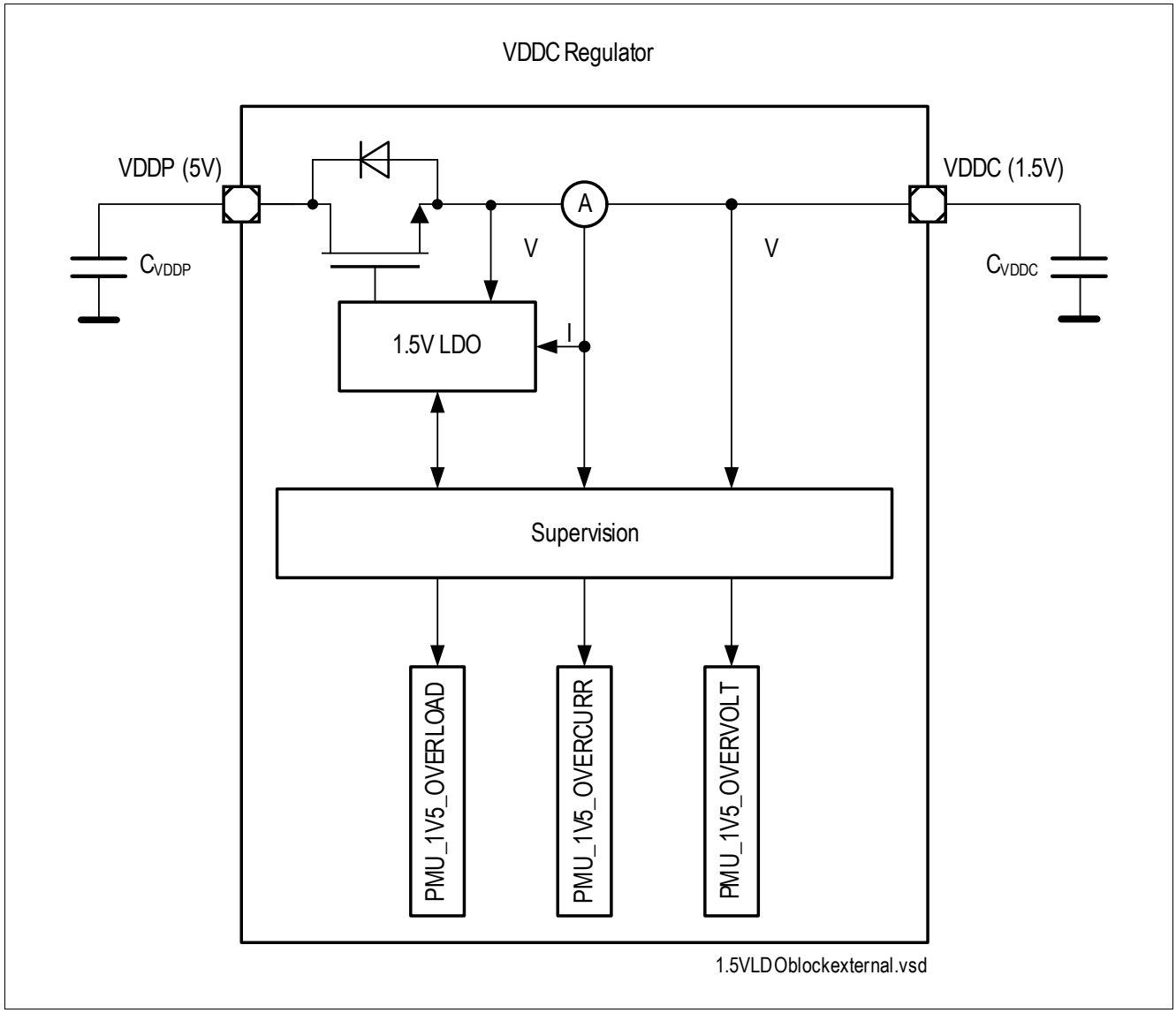


**Figure 7 Module Block Diagram of VDDC Voltage Regulator**

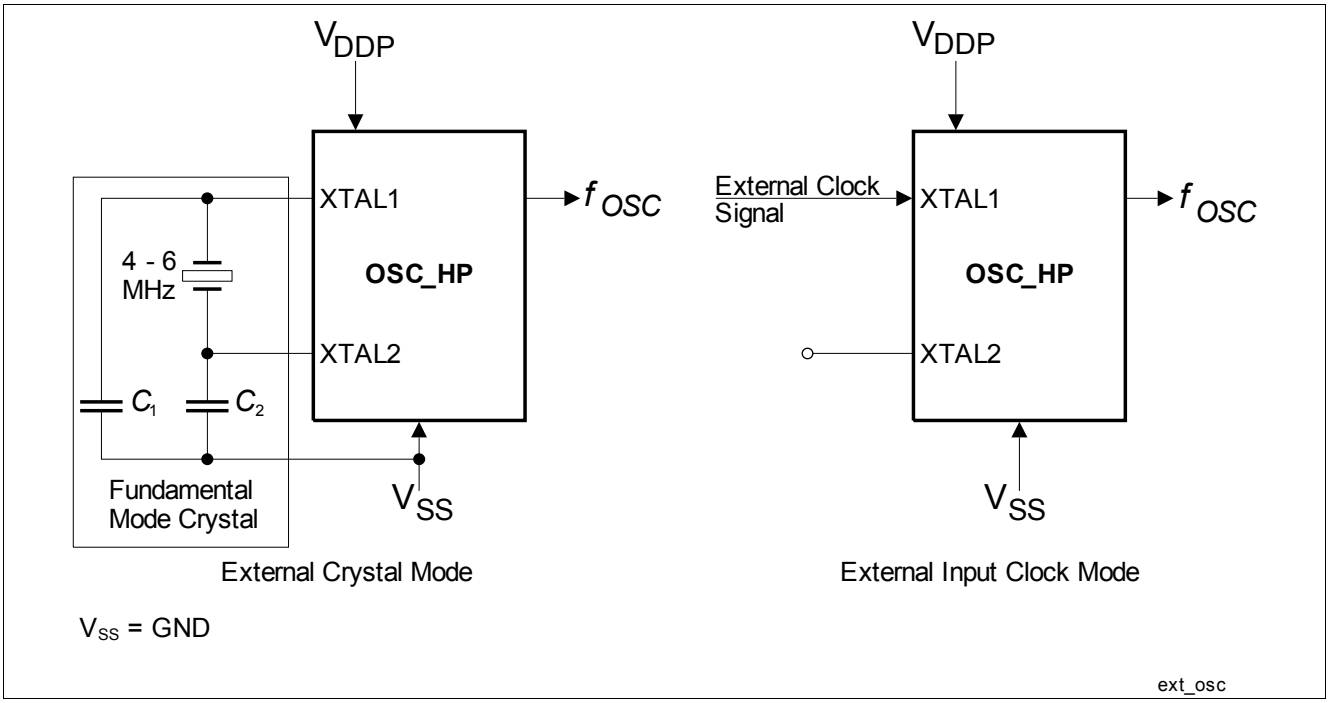


**Figure 11 TLE9842-2QX External Circuitry for the OSC_HP**

# 9 Address Space Organization

The embedded Cortex-M0 MCU offers the following address space organization:

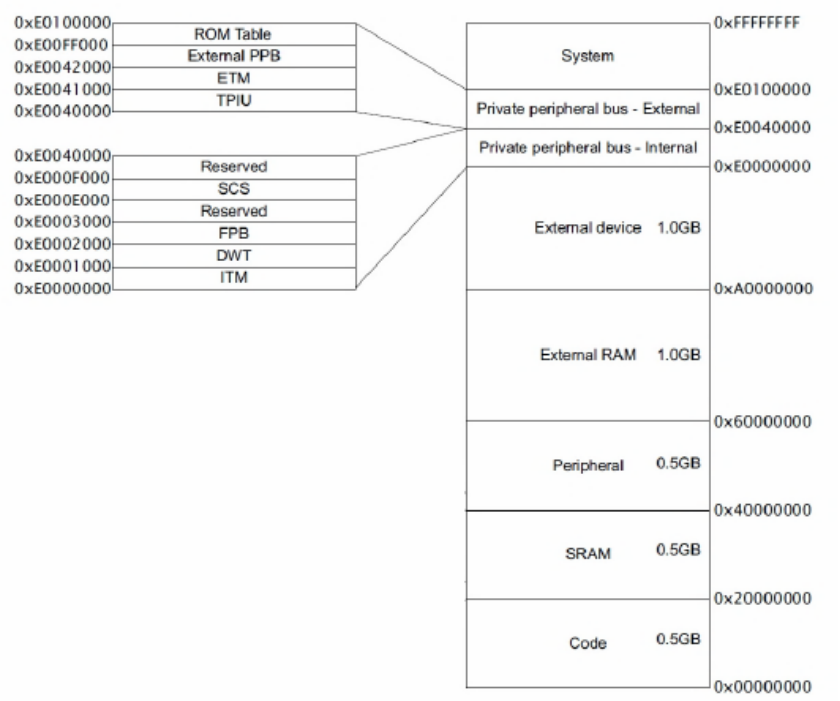


**Figure 16 Original Cortex-M0 Memory Map**

The TLE9842-2QX manipulates operands in the following memory spaces:

- 40 KByte of Flash memory in code space
- 24 KB Boot ROM memory in code space (used for boot code and IP storage)
- 2 KB RAM memory in code space and data space (RAM can be read/written as program memory or external data memory)
- Special function registers (SFRs) in peripheral linear address space, up to 0.5 GBytes

The figure below shows the detailed address alignment of TLE9842-2QX:

# 13 Watchdog Timer (WDT1)

## 13.1 Features

In Active Mode, the WDT1 acts as a windowed watchdog timer, which provides a highly reliable and safe way to recover from software or hardware failures.

The WDT1 is always enabled in Active Mode. In Sleep Mode, Stop Mode and Debug Mode the WDT1 is disabled.

**Functional Features**

- Watchdog Timer is operating with a from the system clock ($f_{SYS}$) independent clock source ($f_{LP\_CLK}$)
- Windowed Watchdog Timer with programmable timing (16, 32, 48, …, 1008ms period) in Active Mode
- Long open window (200 ms) after power-up, reset, wake-up
- Short open window (30 ms) to facilitate Flash programming
- System safety shutdown to Sleep Mode after 5 missed WDT1 services
- Watchdog is disabled in Debug Mode
- Watchdog cannot be deactivated in Normal Mode
- Watchdog reset is stored in reset status register

### 15.2.1 Block Diagram GPT1

**Block GPT1** contains three timers/counters: The core timer T3 and the two auxiliary timers T2 and T4. The maximum resolution is $f_{GPT}/4$. The auxiliary timers of GPT1 may optionally be configured as reload or capture registers for the core timer.

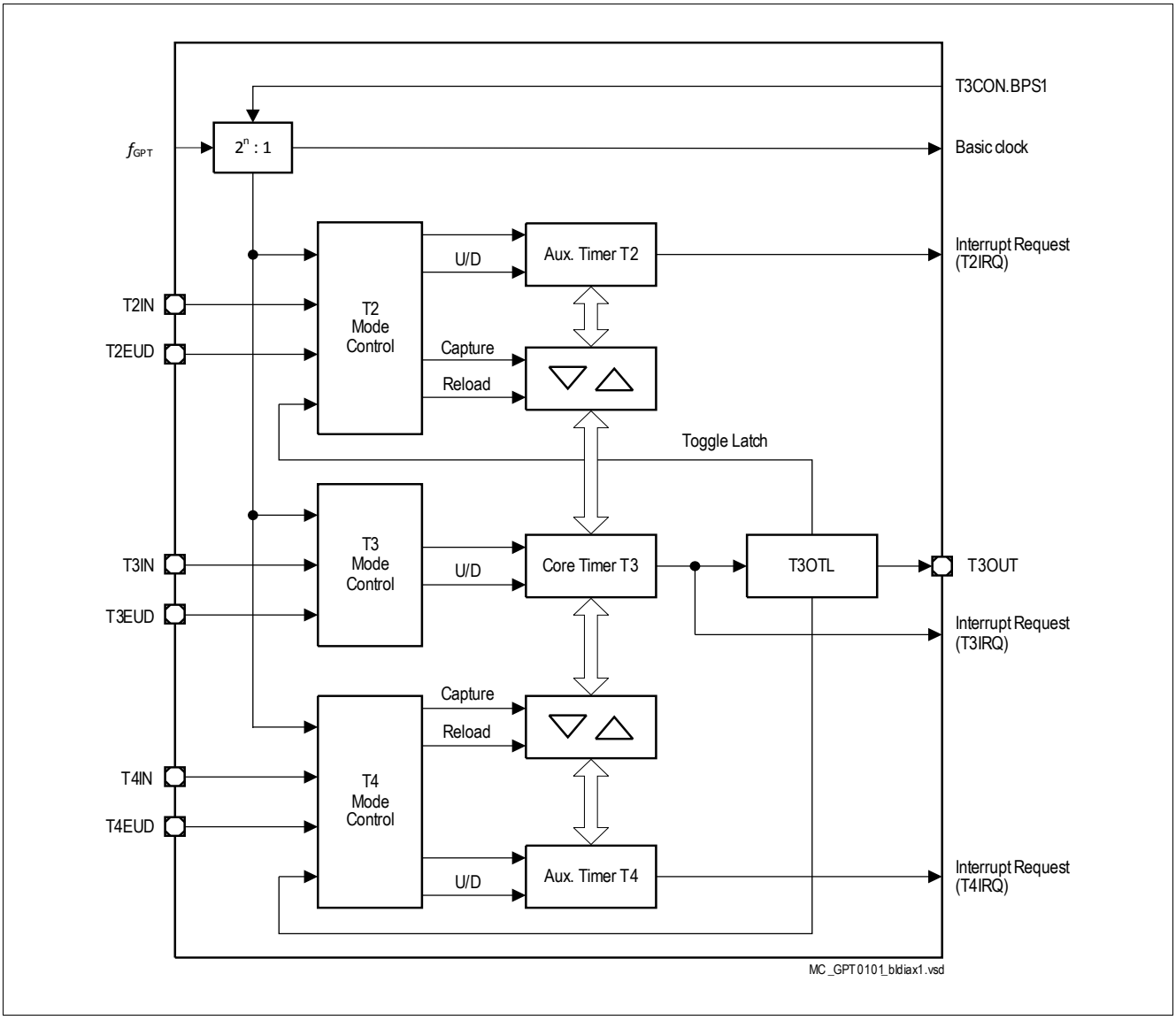


**Figure 23 GPT1 Block Diagram (n = 2 … 5)**

# 16 Timer2 and Timer21

## 16.1 Features

- 16-bit auto-reload mode
  – selectable up or down counting
- One channel 16-bit capture mode
- Baud-rate generator for U(S)ART

## 16.2 Introduction

Two functionally identical timers are implemented: Timer 2 and 21. The description refers to Timer 2 only, but applies to Timer 21 as well.

The timer modules are general purpose 16-bit timer. Timer 2 can function as a timer or counter in each of its modes. As a timer, it counts with an input clock of $f_{sys}/12$ (if prescaler is disabled). As a counter, Timer 2 counts 1-to-0 transitions on pin T2. In the counter mode, the maximum resolution for the count is $f_{sys}/24$ (if prescaler is disabled).

### 16.2.1 Timer2 and Timer21 Modes Overview

**Table 11 Port Registers**

| Mode | Description |
|---|---|
| **Auto-reload** | **Up/Down Count Disabled**<br>• Count up only<br>• Start counting from 16-Bit reload value, overflow at $FFFF_H$<br>• Reload event configurable for trigger by overflow condition only, or by negative/positive edge at input pin T2EX as well<br>• Programmable reload value in register RC2<br>• Interrupt is generated with reload events. |

# 25 High-Side Switch

## 25.1 Features

The high-side switch is optimized for driving resistive loads. Only small line inductance are allowed. Typical applications are single or multiple LEDs of a dashboard, switch illumination or other loads that require a high-side switch.

A cyclic switch activation during Sleep Mode or Stop Mode of the system is also available.

**Functional Features**

- Multi-purpose high-side switch for resistive load connections (only small line inductances are allowed)
- Overcurrent limitation
- Overcurrent detection with thresholds: 25 mA, 50 mA, 100 mA, 150 mA and automatic shutdown
- Overtemperature detection and automatic shutdown
- Open load detection in on mode with open load current of max. 1.5 mA.
- Interrupt signalling of overcurrent, overtemperature and open load condition
- Cyclic switch activation in Sleep Mode and Stop Mode with cyclic sense support and reduced driver capability: max. 40 mA
- PWM capability up to 25 kHz
- Internal connection to System-PWM Generator (CCU6)
- Slew rate control for low EMI characteristic

**Applications hints**

- The voltage at HSx must not exceed the supply voltage by more than 0.3V to prevent a reverse current from HSx to VS.

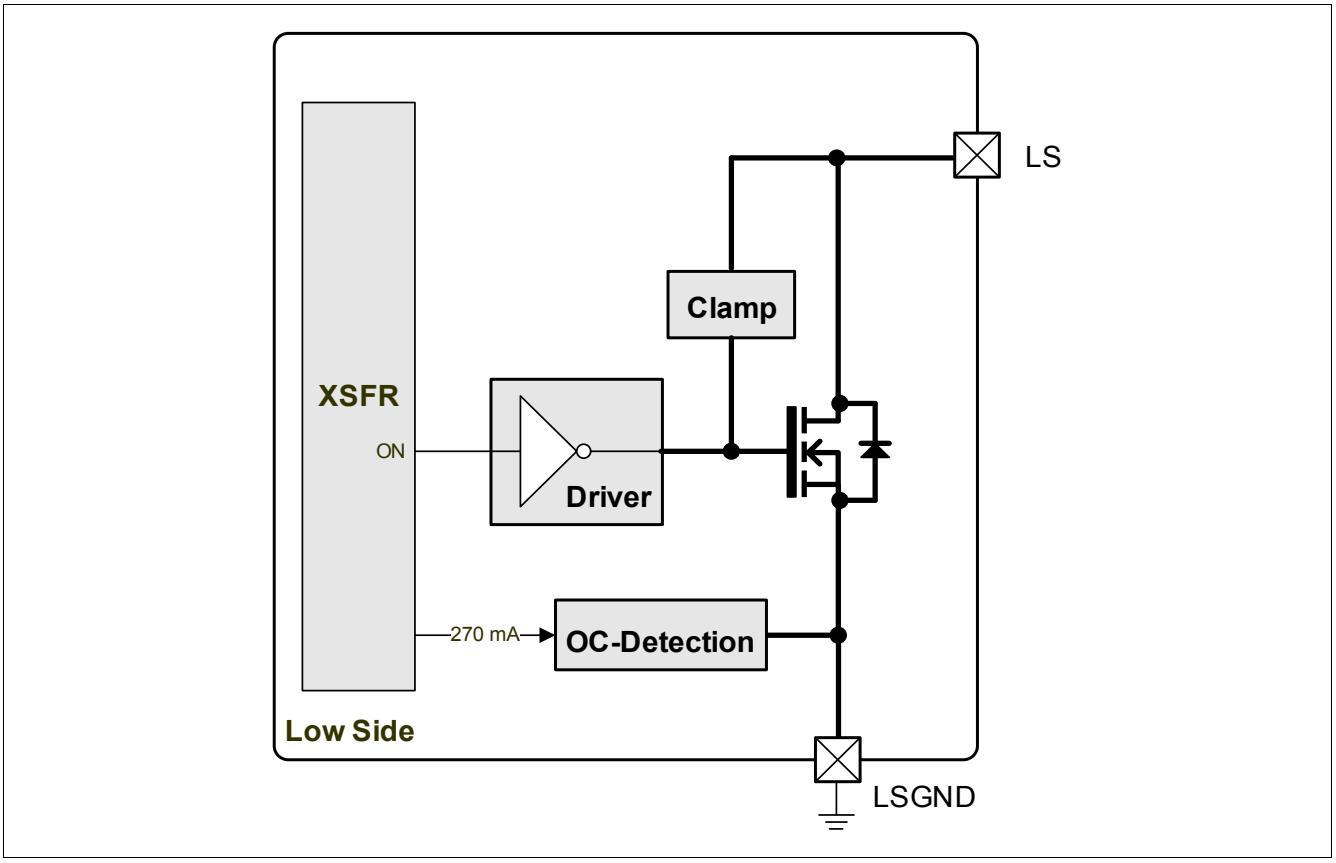


**Figure 34 Module Block Diagram**

## 26.2 Functional Description

The low-side switches can generally be controlled in two different ways:

- In normal mode the output stage is fully controllable through the **SFR** Registers **LSx_CTRL**. Protection functions as overcurrent and overtemperature are available.
- The PWM Mode can also be enabled by a **LSx_CTRL - SFR** bit. The PWM configuration has to be done in the corresponding PWM Module (CCU6). All protection functions are also available in this mode. The maximum PWM frequency must not exceed 25 kHz (fast slew rate only).

**Table 14 External Component (BOM)**

| Symbol | Function | Component |
|---|---|---|
| $C_{1VS}$ | Capacitor 1 at VS pin | 22 µF[1)] |
| $C_{2VS}$ | Capacitor 2 at VS pin | 100 nF[2)3)] |
| $C_{VDDEXT}$ | Capacitor at VDDEXT pin | 330 nF[2)] |
| $C_{VDDC}$ | Capacitor at VDDC pin | 100 nF[2)3)] + 330 nF[2)] |
| $C_{VDDP}$ | Capacitor at VDDP pin | 470 nF[2)3)] + 470 nF[2)] |
| $R_{MONx}$ | Resistor at MONx pin | 3.9 kΩ |
| $C_{MONx}$ | Capacitor at MONx connector | 6.8 nF[4)] |
| $R_{VBAT\_SENSE}$ | Resistor at VBAT_SENSE pin | 3.9 kΩ |
| $C_{VBAT\_SENSE1}$ | Capacitor 1at VBAT_SENSE pin | 10 nF[2)] |
| $C_{VBAT\_SENSE2}$ | Capacitor 2 at VBAT_SENSE connector | 6.8 nF[4)] |
| $C_{LIN}$ | Capacitor at LIN pin | 220 pF |
| $R_{1HS}$ | Resistor at HS pin for LED | e.g. 2.7kΩ |
| $R_{2HS}$ | Resistor at HS pin | 160 Ω[5)] |
| $C_{1HS}$ | Capacitor at HS pin | 6.8nF[2)] |
| $C_{2HS}$ | Capacitor at HS connector | 33nF[4)] |

1) to be dimensioned according to application requirements
2) to reduce the effect of fast voltage transients of Vs, these capacitors should be placed close to the device pin
3) ceramic capacitor
4) for ESD GUN
5) optional, for short to battery protection, calculated for 24V (jump start)

## 27.2 Connection of N.C.

The device contains several N.C. (not connected, no bond wire).

**Table 15 Recommendation for connecting N.C. / N.U. pins**

| type | pin number | recommendation 1 | recommendation 2 | comment |
|---|---|---|---|---|
| N.C. | 27, 28, 29, 38, 40, 41 | GND | | |
| N.C. | 10, 46 | open | GND | neighboring high-voltage pins |

## 27.3 Connection of unused pins

Table 16 shows recommendations how to connect pins, in case they are not needed by the application.

**Table 16 Recommendation for connecting unused pins**

| type | pin number | recommendation 1 (if unused) | recommendation 2 (if unused) |
|---|---|---|---|
| LIN | 1 | open | |
| HS1, HS2 | 3, 4 | VS | open |

### 28.2.3 PMU Core Supply Parameters VDDC

**Table 25 Electrical Characteristics**

$V_S$ = 5.5 V to 28 V, $T_j$ = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Required decoupling capacitance | $C_{VDDC1}$ | 0.1 | – | – | µF | [1] ESR < 1Ω | P_2.2.1 |
| Required buffer capacitance for stability (load jumps) | $C_{VDDC2}$ | 0.33 | – | 1 | µF | [2] – | P_2.2.2 |
| Output Voltage including line regulation @ Active Mode/Stop Mode | $V_{DDCOUT}$ | 1.44 | 1.5 | 1.56 | V | $I_{load}$ < 40mA; with setting of VDDC output voltage to 1.5V in Stop Mode | P_2.2.3 |
| Load Regulation | $V_{DDCLOR}$ | -50 | – | 50 | mV | 2 ... 40mA; C = $C_{VDDC1}$+$C_{VDDC2}$ | P_2.2.4 |
| Line Regulation | $V_{DDCLIR}$ | -25 | – | 25 | mV | $V_s$= 5.5 ... 28V | P_2.2.5 |
| Over Voltage Detection | $V_{DDCOV}$ | 1.58 | – | 1.68 | V | Overvoltage leads to SUPPLY_NMI | P_2.2.6 |
| Under Voltage Reset | $V_{DDVUV}$ | 1.10 | – | 1.19 | V | – | P_2.2.7 |
| Over Current Diagnostic | $I_{VDDCOC}$ | 40 | – | 80 | mA | – | P_2.2.8 |

1) only min. value is tested.

2) Not subject to production test, specified by design.

1) currents used in this table are positive but flowing out the pin VDDEXT
2) only min. value is tested.
3) Not subject to production test, specified by design.
4) When condition is met, the Bit VDDEXT_CTRL.VDDEXT_UV_IS will be set.

### 28.2.5 VPRE Voltage Regulator (PMU Subblock) Parameters

The PMU VPRE Regulator acts as a supply of VDDP and VDDC voltage regulators.

**Table 27 Functional Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Specified Output Current | $I_{VPRE}$ | – | – | 90 | mA | 1) | P_2.4.1 |

1) Not subject to production test, specified by design.

#### 28.2.5.1 Load Sharing of VPRE Regulator

The figure below shows the load sharing concept of VPRE regulator.

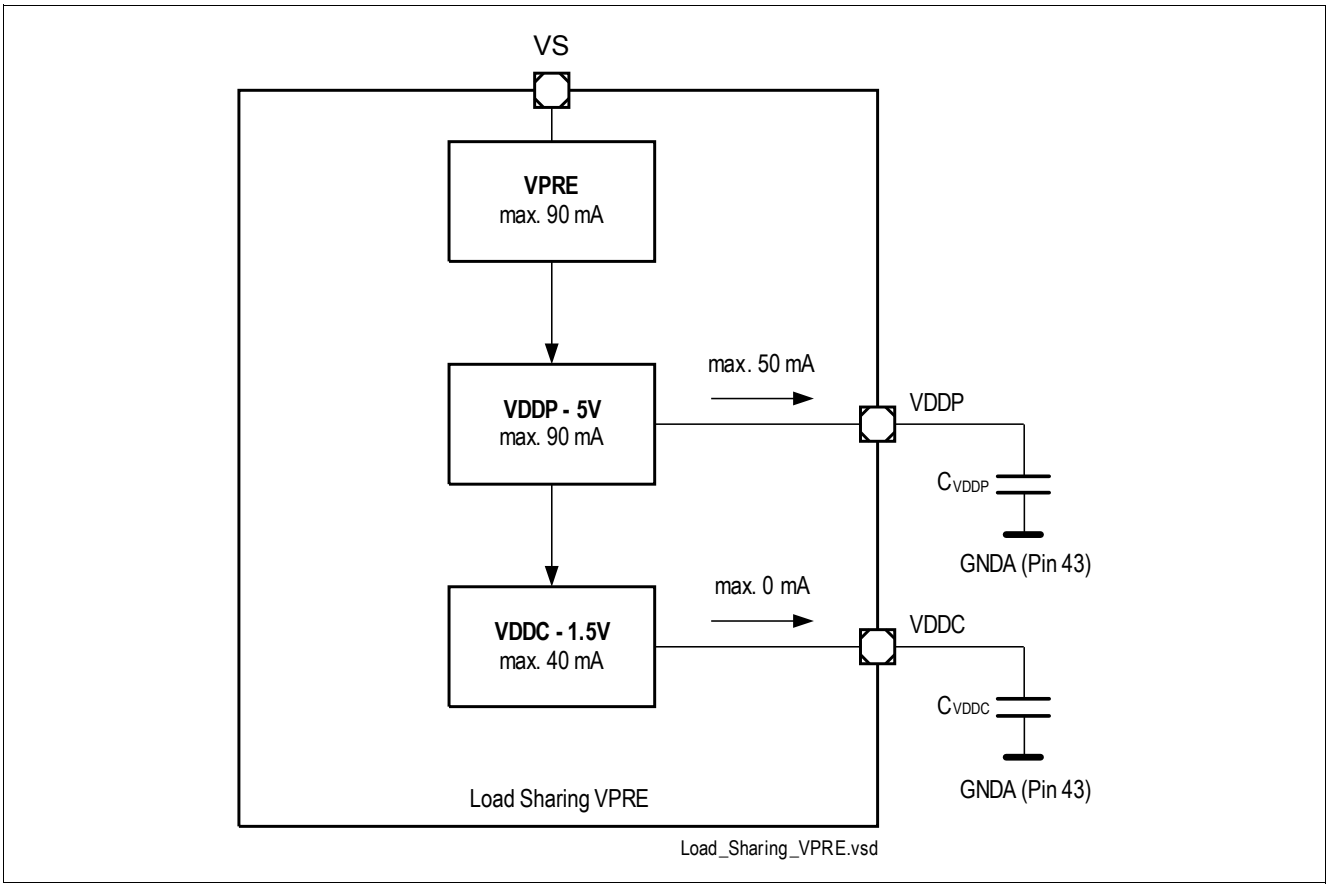


**Figure 36 Load Sharing of VPRE Regulator**

**Table 30 Functional Range** (cont'd)

$V_S$ = 5.5 V to 28 V, $T_j$ = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Low time | $t_{2\_PLLNM}$ | 12 | – | – | ns | [5)6)] – | P_3.2.11 |
| Rise time | $t_{3\_PLLNM}$ | – | 7 | 7 | ns | [5)6)] – | P_3.2.12 |
| Fall time | $t_{4\_PLLNM}$ | – | 7 | 7 | ns | [5)6)] – | P_3.2.13 |

1) Not subject to production test, specified by design.
2) Overload conditions must not occur on pin XTAL1.
3) The amplitude voltage $V_{AX1}$ refers to the offset voltage $V_{OFF}$. This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by $V_{IX1}$.
4) this performance is only valid for Prescaler Mode (VCO Bypass mode).
5) tested with rectangular signal with $V_{IN\_Low} = 0V$ to $V_{IN\_High} = V_{DDC}$
6) this performance is only valid for PLL Normal Mode.

1)Performance of pad drivers, A/D Converter, and Flash module depends on $V_{DDP}$.
If the external supply voltage $V_{DDP}$ becomes lower than the specified operating range, a power reset must be generated. Otherwise, the core supply voltage $V_{DDI}$ may rise above its specified operating range due to parasitic effects.
This power reset can be generated by the on-chip SWD. If the SWD is disabled the power reset must be generated by activating the $\overline{\text{PORST}}$ input

2) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: $V_{OV} > V_{IHmax}$ ($I_{OV} > 0$) or $V_{OV} < V_{ILmin}$ ($I_{OV} < 0$). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltages must remain within the specified limits. Proper operation under overload conditions depends on the application.
   Overload conditions must not occur on pin XTAL1 (powered by $V_{DDIM}$).
3) Not subject to production test, specified by design.
4) An overload current ($I_{OV}$) through a pin injects an error current ($I_{INJ}$) into the adjacent pins. This error current adds to that pin's leakage current ($I_{OZ}$). The value of the error current depends on the overload current and is defined by the overload coupling factor $K_{OV}$. The polarity of the injected error current is reversed from the polarity of the overload current that produces it.
   The total current through a pin is $|I_{TOT}| = |I_{OZ}| + (|I_{OV}| \times K_{OV})$. The additional error current may distort the input voltage on analog inputs.

**Table 38 Supply Voltage Signal Conditioning** (cont'd)

$V_S$ = 5.5 V to 28 V, $T_j$ = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Accuracy of $V_{MONx}$ sense after calibration | $\Delta V_{MONx}$ | -361 | – | 361 | mV | 2) $V_s$= 5.5V to 18V, $T_j$ = -40..125°C, $f_{ADCI} = f_{sys\_max}$. | P_8.1.37 |
| **ADC1 - Port 2.x Voltage Measurement $V_{2.x}$** | | | | | | | |
| Input to output voltage attenuation: VPort2.x | $ATT_{2.x}$ | – | 0.219 | – | | – | P_8.1.15 |
| Nominal operating input voltage range VPort2.x | $V_{Port2.x,range}$ | 0 | – | 5.53 1) | V | 2) Max. value corresponds to typ. ADC full scale input; | P_8.1.16 |
| Accuracy of $V_{Port2.x}$ sense after calibration - with IIR filter | $\Delta V_{Port2.x\_IIR}$ | -43 | – | 43 | mV | $V_s$= 5.5V to 18V, $T_j$ = -40..125°C, $f_{ADCI} = f_{sys\_max}$ ADC1_FILTCOEFF0_11. CHx = 11'b. | P_8.1.34 |
| Accuracy of $V_{Port2.x}$ sense after calibration | $\Delta V_{Port2.x}$ | -67 | – | 67 | mV | $V_s$= 5.5V to 18V, $T_j$ = -40..125°C, $f_{ADCI} = f_{sys\_max}$. | P_8.1.38 |
| **ADC2 - Supply Voltage Measurement $V_S$** | | | | | | | |
| Input to output voltage attenuation: $V_S$ | $ATT_{VS\_ADC2}$ | – | 0.039 | – | | | P_8.1.1 |
| Nominal operating input voltage range $V_S$ | $V_{S,ADC2}$ | 3 | – | 31.05 | V | 2) Max. value corresponds to typ. ADC full scale input; 3V < $V_S$ < 28V | P_8.1.2 |
| Accuracy of $V_S$ after calibration | $\Delta V_{S,ADC2}$ | -270 | – | 270 | mV | $V_s$= 5.5V to 18V, $T_j$ = -40..125°C | P_8.1.3 |
| **ADC2 - VDDEXT Voltage Measurement $V_{DDEXT}$** | | | | | | | |
| Input to output voltage attenuation: VDDEXT | $ATT_{VDDEXT}$ | – | 0.203 | – | | – | P_8.1.17 |
| Nominal operating input voltage range VDDEXT | $V_{DDEXT,range}$ | 0 | – | 5.96 | V | 2) Max. value corresponds to typ. ADC full scale input; | P_8.1.18 |
| **ADC2 - Pad Supply Voltage Measurement $V_{VDDP}$** | | | | | | | |
| Input-to-output voltage attenuation: VDDP | $ATT_{VDDP}$ | – | 0.203 | – | | – | P_8.1.4 |
| Nominal operating input voltage range VDDP | $V_{DDP,range}$ | 0 | – | 5.96 | V | 2) Max. value corresponds to typ. ADC full scale input; | P_8.1.5 |