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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

| Product Status             | Not For New Designs  |
|----------------------------|--|
| Core Processor             | R8C  |
| Core Size                  | 16-Bit   |
| Speed                      | 20MHz  |
| Connectivity               | UART/USART   |
| Peripherals                | POR, PWM, Voltage Detect, WDT  |
| Number of I/O              | 11   |
| Program Memory Size        | 2KB (2K x 8)   |
| Program Memory Type        | FLASH  |
| EEPROM Size                | -  |
| RAM Size                   | 256 x 8  |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V  |
| Data Converters            | A/D 5x10b  |
| Oscillator Type            | Internal   |
| Operating Temperature      | -20°C ~ 85°C (TA)  |
| Mounting Type              | Surface Mount  |
| Package / Case             | 14-TSSOP (0.173", 4.40mm Width)  |
| Supplier Device Package    | 14-TSSOP   |
| Purchase URL               | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2m110ansp-w4 |

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# 1.1.2 Differences between Groups

Table 1.1 lists the Specification Comparison between R8C/M11A Group and R8C/M12A Group. The explanations in 1.1.3 and subsequent sections apply to the R8C/M12A Group specifications only, unless otherwise specified.

| Item          | Function                           | R8C/M11A Group   | R8C/M12A Group   |
|---------------|------------------------------------|--|--|
| Interrupts    | External interrupt inputs          | 6 (INT × 3, key input × 3)   | 8 ( $\overline{INT} \times 4$ , key input $\times 4$ ) |
| I/O ports     | Number of pins                     | 14<br>Non-provided pins:<br>P1_0/AN0/TRCIOD/KI0<br>P3_3/IVCMP3/TRCCLK/INT3<br>P3_4/IVREF3/TRCIOC/INT2<br>P3_5/TRCIOD/KI2/VCOUT3<br>P4_2/TRB0/TXD0/KI3<br>P4_5/INT0/ADTRG | 20   |
|               | Number of CMOS I/O ports           | 11<br>Non-provided ports:<br>P1_0, P3_3, P3_4, P3_5, P4_2,<br>P4_5   | 17   |
|               | Number of high-current drive ports | 5<br>Non-provided ports:<br>P3_3, P3_4, P3_5   | 8  |
| A/D converter | Number of A/D channels             | 5 channels<br>Non-provided port: AN0   | 6 channels   |
| Comparator B  | Number of channels                 | Comparator B1  | Comparator B1, comparator B3                           |

 Table 1.1
 Specification Comparison between R8C/M11A Group and R8C/M12A Group



| Table 1.4 | Specifications | (2) |
|-----------|----------------|-----|
|-----------|----------------|-----|

| Item   | Function | Description  |  |
|--|----------|--|--|
| Flash memory                                 |          | <ul> <li>Program/erase voltage for program ROM: VCC = 1.8 V to 5.5 V</li> <li>Program/erase voltage for data flash: VCC = 1.8 V to 5.5 V</li> <li>Program/erase endurance: 10,000 times (data flash)<br/>10,000 times (program ROM)</li> <li>Program security: ID code check, protection enabled by lock bit</li> <li>Debug functions: On-chip debug, on-board flash rewrite function</li> </ul> |  |
| Operating frequency/<br>Power supply voltage |          | f(XIN) = 20 MHz (VCC = 2.7 V to 5.5 V)<br>f(XIN) = 5 MHz (VCC = 1.8 V to 5.5 V)  |  |
| Temperature range                            |          | -20 °C to 85 °C (N version)<br>-40 °C to 85 °C (D version) <sup>(1)</sup>  |  |
| Package                                      |          | 14-pin TSSOP: [Package code] PTSP0014JA-B<br>14-pin DIP: [Package code] PRDP0014AC-A<br>20-pin LSSOP: [Package code] PLSP0020JB-A<br>20-pin DIP: [Package code] PRDP0020AD-A   |  |

1. Specify the D version if it is to be used.



# 1.3 Block Diagram

Figure 1.2 shows the Block Diagram.



Figure 1.2 Block Diagram



#### 1.4 **Pin Assignment**

Figures 1.3 and 1.4 show Pin Assignment (Top View). Table 1.6 lists the Pin Name Information by Pin Number.



Figure 1.3 R8C/M11A Group Pin Assignment (Top View)





# 2. Central Processing Unit (CPU)

Figure 2.1 shows the 13 CPU Registers. The registers, R0, R1, R2, R3, A0, A1, and FB form a single register bank. The CPU has two register banks.







# 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 through R3. R0 can be split into high-order (R0H) and low-order (R0L) registers to be used separately as 8-bit data registers. The same applies to R1H and R1L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). In the same way as with R0 and R2, R3 and R1 can be used as a 32-bit data register (R3R1).

# 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 functions in the same manner as A0. A1 can be combined with A0 and used as a 32-bit address register (A1A0).

# 2.3 Frame Base Register (FB)

FB is a 16-bit register used for FB relative addressing.

# 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of a relocatable interrupt vector table.

# 2.5 Program Counter (PC)

PC is a 20-bit register that indicates the address of the next instruction to be executed.

# 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of the FLG register is used to switch between USP and ISP.

#### 2.7 Static Base Register (SB)

SB is a 16-bit register used for SB relative addressing.

# 2.8 Flag Register (FLG)

FLG is an 11-bit register that indicates the CPU state.

# 2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated in the arithmetic and logic unit.

# 2.8.2 Debug Flag (D)

The D flag is for debugging only. It must only be set to 0.

# 2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0. Otherwise it is set to 0.

# 2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value. Otherwise it is set to 0.

# 2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is 1.

# 2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow. Otherwise it is set to 0.



| Table 3.2 | SFR Information (2 | ) (1) |
|-----------|--------------------|-------|
|-----------|--------------------|-------|

| Address | Register Name   | Symbol | After Reset              |
|---------|---|--------|--------------------------|
| 0003Ah  | INT Input Filter Select Register 0                              | INTF0  | 00h                      |
| 0003Bh  |   |        |                          |
| 0003Ch  | INT Input Edge Select Register 0                                | ISCR0  | 00h                      |
| 0003Dh  |   |        |                          |
| 0003Eh  | Key Input Enable Register                                       | KIEN   | 00h                      |
| 0003Eh  | ····;   |        |                          |
| 00040h  | Interrupt Priority Level Register 0                             |        | 00h                      |
| 00040h  |   | 12720  | 6611                     |
| 0004111 | Interrupt Priority Loval Pagistar 2                             | 11/1.2 | 00b                      |
| 0004211 | Interrupt Priority Level Register 2                             |        | 00h                      |
| 000430  | Interrupt Priority Level Register 4                             |        | 001                      |
| 00044h  | Interrupt Priority Level Register 4                             |        | 000                      |
| 00045h  | Interrupt Priority Level Register 5                             | ILVL5  | 000                      |
| 00046h  | Interrupt Priority Level Register 6                             | ILVL6  | 00h                      |
| 00047h  | Interrupt Priority Level Register 7                             | ILVL7  | 00h                      |
| 00048h  | Interrupt Priority Level Register 8                             | ILVL8  | 00h                      |
| 00049h  | Interrupt Priority Level Register 9                             | ILVL9  | 00h                      |
| 0004Ah  | Interrupt Priority Level Register A                             | ILVLA  | 00h                      |
| 0004Bh  | Interrupt Priority Level Register B                             | ILVLB  | 00h                      |
| 0004Ch  | Interrupt Priority Level Register C                             | ILVLC  | 00h                      |
| 0004Dh  | Interrupt Priority Level Register D                             | ILVLD  | 00h                      |
| 0004Eh  | Interrupt Priority Level Register E                             | ILVLE  | 00h                      |
| 0004Fh  |   |        |                          |
| 00050h  | Interrupt Monitor Flag Register 0                               | IRR0   | 00h                      |
| 00051h  | Interrupt Monitor Flag Register 1                               | IRR1   | 00h                      |
| 00052h  | Interrupt Monitor Flag Register 2                               | IRR2   | 00h                      |
| 00053h  | External Interrupt Flag Register                                | IRR3   | 00h                      |
| 00054h  |   |        |                          |
| 00055h  |   |        |                          |
| 00056h  |   |        |                          |
| 00057h  |   |        |                          |
| 0005711 | Voltago Monitor Circuit Edgo Soloct Pogistor                    | VCAC   | 00b                      |
| 00050h  | Voltage Monitor Circuit Edge Select Register                    | VCAC   | 0011                     |
| 0005911 | Voltage Detect Register 2                                       | VCA2   | 004004001 (2)            |
| 0005AN  | Vollage Delect Register 2                                       | VCAZ   |                          |
|         |   |        | 00000100b <sup>(3)</sup> |
| 0005Bh  | Voltage Detection 1 Level Select Register                       | VD1LS  | 00000111b                |
| 0005Ch  | Voltage Monitor 0 Circuit Control Register                      | VW0C   | 1100X011b <sup>(2)</sup> |
|         |   |        | 1100X010b <sup>(3)</sup> |
| 0005Dh  | Voltage Monitor 1 Circuit Control Register                      | VW1C   | 10001010b                |
| 0005Eh  | 5   |        |                          |
| 0005Fh  | Reset Source Determination Register                             | RSTFR  | 0000XXXXb <sup>(4)</sup> |
| 00060h  | ······································                          |        |                          |
| 00061h  |   |        |                          |
| 00062h  |   |        |                          |
| 0006211 |   |        |                          |
| 000630  | Llich Speed On Chin Oppillator 10, 422 Mills Control Degister 0 | ED4000 | Volue when chinned       |
| 000055  | High-Speed On-Chip Oscillator 19,432 MHz Control Deviator 1     | ED1000 | Value when shipped       |
| 00065h  | righ-opeed On-Onip Oscillator 10.432 IVIHZ Control Register 1   | FR1001 | value when shipped       |
| 00066h  | Llick Speed On Chin Oppillator Control Devictor 4               |        | Value when shims of      |
| 00067h  | nigh-speed On-Onip Oscillator Control Register 1                |        | value when shipped       |
| 00068h  | nigh-speed On-Unip Oscillator Control Register 2                | FKV2   | value when shipped       |
| 00069h  |   |        |                          |
| 0006Ah  |   |        |                          |
| 0006Bh  |   |        |                          |
| 0006Ch  |   |        |                          |
| 0006Dh  |   |        |                          |
| 0006Eh  |   |        |                          |
| 0006Fh  |   |        |                          |
| 00070h  |   |        |                          |
| 00071h  |   |        |                          |
| 00072h  |   |        |                          |
| 00073h  |   |        |                          |
| 00074h  |   |        |                          |
| 00075h  |   |        |                          |
| 00076h  |   |        |                          |
| 00077h  |   |        |                          |
| 000786  |   |        |                          |
| 000701  |   | L      |                          |
| 0007911 |   |        |                          |

X: Undefined Notes:

1. The blank areas are reserved. No access is allowed.

2. The LVDAS bit in the OFS register is 0.

The LVDAS bit in the OFS register is 1.
 The value after a reset differs depending on the reset source.



| Address | Register Name                             | Symbol  | After Reset |
|---------|---|---------|-------------|
| 0007Ah  |   |         |             |
| 0007Bh  |   |         |             |
| 0007Ch  |   |         |             |
| 0007Dh  |   |         |             |
| 0007Eh  |   |         |             |
| 0007Eh  |   |         |             |
| 000806  | LIARTO Transmit/Receive Mode Register     | LIOMR   | 00b         |
| 000816  | UARTO Bit Poto Pogistor                   |         | XXb         |
| 0000111 | UADTO Dir Nale Register                   | LIOTRI  |             |
| 00082h  |   | UUTBL   |             |
| 00083h  |   | UUIBH   | XXN         |
| 00084h  | UARTU Transmit/Receive Control Register 0 | 0000    | 000010006   |
| 00085h  | UARTO Transmit/Receive Control Register 1 | U0C1    | 000000106   |
| 00086h  | UART0 Receive Buffer Register             | UORBL   | XXh         |
| 00087h  |   | UORBH   | XXh         |
| 00088h  | UART0 Interrupt Flag and Enable Register  | U0IR    | 00h         |
| 00089h  |   |         |             |
| 0008Ah  |   |         |             |
| 0008Bh  |   |         |             |
| 0008Ch  |   |         |             |
| 0008Dh  |   |         |             |
| 0008Eh  |   |         |             |
| 0008Fh  |   |         |             |
| 000906  |   |         |             |
| 00001h  |   | ł       | +           |
| 000911  |   |         |             |
| 000920  |   |         |             |
| 00093h  |   |         |             |
| 00094h  |   |         |             |
| 00095h  |   |         |             |
| 00096h  |   |         |             |
| 00097h  |   |         |             |
| 00098h  | A/D Register 0                            | AD0L    | XXh         |
| 00099h  |   | AD0H    | 000000XXb   |
| 0009Ah  | A/D Register 1                            | AD1L    | XXh         |
| 0009Bh  |   | AD1H    | 000000XXb   |
| 0009Ch  | A/D Mode Register                         | ADMOD   | 00h         |
| 0009Dh  | A/D Input Select Register                 | ADINSEL | 00h         |
| 0009Eh  | A/D Control Register 0                    | ADCON0  | 00h         |
| 0009Eh  | A/D Interrupt Control Status Register     | ADICSR  | 00h         |
| 00000h  |   | ABIOON  | 0011        |
| 000A01  |   |         |             |
| 000A11  |   |         |             |
| 000A2N  |   |         |             |
| 000A3h  |   |         |             |
| 000A4h  |   |         |             |
| 000A5h  |   |         |             |
| 000A6h  |   |         |             |
| 000A7h  |   |         |             |
| 000A8h  |   |         |             |
| 000A9h  | Port P1 Direction Register                | PD1     | 00h         |
| 000AAh  |   |         |             |
| 000ABh  | Port P3 Direction Register                | PD3     | 00h         |
| 000ACh  | Port P4 Direction Register                | PD4     | 00h         |
| 000ADh  | Port PA Direction Register                | PDA     | 00h         |
| 000AEh  |   | 1       | 1           |
| 000AFh  | Port P1 Register                          | P1      | 00h         |
| 000B0h  |   |         | **          |
| 000B0h  | Port P3 Register                          | D3      | 00b         |
| 000825  | Port P4 Register                          | P4      | 00b         |
| 000B2H  | Port DA Register                          | DA      | 00h         |
| 000830  | I ULLA NEGISIEI                           | 17      | 0011        |
| UUUB4h  | Dull Lin Control Degister 4               |         | 006         |
| 000B5h  |   | FURI    | UUN         |
| 000B6h  |   | DUDA    |             |
| 000B7h  | Pull-Up Control Register 3                | PUR3    | 00h         |
| 000B8h  | Pull-Up Control Register 4                | PUR4    | 00h         |
| 000B9h  | Port I/O Function Control Register        | PINSR   | 00h         |
| 000BAh  |   |         |             |
| 000BBh  | Drive Capacity Control Register 1         | DRR1    | 00h         |
| 000BCh  |   |         |             |
| 000BDh  | Drive Capacity Control Register 3         | DRR3    | 00h         |
| 000BFh  |   | 1       | 1           |
| 000BFh  |   | 1       | 1           |
|         |   |         |             |

# Table 3.3SFR Information (3) (1)

X: Undefined Note:

1. The blank areas are reserved. No access is allowed.



| Table 3.4 | SFR Information | (4) (1) |
|-----------|-----------------|---------|
|-----------|-----------------|---------|

| Address | Register Name   | Symbol  | After Reset |
|---------|---|---------|-------------|
| 000C0h  |   |         |             |
| 000C1h  | Open-Drain Control Register 1                                     | POD1    | 00h         |
| 000C2h  |   |         |             |
| 000C3h  | Open-Drain Control Register 3                                     | POD3    | 00h         |
| 000C4h  | Open-Drain Control Register 4                                     | POD4    | 00h         |
| 000C5h  | Port PA Mode Control Register                                     | PAMCR   | 00010001b   |
| 000C6h  |   |         |             |
| 000C7h  |   |         |             |
| 000C8h  | Port 1 Function Mapping Register 0                                | PML1    | 00h         |
| 000C9h  | Port 1 Function Mapping Register 1                                | PMH1    | 00h         |
| 000CAh  |   |         |             |
| 000CBh  |   |         |             |
| 000CCh  | Port 3 Function Mapping Register 0                                | PML3    | 00h         |
| 000CDh  | Port 3 Function Mapping Register 1                                | PMH3    | 00h         |
| 000CEh  | Port 4 Function Mapping Register 0                                | PML4    | 00h         |
| 000CFh  | Port 4 Function Mapping Register 1                                | PMH4    | 00h         |
| 000D0h  |   |         |             |
| 000D1h  | Port 1 Function Mapping Expansion Register                        | PMH1E   | 00h         |
| 000D2h  |   |         |             |
| 000D3h  |   |         |             |
| 000D4h  |   |         |             |
| 000D5h  | Port 4 Function Mapping Expansion Register                        | PMH4E   | 00h         |
| 000D6h  |   |         |             |
| 000D7h  |   |         |             |
| 000D8h  | Timer RJ Counter Register   | TRJ     | FFh         |
| 000D9h  |   |         | FFh         |
| 000DAh  | Timer RJ Control Register   | TRJCR   | 00h         |
| 000DBh  | Timer RJ I/O Control Register                                     | TRJIOC  | 00h         |
| 000DCh  | Timer RJ Mode Register  | TRJMR   | 00h         |
| 000DDh  | Timer RJ Event Select Register                                    | TRJISR  | 00h         |
| 000DEh  | Timer RJ Interrupt Control Register                               | TRJIR   | 00h         |
| 000DFh  |   |         |             |
| 000E0h  | Timer RB Control Register   | TRBCR   | 00h         |
| 000E1h  | Timer RB One-Shot Control Register                                | TRBOCR  | 00h         |
| 000E2h  | Timer RB I/O Control Register                                     | TRBIOC  | 00h         |
| 000E3h  | Timer RB Mode Register  | TRBMR   | 00h         |
| 000E4h  | Timer RB Prescaler Register <sup>(2)</sup>                        | TRBPRE  | FFN         |
|         | Timer RB Primary/Secondary Register (Lower 8 Bits) <sup>(3)</sup> |         |             |
| 000E5h  | Timer RB Primary Register <sup>(2)</sup>                          | TRBPR   | FFh         |
|         | Timer RB Primary Register (Higher 8 Bits) <sup>(3)</sup>          |         |             |
| 000E6h  | Timer RB Secondary Register (2)                                   | TRBSC   | FFh         |
|         | Timer RB Secondary Register (Higher 8 Bits) (3)                   |         |             |
| 000E7h  | Timer RB Interrupt Control Register                               | TRBIR   | 00h         |
| 000E8h  | Timer RC Counter  | TRCCNT  | 00h         |
| 000E9h  |   |         | 00h         |
| 000EAh  | Timer RC General Register A                                       | TRCGRA  | FFh         |
| 000EBh  | -   |         | FFh         |
| 000ECh  | Timer RC General Register B                                       | TRCGRB  | FFh         |
| 000EDh  | -   |         | FFh         |
| 000EEh  | Timer RC General Register C                                       | TRCGRC  | FFh         |
| 000EFh  |   |         | FFh         |
| 000F0h  | Timer RC General Register D                                       | TRCGRD  | FFh         |
| 000F1h  |   |         | FFh         |
| 000F2h  | Timer RC Mode Register  | TRCMR   | 01001000b   |
| 000F3h  | Timer RC Control Register 1                                       | TRCCR1  | 00h         |
| 000F4h  | Timer RC Interrupt Enable Register                                | TRCIER  | 01110000b   |
| 000F5h  | Timer RC Status Register  | TRCSR   | 01110000b   |
| 000F6h  | Timer RC I/O Control Register 0                                   | TRCIOR0 | 10001000b   |
| 000F7h  | Timer RC I/O Control Register 1                                   | TRCIOR1 | 10001000b   |
| 000F8h  | Timer RC Control Register 2                                       | TRCCR2  | 00011000b   |
| 000F9h  | Timer RC Digital Filter Function Select Register                  | TRCDF   | 00h         |
| 000FAh  | Timer RC Output Enable Register                                   | TRCOER  | 01111111b   |
| 000FBh  | Timer RC A/D Conversion Trigger Control Register                  | TRCADCR | 11110000b   |
| 000FCh  | Timer RC Waveform Output Manipulation Register                    | TRCOPR  | 00h         |
| 000FDh  |   |         |             |
| 000FEh  |   |         |             |
| 000FFh  |   |         |             |

The blank areas are reserved. No access is allowed.
 The TCNT16 bit in the TRBMR register is 0.
 The TCNT16 bit in the TRBMR register is 1.



| Address | Register Name                            | Symbol   | After Reset |
|---------|--|----------|-------------|
| 00180h  | Comparator B Control Register            | WCMPR    | 00h         |
| 00181h  | Comparator B1 Interrupt Control Register | WCB1INTR | 00h         |
| 00182h  | Comparator B3 Interrupt Control Register | WCB3INTR | 00h         |
| 00183h  |  |          |             |
| 00184h  |  |          |             |
| 00185h  |  |          |             |
| 00186h  |  |          |             |
| 001001  |  |          |             |
| 0018711 |  |          |             |
| 00188h  |  |          |             |
| 00189h  |  |          |             |
| 0018Ah  |  |          |             |
| 0018Bh  |  |          |             |
| 0018Ch  |  |          |             |
| 0018Dh  |  |          |             |
| 0018Eh  |  |          |             |
| 0018Fh  |  |          |             |
| 00190h  |  |          |             |
| 00191h  |  |          |             |
| 00192h  |  |          |             |
| 00193h  |  |          |             |
| 00194h  |  |          |             |
| 00195h  |  |          |             |
| 00196h  |  |          |             |
| 00197h  |  |          |             |
| 00198h  |  |          |             |
| 00199h  |  |          |             |
| 0019Ah  |  |          |             |
| 0019Bb  |  |          |             |
| 0019Dh  |  |          |             |
| 0019Ch  |  |          |             |
| 0019Dh  |  |          |             |
| 0019Eh  |  |          |             |
| 001911  |  |          |             |
| 001A01  |  |          |             |
| 00140h  |  |          |             |
| 001A2h  |  |          |             |
| 001A30  |  |          |             |
| 001A4n  |  |          |             |
| 001A5h  |  |          |             |
| 001A6h  |  |          |             |
| 001A7h  |  |          |             |
| 001A8h  |  |          | -           |
| 001A9h  | Flash Memory Status Register             | FST      | 1000000b    |
| 001AAh  | Flash Memory Control Register 0          | FMR0     | 00h         |
| 001ABh  | Flash Memory Control Register 1          | FMR1     | 00h         |
| 001ACh  | Flash Memory Control Register 2          | FMR2     | 00h         |
| 001ADh  | Flash Memory Refresh Control Register    | FREFR    | 00h         |
| 001AEh  |  |          |             |
| 001AFh  |  |          |             |
| 001B0h  |  |          |             |
| 001B1h  |  |          |             |
| 001B2h  |  |          |             |
| 001B3h  |  |          |             |
| 001B4h  |  |          |             |
| 001B5h  |  |          |             |
| 001B6h  |  |          |             |
| 001B7h  |  |          |             |
| 001B8h  |  |          |             |
| 001806  |  |          |             |
| 001251  |  |          |             |
| 001DAII |  |          |             |
|         |  |          |             |
| 001BCh  |  |          |             |
|         |  |          |             |
| UU1BEh  |  |          |             |
| 001BFh  |  |          |             |

Table 3.7SFR Information (7) (1)

1. The blank areas are reserved. No access is allowed.



| Symbol        | Parameter  | Condition   |                       | Standard |      |      | 1.1.4.14 |
|---------------|--|---|-----------------------|----------|------|------|----------|
|               |  |   | Condition             |          | Тур. | Max. | Unit     |
|               | Resolution   |   |                       |          | —    | 10   | Bit      |
|               | Absolute accuracy  | AVcc = 5.0 V  | AN0 to AN4, AN7 input | —        | —    | ±3   | LSB      |
|               |  | AVcc = 3.0 V  | AN0 to AN4, AN7 input | _        | —    | ±5   | LSB      |
|               |  | AVcc = 1.8 V  | AN0 to AN4, AN7 input | _        | —    | ±5   | LSB      |
| —             | A/D conversion clock   | $4.0 \text{ V} \le \text{AVcc} \le 5.5 \text{ V}^{(2)}$ |                       | 2        | —    | 20   | MHz      |
|               |  | $3.2 V \le AVcc \le 3$                                  | 5.5 V <sup>(2)</sup>  | 2        | —    | 16   | MHz      |
|               | $\begin{array}{l} 2.7 \ V \leq AVcc \leq 5.5 \ V \ ^{(2)} \\ \hline 1.8 \ V \leq AVcc \leq 5.5 \ V \ ^{(2)} \end{array}$ |   | 2                     | _        | 10   | MHz  |          |
|               |  |   | 2                     | —        | 5    | MHz  |          |
|               | Permissible signal source impedance  |   |                       |          | 3    |      | kΩ       |
| tCONV         | Conversion time  | AVcc = 5.0 V, A/D conversion clock = 20 MHz             |                       | 2.20     | _    | _    | μs       |
| <b>t</b> SAMP | Sampling time  | A/D conversion clock = 20 MHz                           |                       | 0.80     | —    | —    | μs       |
| Via           | Analog input voltage   |   |                       | 0        | —    | AVcc | V        |

 Table 4.3
 A/D Converter Characteristics

1. Vcc/AVcc = 1.8 V to 5.5 V and Vss = 0 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.

2. The A/D conversion result will be undefined in stop mode, or when the flash memory is in low-current-consumption read mode or stopped. Do not perform A/D conversion in these states. Do not enter these states during A/D conversion.

#### Table 4.4 Comparator B Electrical Characteristics

| Symbol | Parameter                              | Condition          | Standard |      |           | Lloit |
|--------|--|--------------------|----------|------|-----------|-------|
|        |  |                    | Min.     | Тур. | Max.      | Onit  |
| Vref   | IVREF1, IVREF3 input reference voltage |                    | 0        | _    | Vcc - 1.4 | V     |
| VI     | IVCMP1, IVCMP3 input voltage           |                    | -0.3     | _    | Vcc + 0.3 | V     |
| —      | Offset                                 |                    | _        | 5    | 100       | mV    |
| td     | Comparator output delay time (2)       | VI = Vref ± 100 mV | -        | 0.1  | —         | μS    |
| ICMP   | Comparator operating current           | Vcc = 5.0 V        | _        | 17.5 | —         | μA    |

Notes:

1. Vcc = 2.7 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.

2. When the digital filter is disabled.



| Symbol              | Parameter  | Condition                   | 1          | Llnit |                                |       |
|---------------------|--|-----------------------------|------------|-------|--------------------------------|-------|
| Symbol              | Falameter  | Condition                   | Min.       | Тур.  | Max.                           | Unit  |
|                     | Program/erase endurance (2)  |                             | 10,000 (3) |       |                                | times |
| —                   | Byte programming time (program/erase endurance $\leq$ 1,000 times)     |                             |            | 80    | —                              | μs    |
|                     | Byte programming time<br>(program/erase endurance > 1,000<br>times)    |                             | _          | 160   | _                              | μS    |
|                     | Block erase time   |                             |            | 0.12  |                                | S     |
| td(SR-SUS)          | Transition time to suspend   |                             | _          |       | 0.25 + CPU clock<br>× 3 cycles | ms    |
| —                   | Time from suspend until erase restart                                  |                             | -          |       | 30 + CPU clock<br>× 1 cycle    | μS    |
| td(CMDRST<br>READY) | Time from when command is forcibly terminated until reading is enabled |                             | -          |       | 30 + CPU clock<br>× 1 cycle    | μS    |
| _                   | Program/erase voltage  |                             | 1.8        |       | 5.5                            | V     |
| _                   | Read voltage   |                             | 1.8        |       | 5.5                            | V     |
| _                   | Program/erase temperature  |                             | 0          |       | 60                             | °C    |
| —                   | Data hold time (7)   | Ambient temperature = 85 °C | 10         |       | _                              | years |

Table 4.5 Flash Memory (Program ROM) Electrical Characteristics

1. Vcc = 2.7 V to 5.5 V and Topr = 0 °C to 60 °C, unless otherwise specified.

2. Definition of program/erase endurance

The number of program/erase cycles is defined on a per-block basis.

If the number of cycles is 10,000, each block can be erased 10,000 times.

For example, if 1,024 cycles of 1-byte-write are performed to different addresses in 1 Kbyte of block A, and then the block is erased, the number of cycles is counted as one. Note, however, that the same address must not be programmed more than once before completion of an erase (overwriting prohibited).

3. This indicates the number of times up to which all electrical characteristics can be guaranteed after the last programming/ erase operation. Operation is guaranteed for any number of operations in the range of 1 to the specified minimum (Min).

4. In a system that executes multiple programming operations, the actual erase count can be reduced by shifting the write addresses in sequence and programming so that as much of the flash memory as possible is used before performing an erase operation. For example, when programming in 16-byte units, the effective number of rewrites can be minimized by programming up to 128 units before erasing them all in one operation. It is also advisable to retain data on the number of erase operations for each block and establish a limit for the number of erase operations performed.

5. If an error occurs during a block erase, execute a clear status register command and then a block erase command at least three times until the erase error does not occur.

6. For information on the program/erase failure rate, contact a Renesas technical support representative.

7. The data hold time includes the time that the power supply is off and the time the clock is not supplied.



| Symbol  | Beremeter   | Condition   |      |      | Lloit |      |
|---------|---|---|------|------|-------|------|
| Symbol  | Falameter   | Condition   | Min. | Тур. | Max.  | Unit |
| Vdet0   | Voltage detection level Vdet0_0 <sup>(2)</sup>                            |   | 1.80 | 1.90 | 2.05  | V    |
|         | Voltage detection level Vdet0_1 <sup>(2)</sup>                            |   | 2.15 | 2.35 | 2.50  | V    |
|         | Voltage detection level Vdet0_2 (2)                                       |   | 2.70 | 2.85 | 3.05  | V    |
|         | Voltage detection level Vdet0_3 (2)                                       |   | 3.55 | 3.80 | 4.05  | V    |
| —       | Voltage detection 0 circuit response time <sup>(3)</sup>                  | When Vcc decreases from 5 V<br>to (Vdet0_0 - 0.1) V | _    | 30   | _     | μS   |
| —       | Self power consumption in voltage detection circuit                       | VC0E = 1, Vcc = 5.0 V                               | _    | 1.5  | _     | μΑ   |
| td(E-A) | Wait time until voltage detection circuit operation starts <sup>(4)</sup> |   | _    | —    | 100   | μS   |

 Table 4.7
 Voltage Detection 0 Circuit Electrical Characteristics

1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version).

2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.

3. The response time is from when the voltage passes Vdet0 until the voltage monitor 0 reset is generated.

4. The wait time is necessary for the voltage detection circuit to operate when the VC0E bit in the VCA2 register is set to 0 and then 1.

| Table 4.8 | Voltage Detection | 1 Circuit | Electrical | Characteristics |
|-----------|-------------------|-----------|------------|-----------------|
|           |                   |           |            | •               |

| Symbol  | Doromotor   | Condition  |      | Linit |      |      |
|---------|---|--|------|-------|------|------|
| Symbol  | Faranielei  | Condition  | Min. | Тур.  | Max. | Onit |
| Vdet1   | Voltage detection level Vdet1_1 <sup>(2)</sup>                            | When Vcc decreases                               | 2.15 | 2.35  | 2.55 | V    |
|         | Voltage detection level Vdet1_3 <sup>(2)</sup>                            | When Vcc decreases                               | 2.45 | 2.65  | 2.85 | V    |
|         | Voltage detection level Vdet1_5 <sup>(2)</sup>                            | When Vcc decreases                               | 2.75 | 2.95  | 3.15 | V    |
|         | Voltage detection level Vdet1_7 <sup>(2)</sup>                            | When Vcc decreases                               | 3.00 | 3.25  | 3.55 | V    |
|         | Voltage detection level Vdet1_9 <sup>(2)</sup>                            | When Vcc decreases                               | 3.30 | 3.55  | 3.85 | V    |
|         | Voltage detection level Vdet1_B (2)                                       | When Vcc decreases                               | 3.60 | 3.85  | 4.15 | V    |
|         | Voltage detection level Vdet1_D (2)                                       | When Vcc decreases                               | 3.90 | 4.15  | 4.45 | V    |
|         | Voltage detection level Vdet1_F (2)                                       | When Vcc decreases                               | 4.20 | 4.45  | 4.75 | V    |
| —       | Hysteresis width at the rising of Vcc in                                  | Vdet1_1 to Vdet1_5 selected                      |      | 0.07  | —    | V    |
|         | voltage detection 1 circuit   | Vdet1_7 to Vdet1_F selected                      |      | 0.10  | _    | V    |
| —       | Voltage detection 1 circuit response time <sup>(3)</sup>                  | When Vcc decreases from 5 V to (Vdet1_0 - 0.1) V | _    | 60    | 150  | μS   |
| -       | Self power consumption in voltage detection circuit                       | VC1E = 1, Vcc = 5.0 V                            | _    | 1.7   | —    | μΑ   |
| td(E-A) | Wait time until voltage detection circuit operation starts <sup>(4)</sup> |  | —    | —     | 100  | μS   |

Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version).

2. Select the voltage detection level with bits VD1S1 to VD1S3 in the VD1LS register.

3. The response time is from when the voltage passes Vdet1 until the voltage monitor 1 interrupt request is generated.

4. The wait time is necessary for the voltage detection circuit to operate when the VC1E bit in the VCA2 register is set to 0 and then 1.



| Symbol | Boromotor                                | Dookogo      | Condition                       |        | Standard |        | Unit |
|--------|--|--------------|---------------------------------|--------|----------|--------|------|
| Symbol | Farameter                                | гаскауе      | Condition                       | Min.   | Тур.     | Max.   | Unit |
| —      | High-speed on-chip oscillator            | 14-pin TSSOP | Vcc = 1.8 V to 5.5 V,           | 19.2   | 20.0     | 20.8   | MHz  |
|        | frequency after reset is                 | 20-pin LSSOP | -20 °C ≤ Topr ≤ 85 °C           |        |          |        |      |
|        | cleared                                  | 14-pin DIP   |                                 | 19.0   | 20.0     | 21.0   | MHz  |
|        |  | 20-pin DIP   |                                 |        |          |        |      |
|        |  | 14-pin TSSOP | Vcc = 1.8 V to 5.5 V,           | 19.0   | 20.0     | 21.0   | MHz  |
|        |  | 20-pin LSSOP | -40 °C $\leq$ Topr $\leq$ 85 °C |        |          |        |      |
|        | High-speed on-chip oscillator            | 14-pin TSSOP | Vcc = 1.8 V to 5.5 V,           | 17.694 | 18.432   | 19.169 | MHz  |
|        | frequency when the FR18S0                | 20-pin LSSOP | -20 °C $\leq$ Topr $\leq$ 85 °C |        |          |        |      |
|        | register adjustment value is             | 14-pin DIP   |                                 | 17.510 | 18.432   | 19.353 | MHz  |
|        | written into the FRV1 register           | 20-pin DIP   |                                 |        |          |        |      |
|        | and the FR18S1 register                  | 14-pin TSSOP | Vcc = 1.8 V to 5.5 V,           | 17.510 | 18.432   | 19.353 | MHz  |
|        | adjustment value into the                | 20-pin LSSOP | -40 °C $\leq$ Topr $\leq$ 85 °C |        |          |        |      |
|        | FRV2 register (2)                        |              |                                 |        |          |        |      |
| -      | Oscillation stabilization time           | —            |                                 | _      | _        | 30     | μS   |
| _      | Self power consumption at<br>oscillation | _            | Vcc = 5.0 V, Topr = 25 °C       | _      | 530      |        | μĀ   |

| Table 4.10 | High-Speed On-Chi | o Oscillator Circuit | Electrical Characteristics |
|------------|-------------------|----------------------|----------------------------|
|            |                   |                      |                            |

1. Vcc = 1.8 V to 5.5 V, Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.

2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0 % when the serial interface is used in UART mode.

#### Table 4.11 Low-Speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Baramator                              | Condition                           |      | Linit |      |      |
|--------|--|-------------------------------------|------|-------|------|------|
| Symbol | Falanetei                              | Condition                           | Min. | Тур.  | Max. | Onit |
| fLOCO  | Low-speed on-chip oscillator frequency |                                     | 60   | 125   | 250  | kHz  |
| —      | Oscillation stabilization time         |                                     | —    | —     | 35   | μS   |
| —      | Self power consumption at oscillation  | Vcc = 5.0 V, Topr = 25 $^{\circ}$ C | —    | 2     |      | μΑ   |
|        |  |                                     |      |       |      |      |

Note:

1. Vcc = 1.8 V to 5.5 V, Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.

#### Table 4.12 Power Supply Circuit Timing Characteristics

| Symbol  | Peremeter   | Condition |      | Linit |       |      |
|---------|---|-----------|------|-------|-------|------|
| Symbol  | Falametei   | Condition | Min. | Тур.  | Max.  | Unit |
| td(P-R) | Time for internal power supply stabilization during power-on <sup>(2)</sup> |           |      |       | 2,000 | μS   |

Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = 25 °C.

2. Wait time until the internal power supply generation circuit stabilizes during power-on.



| Symbol  | D                   | Condition   |  | S           | Unit      |      |      |      |
|---------|---------------------|---|--|-------------|-----------|------|------|------|
| Symbol  |                     |   | Cond                                     |             | Min.      | Тур. | Max. | Onit |
| Vон     | Output high voltage | P1_2, P1_3, P1_4, P1_5,<br>P3_3, P3_4, P3_5, P3_7 <sup>(2)</sup>  | When drive IOH = -20 mA capacity is high |             | Vcc - 2.0 | —    | Vcc  | V    |
|         |                     |   | When drive<br>capacity is low            | Іон = -5 mA | Vcc - 2.0 | _    | Vcc  | V    |
|         |                     | P1_0, P1_1, P1_6, P1_7,<br>P4_2, P4_5, P4_6, P4_7,<br>PA_0  |  | юн = -5 mA  | Vcc - 2.0 | _    | Vcc  | V    |
| Vol     | Output low voltage  | P1_2, P1_3, P1_4, P1_5,<br>P3_3, P3_4, P3_5, P3_7 <sup>(2)</sup>  | When drive<br>capacity is high           | IoL = 20 mA | _         | _    | 2.0  | V    |
|         |                     |   | When drive<br>capacity is low            | IOL = 5 mA  |           | —    | 2.0  | V    |
|         |                     | P1_0, P1_1, P1_6, P1_7,<br>P4_2, P4_5, P4_6, P4_7,<br>PA_0  |  | Iol = 5 mA  |           | _    | 2.0  | V    |
| VT+-VT- | Hysteresis          | INT0, INT1, INT2, INT3,<br>KI0, KI1, KI2, KI3,<br>TRJIO, TRCIOA, TRCIOB,<br>TRCIOC, TRCIOD,<br>RXD0, CLK0 | Vcc = 5 V                                |             | 0.1       | 1.2  | _    | V    |
|         |                     | RESET   | Vcc = 5 V                                |             | 0.1       | 1.2  |      | V    |
| Ін      | Input high current  |   | VI = 5 V, Vcc = 5.0 V                    |             | —         | _    | 5.0  | μA   |
| lı∟     | Input low current   |   | VI = 0 V, $Vcc = 5$                      | 5.0 V       | —         | —    | -5.0 | μA   |
| RPULLUP | Pull-up resistance  |   | VI = 0 V, $Vcc = 5$                      | 5.0 V       | 25        | 50   | 100  | kΩ   |
| RfXIN   | Feedback resistance | XIN   |  |             | —         | 2.2  | —    | MΩ   |
| VRAM    | RAM hold voltage    |   | In stop mode                             |             | 1.8       | —    | —    | V    |

Table 4.13 DC Characteristics (1) [4.0 V  $\leq$  Vcc  $\leq$  5.5 V]

1. 4.0 V ≤ Vcc ≤ 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), f(XIN) = 20 MHz, unless otherwise specified.

2. High drive capacity can also be used while the peripheral output function is used.



#### Timing Requirements (Vcc = 5 V, Vss = 0 V at Topr = 25 °C, unless otherwise specified)

#### Table 4.15 External Clock Input (XIN)

| Symbol   | Parameter            |      | Standard |      |  |
|----------|----------------------|------|----------|------|--|
|          | Falameter            | Min. | Max.     | Unit |  |
| tc(XIN)  | XIN input cycle time | 50   |          | ns   |  |
| twh(xin) | XIN input high width | 24   | _        | ns   |  |
| twl(XIN) | XIN input low width  | 24   | _        | ns   |  |



#### Figure 4.4 External Clock Input Timing When Vcc = 5 V

#### Table 4.16 TRJIO Input

| Symbol     | Daramatar              | Stan | Unit |      |
|------------|------------------------|------|------|------|
|            | Falanelei              | Min. | Max. | Unit |
| tc(TRJIO)  | TRJIO input cycle time | 100  | _    | ns   |
| twh(trjio) | TRJIO input high width | 40   | _    | ns   |
| twl(trjio) | TRJIO input low width  | 40   | _    | ns   |



Figure 4.5 TRJIO Input Timing When Vcc = 5 V



# Table 4.26 DC Characteristics (6) [1.8 V $\leq$ Vcc < 2.7 V] (Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified)

|        |   |  | Condition              |                      |               |                   |                                  |   |      |   |  |      |     |    |
|--------|---|--|------------------------|----------------------|---------------|-------------------|----------------------------------|---|------|---|--|------|-----|----|
| Symbol | Parameter                                     |  | Oscillation<br>Circuit | On-Chip C            | Scillator     | CPU               | Low-Power-                       | Other   |      | Standard                                      |  | Unit |     |    |
|        |   |  | XIN (2)                | High-<br>Speed       | Low-<br>Speed | Clock             | Setting                          | Other   | Min. | Тур. <sup>(3)</sup>                           | Max.   |      |     |    |
| lcc    | Power<br>supply                               | High-speed<br>clock mode                   | 5 MHz                  | Off                  | 125 kHz       | No<br>division    | —                                |   | -    | 1.0   | _  | mA   |     |    |
|        | current (1)                                   |  | 5 MHz                  | Off                  | 125 kHz       | Division<br>by 8  | —                                |   | —    | 0.6   | _  | mA   |     |    |
|        |   | High-speed<br>on-chip                      | Off                    | 5 MHz <sup>(4)</sup> | 125 kHz       | No<br>division    |                                  |   | —    | 1.6   | 6.5  | mA   |     |    |
|        | oscil<br>mod<br>on-ci<br>oscil<br>mod<br>Wait | oscillator<br>mode                         | Off                    | 5 MHz <sup>(4)</sup> | 125 kHz       | Division<br>by 8  |                                  |   | —    | 1.1   | _  | mA   |     |    |
|        |   |  | Off                    | 4 MHz <sup>(4)</sup> | 125 kHz       | Division<br>by 16 | MSTTRC = 1                       |   | —    | 1.0   | _  | mA   |     |    |
|        |   | Low-speed<br>on-chip<br>oscillator<br>mode | Off                    | Off                  | 125 kHz       | Division<br>by 8  | FMR27 = 1<br>LPE = 0             |   | _    | 60  | 200  | μΑ   |     |    |
|        |   | Wait mode                                  | Off                    | Off                  | 125 kHz       | _                 | VC1E = 0<br>VC0E = 0<br>LPE = 1  | Peripheral<br>clock supplied<br>during WAIT<br>instruction<br>execution | —    | 15  | 90   | μΑ   |     |    |
|        |   |  |                        |                      |               | Off               | Off                              | 125 kHz   | _    | VC1E = 0<br>VC0E = 0<br>LPE = 1<br>WCKSTP = 1 | Peripheral<br>clock stopped<br>during WAIT<br>instruction<br>execution | —    | 4.0 | 80 |
|        |   | Stop mode                                  | Off                    | Off                  | Off           | —                 | VC1E = 0<br>VC0E = 0<br>STPM = 1 | Topr = 25 °C<br>Peripheral<br>clock stopped                             | -    | 1.0   | 4.0  | μΑ   |     |    |
|        |   |  | Off                    | Off                  | Off           | _                 | VC1E = 0<br>VC0E = 0<br>STPM = 1 | Topr = 85 °C<br>Peripheral<br>clock stopped                             | —    | 1.5   | —  | μΑ   |     |    |

Notes:

1. Vcc = 1.8 V to 2.7 V, single-chip mode, output pins are open, and other pins are connected to Vss.

2. When the XIN input is a square wave.

3. Vcc = 2.2 V

4. Set the system clock to 5 MHz or 4 MHz with the PHISEL register.



#### Timing Requirements (Vcc = 2.2 V, Vss = 0 V at Topr = 25 °C, unless otherwise specified)

#### Table 4.27 External Clock Input (XIN)

| Symbol   | Parameter            | Standard |      | Lloit |
|----------|----------------------|----------|------|-------|
|          |                      | Min.     | Max. | Offic |
| tc(XIN)  | XIN input cycle time | 200      |      | ns    |
| twh(xin) | XIN input high width | 90       | _    | ns    |
| twl(XIN) | XIN input low width  | 90       | _    | ns    |



#### Figure 4.12 External Clock Input Timing When Vcc = 2.2 V

#### Table 4.28 TRJIO Input

| Symbol     | Parameter              | Standard |      | Linit |
|------------|------------------------|----------|------|-------|
|            |                        | Min.     | Max. | Offic |
| tc(TRJIO)  | TRJIO input cycle time | 500      | _    | ns    |
| twh(trjio) | TRJIO input high width | 200      | _    | ns    |
| twl(trjio) | TRJIO input low width  | 200      | _    | ns    |



Figure 4.13 TRJIO Input Timing When Vcc = 2.2 V









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