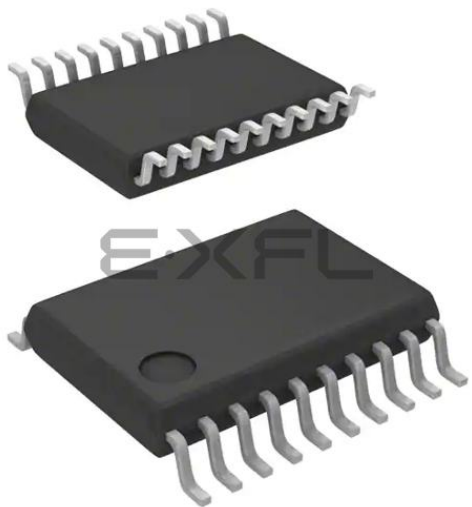




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	17
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2m120adsp-w4

Table 1.2 lists the R8C/M11A Group Register Settings. These settings correspond to the specification differences between the R8C/M11A Group and R8C/M12A Group.

Table 1.2 R8C/M11A Group Register Settings

Related Function	Register Name	Address	Bit	Setting Method for Access
INT3	INTEN	00038h	INT3EN	Reserved bit. Set to 0.
	INTF0	0003Ah	INT3F0, INT3F1	Reserved bits. Set to 0.
	ISCR0	0003Ch	INT3SA, INT3SB	Reserved bits. Set to 0.
	ILVLD	0004Dh	ILVLD0, ILVLD1	Reserved bits. Set to 0.
	IRR3	00053h	IRI3	Reserved bit. Set to 0.
KI0	KIEN	0003Eh	KI0EN, KI0PL	Reserved bits. Set to 0.
Comparator B3 interrupt	ILVL2	00042h	ILVL24, ILVL25	Reserved bits. Set to 0.
	IRR2	00052h	IRCMP3	Reserved bit. Set to 0.
P1_0	PD1	000A9h	PD1_0	Reserved bit. Set to 0.
	P1	000AFh	P1_0	Reserved bit. Set to 0.
	PUR1	000B5h	PU1_0	Reserved bit. Set to 0.
	POD1	000C1h	POD1_0	Reserved bit. Set to 0.
	PML1	000C8h	P10SEL0, P10SEL1	Reserved bits. Set to 0.
P3_3, P3_4, P3_5	PD3	000ABh	PD3_3, PD3_4, PD3_5	Reserved bits. Set to 0.
	P3	000B1h	P3_3, P3_4, P3_5	Reserved bits. Set to 0.
	PUR3	000B7h	PU3_3, PU3_4, PU3_5	Reserved bits. Set to 0.
	DRR3	000BDh	DRR3_3, DRR3_4, DRR3_5	Reserved bits. Set to 0.
	POD3	000C3h	POD3_3, POD3_4, POD3_5	Reserved bits. Set to 0.
	PML3	000CCh	P33SEL0, P33SEL1	Reserved bits. Set to 0.
	PMH3	000CDh	P34SEL0, P34SEL1, P35SEL0, P35SEL1	Reserved bits. Set to 0.
P4_2, P4_5	PD4	000ACh	PD4_2, PD4_5	Reserved bits. Set to 0.
	P4	000B2h	P4_2, P4_5	Reserved bits. Set to 0.
	PUR4	000B8h	PU4_2, PU4_5	Reserved bits. Set to 0.
	POD4	000C4h	POD4_2, POD4_5	Reserved bits. Set to 0.
	PML4	000CEh	P42SEL0, P42SEL1	Reserved bits. Set to 0.
	PMH4	000CFh	P45SEL0, P45SEL1	Reserved bits. Set to 0.
AN0	ADINSEL	0009Dh	CH0, ADGSEL0, ADGSEL1	Do not set to 000.
Comparator B3	WCMPR	00180h	WCB3M0, WCB3OUT	Reserved bits. Set to 0.
	WCB3INTR	00182h	All bits	Reserved register. No access is allowed.

Table 1.4 Specifications (2)

Item	Function	Description
Flash memory		• Program/erase voltage for program ROM: VCC = 1.8 V to 5.5 V • Program/erase voltage for data flash: VCC = 1.8 V to 5.5 V • Program/erase endurance: 10,000 times (data flash) 10,000 times (program ROM) • Program security: ID code check, protection enabled by lock bit • Debug functions: On-chip debug, on-board flash rewrite function
Operating frequency/ Power supply voltage		f(XIN) = 20 MHz (VCC = 2.7 V to 5.5 V) f(XIN) = 5 MHz (VCC = 1.8 V to 5.5 V)
Temperature range		-20 °C to 85 °C (N version) -40 °C to 85 °C (D version) ⁽¹⁾
Package		14-pin TSSOP: [Package code] PTSP0014JA-B 14-pin DIP: [Package code] PRDP0014AC-A 20-pin LSSOP: [Package code] PLSP0020JB-A 20-pin DIP: [Package code] PRDP0020AD-A

Note:

1. Specify the D version if it is to be used.

1.4 Pin Assignment

Figures 1.3 and 1.4 show Pin Assignment (Top View). Table 1.6 lists the Pin Name Information by Pin Number.

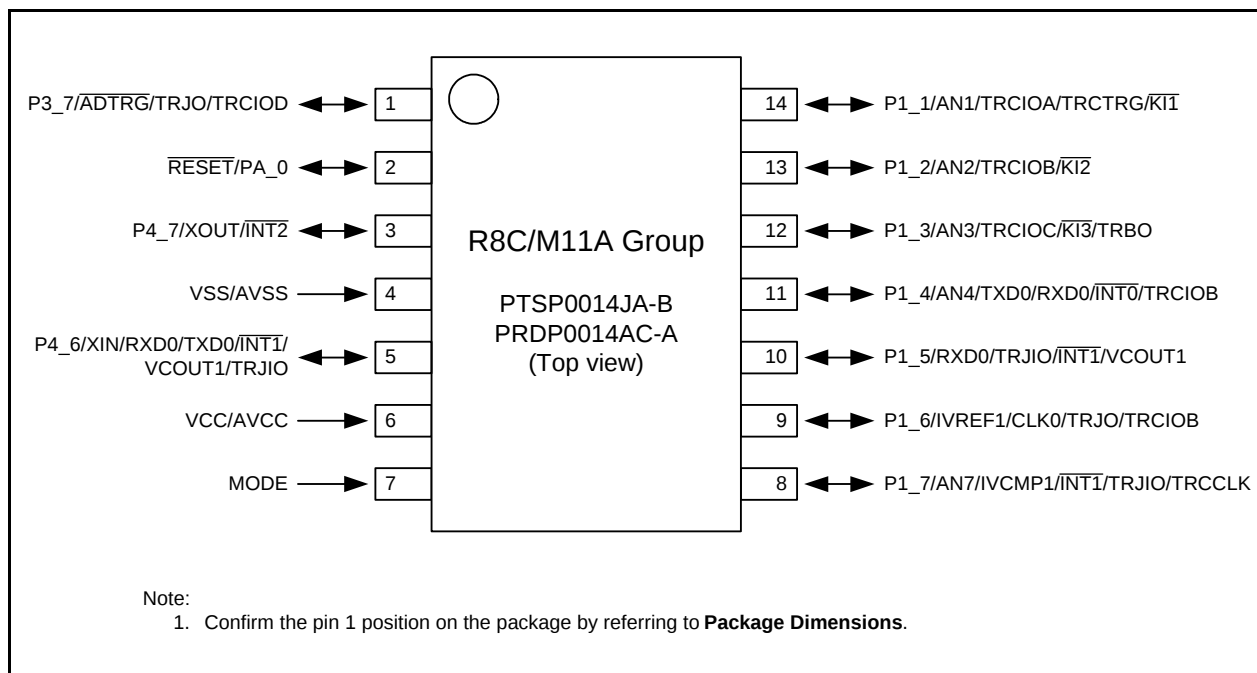


Figure 1.3 R8C/M11A Group Pin Assignment (Top View)

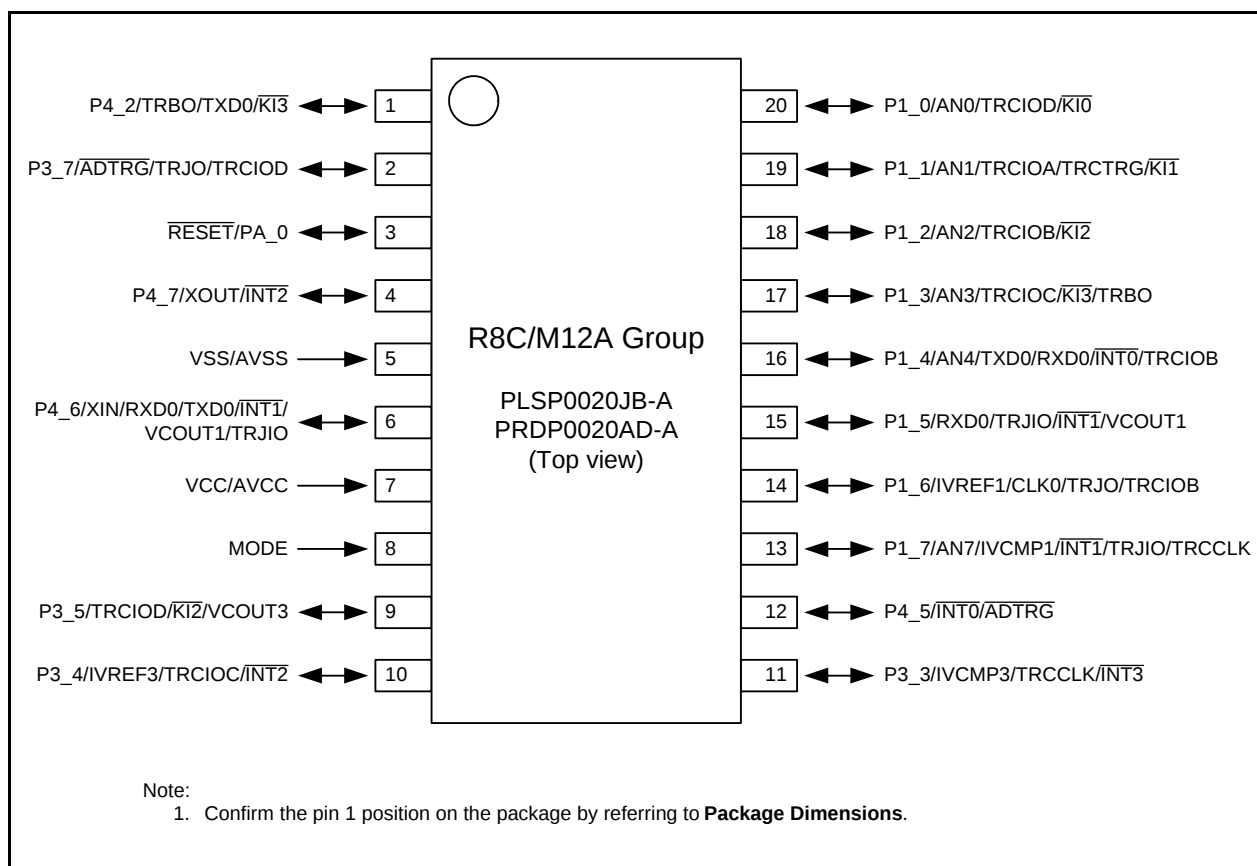


Figure 1.4 R8C/M12A Group Pin Assignment (Top View)

Table 1.6 Pin Name Information by Pin Number

Pin Number		Control Pin	Port	I/O Pins for Peripheral Functions			
R8C/M11A Group	R8C/M12A Group			Interrupt	Timer	Serial Interface	A/D Converter, Comparator B
	1		P4_2	$\overline{\text{KI3}}$	TRBO	TXD0	
1	2		P3_7		TRJO/TRCIOD		$\overline{\text{ADTRG}}$
2	3	$\overline{\text{RESET}}$	PA_0				
3	4	XOUT	P4_7	$\overline{\text{INT2}}$			
4	5	VSS/AVSS					
5	6	XIN	P4_6	$\overline{\text{INT1}}$	TRJIO	RXD0/TXD0	VCOUT1
6	7	VCC/AVCC					
7	8	MODE					
	9		P3_5	$\overline{\text{KI2}}$	TRCIOD		VCOUT3
	10		P3_4	$\overline{\text{INT2}}$	TRCIOC		IVREF3
	11		P3_3	$\overline{\text{INT3}}$	TRCCLK		IVCMP3
	12		P4_5	$\overline{\text{INT0}}$			$\overline{\text{ADTRG}}$
8	13		P1_7	$\overline{\text{INT1}}$	TRJIO/TRCCLK		AN7/IVCMP1
9	14		P1_6		TRJO/TRCIOB	CLK0	IVREF1
10	15		P1_5	$\overline{\text{INT1}}$	TRJIO	RXD0	VCOUT1
11	16		P1_4	$\overline{\text{INT0}}$	TRCIOB	RXD0/TXD0	AN4
12	17		P1_3	$\overline{\text{KI3}}$	TRBO/TRCIOC		AN3
13	18		P1_2	$\overline{\text{KI2}}$	TRCIOB		AN2
14	19		P1_1	$\overline{\text{KI1}}$	TRCIOA/TRCTRG		AN1
	20		P1_0	$\overline{\text{KI0}}$	TRCIOD		AN0

1.5 Pin Functions

Table 1.7 lists the Pin Functions.

Table 1.7 Pin Functions

Item	Pin Name	I/O	Description
Power supply input	VCC, VSS	—	Apply 1.8 V through 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	—	Power supply input for the A/D converter. Connect a capacitor between pins AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Applying a low level to this pin resets the MCU.
MODE	MODE	I	Connect this pin to the VCC pin via a resistor.
XIN clock input	XIN	I	I/O for the XIN clock generation circuit.
XIN clock output	XOUT	O	Connect a ceramic resonator or a crystal oscillator between pins XIN and XOUT. ⁽¹⁾ To use an external clock, input it to the XIN pin. P4_7 can be used as an I/O port at this time.
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input.
I/O ports	P1_0 to P1_7, P3_0 to P3_5, P3_7, P4_2, P4_5 to P4_7, PA_0	I/O	CMOS I/O ports. Each port has an I/O select direction register, enabling switching input and output for each port. For input ports other than PA_0, the presence or absence of a pull-up resistor can be selected by a program. P1_2 to P1_5, P3_3 to P3_5, and P3_7 can be used as LED drive ports.
Timer RJ2	TRJIO	I/O	Timer RJ2 I/O.
	TRJO	O	Timer RJ2 output.
Timer RB2	TRBO	O	Timer RB2 output.
Timer RC	TRCCLK	I	External clock input.
	TRCTRG	I	External trigger input.
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O.
Serial interface	CLK0	I/O	Transfer clock I/O.
	RXD0	I	Serial data input.
	TXD0	O	Serial data output.
A/D converter	AN0 to AN4, AN7	I	Analog input for the A/D converter.
	ADTRG	I	External trigger input for the A/D converter.
Comparator B	IVCMP1, IVCMP3	I	Analog voltage input for comparator B.
	IVREF1, IVREF3	I	Reference voltage input for comparator B.
	VCOUT1, VCOUT3	O	Comparison result output for comparator B.

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

3. Address Space

3.1 Memory Map

Figure 3.1 shows the Memory Map. The R8C/M11A Group and R8C/M12A Group have a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated at lower addresses, beginning with address 0FFFFh. For example, an 8-Kbyte internal ROM area is allocated at addresses 0E000h to 0FFFFh. The fixed interrupt vector table is allocated at addresses 0FFDCh to 0FFFFh. The start address of each interrupt routine is stored here.

The internal ROM (data flash) is allocated at addresses 03000h to 037FFh.

The internal RAM is allocated at higher addresses, beginning with address 00400h. For example, a 512-byte internal RAM area is allocated at addresses 00400h to 005FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated at addresses 00000h to 002FFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.

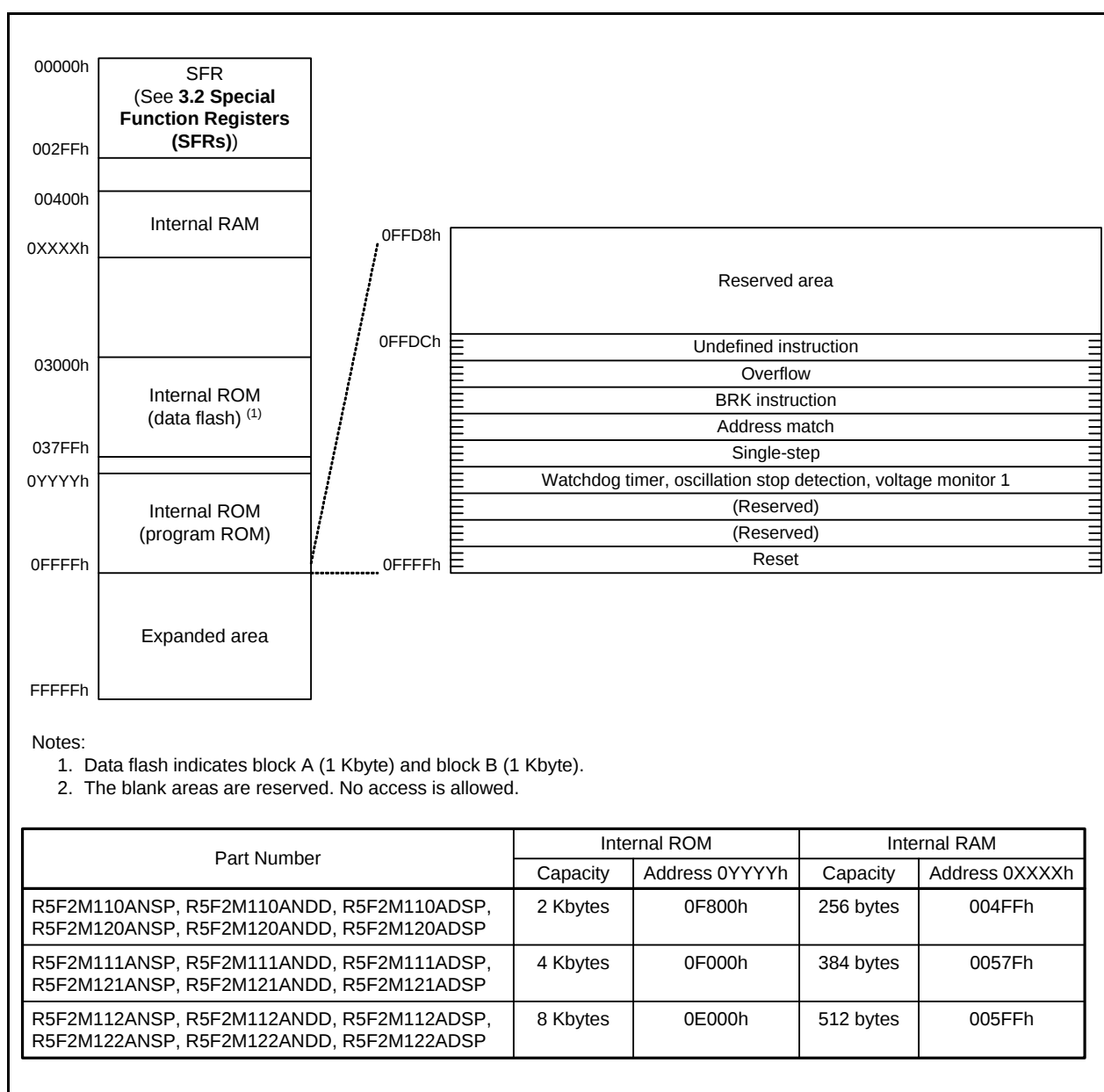


Figure 3.1 Memory Map

Table 3.4 SFR Information (4) (1)

Address	Register Name	Symbol	After Reset
000C0h			
000C1h	Open-Drain Control Register 1	POD1	00h
000C2h			
000C3h	Open-Drain Control Register 3	POD3	00h
000C4h	Open-Drain Control Register 4	POD4	00h
000C5h	Port PA Mode Control Register	PAMCR	00010001b
000C6h			
000C7h			
000C8h	Port 1 Function Mapping Register 0	PML1	00h
000C9h	Port 1 Function Mapping Register 1	PMH1	00h
000CAh			
000CBh			
000CCh	Port 3 Function Mapping Register 0	PML3	00h
000CDh	Port 3 Function Mapping Register 1	PMH3	00h
000CEh	Port 4 Function Mapping Register 0	PML4	00h
000CFh	Port 4 Function Mapping Register 1	PMH4	00h
000D0h			
000D1h	Port 1 Function Mapping Expansion Register	PMH1E	00h
000D2h			
000D3h			
000D4h			
000D5h	Port 4 Function Mapping Expansion Register	PMH4E	00h
000D6h			
000D7h			
000D8h	Timer RJ Counter Register	TRJ	FFh
000D9h			FFh
000DAh	Timer RJ Control Register	TRJCR	00h
000DBh	Timer RJ I/O Control Register	TRJIOC	00h
000DCh	Timer RJ Mode Register	TRJMR	00h
000DDh	Timer RJ Event Select Register	TRJISR	00h
000DEh	Timer RJ Interrupt Control Register	TRJIR	00h
000DFh			
000E0h	Timer RB Control Register	TRBCR	00h
000E1h	Timer RB One-Shot Control Register	TRBOCR	00h
000E2h	Timer RB I/O Control Register	TRBIOC	00h
000E3h	Timer RB Mode Register	TRBMR	00h
000E4h	Timer RB Prescaler Register (2)	TRBPRE	FFh
	Timer RB Primary/Secondary Register (Lower 8 Bits) (3)		
000E5h	Timer RB Primary Register (2)	TRBPR	FFh
	Timer RB Primary Register (Higher 8 Bits) (3)		
000E6h	Timer RB Secondary Register (2)	TRBSC	FFh
	Timer RB Secondary Register (Higher 8 Bits) (3)		
000E7h	Timer RB Interrupt Control Register	TRBIR	00h
000E8h	Timer RC Counter	TRCCNT	00h
000E9h			00h
000EAh	Timer RC General Register A	TRCGRA	FFh
000EBh			FFh
000ECh	Timer RC General Register B	TRCGRB	FFh
000EDh			FFh
000EEh	Timer RC General Register C	TRCGRC	FFh
000EFh			FFh
000F0h	Timer RC General Register D	TRCGRD	FFh
000F1h			FFh
000F2h	Timer RC Mode Register	TRCMR	01001000b
000F3h	Timer RC Control Register 1	TRCCR1	00h
000F4h	Timer RC Interrupt Enable Register	TRCIER	01110000b
000F5h	Timer RC Status Register	TRCSR	01110000b
000F6h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
000F7h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
000F8h	Timer RC Control Register 2	TRCCR2	00011000b
000F9h	Timer RC Digital Filter Function Select Register	TRCDF	00h
000FAh	Timer RC Output Enable Register	TRCOER	01111111b
000FBh	Timer RC A/D Conversion Trigger Control Register	TRCADCR	11110000b
000FCh	Timer RC Waveform Output Manipulation Register	TRCOPR	00h
000FDh			
000FEh			
000FFh			

Notes:

1. The blank areas are reserved. No access is allowed.
2. The TCNT16 bit in the TRBMR register is 0.
3. The TCNT16 bit in the TRBMR register is 1.

Table 3.5 SFR Information (5) (1)

Address	Register Name	Symbol	After Reset
00100h			
00101h			
00102h			
00103h			
00104h			
00105h			
00106h			
00107h			
00108h			
00109h			
0010Ah			
0010Bh			
0010Ch			
0010Dh			
0010Eh			
0010Fh			
00110h			
00111h			
00112h			
00113h			
00114h			
00115h			
00116h			
00117h			
00118h			
00119h			
0011Ah			
0011Bh			
0011Ch			
0011Dh			
0011Eh			
0011Fh			
00120h			
00121h			
00122h			
00123h			
00124h			
00125h			
00126h			
00127h			
00128h			
00129h			
0012Ah			
0012Bh			
0012Ch			
0012Dh			
0012Eh			
0012Fh			
00130h			
00131h			
00132h			
00133h			
00134h			
00135h			
00136h			
00137h			
00138h			
00139h			
0013Ah			
0013Bh			
0013Ch			
0013Dh			
0013Eh			
0013Fh			

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.7 SFR Information (7) (1)

Address	Register Name	Symbol	After Reset
00180h	Comparator B Control Register	WCMPR	00h
00181h	Comparator B1 Interrupt Control Register	WCB1INTR	00h
00182h	Comparator B3 Interrupt Control Register	WCB3INTR	00h
00183h			
00184h			
00185h			
00186h			
00187h			
00188h			
00189h			
0018Ah			
0018Bh			
0018Ch			
0018Dh			
0018Eh			
0018Fh			
00190h			
00191h			
00192h			
00193h			
00194h			
00195h			
00196h			
00197h			
00198h			
00199h			
0019Ah			
0019Bh			
0019Ch			
0019Dh			
0019Eh			
0019Fh			
001A0h			
001A1h			
001A2h			
001A3h			
001A4h			
001A5h			
001A6h			
001A7h			
001A8h			
001A9h	Flash Memory Status Register	FST	10000000b
001AAh	Flash Memory Control Register 0	FMR0	00h
001ABh	Flash Memory Control Register 1	FMR1	00h
001ACh	Flash Memory Control Register 2	FMR2	00h
001ADh	Flash Memory Refresh Control Register	FREFR	00h
001AEh			
001AFh			
001B0h			
001B1h			
001B2h			
001B3h			
001B4h			
001B5h			
001B6h			
001B7h			
001B8h			
001B9h			
001BAh			
001BBh			
001BCh			
001BDh			
001BEh			
001BFh			

Note:

1. The blank areas are reserved. No access is allowed.

4. Electrical Characteristics

Table 4.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V _{CC} /AV _{CC}	Power supply voltage			-0.3 to 6.5	V
V _i	Input voltage	XIN	XIN-XOUT oscillation on (oscillation circuit used) ⁽¹⁾	-0.3 to 1.9	V
			XIN-XOUT oscillation off (oscillation circuit not used) ⁽¹⁾	-0.3 to V _{CC} + 0.3	V
		Other pins		-0.3 to V _{CC} + 0.3	V
V _o	Output voltage	XOUT	XIN-XOUT oscillation on (oscillation circuit used) ⁽¹⁾	-0.3 to 1.9	V
			XIN-XOUT oscillation off (oscillation circuit not used) ⁽¹⁾	-0.3 to V _{CC} + 0.3	V
		Other pins		-0.3 to V _{CC} + 0.3	V
P _d	Power consumption		-40 °C ≤ Topr ≤ 85 °C	500	mW
T _{opr}	Operating ambient temperature			-20 to 85 (N version)/ -40 to 85 (D version)	°C
T _{stg}	Storage temperature			-60 to 150	°C

Note:

1. When the oscillation circuit is used: bits CKPT1 to CKPT0 in the EXCKCR register are set to 11b
When the oscillation circuit is not used: bits CKPT1 to CKPT0 in the EXCKCR register are set to any value other than 11b

Table 4.2 Recommended Operating Conditions

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V _{CC} /AV _{CC}	Power supply voltage			1.8	—	5.5	V
V _{SS} /AV _{SS}	Power supply voltage			—	0	—	V
V _{IH}	Input high voltage	Other than CMOS input		0.8 V _{CC}	—	V _{CC}	V
		CMOS input	4.0 V ≤ V _{CC} ≤ 5.5 V	0.65 V _{CC}	—	V _{CC}	V
			2.7 V ≤ V _{CC} < 4.0 V	0.7 V _{CC}	—	V _{CC}	V
			1.8 V ≤ V _{CC} < 2.7 V	0.8 V _{CC}	—	V _{CC}	V
V _{IL}	Input low voltage	Other than CMOS input		0	—	0.2 V _{CC}	V
		CMOS input	4.0 V ≤ V _{CC} ≤ 5.5 V	0	—	0.4 V _{CC}	V
			2.7 V ≤ V _{CC} < 4.0 V	0	—	0.3 V _{CC}	V
			1.8 V ≤ V _{CC} < 2.7 V	0	—	0.2 V _{CC}	V
I _{OH} (sum)	Peak sum output high current	Sum of all pins I _{OH} (peak)		—	—	-160	mA
I _{OH} (sum)	Average sum output high current	Sum of all pins I _{OH} (avg)		—	—	-80	mA
I _{OH} (peak)	Peak output high current		When drive capacity is low	—	—	-10	mA
			When drive capacity is high ⁽⁵⁾	—	—	-40	mA
I _{OH} (avg)	Average output high current		When drive capacity is low	—	—	-5	mA
			When drive capacity is high ⁽⁵⁾	—	—	-20	mA
I _{OL} (sum)	Peak sum output low current	Sum of all pins I _{OL} (peak)		—	—	160	mA
I _{OL} (sum)	Average sum output low current	Sum of all pins I _{OL} (avg)		—	—	80	mA
I _{OL} (peak)	Peak output low current		When drive capacity is low	—	—	10	mA
			When drive capacity is high ⁽⁵⁾	—	—	40	mA
I _{OL} (avg)	Average output low current		When drive capacity is low	—	—	5	mA
			When drive capacity is high ⁽⁵⁾	—	—	20	mA
f _(XIN)	XIN oscillation frequency		2.7 V ≤ V _{CC} ≤ 5.5 V	2	—	20	MHz
			1.8 V ≤ V _{CC} < 2.7 V	2	—	5	MHz
	XIN clock input oscillation frequency		2.7 V ≤ V _{CC} ≤ 5.5 V	0	—	20	MHz
			1.8 V ≤ V _{CC} < 2.7 V	0	—	5	MHz
f _{HOCO}	High-speed on-chip oscillator oscillation frequency ⁽³⁾		1.8 V ≤ V _{CC} ≤ 5.5 V	—	20	—	MHz
f _{LOCO}	Low-speed on-chip oscillator oscillation frequency ⁽⁴⁾		1.8 V ≤ V _{CC} ≤ 5.5 V	—	125	—	kHz
—	System clock frequency		2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	20	MHz
			1.8 V ≤ V _{CC} < 2.7 V	—	—	5	MHz
f _s	CPU clock frequency		2.7 V ≤ V _{CC} ≤ 5.5 V	0	—	20	MHz
			1.8 V ≤ V _{CC} < 2.7 V	0	—	5	MHz

Notes:

1. V_{CC} = 1.8 V to 5.5 V and T_{opr} = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. For details, see **Table 4.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics**.
4. For details, see **Table 4.11 Low-Speed On-Chip Oscillator Circuit Electrical Characteristics**.
5. The pins with high drive capacity are P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, and P3_7.

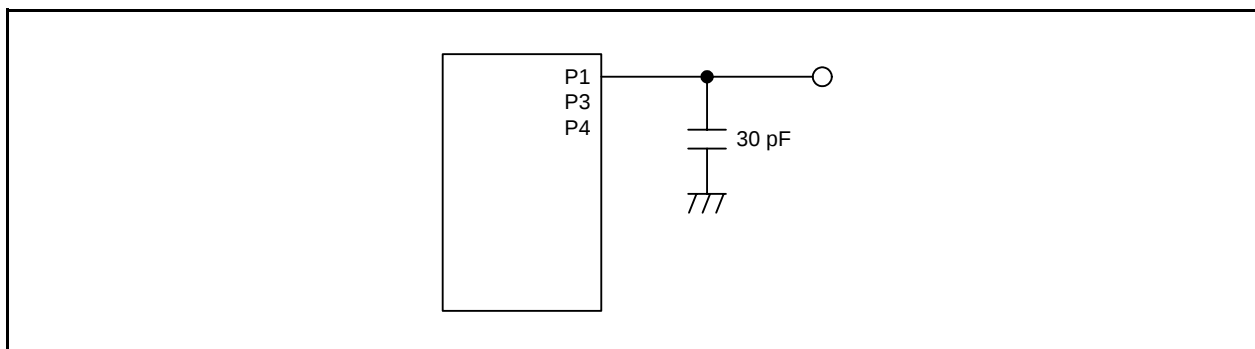
**Figure 4.1 Ports P1, P3, and P4 Timing Measurement Circuit**

Table 4.7 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet0	Voltage detection level Vdet0_0 ⁽²⁾		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 ⁽²⁾		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 ⁽²⁾		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 ⁽²⁾		3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time ⁽³⁾	When Vcc decreases from 5 V to (Vdet0_0 - 0.1) V	—	30	—	μs
—	Self power consumption in voltage detection circuit	VC0E = 1, Vcc = 5.0 V	—	1.5	—	μA
t _d (E-A)	Wait time until voltage detection circuit operation starts ⁽⁴⁾		—	—	100	μs

Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. The response time is from when the voltage passes Vdet0 until the voltage monitor 0 reset is generated.
4. The wait time is necessary for the voltage detection circuit to operate when the VC0E bit in the VCA2 register is set to 0 and then 1.

Table 4.8 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet1	Voltage detection level Vdet1_1 ⁽²⁾	When Vcc decreases	2.15	2.35	2.55	V
	Voltage detection level Vdet1_3 ⁽²⁾	When Vcc decreases	2.45	2.65	2.85	V
	Voltage detection level Vdet1_5 ⁽²⁾	When Vcc decreases	2.75	2.95	3.15	V
	Voltage detection level Vdet1_7 ⁽²⁾	When Vcc decreases	3.00	3.25	3.55	V
	Voltage detection level Vdet1_9 ⁽²⁾	When Vcc decreases	3.30	3.55	3.85	V
	Voltage detection level Vdet1_B ⁽²⁾	When Vcc decreases	3.60	3.85	4.15	V
	Voltage detection level Vdet1_D ⁽²⁾	When Vcc decreases	3.90	4.15	4.45	V
	Voltage detection level Vdet1_F ⁽²⁾	When Vcc decreases	4.20	4.45	4.75	V
—	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_1 to Vdet1_5 selected	—	0.07	—	V
		Vdet1_7 to Vdet1_F selected	—	0.10	—	V
—	Voltage detection 1 circuit response time ⁽³⁾	When Vcc decreases from 5 V to (Vdet1_0 - 0.1) V	—	60	150	μs
—	Self power consumption in voltage detection circuit	VC1E = 1, Vcc = 5.0 V	—	1.7	—	μA
t _d (E-A)	Wait time until voltage detection circuit operation starts ⁽⁴⁾		—	—	100	μs

Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version).
2. Select the voltage detection level with bits VD1S1 to VD1S3 in the VD1LS register.
3. The response time is from when the voltage passes Vdet1 until the voltage monitor 1 interrupt request is generated.
4. The wait time is necessary for the voltage detection circuit to operate when the VC1E bit in the VCA2 register is set to 0 and then 1.

Table 4.9 Power-On Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power Vcc rise gradient		0	—	50,000	mV/msec

Notes:

1. The measurement condition is $T_{opr} = -20\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$ (N version)/ $-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$ (D version), unless otherwise specified.
2. To use the power-on reset function, enable the voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

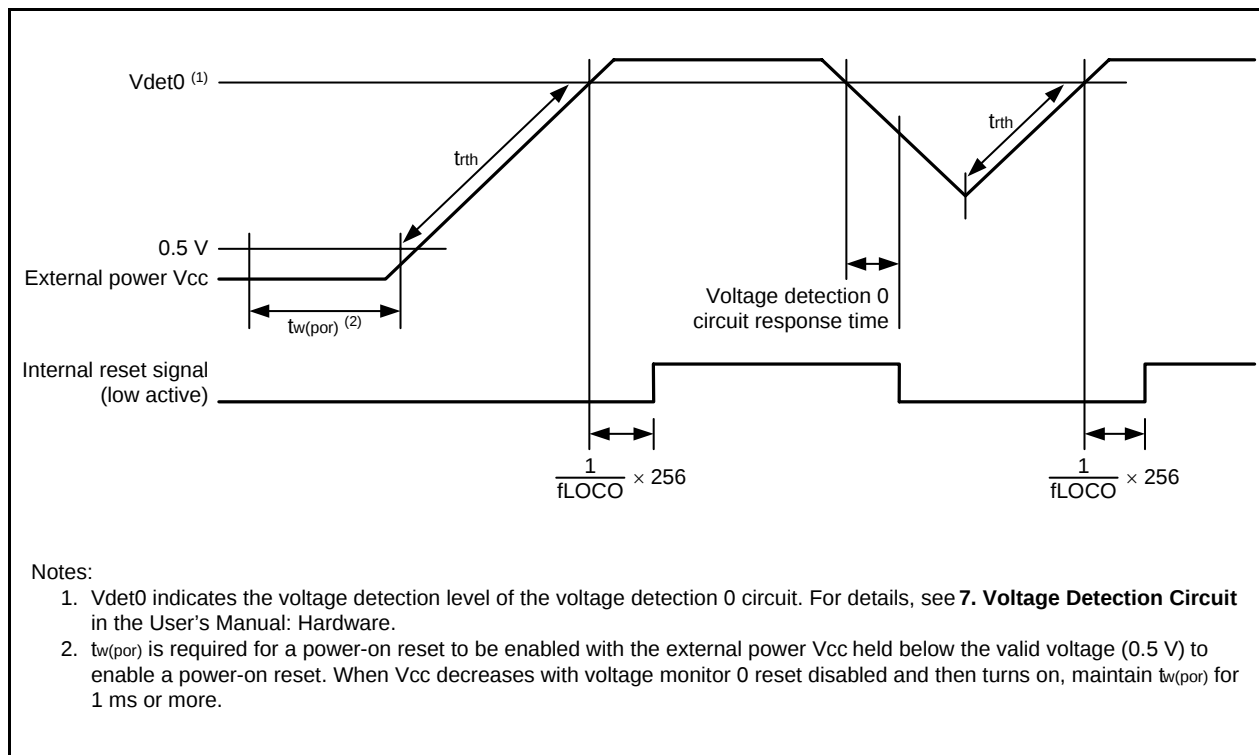
**Figure 4.3 Power-On Reset Circuit Electrical Characteristics**

Table 4.13 DC Characteristics (1) [$4.0\text{ V} \leq V_{CC} \leq 5.5\text{ V}$]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output high voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I _{OH} = -20 mA	V _{CC} - 2.0	—	V _{CC}	V
			When drive capacity is low	I _{OH} = -5 mA	V _{CC} - 2.0	—	V _{CC}	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I _{OH} = -5 mA	V _{CC} - 2.0	—	V _{CC}	V
V _{OL}	Output low voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I _{OL} = 20 mA	—	—	2.0	V
			When drive capacity is low	I _{OL} = 5 mA	—	—	2.0	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I _{OL} = 5 mA	—	—	2.0	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, TRJIO, TRCIOA, TRCIOB, TRCIO, TRCIOD, RXD0, CLK0	V _{CC} = 5 V		0.1	1.2	—	V
		RESET	V _{CC} = 5 V		0.1	1.2	—	V
I _{IH}	Input high current		V _I = 5 V, V _{CC} = 5.0 V		—	—	5.0	μA
I _{IL}	Input low current		V _I = 0 V, V _{CC} = 5.0 V		—	—	-5.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 5.0 V		25	50	100	kΩ
R _{fXIN}	Feedback resistance	XIN			—	2.2	—	MΩ
V _{RAM}	RAM hold voltage		In stop mode		1.8	—	—	V

Notes:

1. $4.0\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), f(XIN) = 20 MHz, unless otherwise specified.
2. High drive capacity can also be used while the peripheral output function is used.

Timing Requirements ($V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

Table 4.15 External Clock Input (XIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(XIN)$	XIN input cycle time	50	—	ns
$t_{WH}(XIN)$	XIN input high width	24	—	ns
$t_{WL}(XIN)$	XIN input low width	24	—	ns

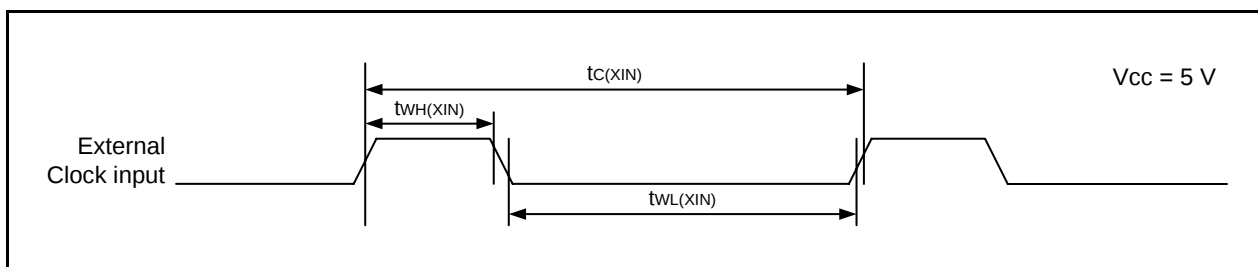


Figure 4.4 External Clock Input Timing When $V_{CC} = 5\text{ V}$

Table 4.16 TRJIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(TRJIO)$	TRJIO input cycle time	100	—	ns
$t_{WH}(TRJIO)$	TRJIO input high width	40	—	ns
$t_{WL}(TRJIO)$	TRJIO input low width	40	—	ns

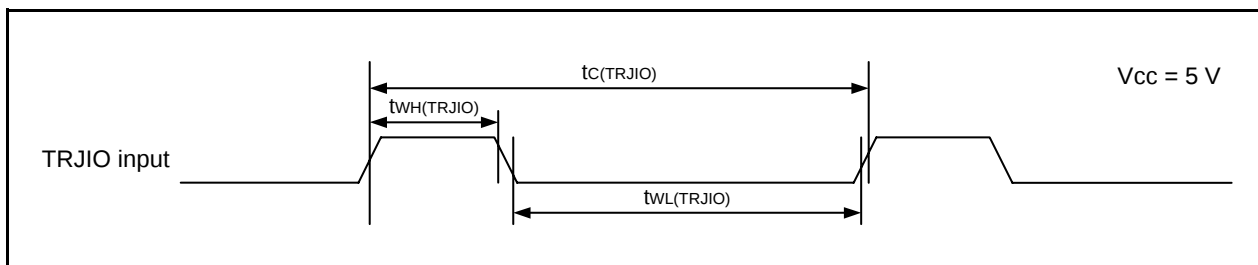
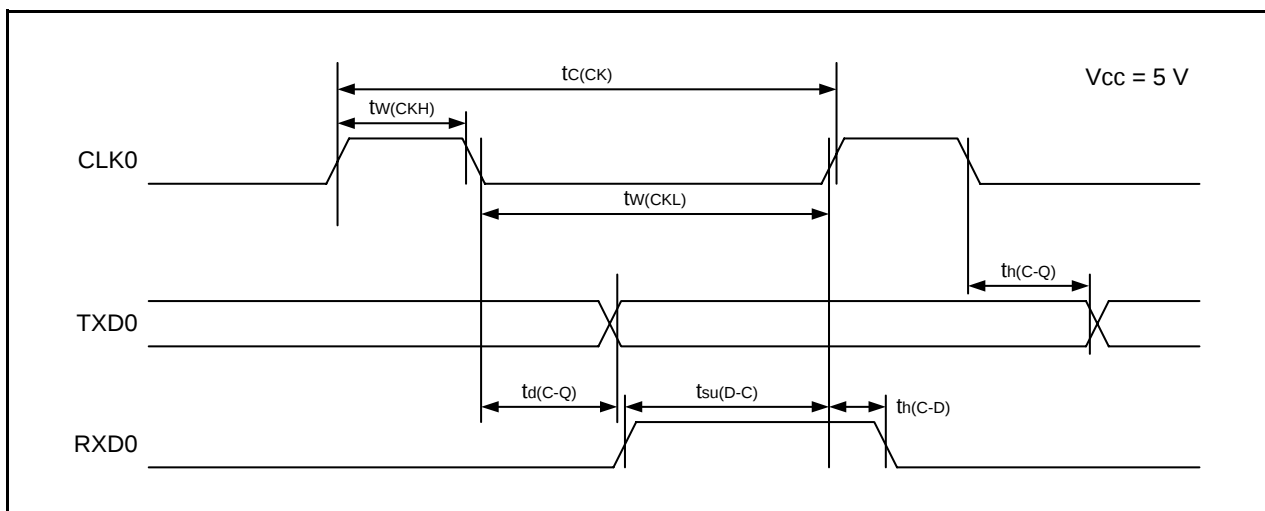


Figure 4.5 TRJIO Input Timing When $V_{CC} = 5\text{ V}$

Table 4.17 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	200	—	ns
$t_{w(CKH)}$	CLK0 input high width	100	—	ns
$t_{w(CKL)}$	CLK0 input low width	100	—	ns
$t_{d(C-Q)}$	TXD0 output delay time	—	50	ns
$t_{h(C-Q)}$	TXD0 hold time	0	—	ns
$t_{su(D-C)}$	RXD0 input setup time	50	—	ns
$t_{h(C-D)}$	RXD0 input hold time	90	—	ns

**Figure 4.6 Serial Interface Timing When Vcc = 5 V****Table 4.18 External Interrupt $\overline{INTi}$ Input, Key Input Interrupt $\overline{Kli}$ ($i = 0$ to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input high width, $\overline{Kli}$ input high width	250 (1)	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input low width, $\overline{Kli}$ input low width	250 (2)	—	ns

Notes:

1. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input high width is $(1/\text{digital filter clock frequency} \times 3)$ or the minimum value of the standard, whichever is greater.
2. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input low width is $(1/\text{digital filter clock frequency} \times 3)$ or the minimum value of the standard, whichever is greater.

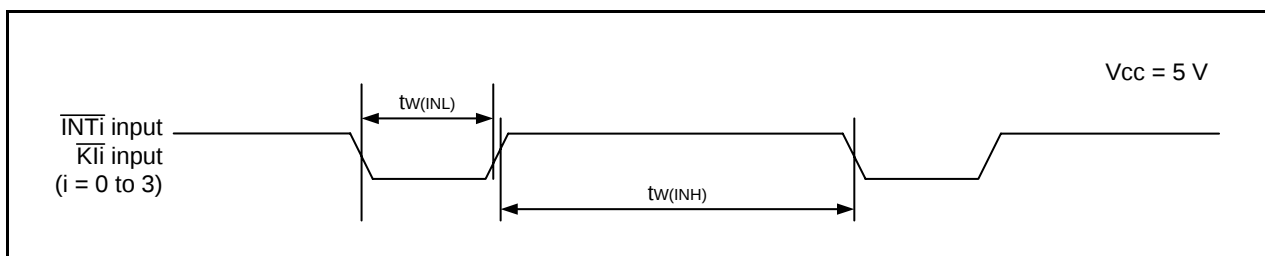
**Figure 4.7 Timing for External Interrupt $\overline{INTi}$ Input and Key Input Interrupt $\overline{Kli}$ When Vcc = 5 V**

Table 4.26 DC Characteristics (6) [1.8 V ≤ V_{CC} < 2.7 V]
(Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified)

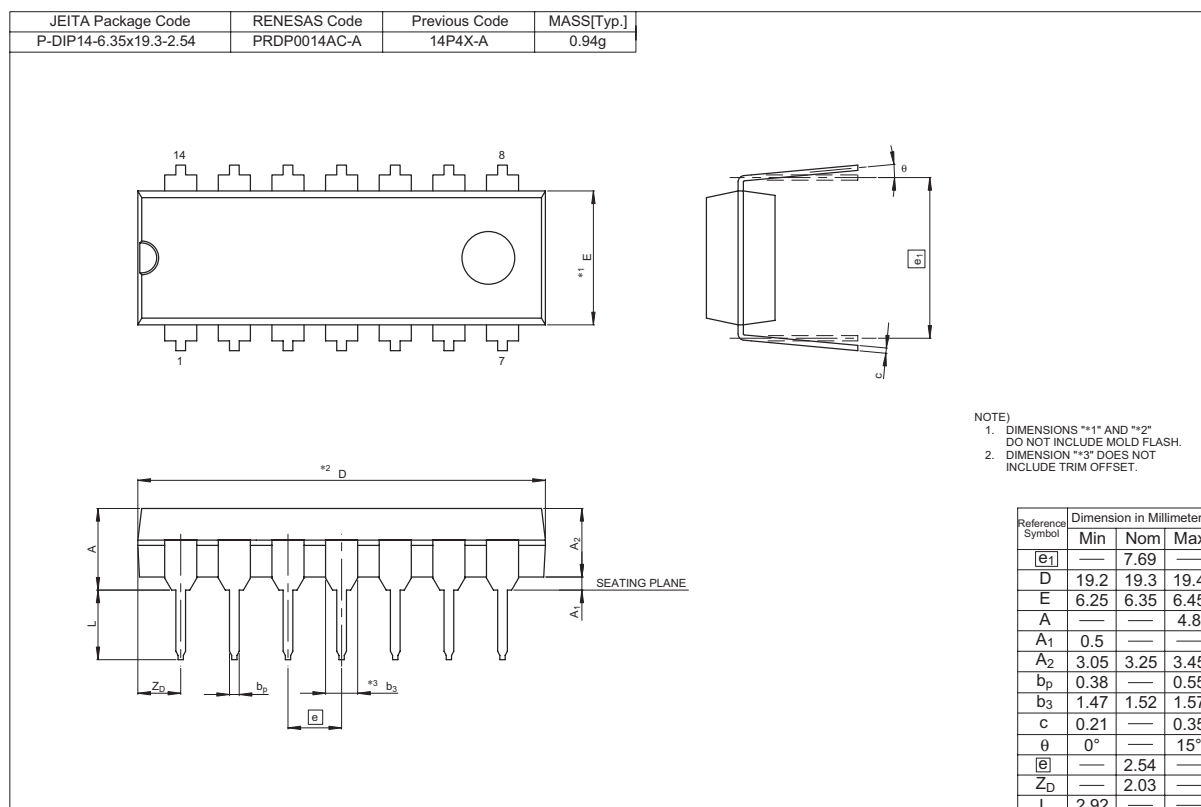
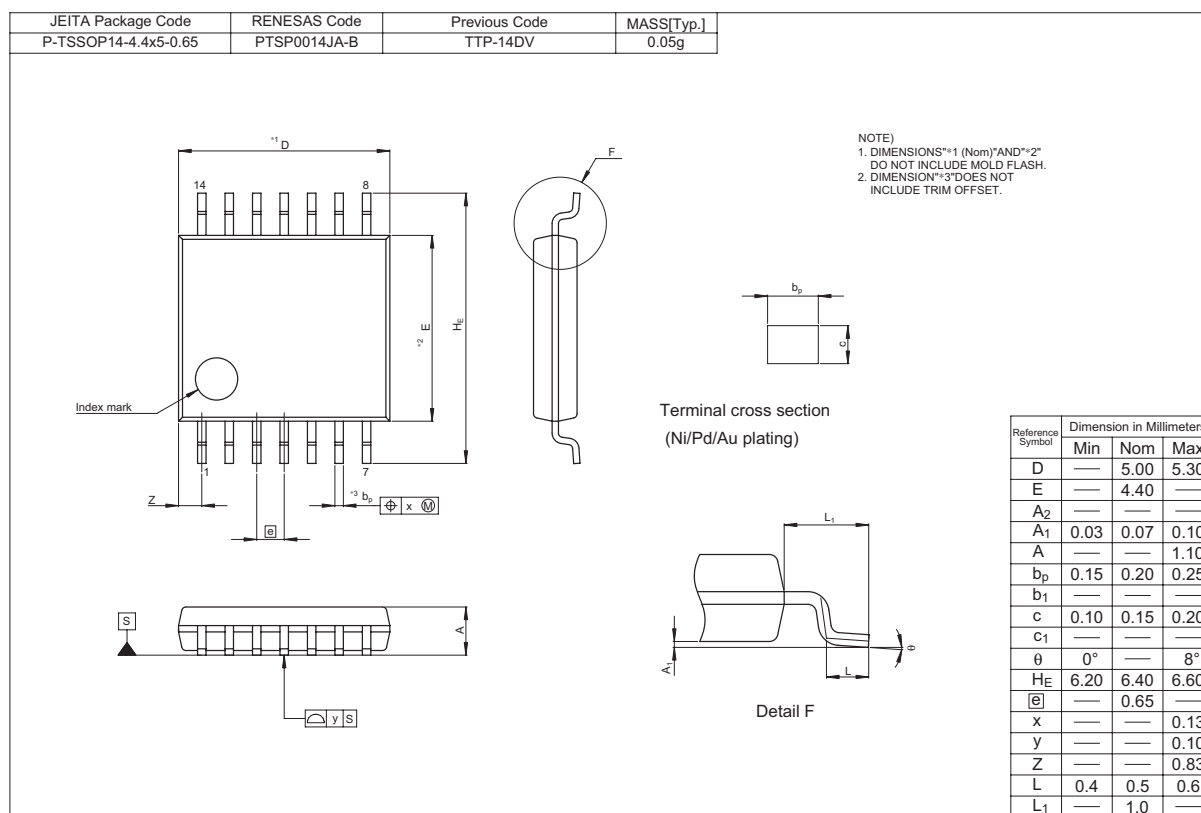
Symbol	Parameter		Condition									Unit
			Oscillation Circuit	On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Standard			
			XIN (2)	High-Speed	Low-Speed				Min.	Typ. (3)	Max.	
Icc	Power supply current (1)	High-speed clock mode	5 MHz	Off	125 kHz	No division	—		—	1.0	—	mA
			5 MHz	Off	125 kHz	Division by 8	—		—	0.6	—	mA
		High-speed on-chip oscillator mode	Off	5 MHz (4)	125 kHz	No division			—	1.6	6.5	mA
			Off	5 MHz (4)	125 kHz	Division by 8			—	1.1	—	mA
			Off	4 MHz (4)	125 kHz	Division by 16	MSTTRC = 1		—	1.0	—	mA
		Low-speed on-chip oscillator mode	Off	Off	125 kHz	Division by 8	FMR27 = 1 LPE = 0		—	60	200	μA
		Wait mode	Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1	Peripheral clock supplied during WAIT instruction execution	—	15	90	μA
			Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1 WCKSTP = 1	Peripheral clock stopped during WAIT instruction execution	—	4.0	80	μA
		Stop mode	Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 25 °C Peripheral clock stopped	—	1.0	4.0	μA
			Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 85 °C Peripheral clock stopped	—	1.5	—	μA

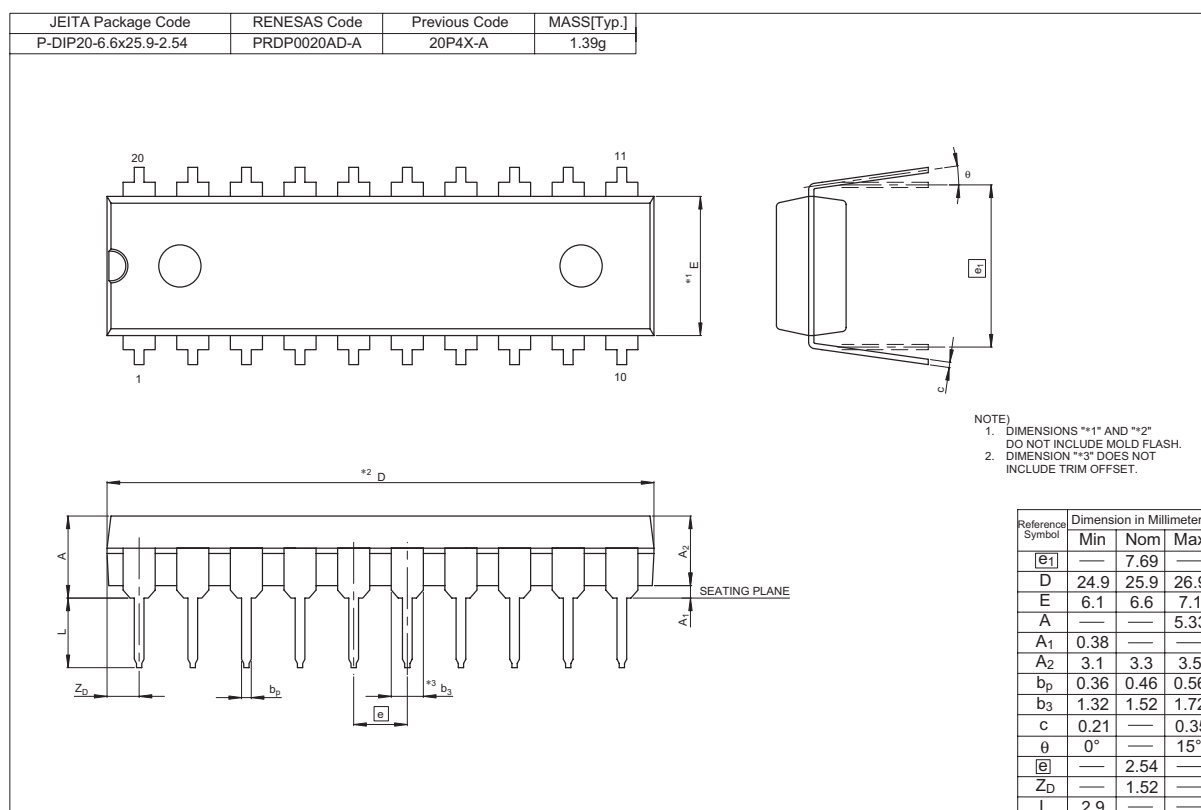
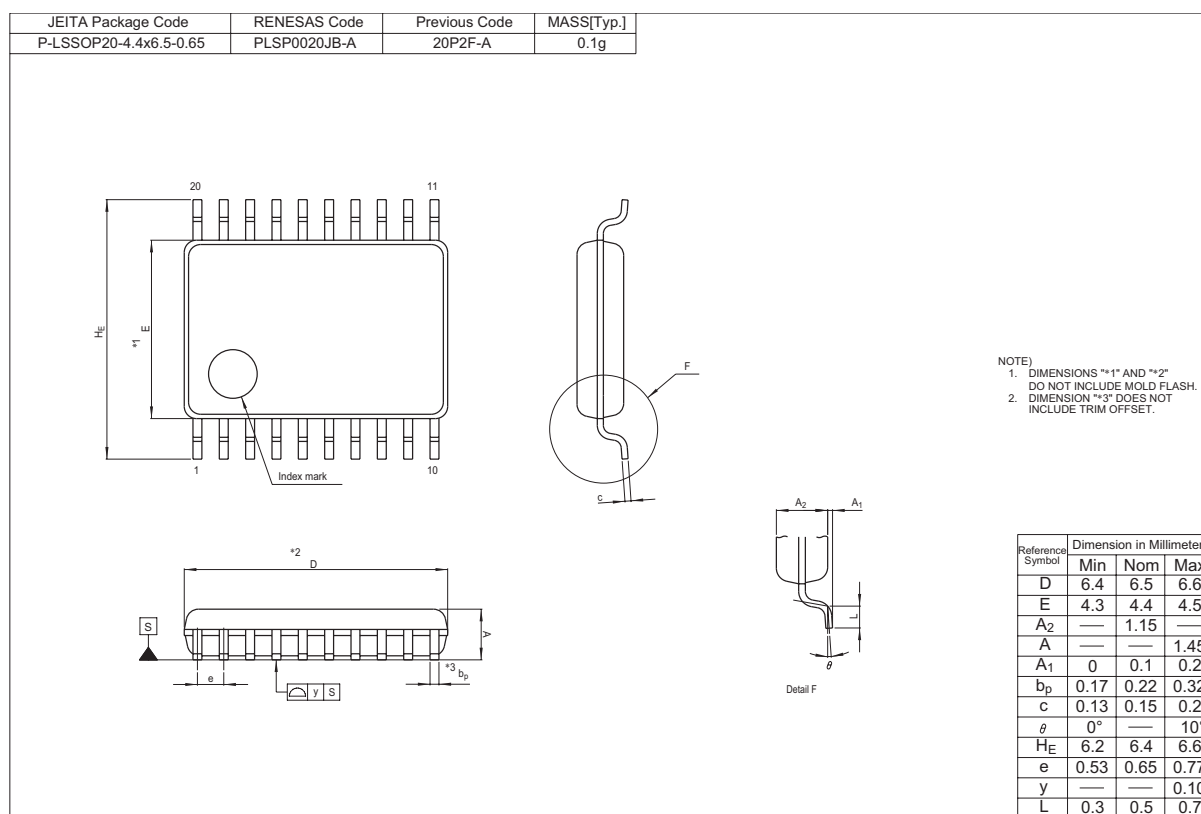
Notes:

1. V_{CC} = 1.8 V to 2.7 V, single-chip mode, output pins are open, and other pins are connected to V_{SS}.
2. When the XIN input is a square wave.
3. V_{CC} = 2.2 V
4. Set the system clock to 5 MHz or 4 MHz with the PHISEL register.

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.





General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.